



The Abdus Salam
International Centre
for Theoretical Physics



1st Mesoamerican Workshop on Reconfigurable X-ray Scientific Instrumentation for Cultural Heritage

Lab 0: User environment

Antigua Guatemala, Junio 2025

Maynor Ballina



Welcome: Lab tutors



Maynor Ballina (ICTP, UNITS) [Guatemala]

Dr. Luis Garcia (ICTP) [Guatemala]



Dr. Romina Molina (ICTP) [Argentina]

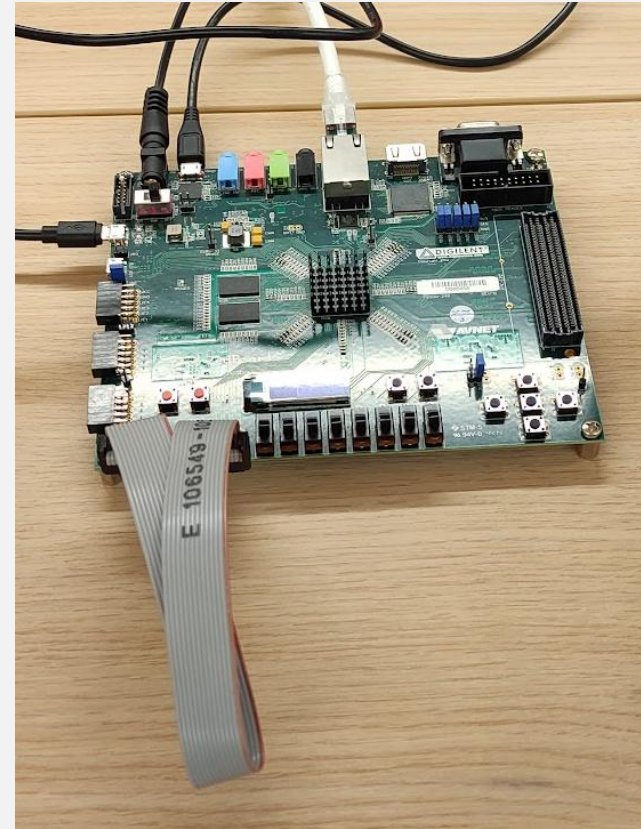
Dr. Fabian Castano (UdeA) [Colombia]



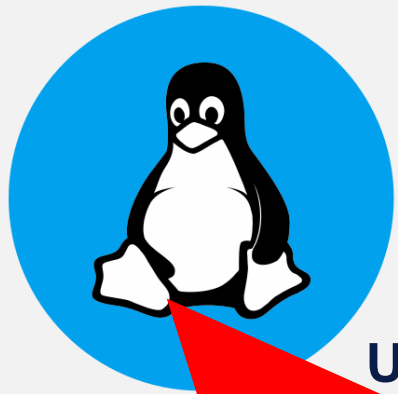
M.Eng. Jorge Balsells (USAC) [Guatemala]

Labs Overview:

- **Lab 0:**
User environment
- **Lab 1:**
Getting started with SoC-FPGA
- **Lab 2:**
Reconfigurable instrumentation on SoC-FPGA: digital oscilloscope using comblock and RTL instantiation
- **Lab 3:**
Soc-FPGA Development Framework for Analog signal interfaces
- **Lab 4:**
Digital Pulse Processing Electronics for X-ray Photon Detection in Cultural Heritage Analysis
- **Lab 5:**
Introduction to machine learning and SoC/FPGA



User Environment:



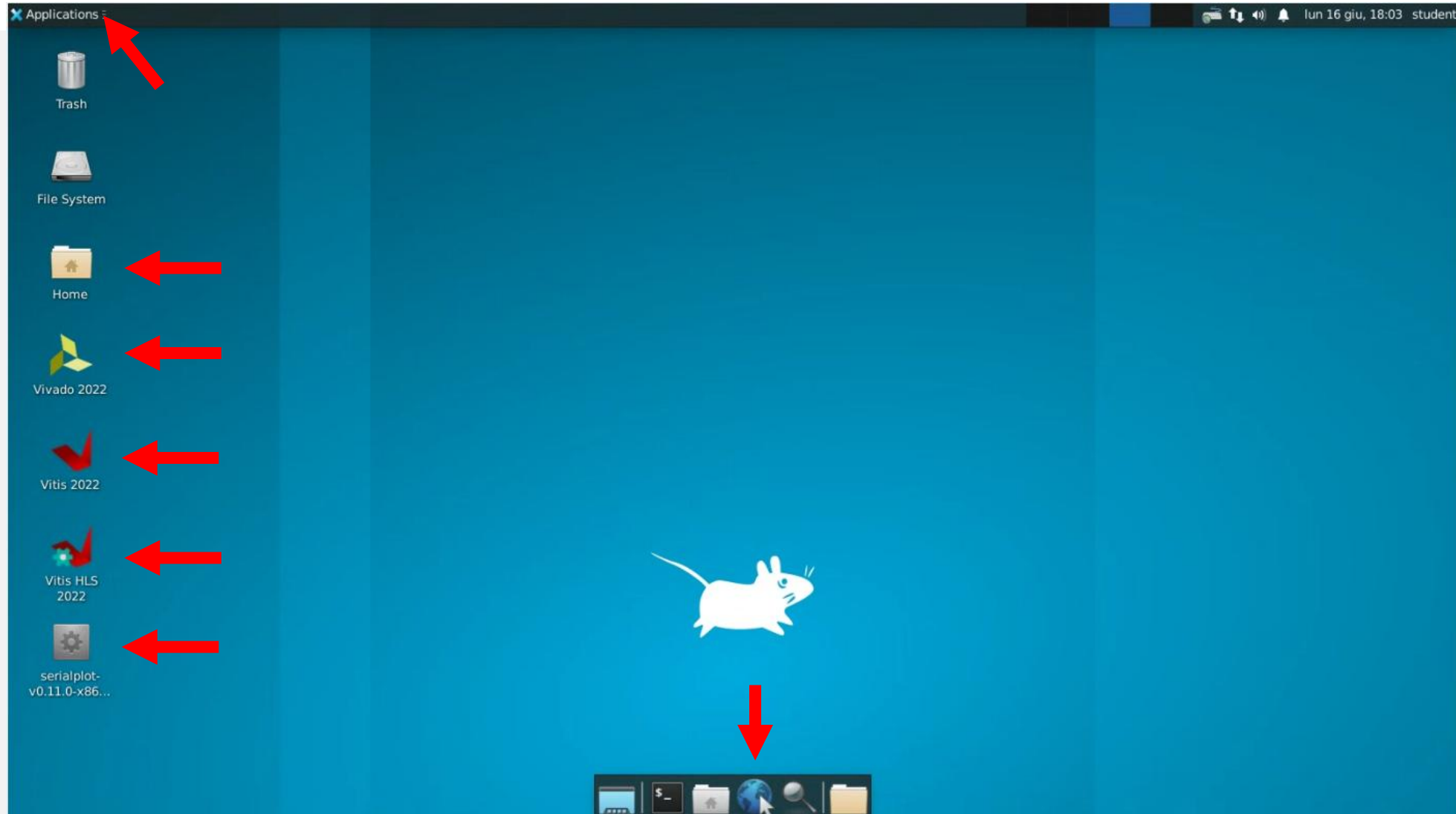
User Environment

User: student
Password: workspace

**Raise your
hand**

A login form is displayed on a blue background with a subtle dot pattern. The form consists of a dark teal rounded rectangle containing a text input field with the label 'student' and a password input field with the label 'Password'. A small white circle is visible to the right of the 'student' input field.

User Environment:



Important links:

<https://gitlab.com/ictp-mlab/smr-4078>



A screenshot of the GitLab web interface for the repository 'smr-4078' under the 'ICTP-MLAB' namespace. The left sidebar shows the project navigation menu with options like Pinned, Issues, Merge requests, Manage, Plan, Code, Build, Secure, Deploy, Operate, Monitor, Analyze, and Settings. The main content area shows a list of files: 'LICENSE' (added 2 years ago) and 'README.md' (updated 3 hours ago). Below the file list, the 'README.md' content is displayed, featuring a blue header with the title '1st Mesoamerican Workshop on Reconfigurable X-ray Scientific Instrumentation for Cultural Heritage'. The header also includes logos for ICTP (The Abdus Salam International Centre for Theoretical Physics), IAEA, and UNESCO. The background of the header has a blue circular pattern of white dots.

Important links:

<https://gitlab.com/ictp-mlab/smr-4078/-/wikis/home>

ICTP-MLAB / smr4078 / Wiki / Home

Home

Last edited by **Maynor Ballina LTP** 3 hours ago

ICTP The Abdus Salam International Centre for Theoretical Physics

IAEA International Atomic Energy Agency

unesco United Nations Educational, Scientific and Cultural Organization

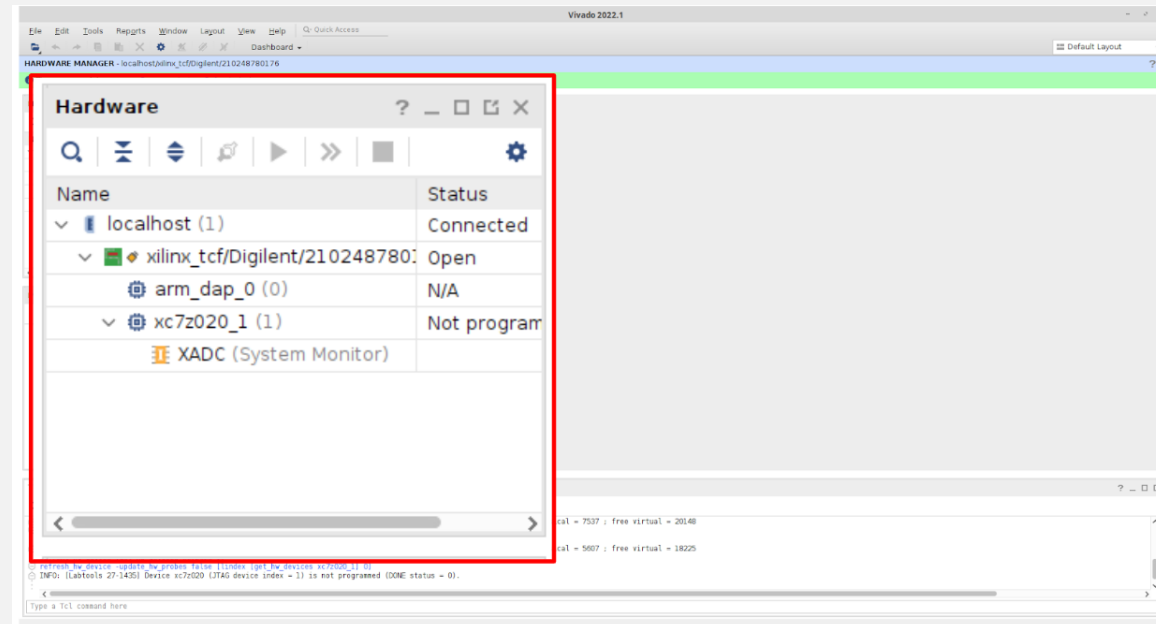
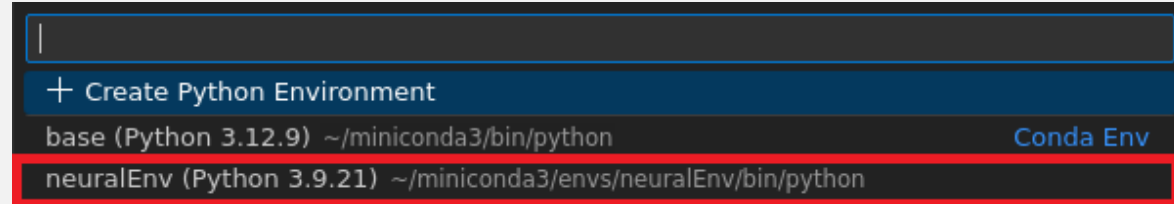
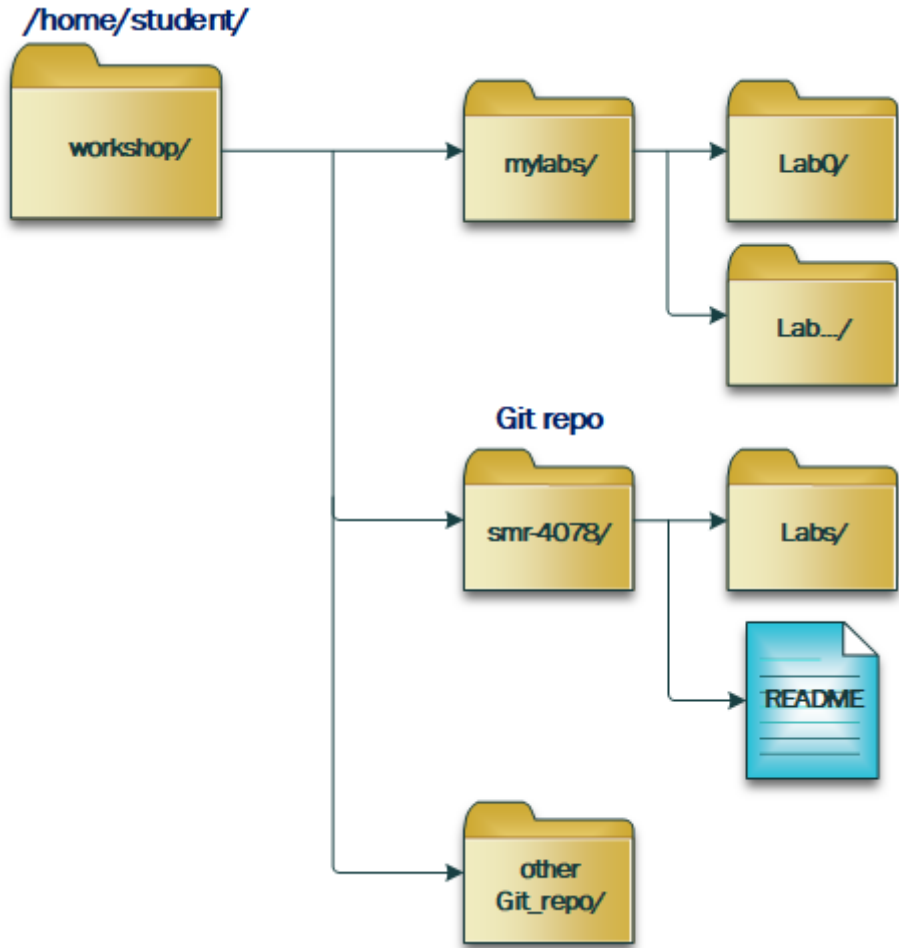
1st Mesoamerican Workshop on Reconfigurable X-ray Scientific Instrumentation for Cultural Heritage

Lab Guides

- Lab 0: User environment
- Lab 1: Getting started with SoC-FPGA



Labs 0:





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Lab 1: Getting started with SoC-FPGA

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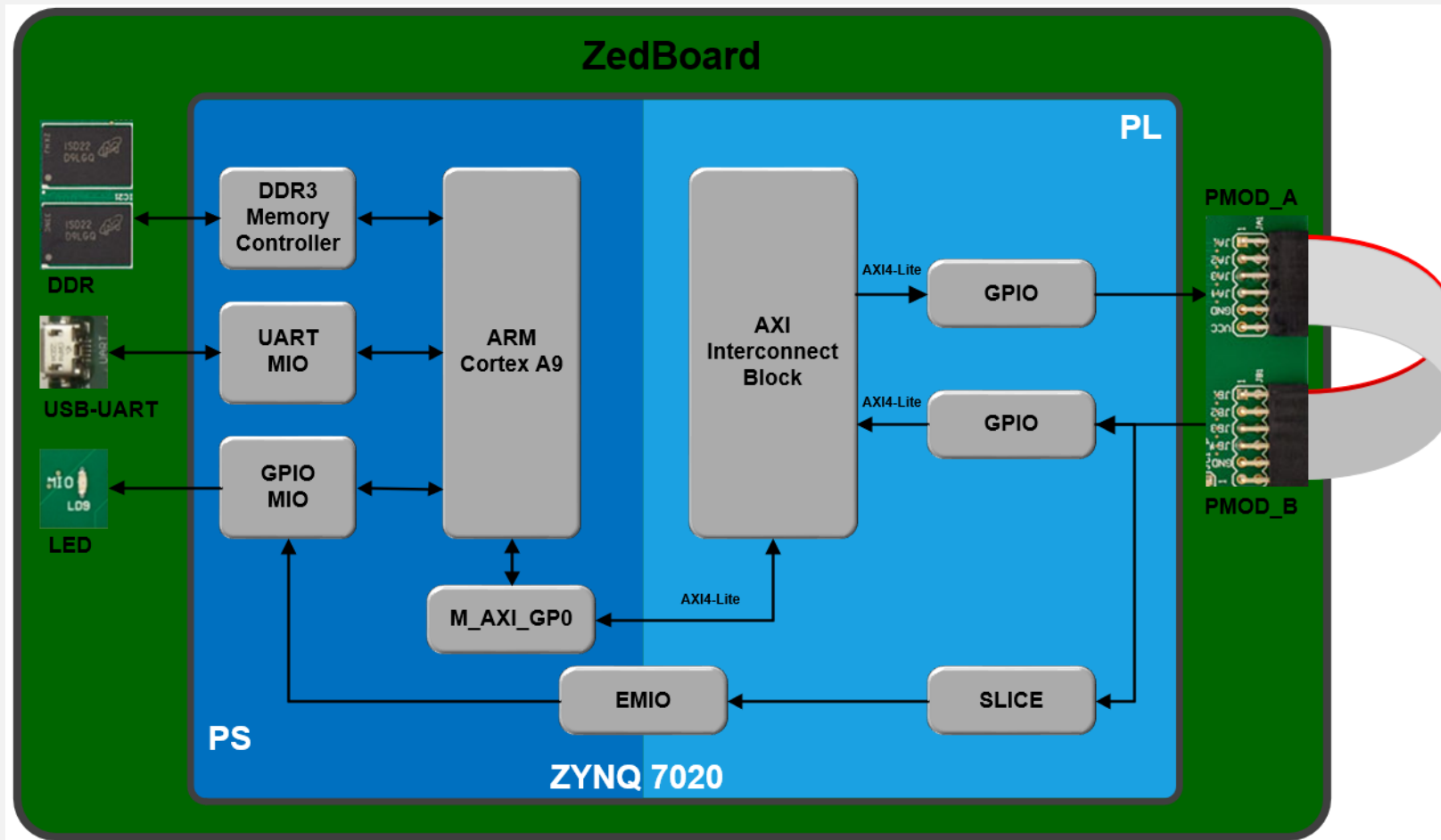
Maynor Ballina



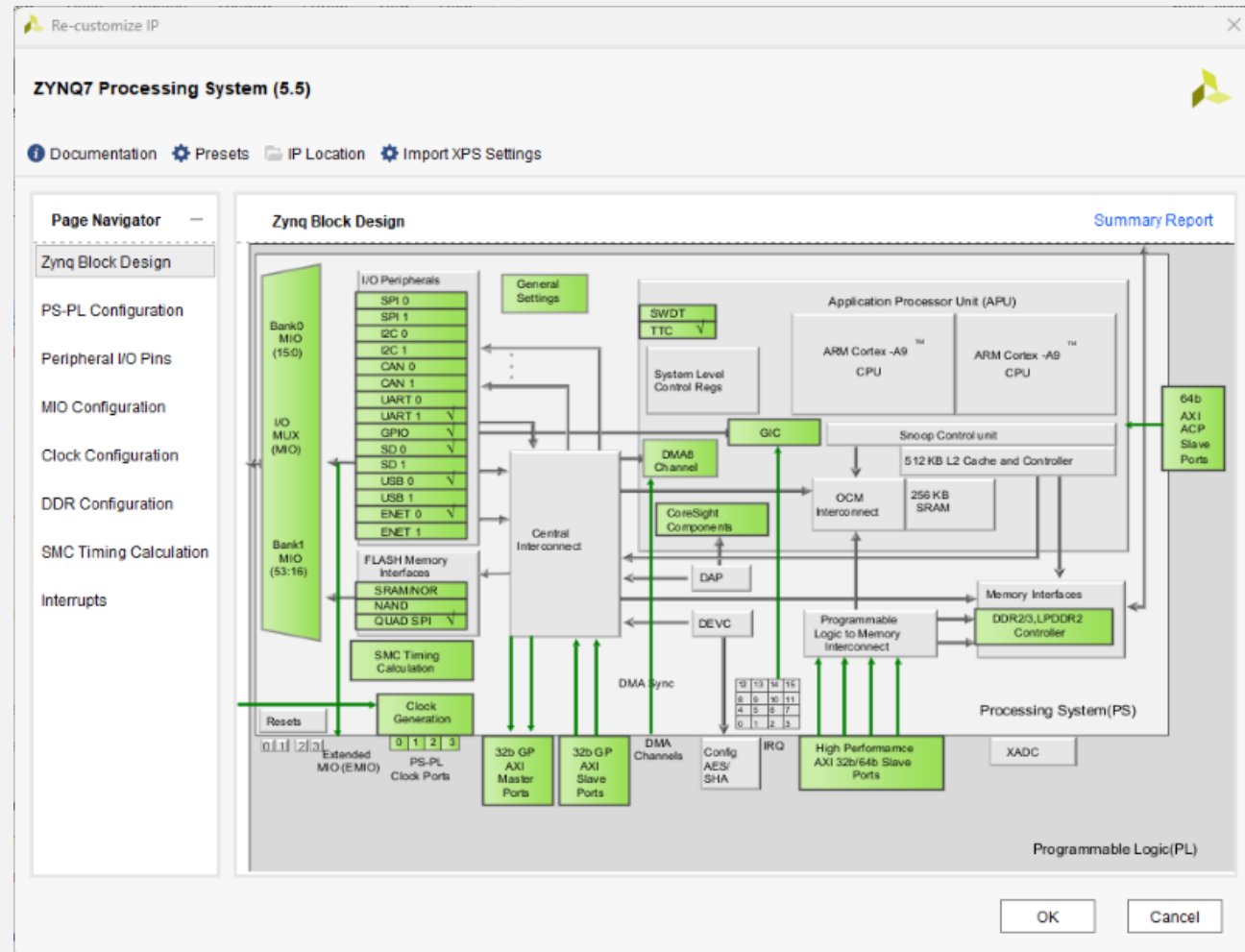
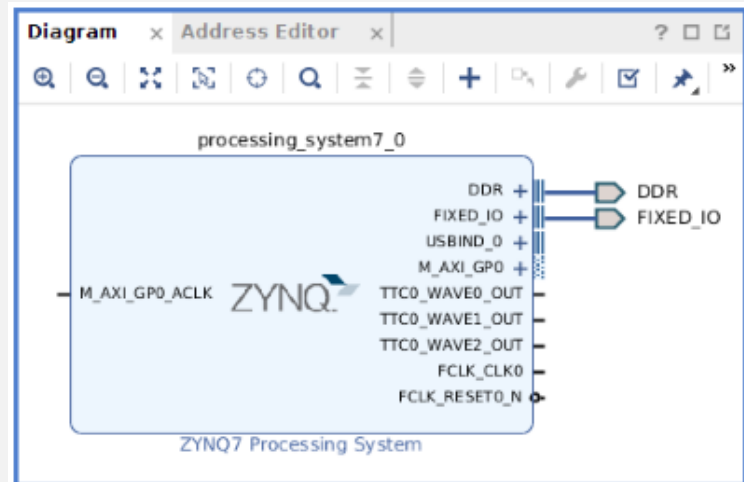
Labs 1: Objectives

- Acquire the knowledge of the SoC-FPGA design flow using the Vitis Unified Software Platform.
- Create the hardware to configure the FPGA part of the SoC, configure the PS instantiate the GPIO blocks and understand the communication between the different components of the design
- Create the 'C' application that will run on the PS to control the reading and the writing of the generated hardware
- Test the complete design on the ZedBoard platform to verify the implementation.

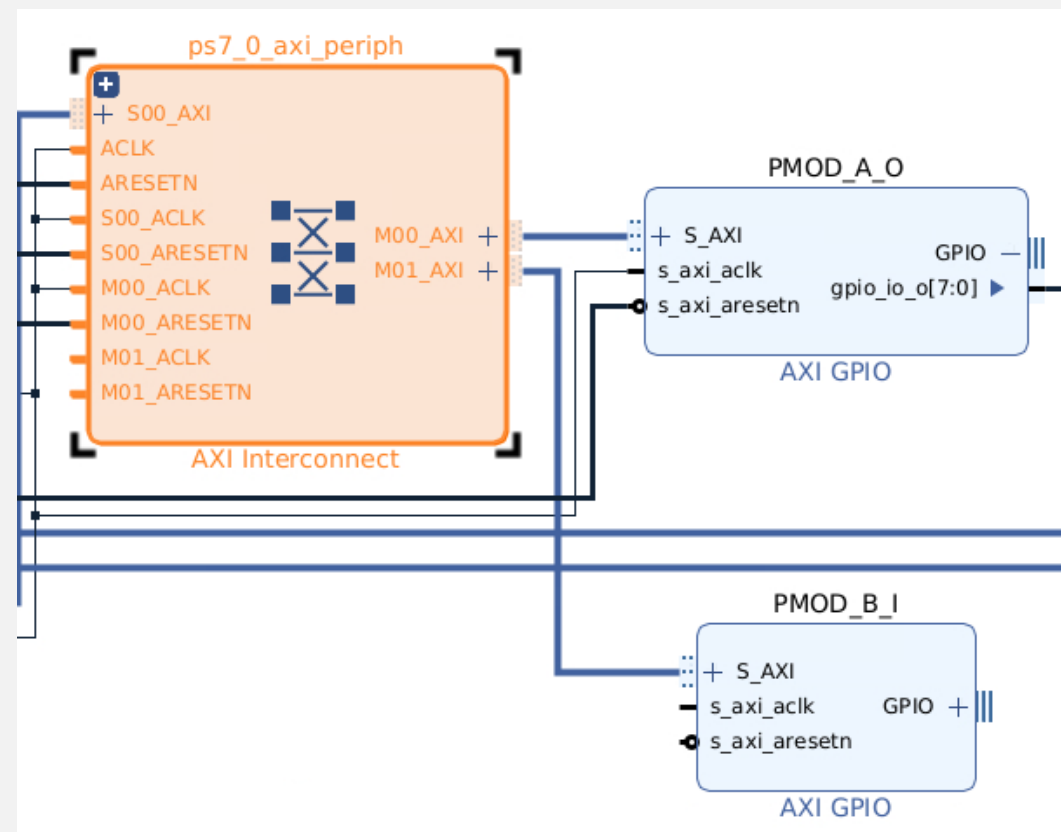
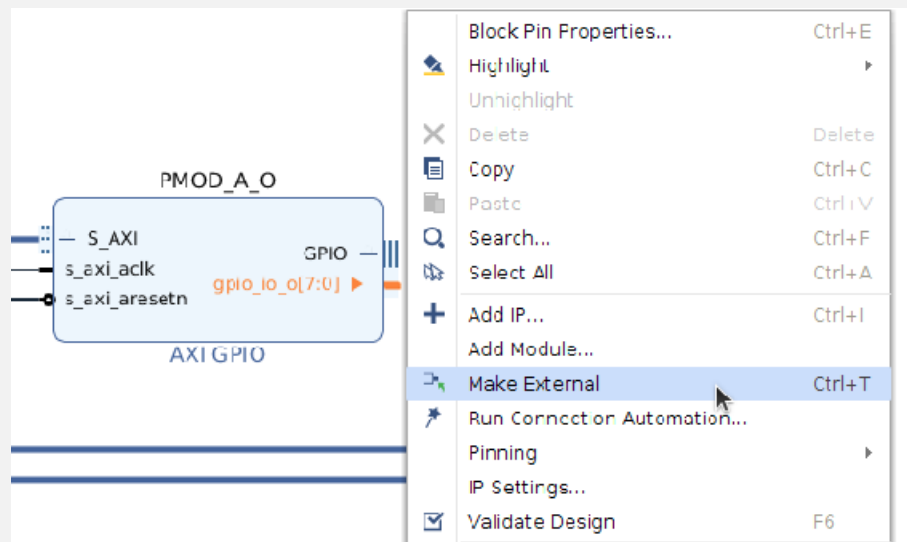
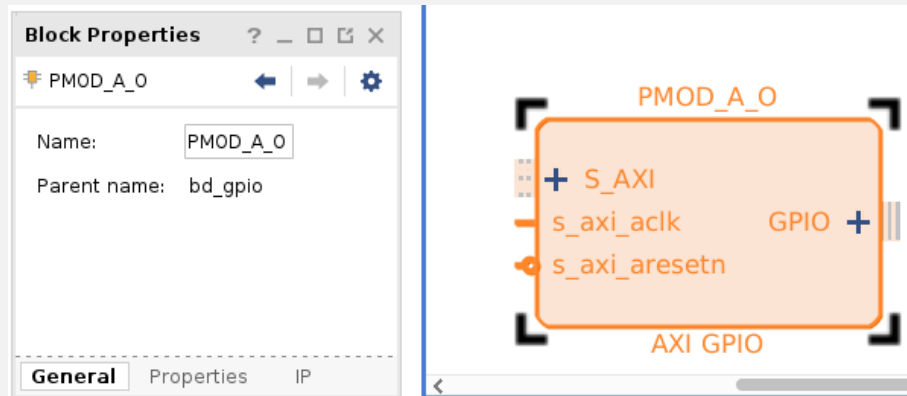
Labs 1: Design description



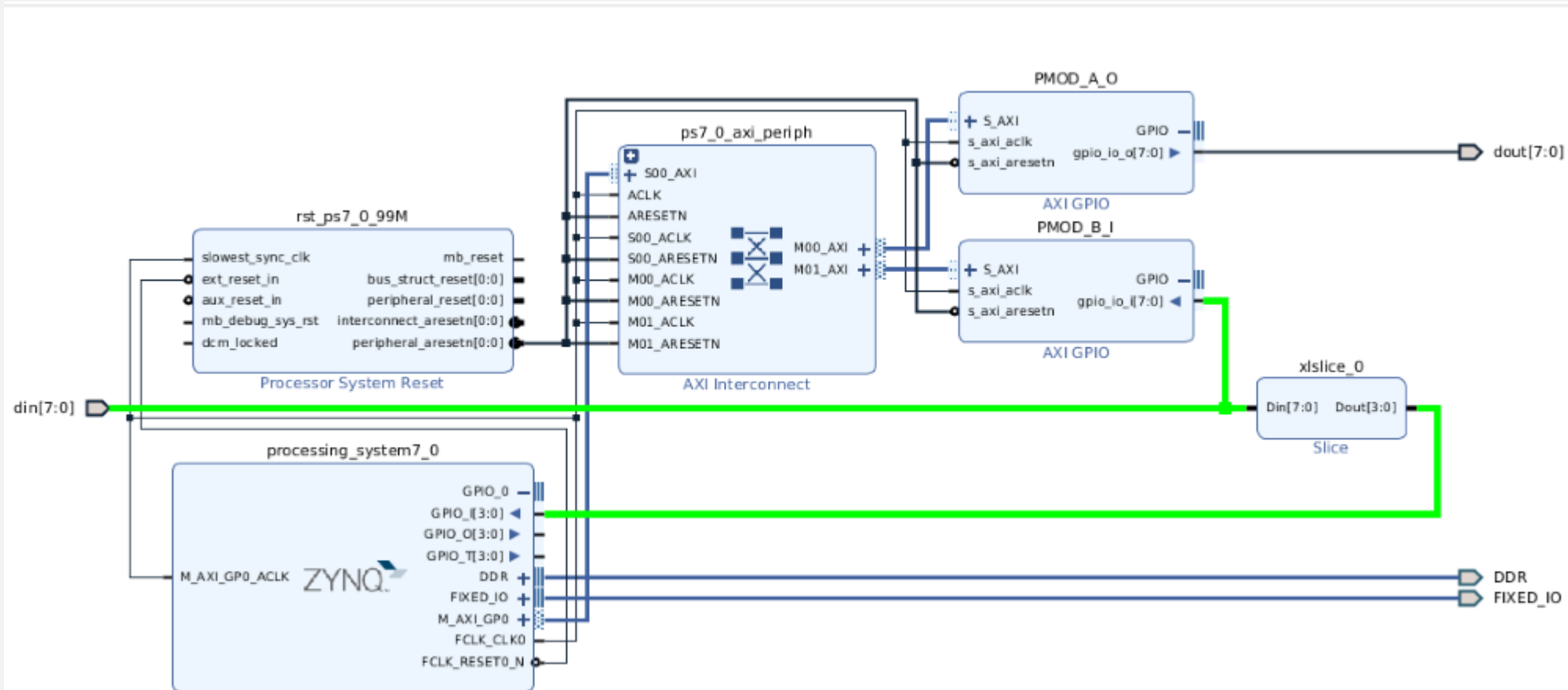
Labs 1: Hardware



Labs 1: Steps



Labs 1: Final Block Design



Labs 1: Software

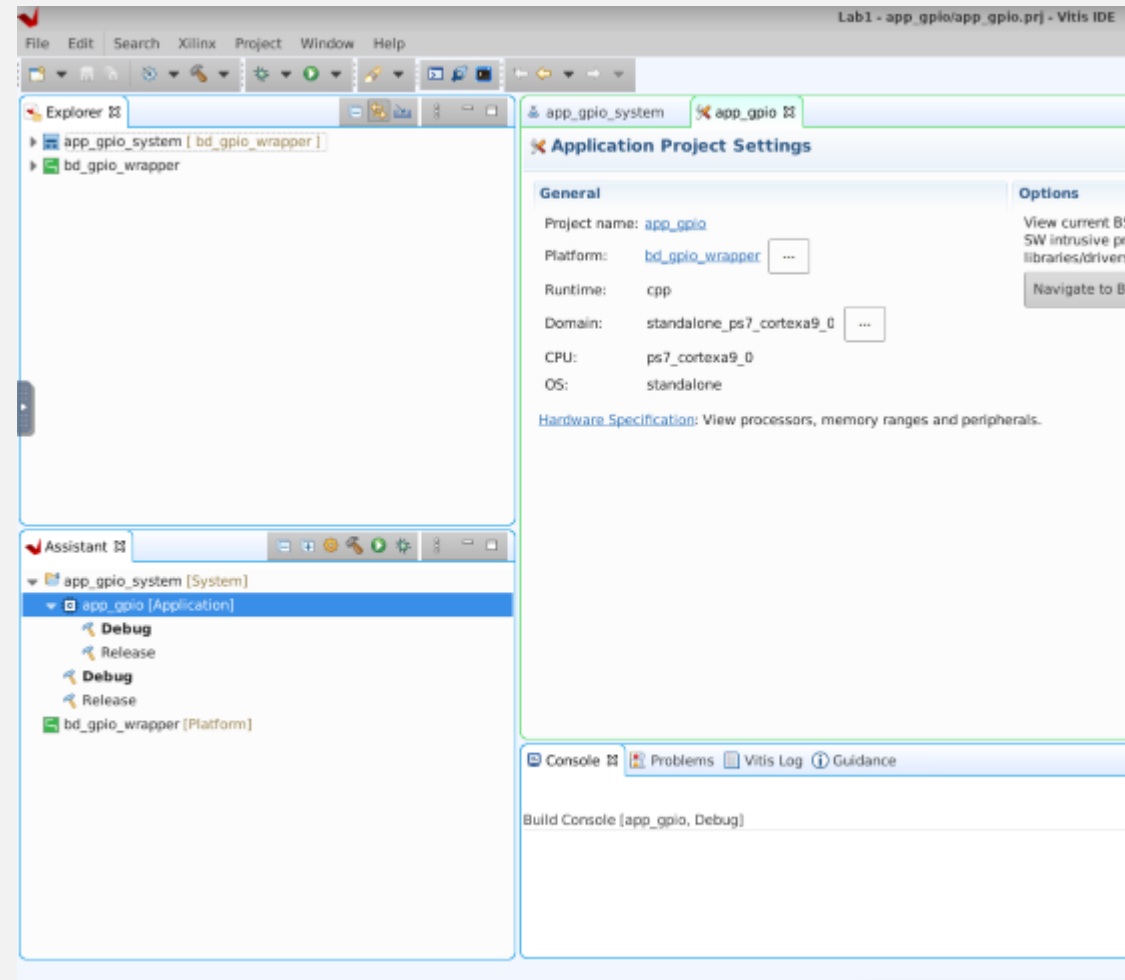
- Application project
- C program
- AXI Communication

```
Build Console [app_gpio, Debug]

Building target: app_gpio.elf
Invoking: ARM v7 gcc linker
arm-none-eabi-gcc -mcpu=cortex-a9 -mfpu=vfpv3 -mfloat-abi=hard -Wl,-build-id=0 -o app_gpio.elf
Finished building target: app_gpio.elf

Invoking: ARM v7 Print Size
arm-none-eabi-size app_gpio.elf |tee "app_gpio.elf.size"
  text  data  bss  dec  hex filename
27021  1184  22616  50821  c685 app_gpio.elf
Finished building: app_gpio.elf.size

16:39:16 Build Finished (took 645ms)
```



Labs 1: Results

- PL Hardware
- PS program
- AXI Communication
- PMOD data transfer

Optional:

- Challenge

```
PMODA Output: 213, PMODB Receive: 213 PSGPIO Receive 13
PMODA Output: 214, PMODB Receive: 214 PSGPIO Receive 13
PMODA Output: 215, PMODB Receive: 215 PSGPIO Receive 13
PMODA Output: 216, PMODB Receive: 216 PSGPIO Receive 13
PMODA Output: 217, PMODB Receive: 217 PSGPIO Receive 13
PMODA Output: 218, PMODB Receive: 218 PSGPIO Receive 13
PMODA Output: 219, PMODB Receive: 219 PSGPIO Receive 13
PMODA Output: 220, PMODB Receive: 220 PSGPIO Receive 13
PMODA Output: 221, PMODB Receive: 221 PSGPIO Receive 13
PMODA Output: 222, PMODB Receive: 222 PSGPIO Receive 13
PMODA Output: 223, PMODB Receive: 223 PSGPIO Receive 13
PMODA Output: 224, PMODB Receive: 224 PSGPIO Receive 14
PMODA Output: 225, PMODB Receive: 225 PSGPIO Receive 14
PMODA Output: 226, PMODB Receive: 226 PSGPIO Receive 14
PMODA Output: 227, PMODB Receive: 227 PSGPIO Receive 14
PMODA Output: 228, PMODB Receive: 228 PSGPIO Receive 14
PMODA Output: 229, PMODB Receive: 229 PSGPIO Receive 14
PMODA Output: 230, PMODB Receive: 230 PSGPIO Receive 14
PMODA Output: 231, PMODB Receive: 231 PSGPIO Receive 14
PMODA Output: 232, PMODB Receive: 232 PSGPIO Receive 14
PMODA Output: 233, PMODB Receive: 233 PSGPIO Receive 14
PMODA Output: 234, PMODB Receive: 234 PSGPIO Receive 14
PMODA Output: 235, PMODB Receive: 235 PSGPIO Receive 14
PMODA Output: 236, PMODB Receive: 236 PSGPIO Receive 14
PMODA Output: 237, PMODB Receive: 237 PSGPIO Receive 14
PMODA Output: 238, PMODB Receive: 238 PSGPIO Receive 14
PMODA Output: 239, PMODB Receive: 239 PSGPIO Receive 14
```



User: student
Password: workspace

WARNING: Limited space.
Please handle the power supply connections, development boards, and computers with care.