1st Mesoamerican Workshop on Reconfigurable X-ray Scientific Instrumentation for Cultural Heritage

The RVI communication block: ComBlock

Antigua Guatemala, June 2025

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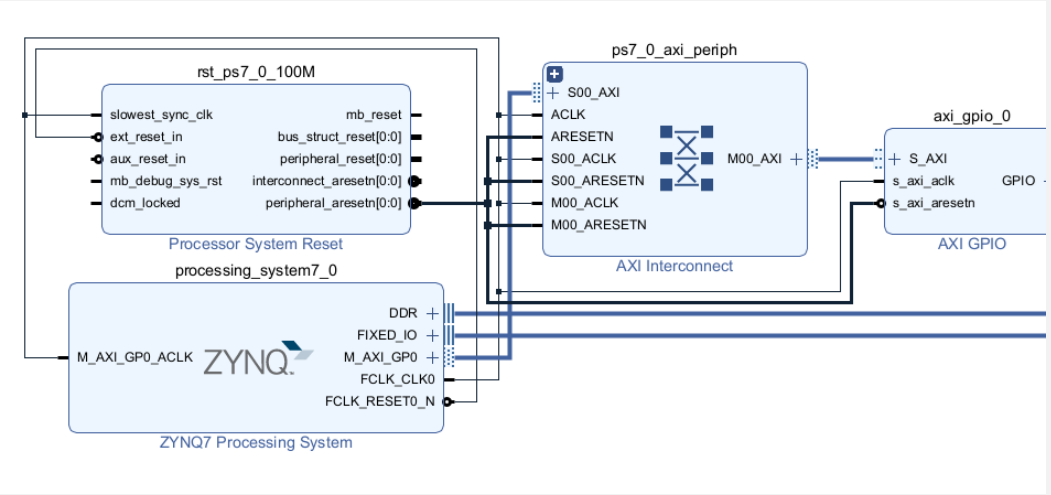
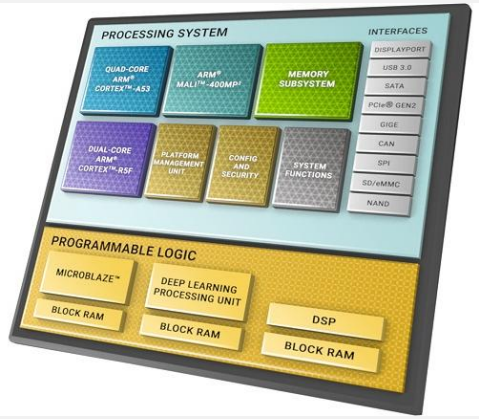
Introduction

- Vendor specific interconnects (AXI, AVALON, Chiplink).
- What we learned yesterday?
  - ✓ AXI interconnect,
  - ✓ memory address,
  - ✓ data.
- Communication Block (ComBlock).

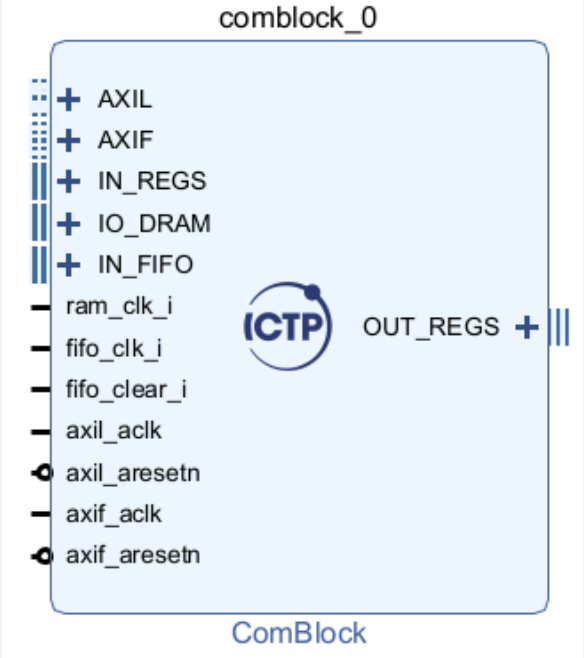




What is the ComBlock?

A communication block that abstracts you from the AXI protocol.

- Interconnects: AXI - Known interfaces (registers, RAM and FIFOs).
- Configurable resources, width, length, etc.
- Simple Clock-Domain-Crossing with FIFOs and TDPRAM.
- C driver for easy complete project integration.



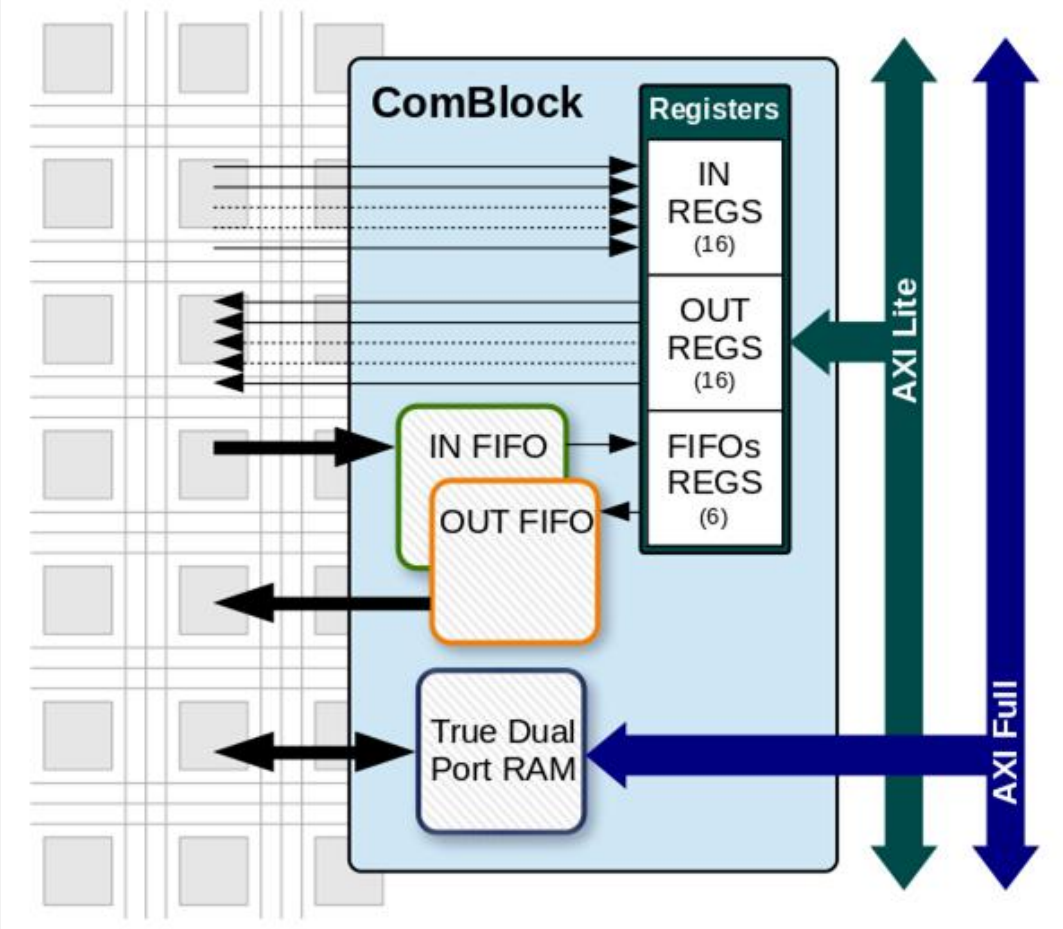
Features

Input/Output Interfaces:

- I/O Registers
- I/O FIFOs
- TDPRAM (True Dual Port RAM) Memory

AXI Compatibility:

- AXI Lite: Supports access to registers and FIFOs through this lightweight, low-bandwidth interface.
- AXI Full: Used to access TDPRAM, ideal for larger, high-performance data transfers.

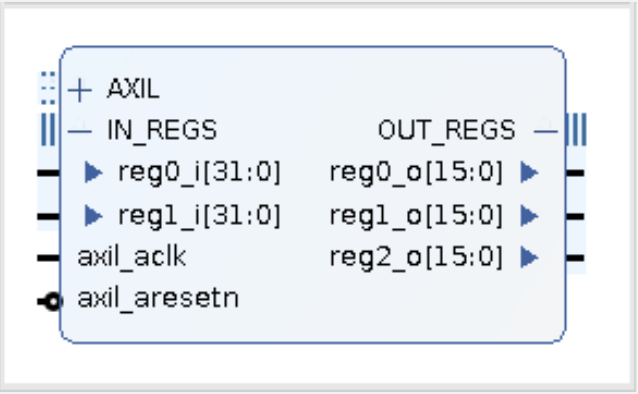


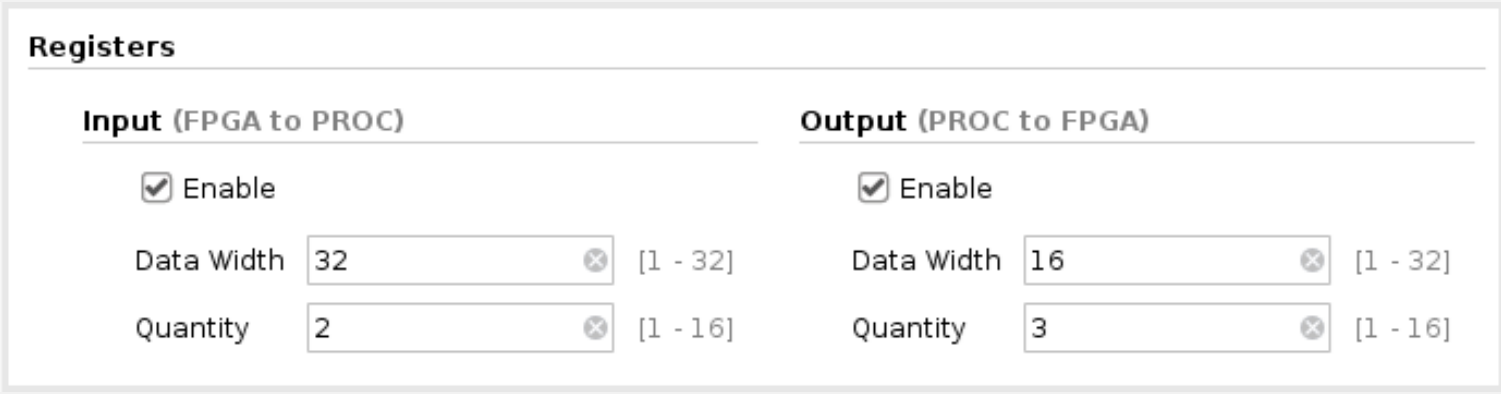
Registers

16 Input Registers: Communication from the FPGA to the processor.
16 Output Registers: Communication from the processor to the FPGA.

Flexible Configuration:

- User-configurable data width: From 1 to 32 bits, depending on application requirements.
- Independent enable for input and output registers: Allowing a more optimized design tailored to different communication needs.





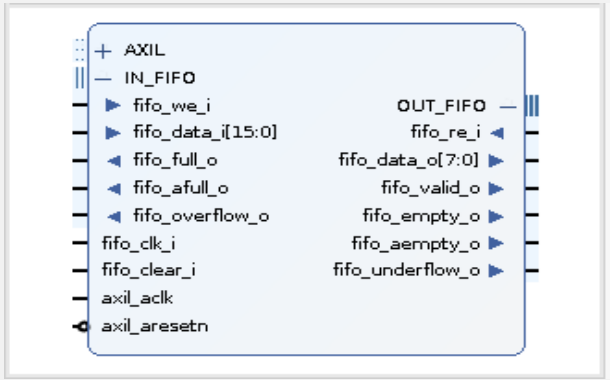
FIFOs

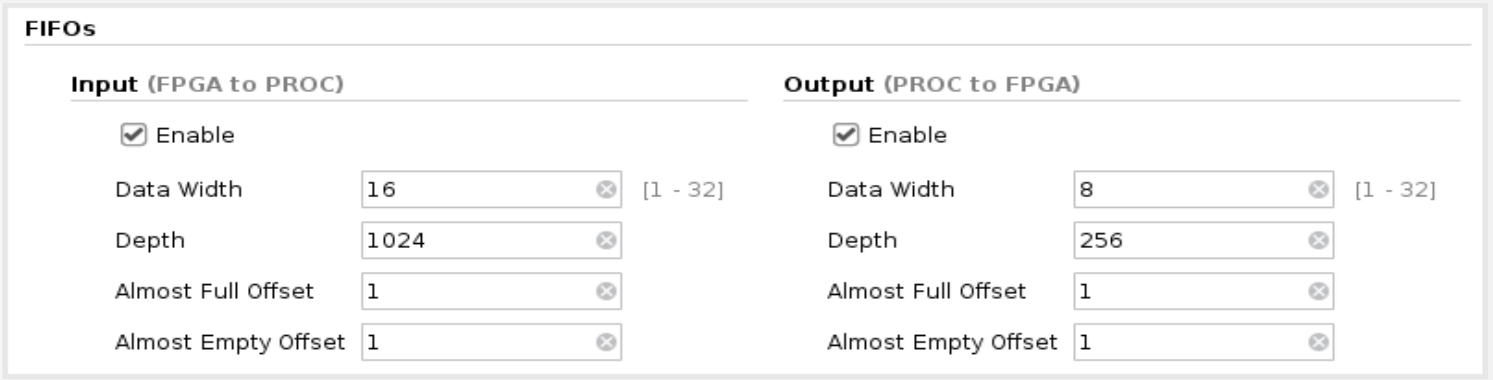
Input and Output FIFOs: Input: FPGA → Processor, Output: Processor → FPGA

Customizable Width and Depth: Both the data width and FIFO depth can be configured.

Asynchronous Operation: The FIFOs support safe clock domain crossing, enabling integration into heterogeneous systems.

Processor-Side Control Registers: Allow reading of occupancy level, as well as resetting or clearing the queues.





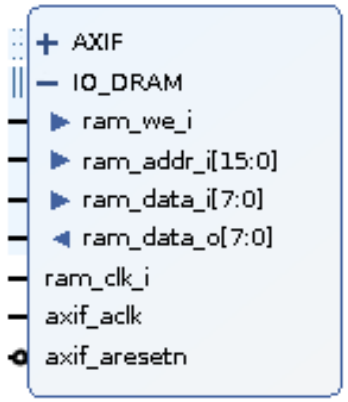
TDPRAM

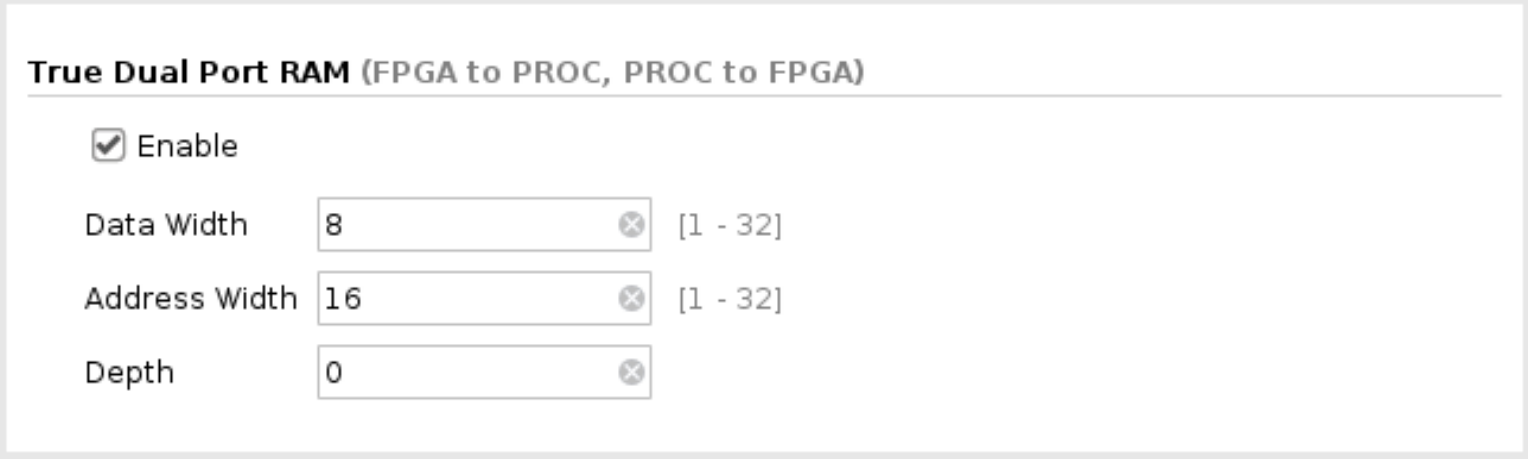
Simultaneous Bidirectional Access: The FPGA and processor can perform read and write operations independently and concurrently.

Clock Domain Crossing (CDC): Designed to operate in systems with different clock domains, enabling safe and lossless data transfer.

User-Configurable Parameters: Data width, address width, and depth.

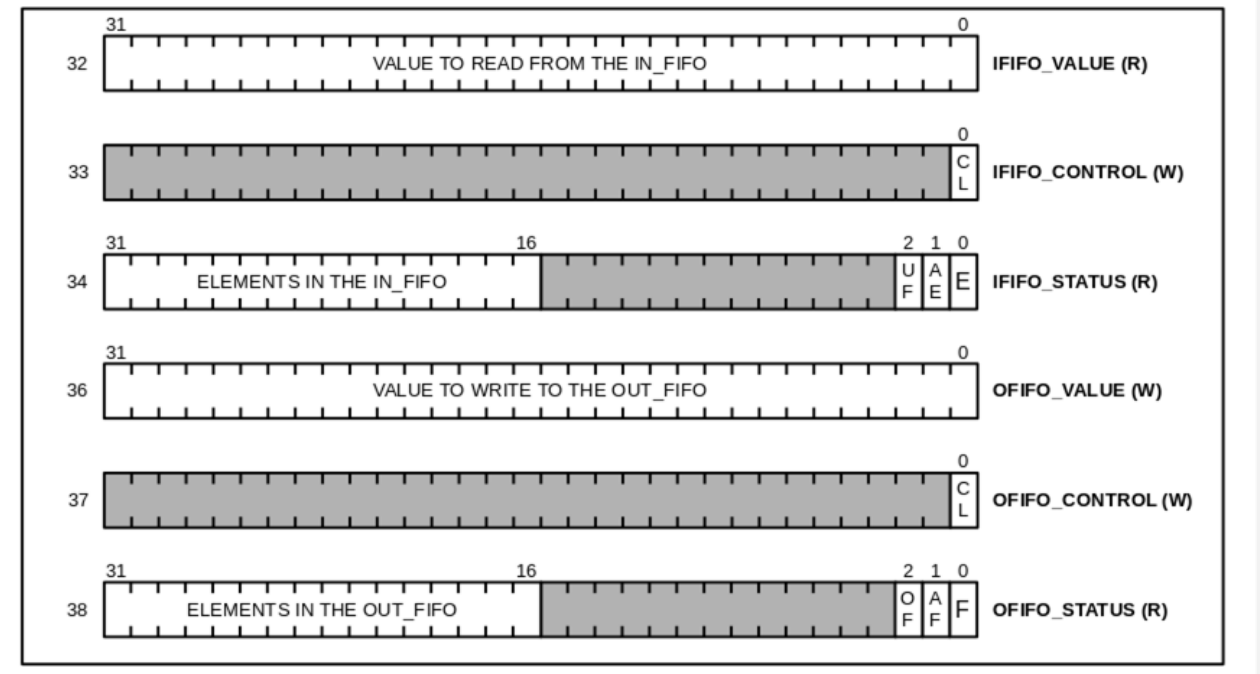
Example: If the address width is 10 bits, the default depth will be $2^{10} = 1024$.





Processor Interaction

- Device information in **xparameters.h**.
- Register mappings in **comblock.h**.
- CB_IREG, CB_OREG, ...
- Control registers.



C Drives

- Read and write functions **single memory position**:

  void **cbWrite**(UINTPTR baseaddr, u32 reg, u32 value)

  u32 **cbRead**(UINTPTR baseaddr, u32 reg)

- Read and write several **contiguous memory positions**:

  void **cbWriteBulk**(UINTPTR baseaddr, int *buffer, u32 depth)

  void **cbReadBulk**(int *buffer, UINTPTR baseaddr, u32 depth)

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Lab 2: Reconfigurable instrumentation on SoC-FPGA

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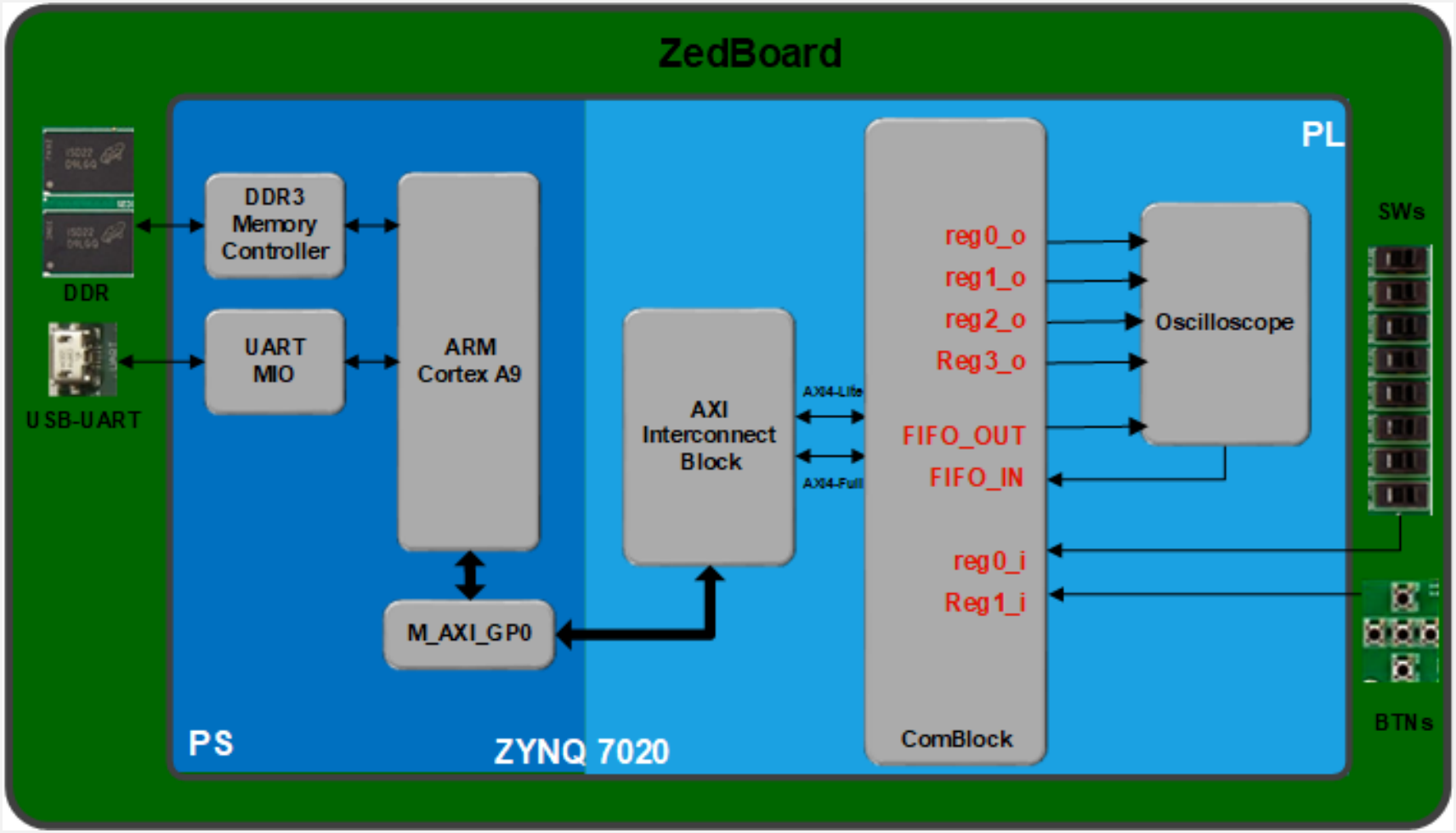
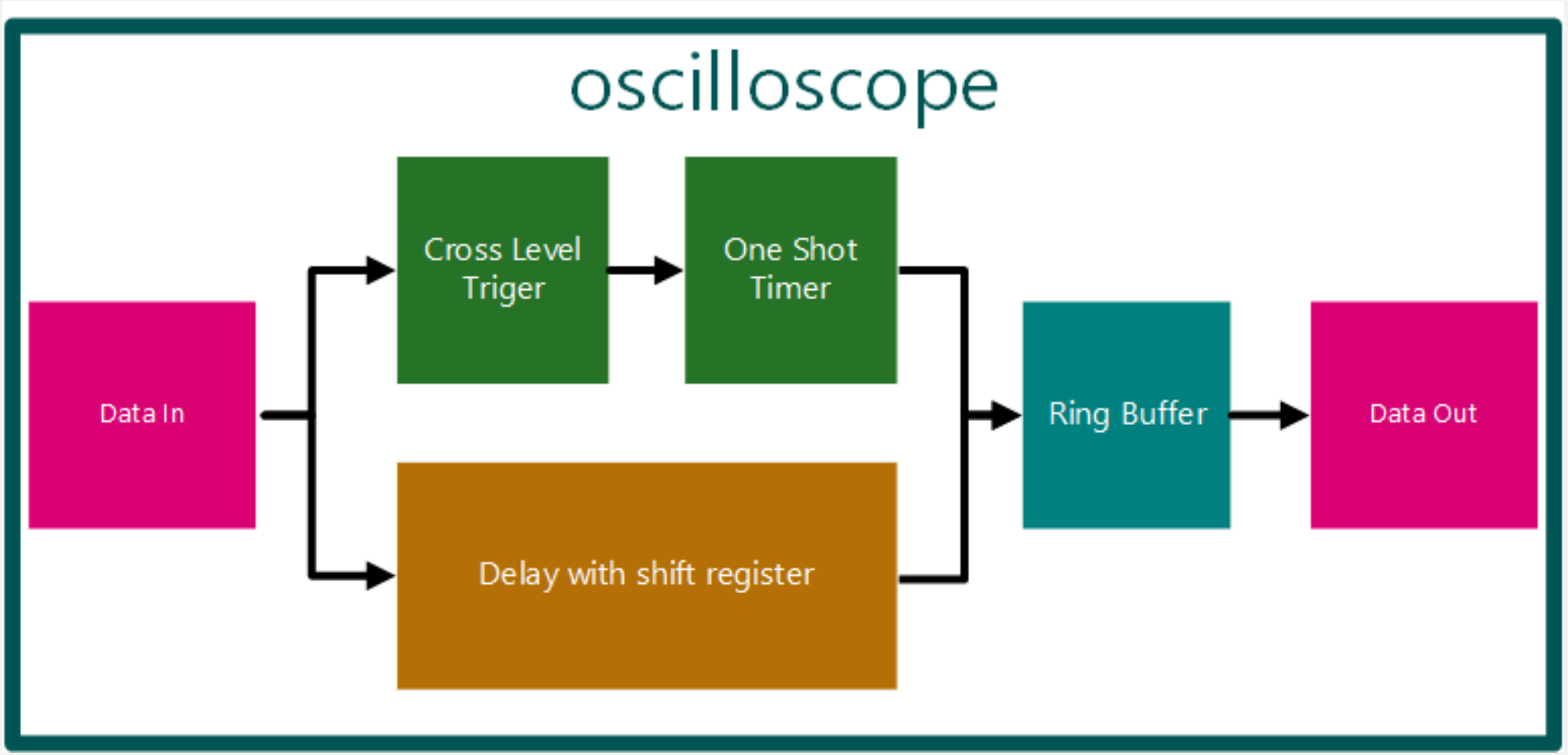
Labs 2: Objectives

- Simulate a cross-level trigger and understand the VHDL code.
- Use and configuration of the **ComBlock** IP.
- Understand the data transfer between PL and PS using **ComBlock** IP.
- Instantiate RTL blocks and control them through the **ComBlock** registers.
- Perform data streaming to the **oscilloscope** through the **ComBlock** FIFO.
- Test the complete design on the ZedBoard platform to verify the implementation.

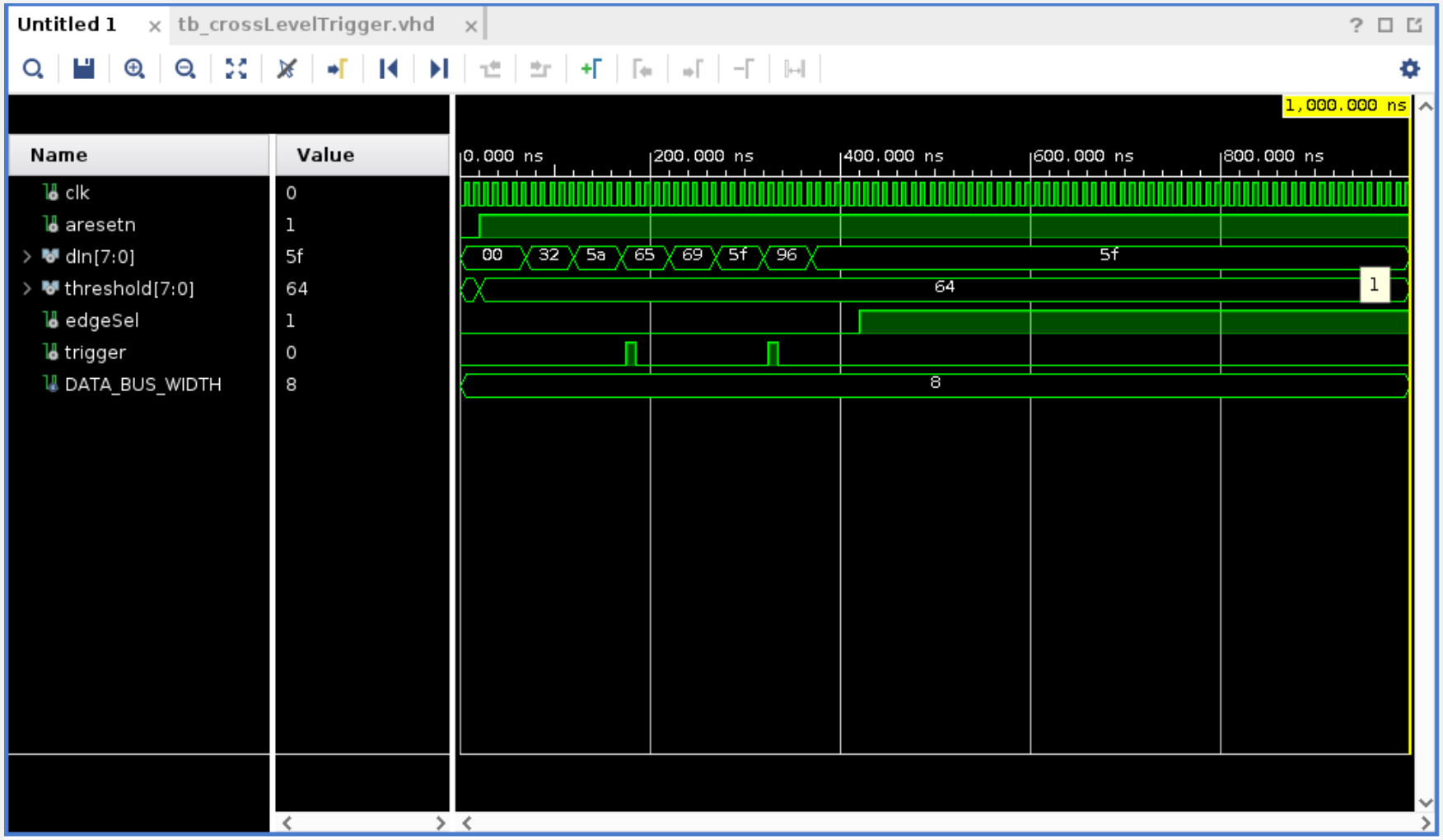
Labs 2: Design description



Labs 2: Oscilloscope

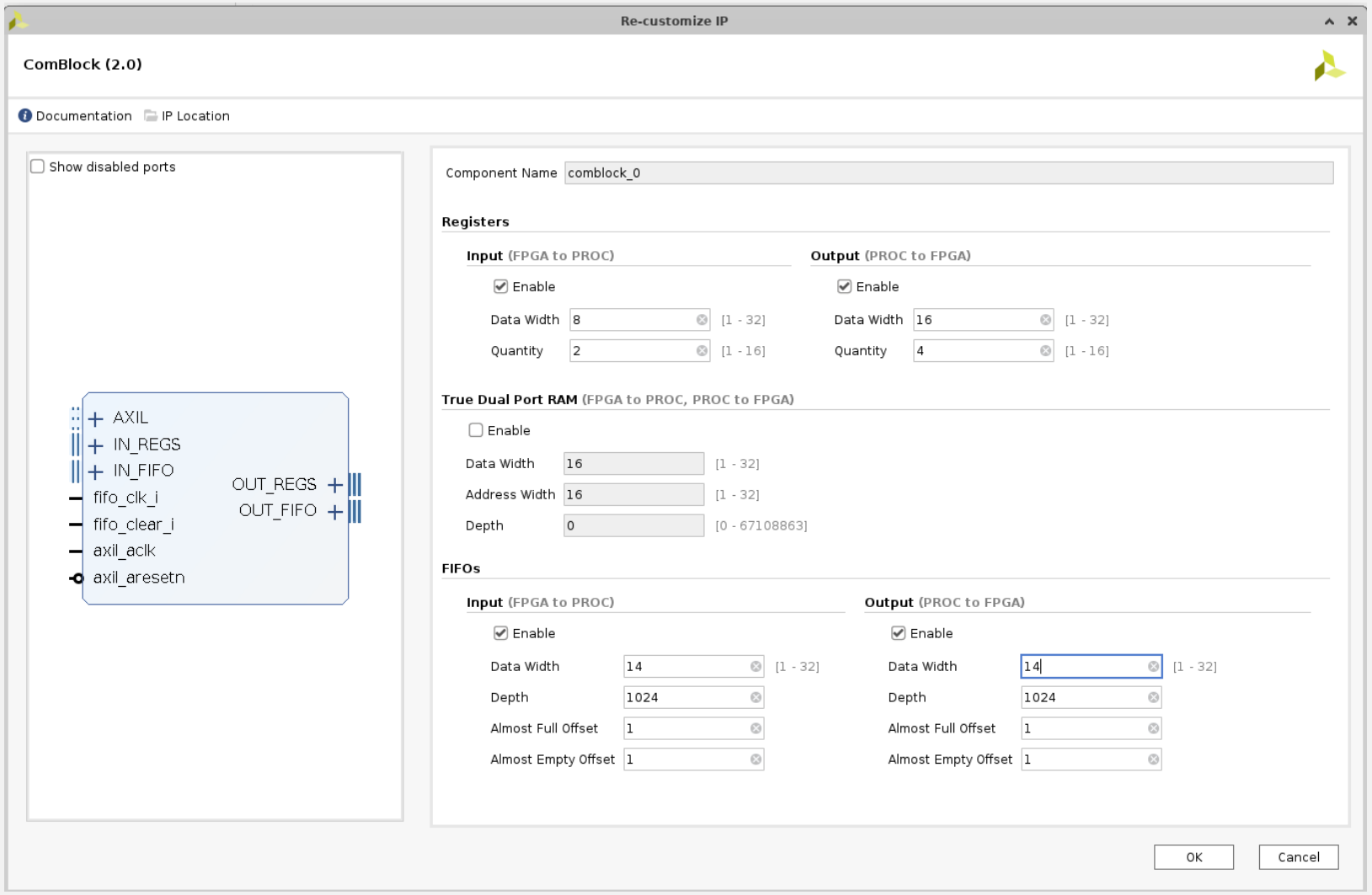


Labs 2: Simulation



Labs 2: Hardware

Comblock Configuration



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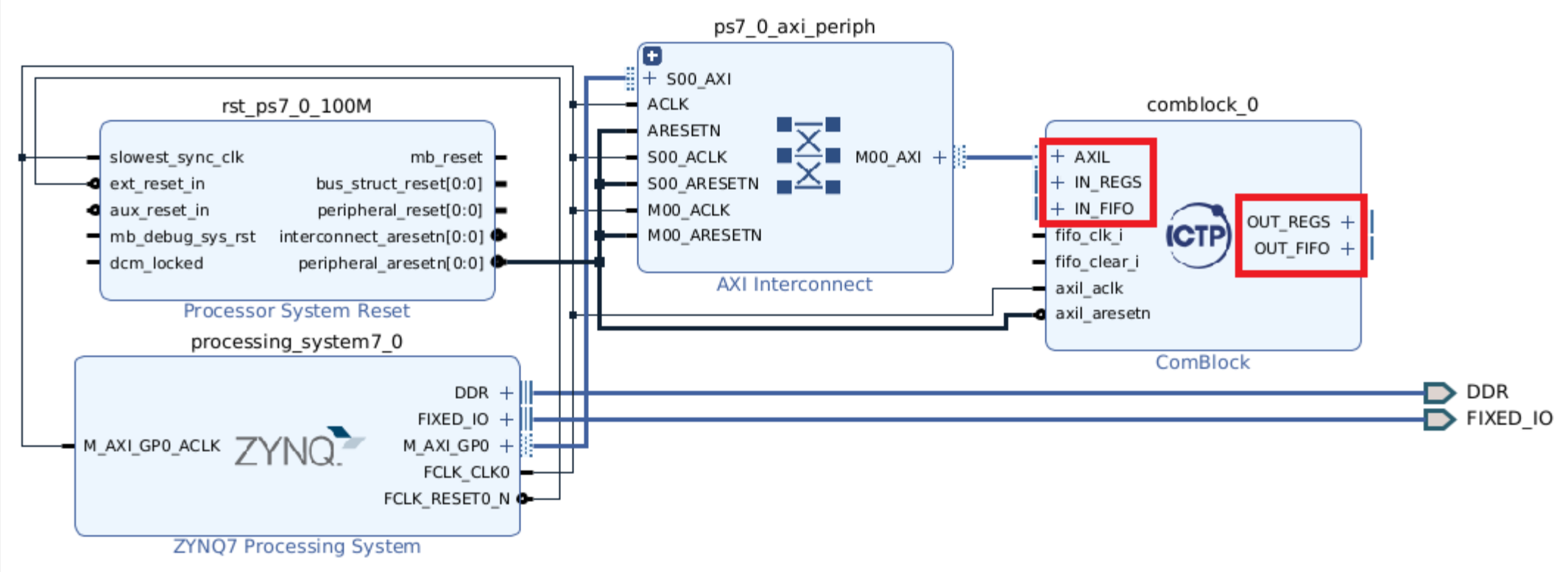

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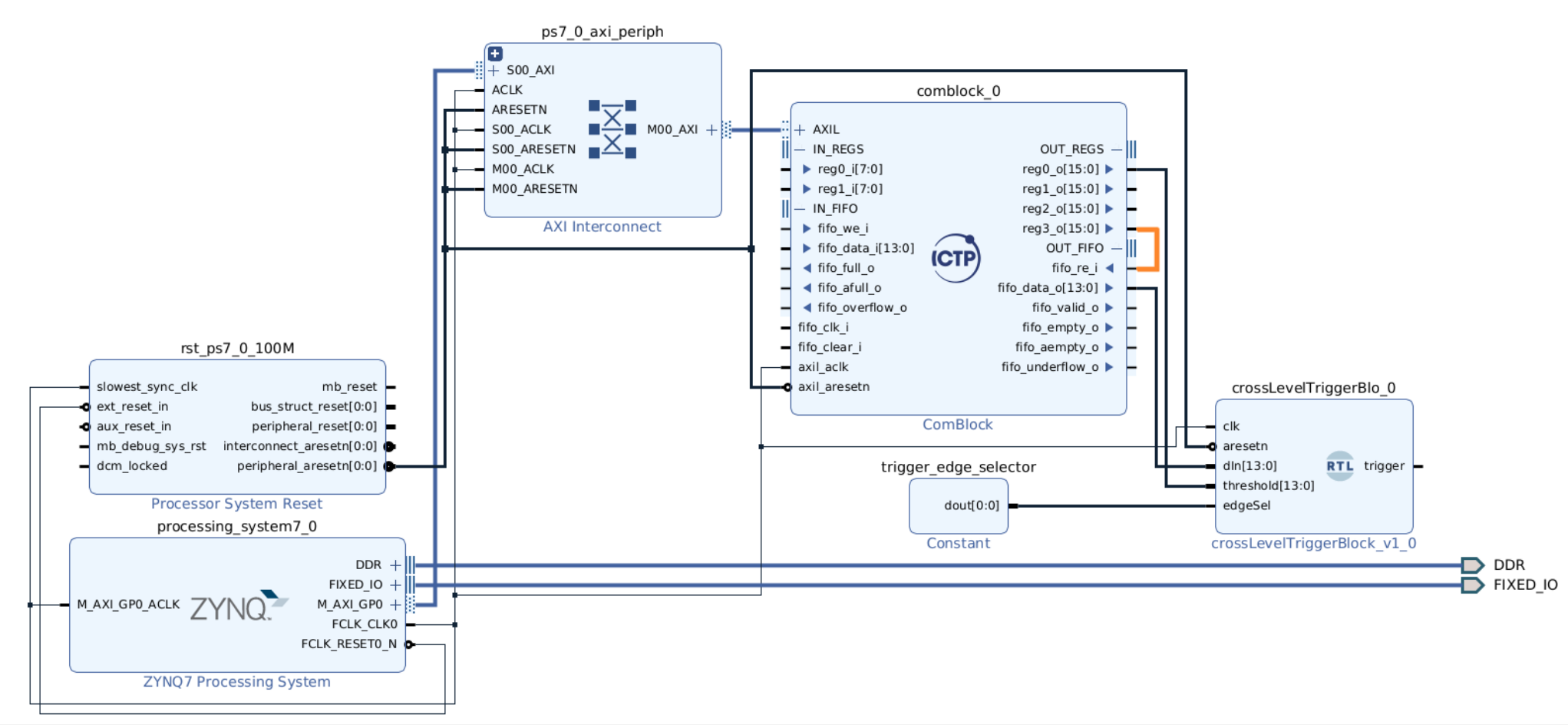
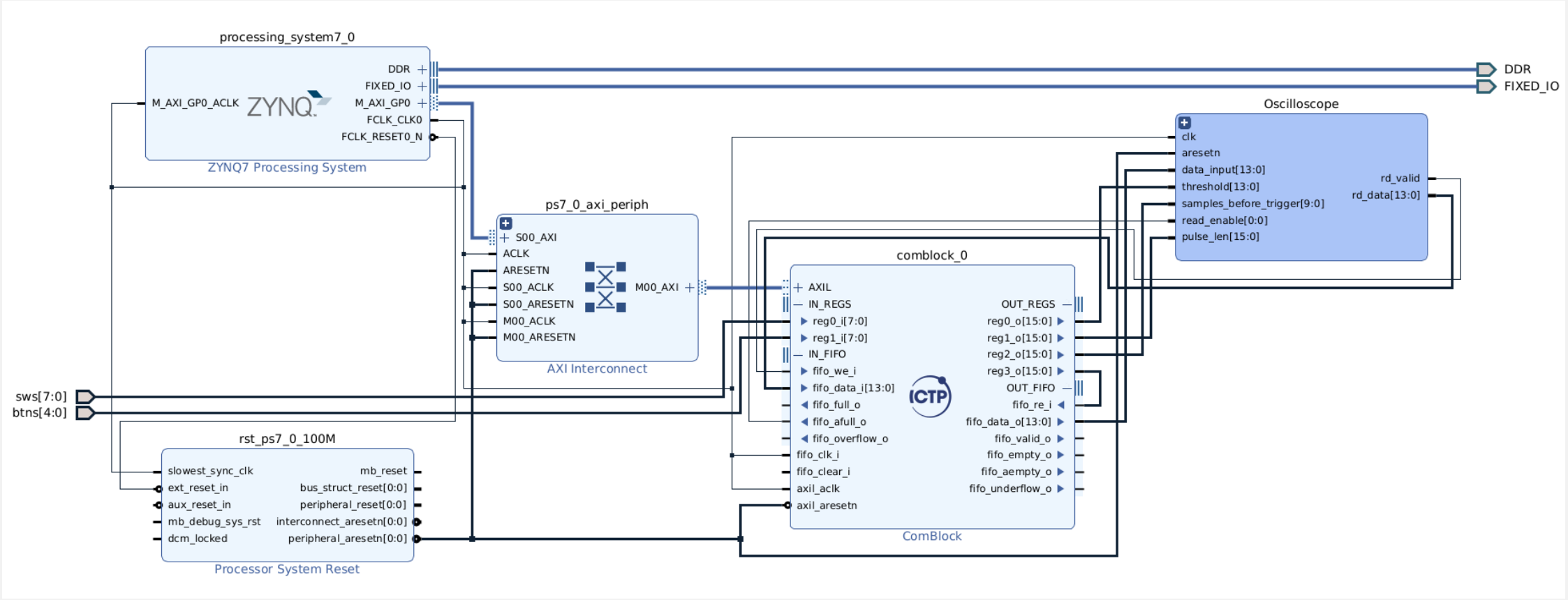
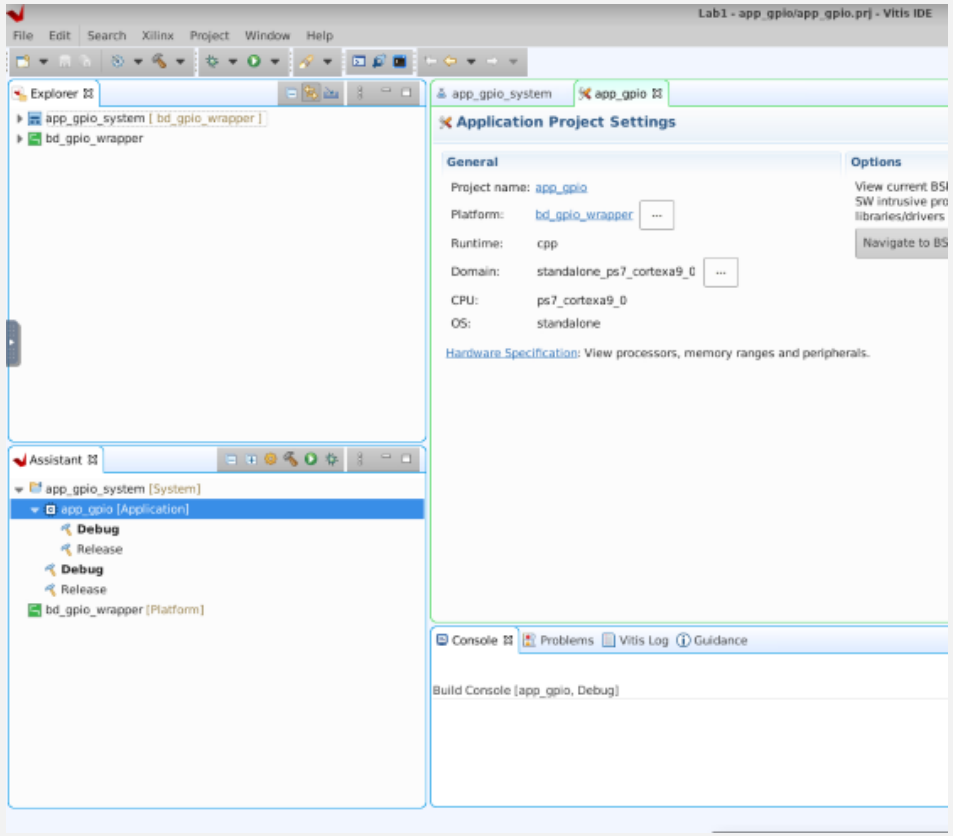


Labs 2: Final Block Design



Labs 2: Software

- C driver using ComBlock instructions
- Handles configuration and data exchange.
- Uses the waveform.h file.
- Allows changes to threshold, pre-trigger samples, and pulse length.
- Software interface lets you adjust parameter values.
- Buttons are used to interact with the oscilloscope.



Labs 2: Results

- PL Hardware
- PS program
- Comblock Communication
- data transfer, that you plot

Optional:

- Challenge