Joint ICTP-IAEA School on Detector Signal Processing and Machine Learning for Scientific Instrumentation and Reconfigurable Computing

The Abdus Salam International Centre for Theoretical Physics

IAEA International Atomic Energy Agency

unesco United Nations Educational, Scientific and Cultural Organization

Development Board: Zynq PSoC

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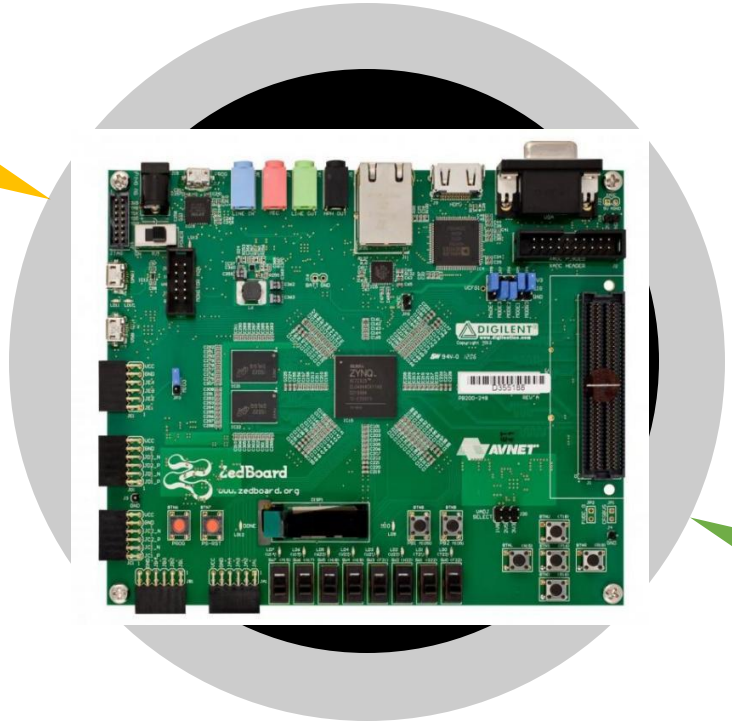
ZedBoard

AVNET

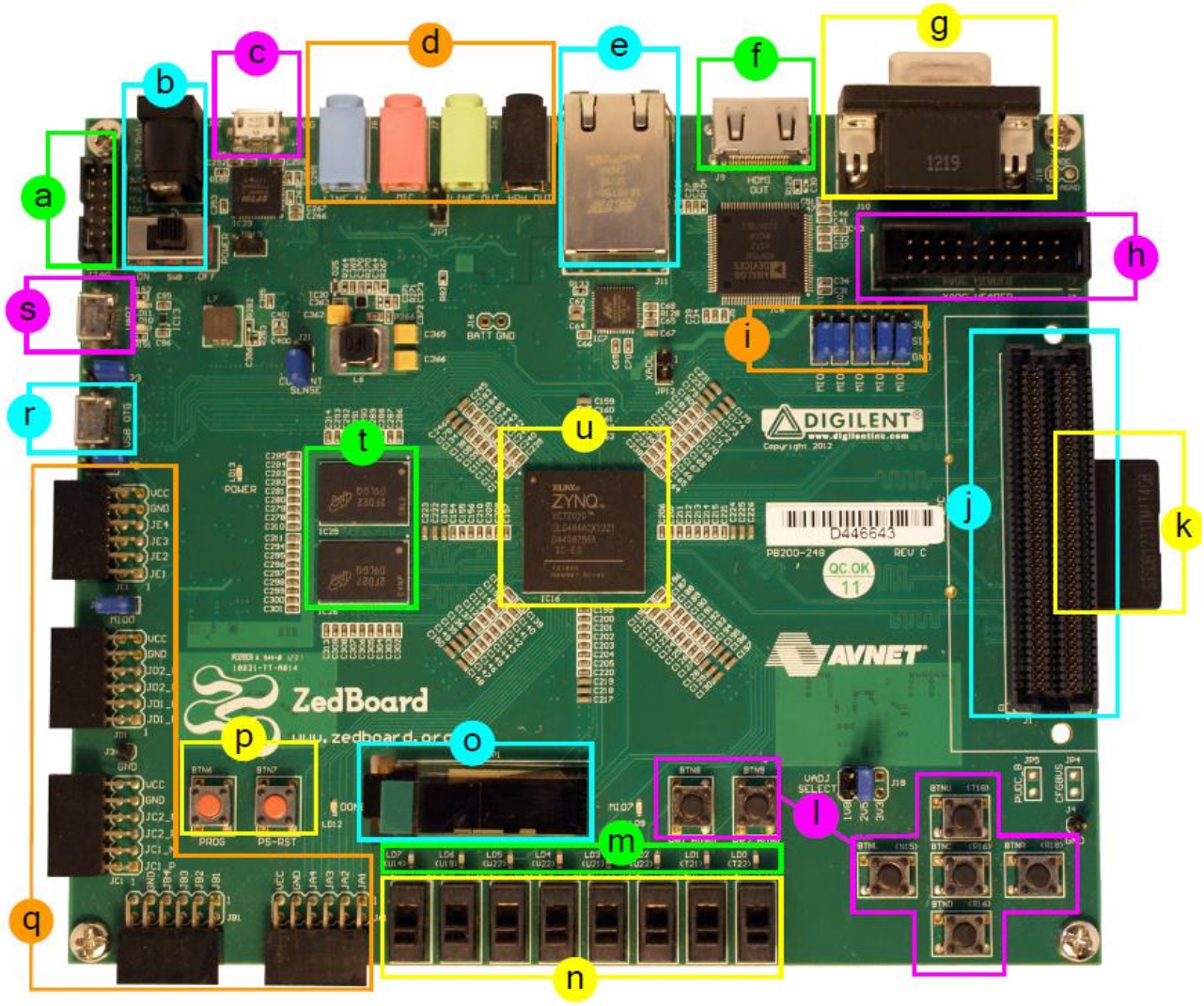
ZedBoard™ is a complete development kit for designers interested in exploring designs using the AMD Xilinx Zynq®-7000 All Programmable SoC. The board contains all the necessary interfaces and supporting functions to enable a wide range of applications.
The expandability features of the board make it ideal for rapid prototyping and proof-of-concept development.



DIGILENT

ZedBoard™ is a low-cost development board for the Xilinx Zynq-7000 all programmable SoC (AP SoC). This board contains everything necessary to create a Linux®, Android®, Windows®, or other ₒₛ/RTOS based design. Additionally, several expansion connectors expose the processing system and programmable logic I/Os for easy user access.

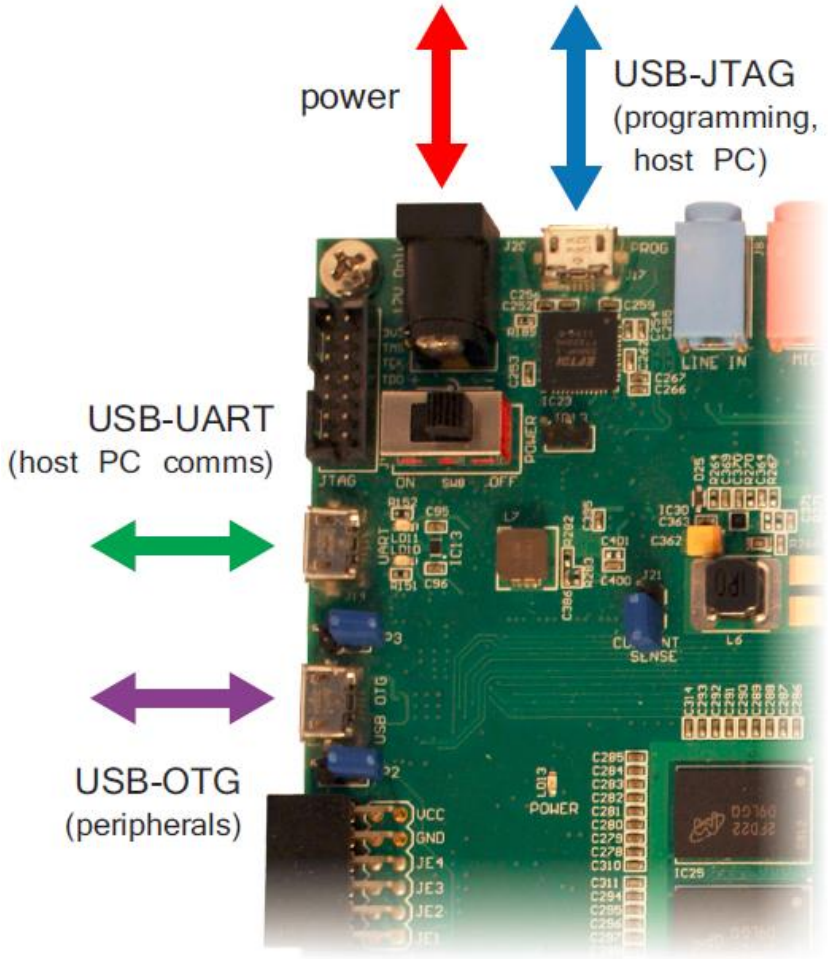
ZedBoard Main Components



a Xilinx JTAG connector
b Power input and switch
c USB-JTAG (programming)
d Audio ports
e Ethernet port
f HDMI port (output)
g VGA port

h XADC header port
i Configuration jumpers
j FMC connector
k SD card (underside)
l User push buttons
m LEDs
n Switches
o OLED display
p Prog & reset push buttons
q 5 x Pmod connector ports
r USB-OTG peripheral port
s USB-UART port
t DDR3 memory
u Zynq device (+ heatsink)

ZedBoard Main Connectors

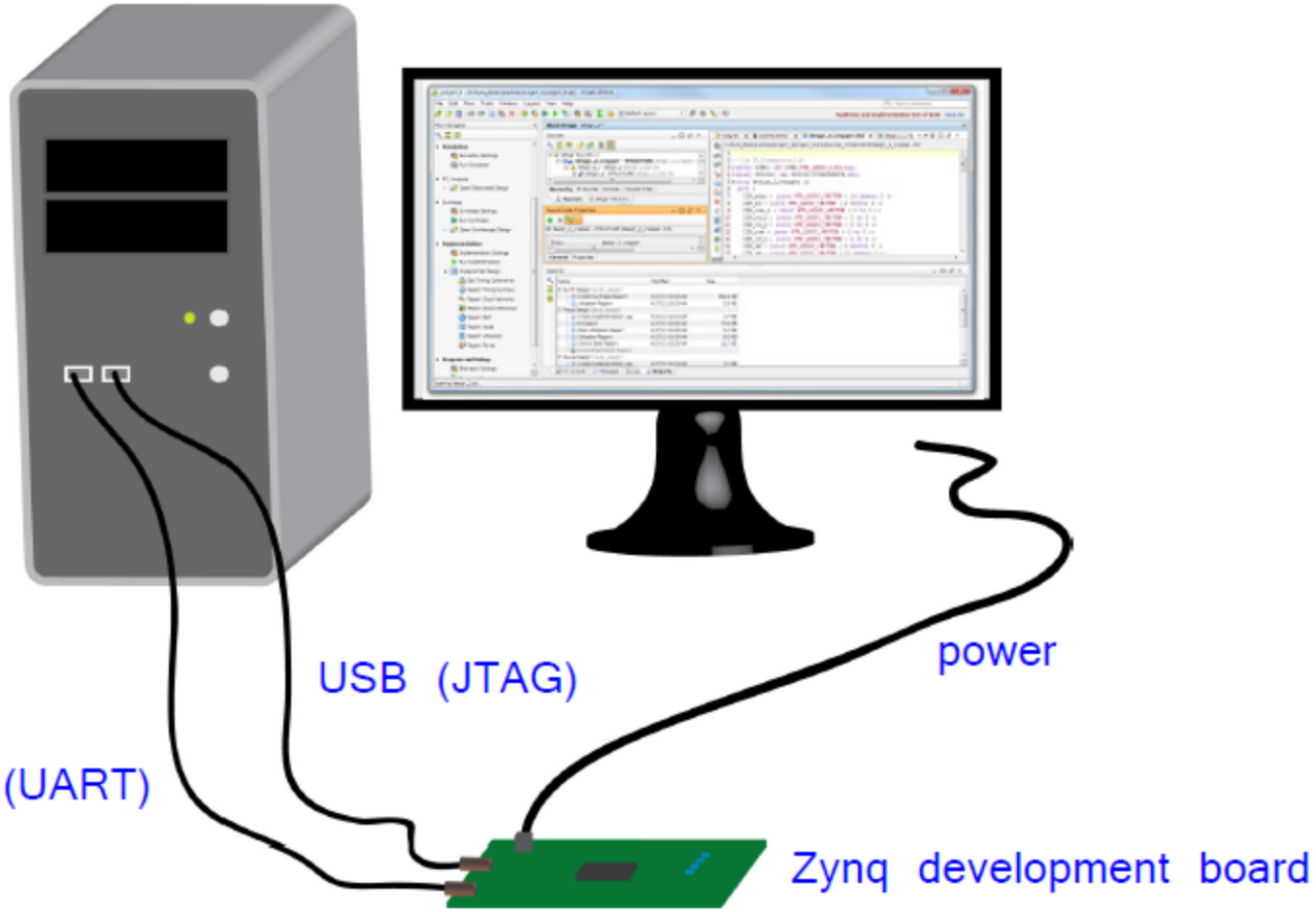


Connection Between PC-ZedBoard

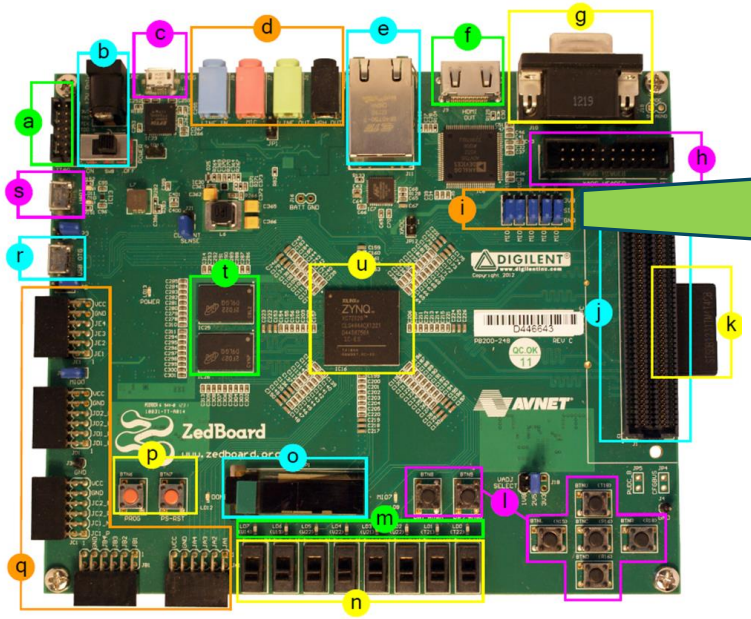
Windows / Linux computer

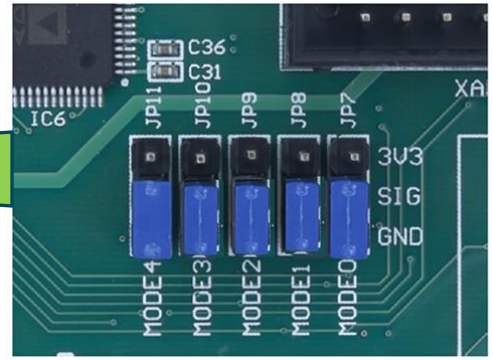
16GB/32GB+ RAM

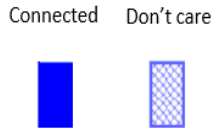
Xilinx design tools

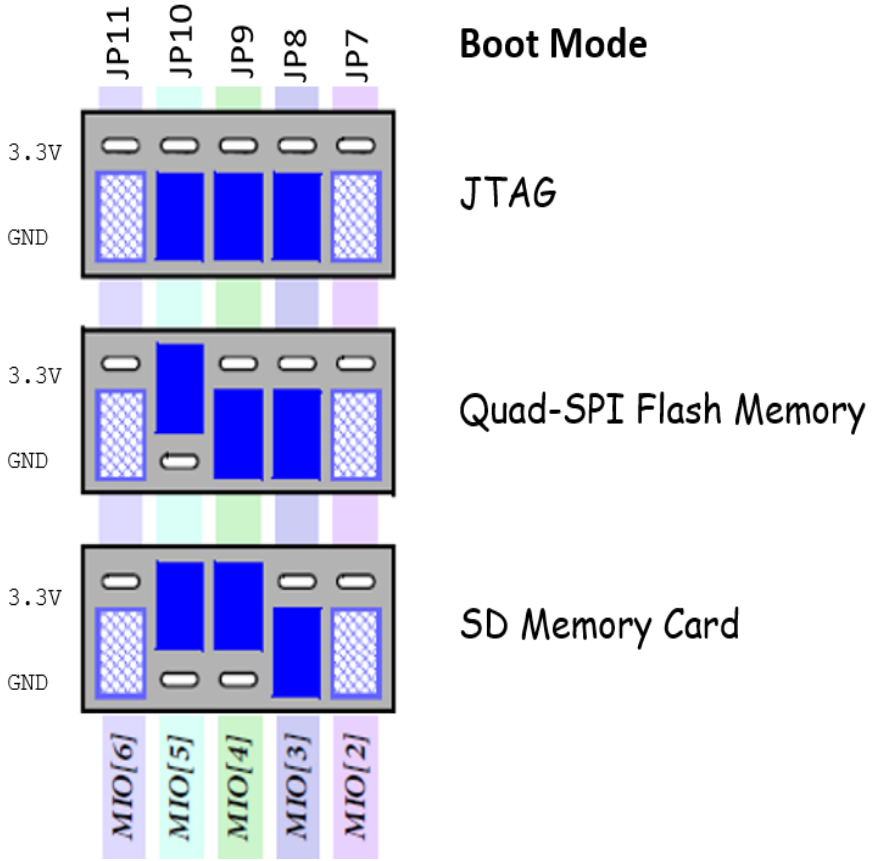


Configuring the ZedBoard - Options









256 Mbit- Serial NOR Flash

PMOD

10/100/1000 Ethernet Phy

USB OTG

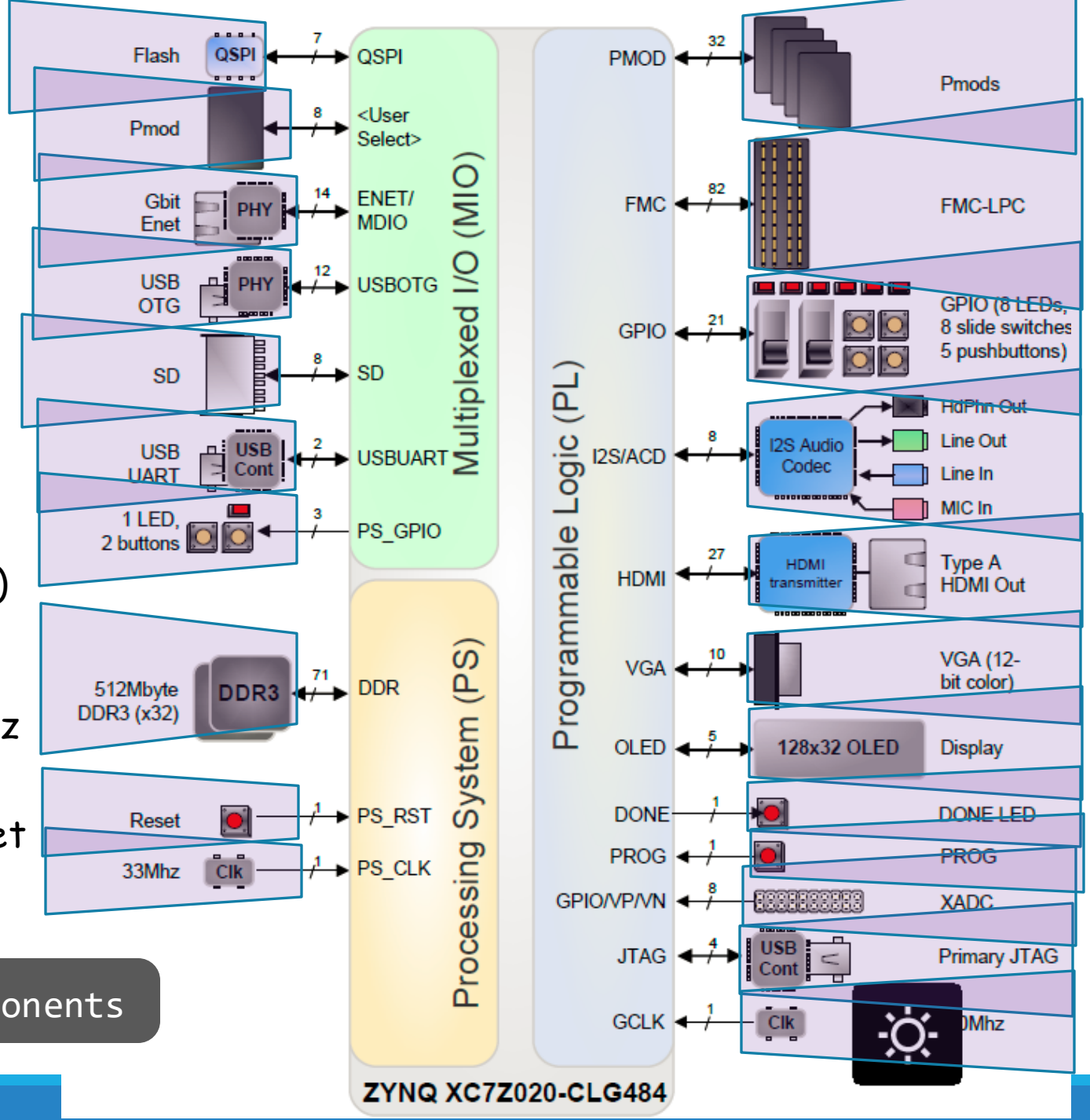
SD Card

USB-UART

LD9 (PS)
Buttons (PS)

512MB (32 bits)533MHz

Processor Subsystem Reset
Clock



PMOD

LPC FMC Connector
68 Single Ended
34 Differential

LEDs (8)

User I/O
Push Buttons(5)
DIP Switch(8)

AUDIO

HDMI

VGA

OLED

Done Blue LED
Program Push Button

Analog Mixed Signalling (AMS) Connector

USB-JTAG

PL Clock Source
100MHz

ZedBoard: main components

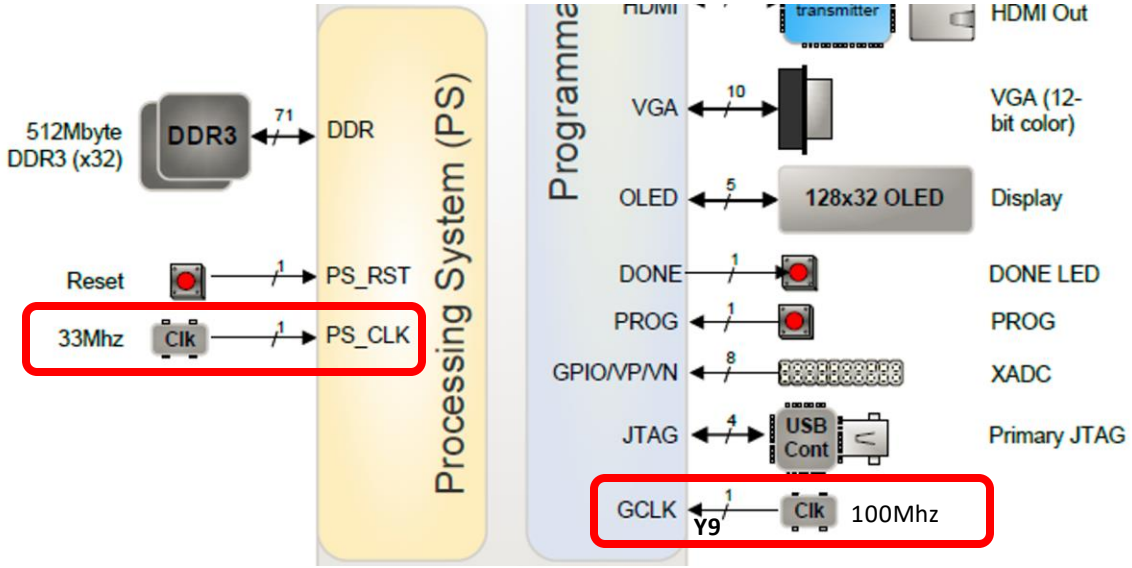
ZedBoard Hardware User Guide

Available in the Workshop's GitLab

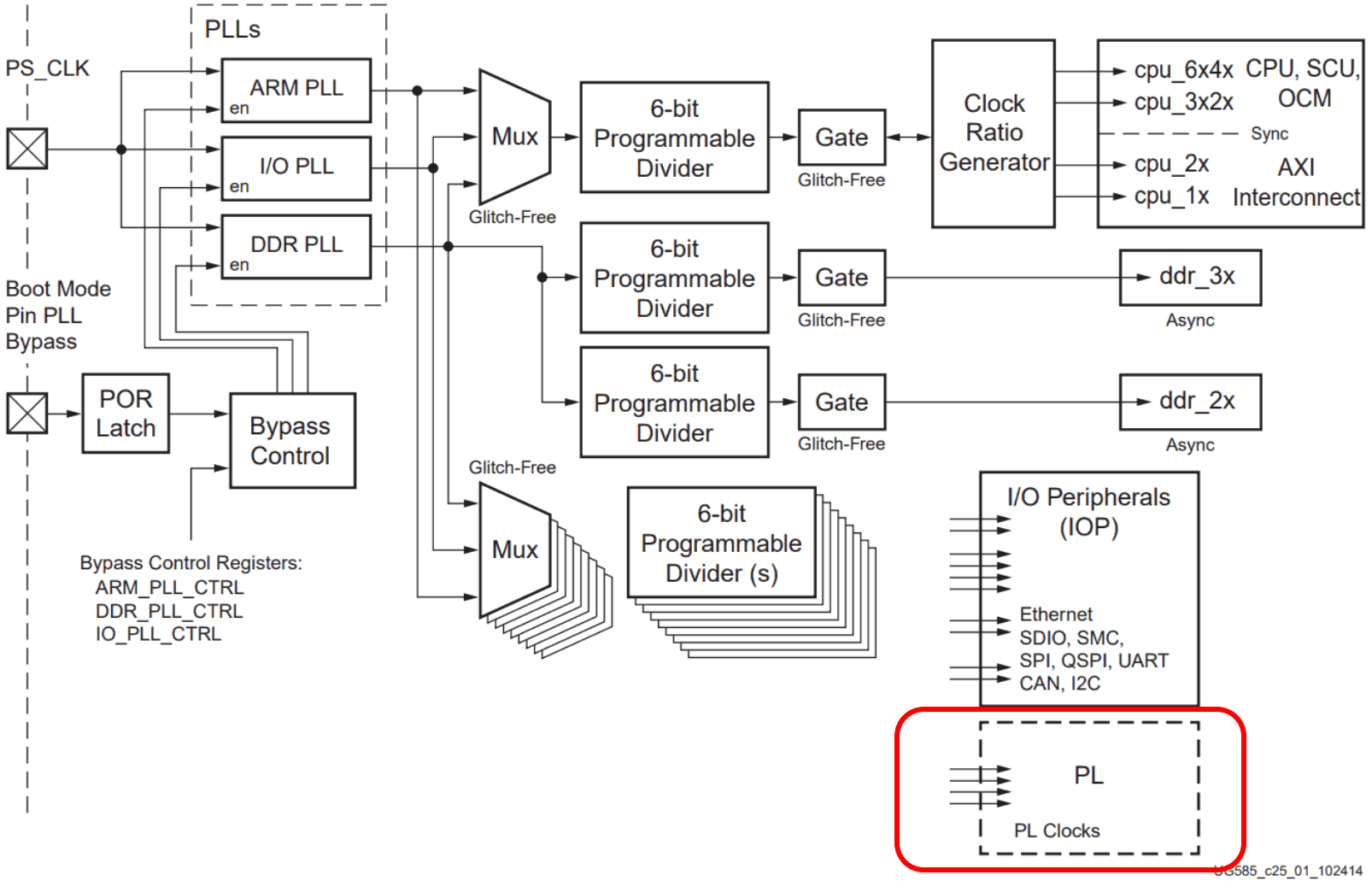
ZedBoard Clock Sources

2.5 Clock sources

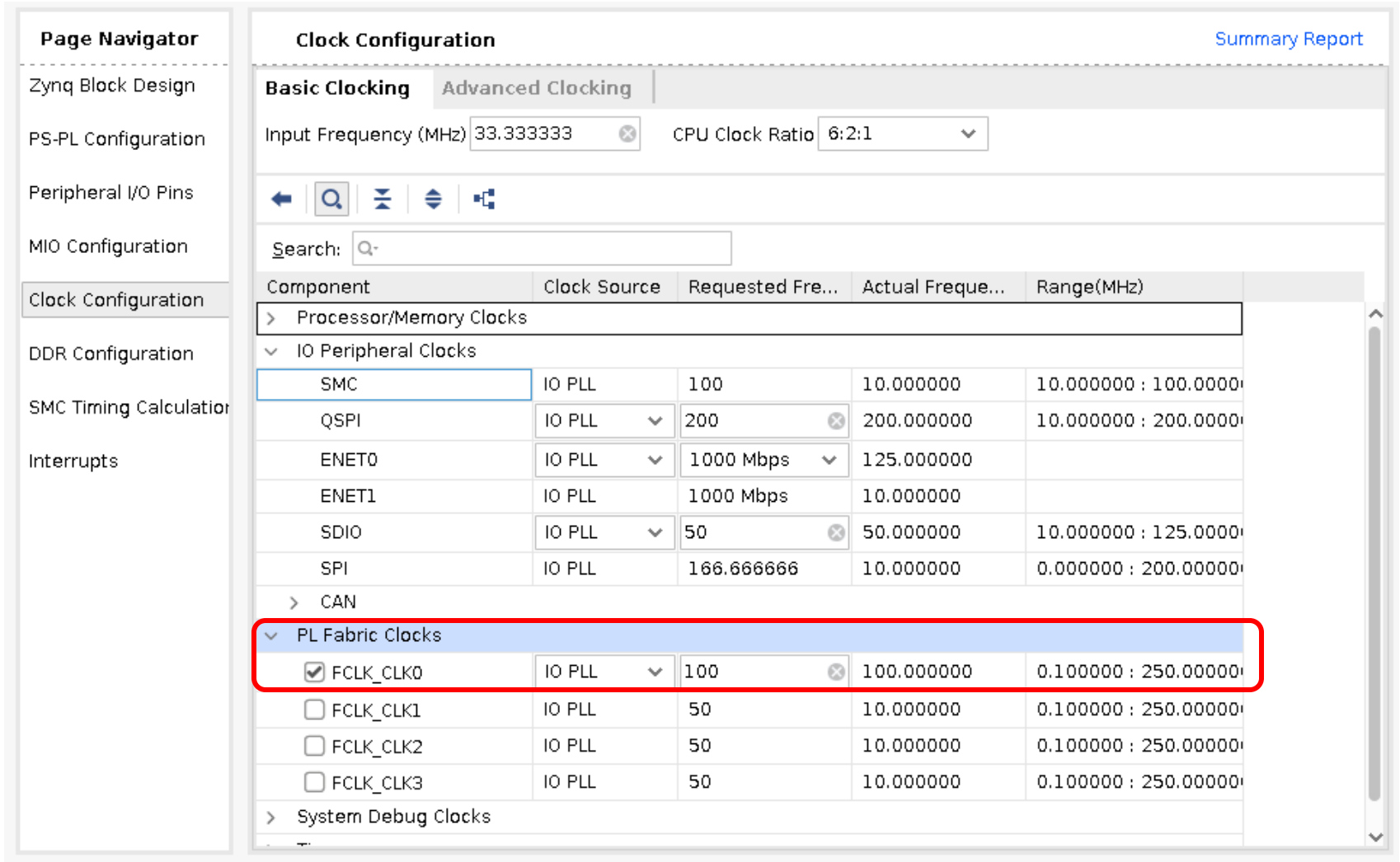
The Zynq-7000 AP SoC's PS subsystem uses a dedicated 33.3333 MHz clock source, IC18, Fox 767-33.333333-12, with series termination. The PS infrastructure can generate up to four PLL-based clocks for the PL system. An on-board 100 MHz oscillator, IC17, Fox 767-100-136, supplies the PL subsystem clock input on bank 13, pin Y9.



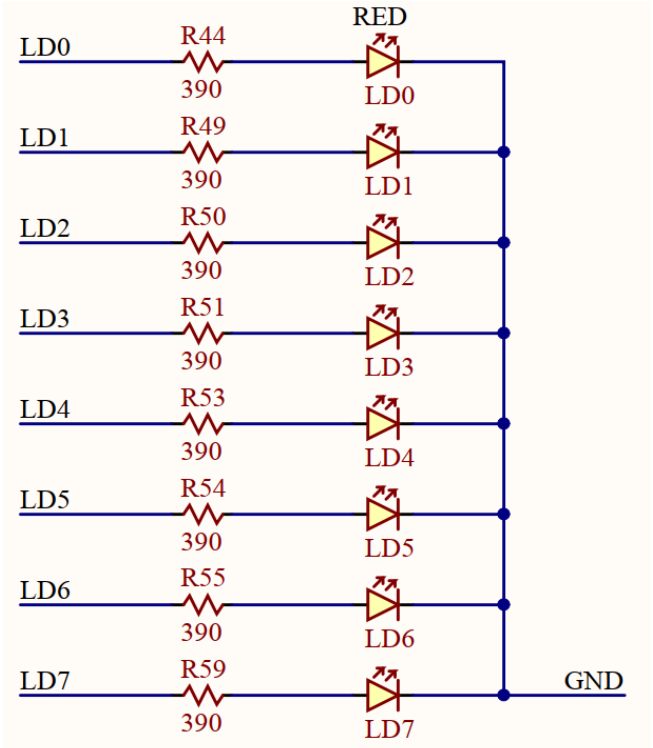
Zynq Clock Resources



Zynq Clock Resources – Configuration in Vivado



ZedBoard Available I/O for the User (1)



2.7.3 User LEDs

The ZedBoard has eight user LEDs, LD0 – LD7. A logic high from the Zynq-7000 AP SoC I/O causes the LED to turn on. LED's are sourced from 3.3V banks through 390Ω resistors.

Table 14 - LED Connections

Signal Name	Subsection	Zynq pin
LD0	PL	T22
LD1	PL	T21
LD2	PL	U22
LD3	PL	U21
LD4	PL	V22
LD5	PL	W22
LD6	PL	U19
LD7	PL	U14
LD9	PS	D5 (MIO7)

Constraint File (.xdc file)

```
# ----------------------------------------------------------
# User LEDs - Bank 33
# ----------------------------------------------------------
set_property PACKAGE_PIN T22 [get_ports {LD0}];  # "LD0"
set_property PACKAGE_PIN T21 [get_ports {LD1}];  # "LD1"
set_property PACKAGE_PIN U22 [get_ports {LD2}];  # "LD2"
set_property PACKAGE_PIN U21 [get_ports {LD3}];  # "LD3"
set_property PACKAGE_PIN V22 [get_ports {LD4}];  # "LD4"
set_property PACKAGE_PIN W22 [get_ports {LD5}];  # "LD5"
set_property PACKAGE_PIN U19 [get_ports {LD6}];  # "LD6"
set_property PACKAGE_PIN U14 [get_ports {LD7}];  # "LD7"
```

Signal name you want to assosiate with LD0.
e.g.: *pwm_led*

ZedBoard Available I/Os for the User (2)

2.7 User I/O

2.7.1 User Push Buttons

The ZedBoard provides 7 user GPIO push buttons to the Zynq-7000 AP SoC; five on the PL-side and two on the PS-side.

Pull-downs provide a known default state, pushing each button connects to Vcco.

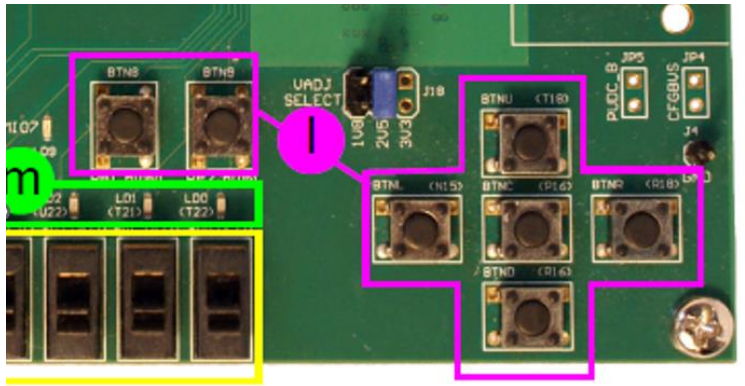
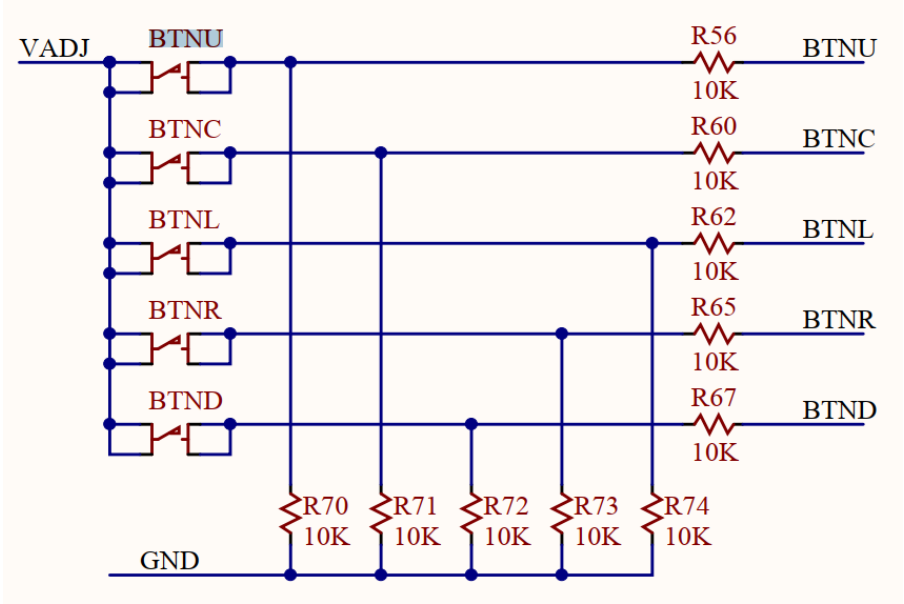


Table 12 - Push Button Connections

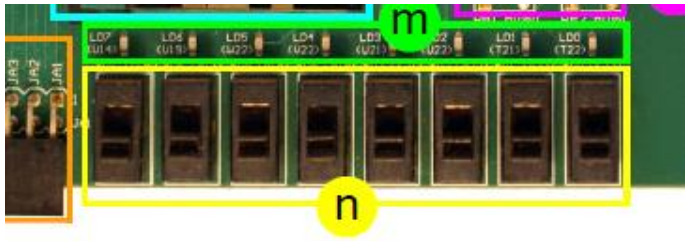
Signal Name	Subsection	Zynq pin
BTNU	PL	T18
BTNR	PL	R18
BTND	PL	R16
BTNC	PL	P16
BTNL	PL	N15
PB1	PS	D13 (MIO 50)
PB2	PS	C10 (MIO 51)



Constraint File (.xdc file)

```
# ----------------------------------------------------------
# User Push Buttons - Bank 34
# ----------------------------------------------------------
set_property PACKAGE_PIN P16 [get_ports {BTNC}];  # "BTNC"
set_property PACKAGE_PIN R16 [get_ports {BTND}];  # "BTND"
set_property PACKAGE_PIN N15 [get_ports {BTNL}];  # "BTNL"
set_property PACKAGE_PIN R18 [get_ports {BTNR}];  # "BTNR"
set_property PACKAGE_PIN T18 [get_ports {BTNU}];  # "BTNU"
```

ZedBoard Available I/O for the User (3)

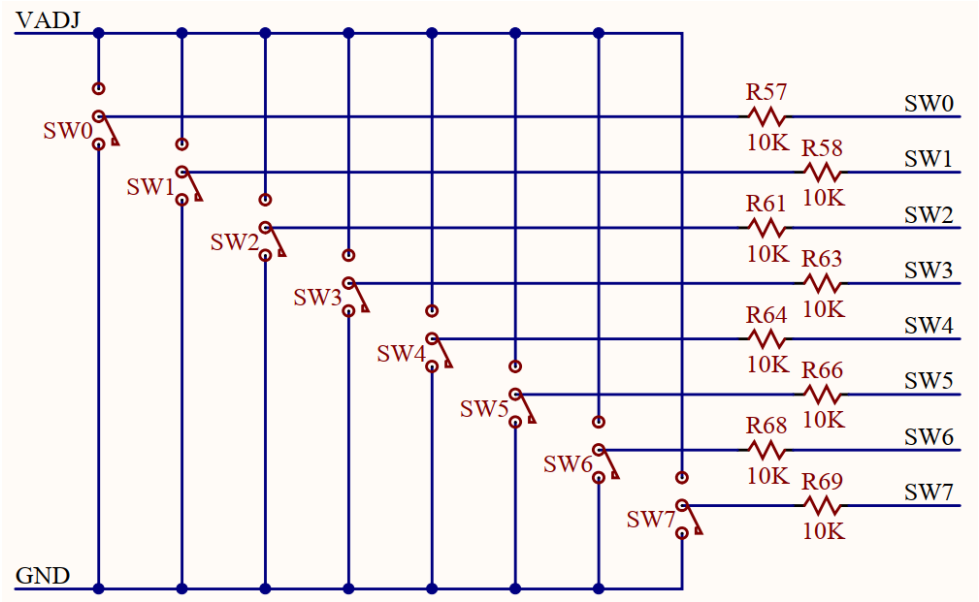


2.7.2 User DIP Switches

The ZedBoard has eight user dip switches, SW0-SW7, providing user input. SPDT switches connect the I/O through a 10kΩ resistor to the VADJ voltage supply or GND.

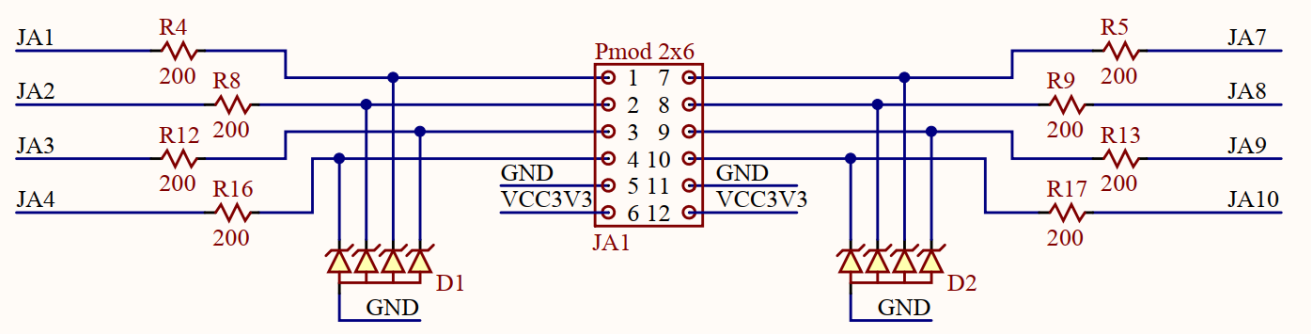
Table 13 - DIP Switch Connections

Signal Name	Zynq pin
SW0	F22
SW1	G22
SW2	H22
SW3	F21
SW4	H19
SW5	H18
SW6	H17
SW7	M15



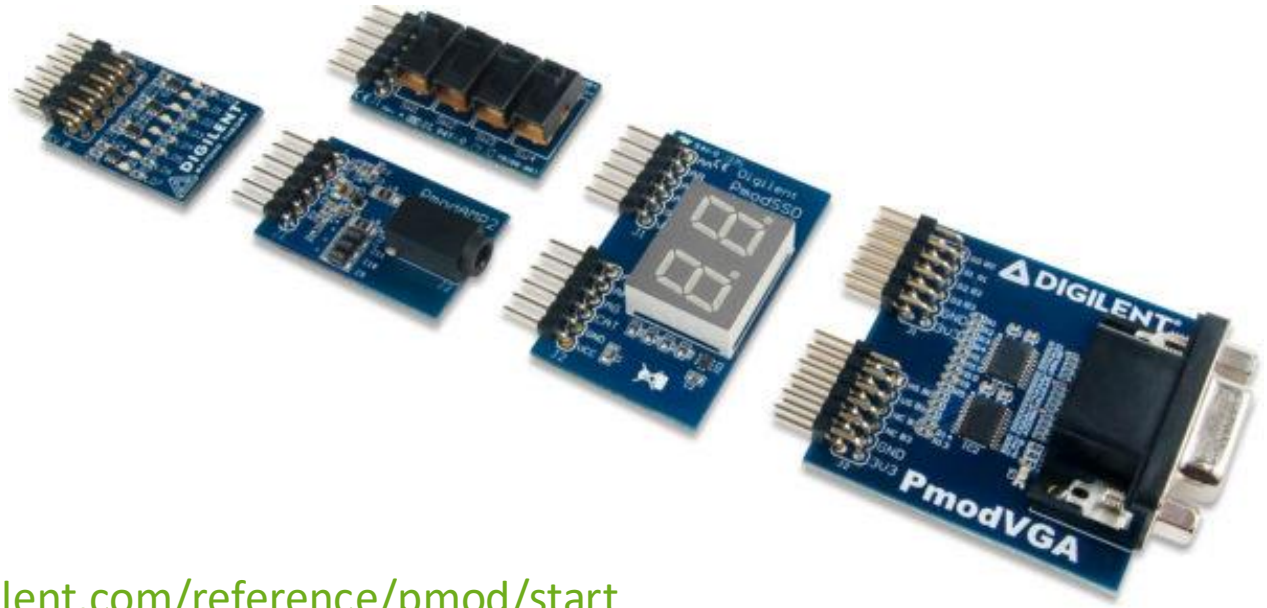

```
# ------------------------------------------------------------
# User DIP Switches - Bank 35
# ------------------------------------------------------------
set_property PACKAGE_PIN F22 [get_ports {SW0}];  # "SW0"
set_property PACKAGE_PIN G22 [get_ports {SW1}];  # "SW1"
set_property PACKAGE_PIN H22 [get_ports {SW2}];  # "SW2"
set_property PACKAGE_PIN F21 [get_ports {SW3}];  # "SW3"
set_property PACKAGE_PIN H19 [get_ports {SW4}];  # "SW4"
set_property PACKAGE_PIN H18 [get_ports {SW5}];  # "SW5"
set_property PACKAGE_PIN H17 [get_ports {SW6}];  # "SW6"
set_property PACKAGE_PIN M15 [get_ports {SW7}];  # "SW7"
```

ZedBoard PMODs Connectors



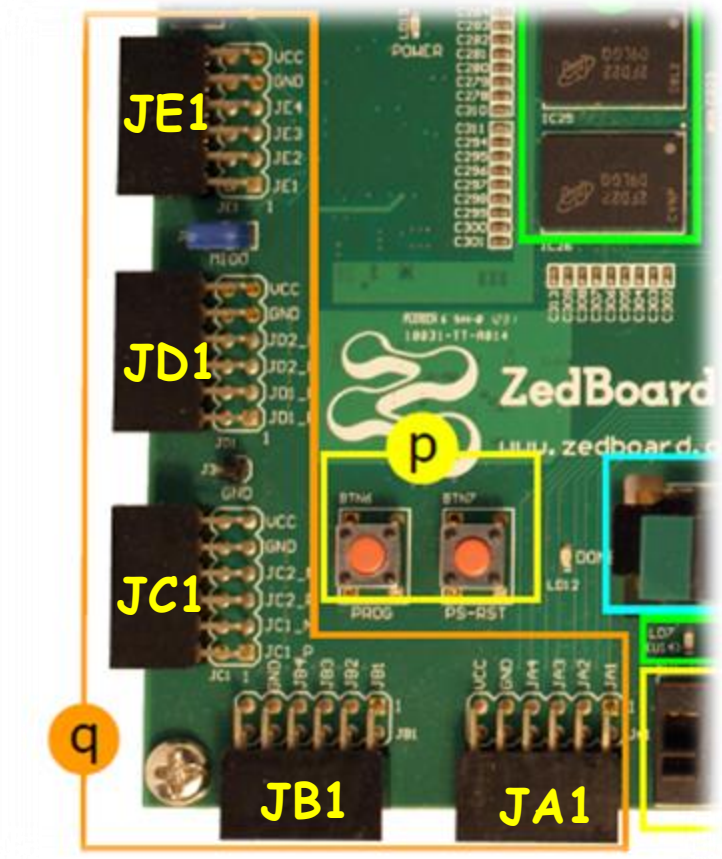
PMODs are a series of small I/O interface boards standardized by the Digilent company.

They offer a way to **extend** the I/O capabilities of any board with PMOD connectors.



https://digilent.com/reference/pmod/start

ZedBoard PMODs Connectors



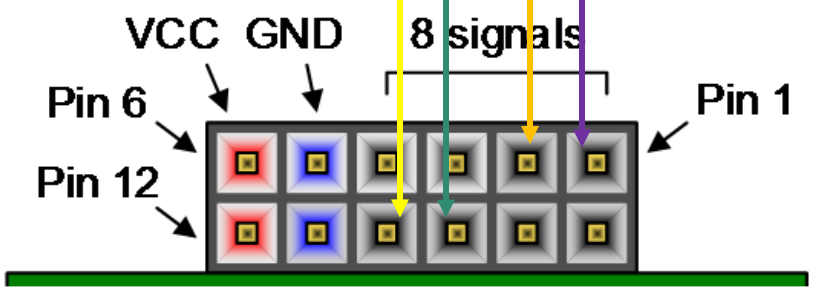
ZedBoard has five **PMODs** connectors:

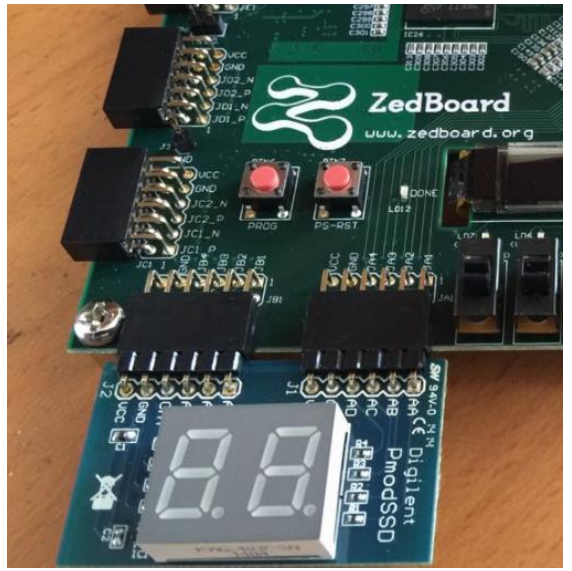
- **JA1**, **JB1**, **JC1** and **JD1** are connected to the **PL** side of the Zynq
- All four are connected to 3.3V (Bank 13)
- **JC1** and **JD1** are routed keeping in mind the equal dealy of each routing line:
  - Mainly to support LVDS (it can run up to 525MHz)
- JE1 is connected to the PS side of the Zynq, on MIO pins 0, 9 to 15. 3.3V.

ZedBoard PMOD Connectors

Table 16 - Pmod Connections

Pmod	Signal Name	Zynq pin	Pmod	Signal Name	Zynq pin
JA1	JA1	Y11	JB1	JB1	W12
	JA2	AA11		JB2	W11
	JA3	Y10		JB3	V10
	JA4	AA9		JB4	W8
	JA7	AB11		JB7	V12
	JA8	AB10		JB8	W10
	JA9	AB9		JB9	V9
	JA10	AA8		JB10	V8





Constraint File (.xdc file)

```
# ------------------------------------------------------------
# JA Pmod - Bank 13
# ------------------------------------------------------------
set_property PACKAGE_PIN Y11  [get_ports {JA1}];  # "JA1"
set_property PACKAGE_PIN AA8  [get_ports {JA10}]; # "JA10"
set_property PACKAGE_PIN AA11 [get_ports {JA2}];  # "JA2"
set_property PACKAGE_PIN Y10  [get_ports {JA3}];  # "JA3"
set_property PACKAGE_PIN AA9  [get_ports {JA4}];  # "JA4"
set_property PACKAGE_PIN AB11 [get_ports {JA7}];  # "JA7"
set_property PACKAGE_PIN AB10 [get_ports {JA8}];  # "JA8"
set_property PACKAGE_PIN AB9  [get_ports {JA9}];  # "JA9"
```

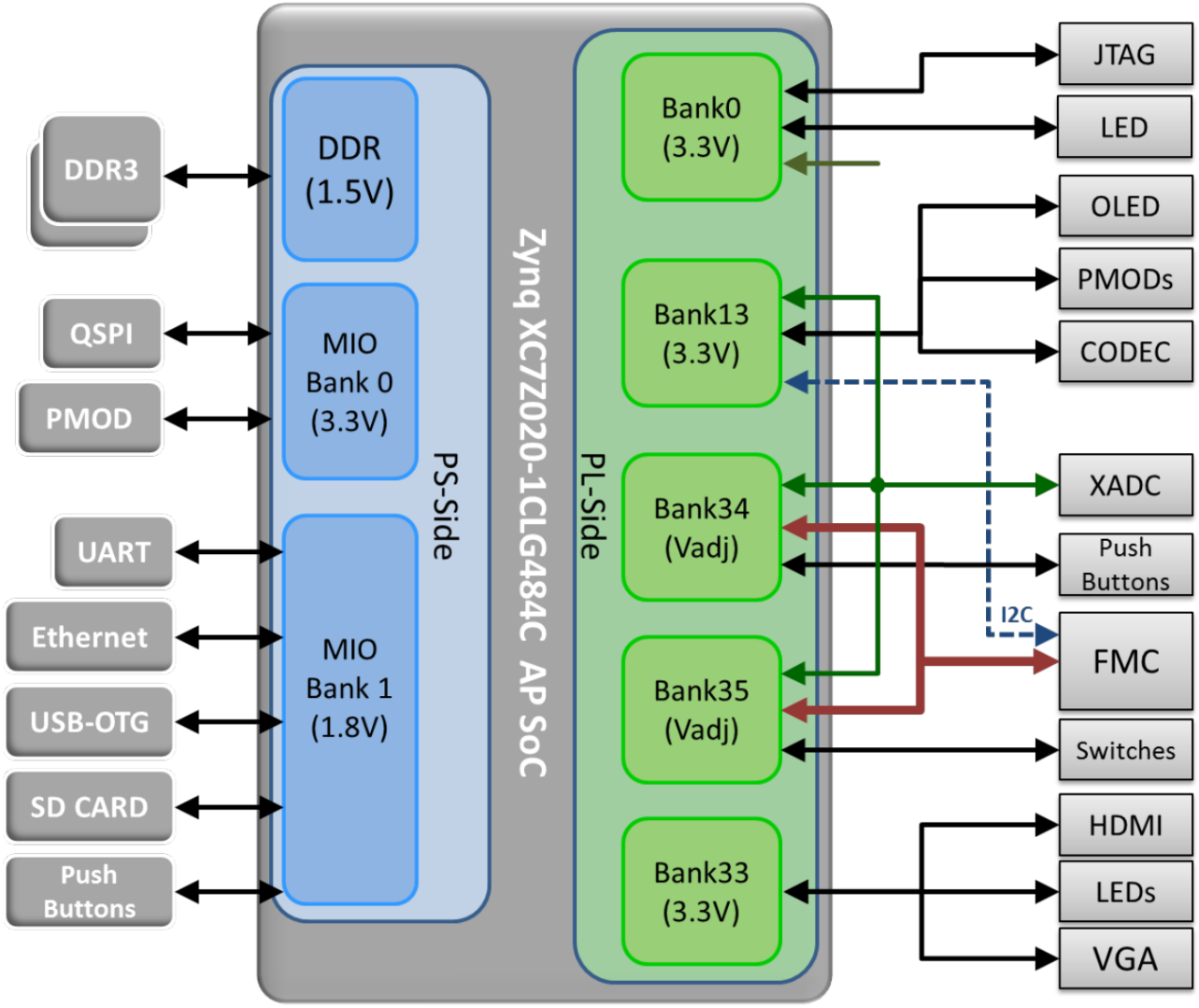
Signal name you want to assosiate with JA1.
e.g.: *adc_reset*

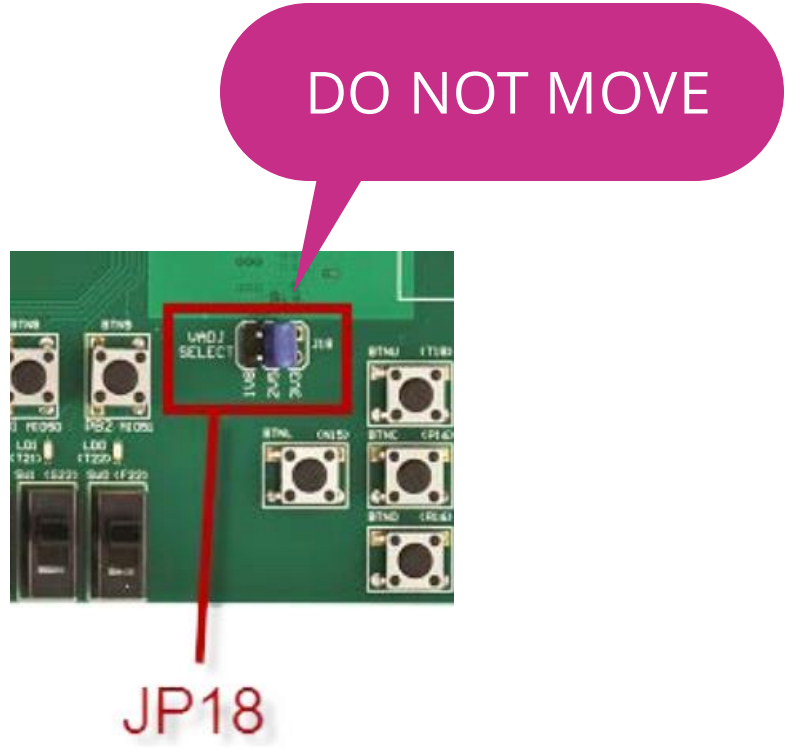
ZedBoard PMOD Connectors

Pmod	Signal Name	Zynq pin	Pmod	Signal Name	Zynq pin
JC1 Differential	JC1_N	AB6	JD1 Differential	JD1_N	W7
	JC1_P	AB7		JD1_P	V7
	JC2_N	AA4		JD2_N	V4
	JC2_P	Y4		JD2_P	V5
	JC3_N	T6		JD3_N	W5
	JC3_P	R6		JD3_P	W6
	JC4_N	U4		JD4_N	U5
	JC4_P	T4		JD4_P	U6

Pmod	Signal Name	Zynq pin	MIO
JE1 MIO Pmod	JE1	A6	MIO13
	JE2	G7	MIO10
	JE3	B4	MIO11
	JE4	C5	MIO12
	JE7	G6	MIO0
	JE8	C4	MIO9
	JE9	B6	MIO14
	JE10	E6	MIO15

ZedBoard Bank Power Voltages

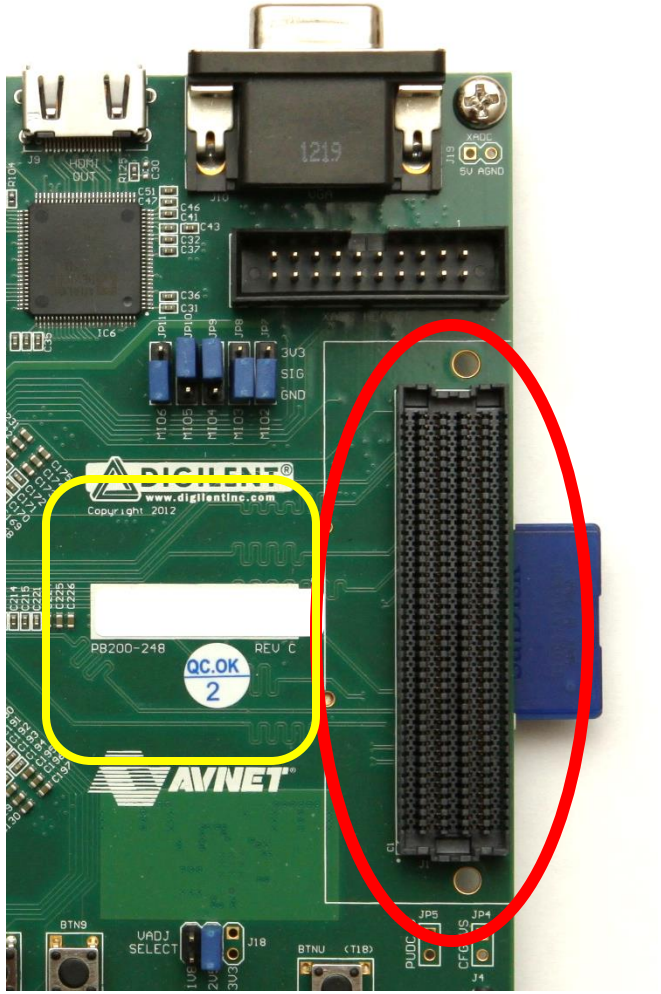




Vadj is selectad by JP18:

- 1.8V
- 2.5V
- 3.3V

LPC FMC Connector

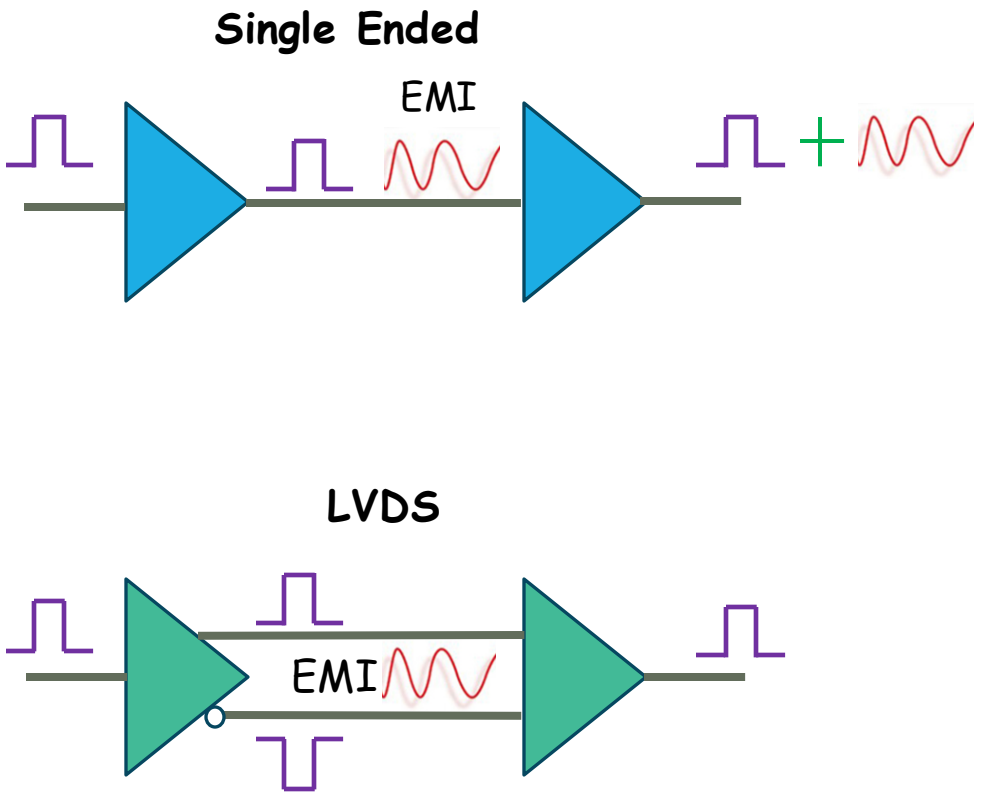


LPC: Low-Pin-Count

FMC: FPGA Mezzanine Card

- ✓ The LPC FMC exposes *68 single-ended I/O*, which can be configured as *34 differential pairs*.
- ✓ ADC500: an ICTP MLAB board is plugged into the LPC FMC and will be used in the final lab.

LVDS – Single Ended



Single Ended	Low Voltage Differential Signals (LVDS)
Advantages	
Low System Cost	Low sensitivity to crosstalk
Simple to Implement	Groung Noise Rejection
Almost any Microprocessor, Microcomputer has it.	Common Mode Noise Rejection (minimize EMI*, Low Jitter, Low Skew)
	Great Signal Integrity
	Low Power
Disadvantages	
Noise and Crosstalk	Twisted Cable Required
Ground Shifts	Higher Cost
Low Data Rate	

*EMI: electromagnetic interference

ZedBoard + ICTP-INFN ADC500