The Abdus Salam International Centre for Theoretical Physics

IAEA International Atomic Energy Agency

WELCOME to the

Joint ICTP-IAEA School on Detector Signal Processing and Machine Learning for Scientific Instrumentation and Reconfigurable Computing

27 October – 07 November, 2025

ICTP Organizer

Maria Liz CRESPO

IAEA Organizers

Kalliopi KANAKI

Mladen BOGOBAC

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SCHOOL PROGRAMME

- The School takes place at the ICTP AGH:
  - Kastler Lecture Hall (Lectures)
  - Informatics Lab (Hands-on sessions)

- School website: **https://indico.ictp.it/event/10875/**

  (Detailed Schedule & Slides and List of Participants)

- School's email (secretariat): smr4110@ictp.it

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SCHOOL PROGRAMME

- **Daily timetable (9:00 – 18:00):**

Timetable	
9:00 - 10:00	lectures
10:00 - 10:30	**coffee-break**
10:30 - 12:30	lectures
12:30 - 14:00	**lunch**
14:00 - 16:00	lectures / lab activities
16:00 - 16:15	**coffee-break**
16:15 - 18:00	lab activities

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PARTICIPANTS

- Requests for participation: 263 applicants from 57 different countries
- **Selected: 45 participants from 29 different nationalities**

Algeria	Georgia	Malaysia
Argentina	Ghana	Mexico
Bangladesh	Guatemala	Pakistan
Bosnia	Honduras	Panama
Brazil	India	Peru
Cameroon	Indonesia	Romania
Colombia	Iran	Russia
Costa Rica	Italy	Tunisia
Croatia	Jordan	Venezuela
Egypt	Kenya	

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Lecturers and Lab Tutors

BALLINA ESCOBAR Maynor (Guatemala/Italy)

CASTAÑO USUGA Fabián (Colombia)

CICUTTIN Andres (Italy)

GARCIA ORDOÑEZ Luis (Guatemala/Italy)

MOLINA Romina (Argentina/Italy)

MORALES ARGUETA Ivan (Guatemala/Austria)

NINKOVIC Vukan (Serbia)

RINCON CALLE Fernando (Spain)

SISTERNA Cristian (Argentina)

VUKOBRATOVIC Dejan (Serbia)

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Speakers and Lab Tutors

RAZAIDI BIN HUSSIN (Malaysia)

REAZ Mamun Bin Ibne (Bangladesh/Malaysia)

SAWAL HAMID BIN MD ALI (Malaysia)

GROSSI BASSI Antonio (Brazil/Italy)

PALAVANDISHVILI Ana (Georgia)

Main Topics

- **Fully-Programmable FPGA-based System on Chip (SoC-FPGA)**
  - Architecture and Design Methodology
- **Applied Machine Learning (ML)**
  - End-to-End Workflow for Deploying ML Models on SoC-FPGA
- **Detector Signal Processing**
  - Pulse Acquisition and Characterization
  - Digital Pulse Processing on SoC-FPGA

Lab Activities

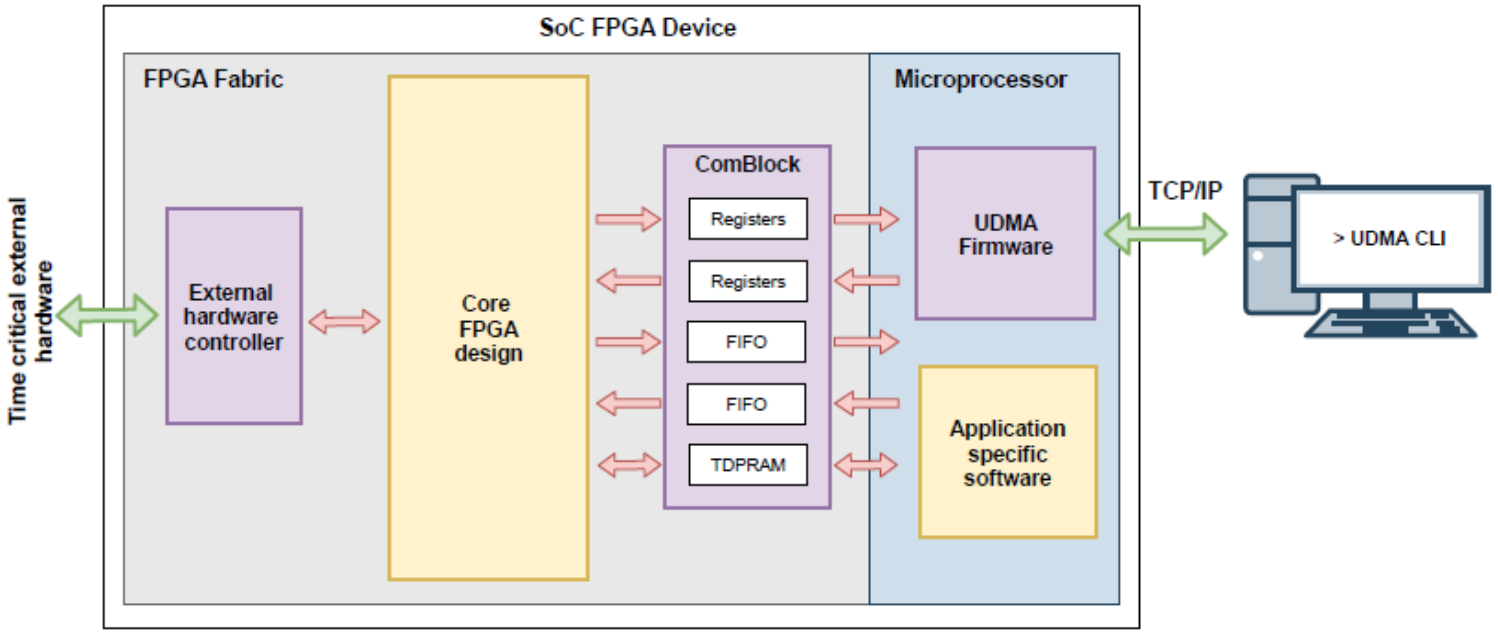
- GitLab link (guides for lab activities):
  https://gitlab.com/ictp-mlab/smr-4110/

- Lab tutors will provide assistance during lab activities
- Lab activities will be conducted **in pairs**

- Vivado IDE 2022.2 (Xilinx)
- ZedBoard: Xilinx Zynq-7000 All-Programmable SoC
- ADC and DAC
- SiPM detectors

Lab Activities

- **SoC-FPGA Development Framework:**



Recommendations:

1) Be on time

2) Attend at least 90% of the lectures + labs to receive the Diploma

3) Feel free to ask questions!

WHAT ABOUT YOU?

NAME

COUNTRY

UNIVERSITY / INSTITUTE

AREA OF RESEARCH

INTEREST IN THE SCHOOL