

Joint ICTP-IAEA School on Detector Signal Processing and Machine Learning for Scientific Instrumentation and Reconfigurable Computing

Introduction to Machine Learning and Edge AI

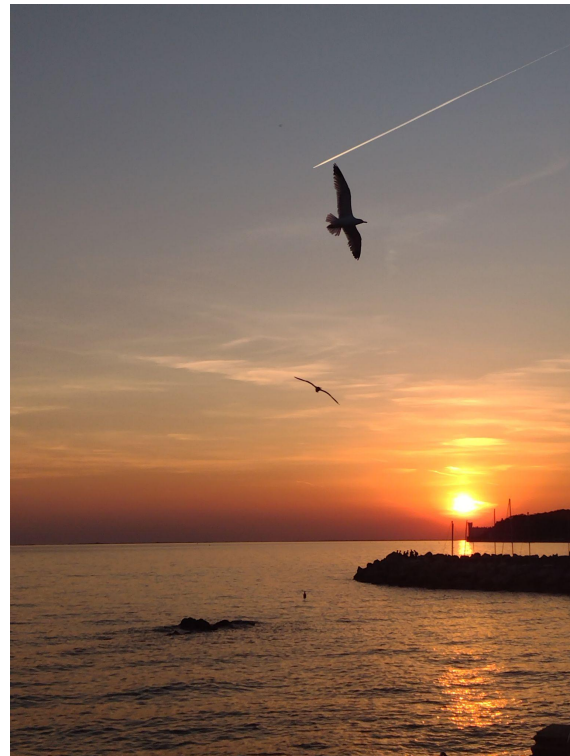
smr4110 | Trieste, Italy - 2025

Romina Soledad Molina, Ph.D.



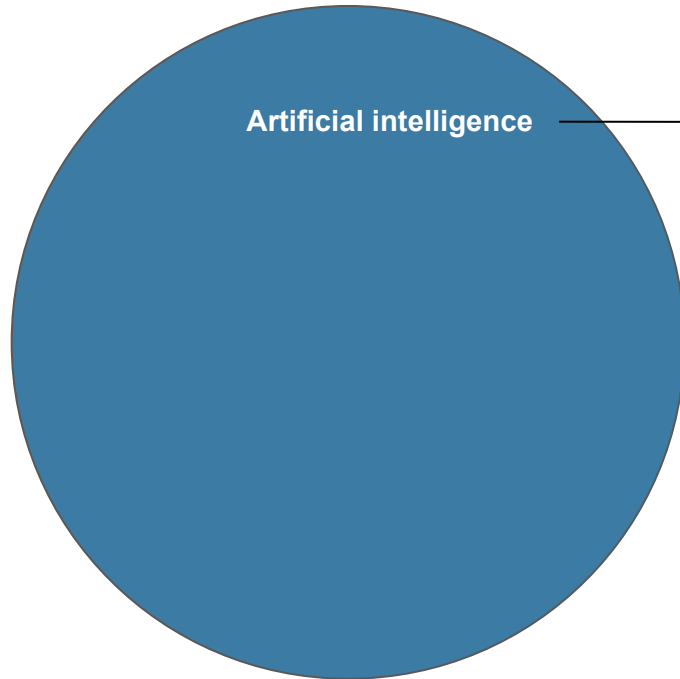
Outline

- Introduction.
- AI beyond 2025.
- What is Edge AI?
- What the Literature Says.
- Integrating Every Layer of Edge AI Design.
- Case Study for FPGA-based Edge AI:
MNIST Binary Classification.



Introduction

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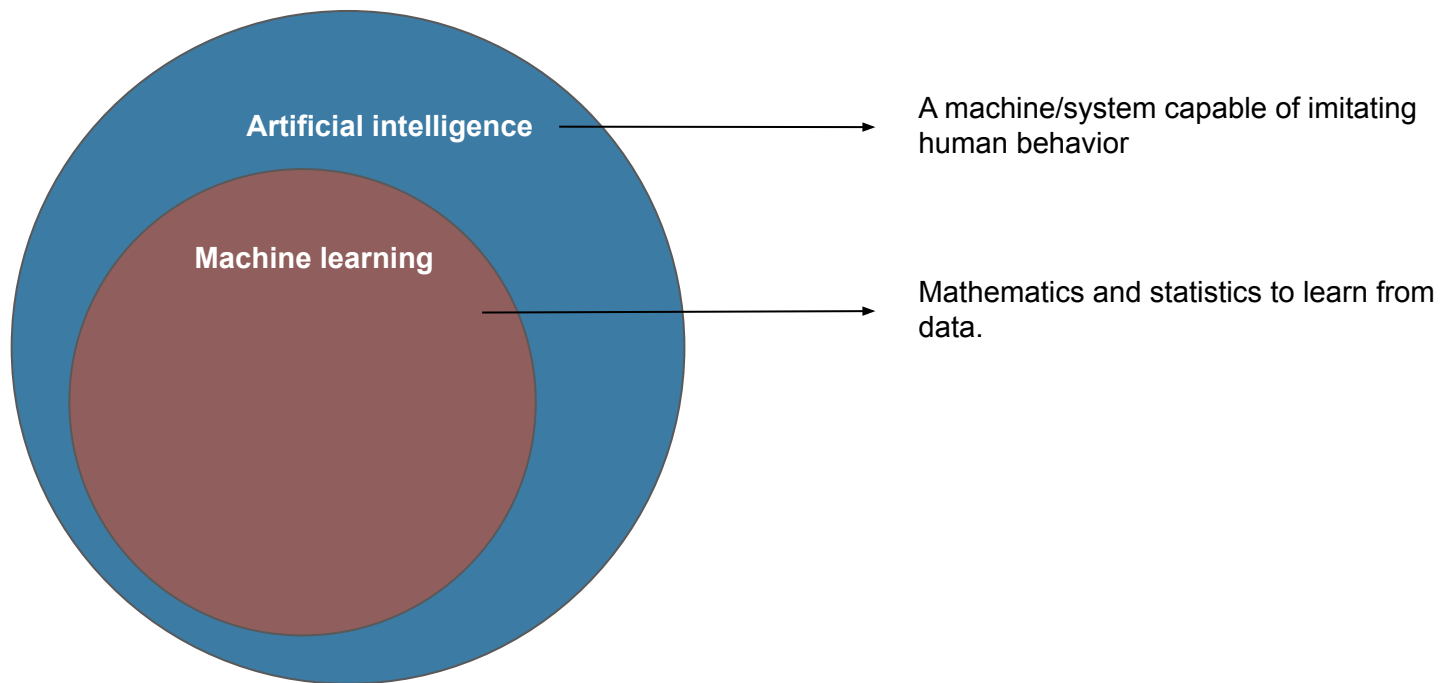


Artificial intelligence

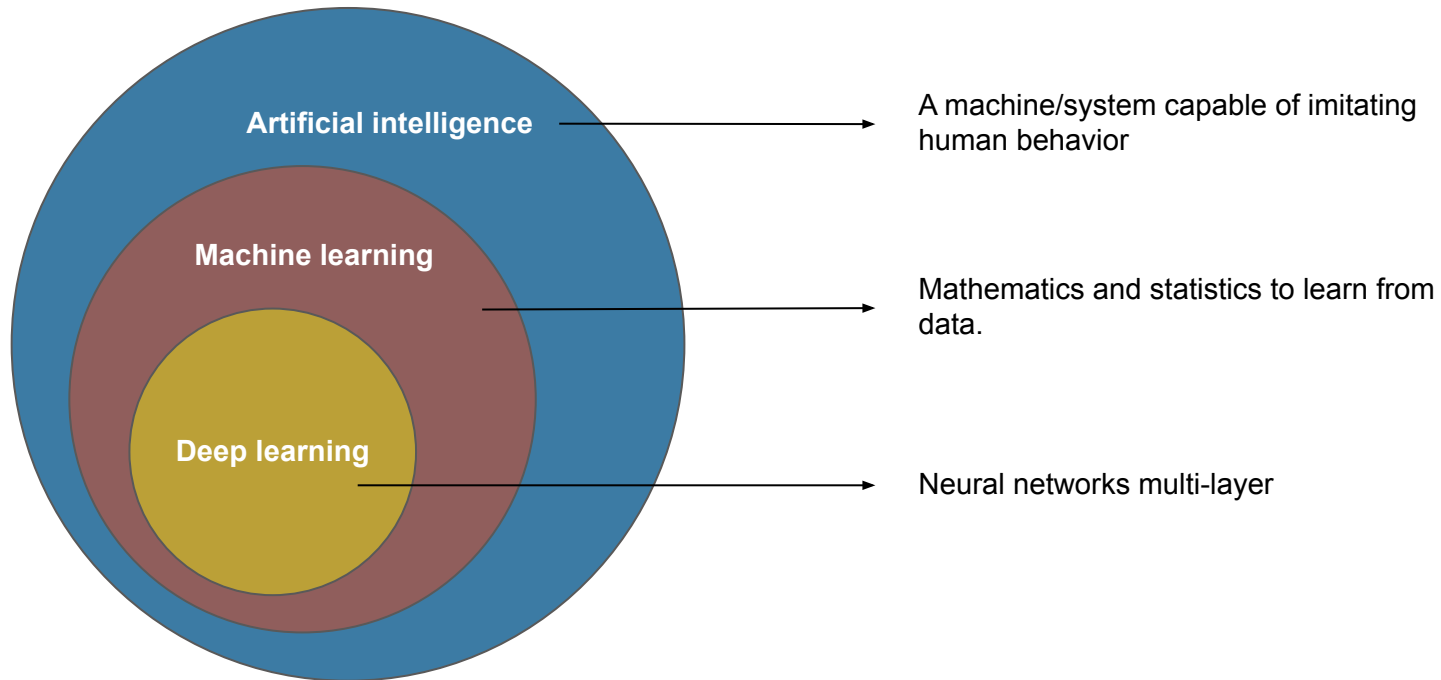


A machine/system capable of imitating
human behavior

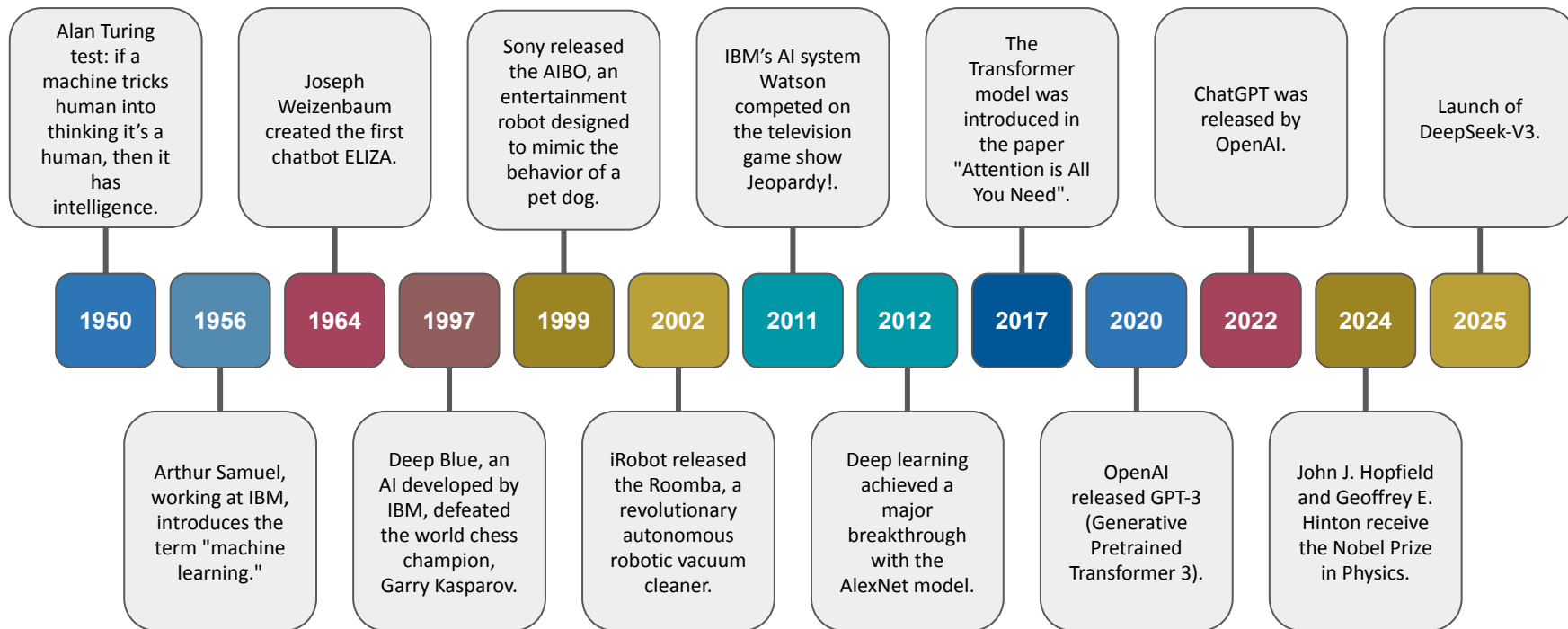
Introduction



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Why has the explosion of AI happened in recent years? Three main components

Big data

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Software

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Hardware

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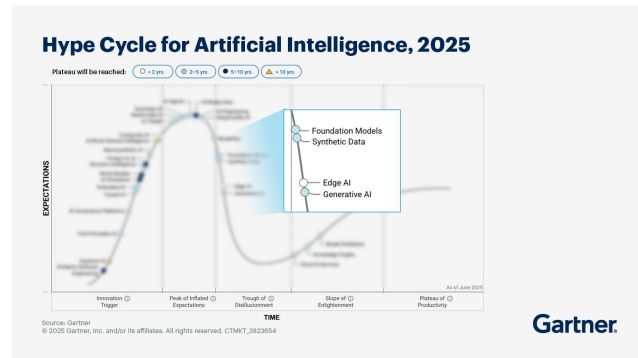
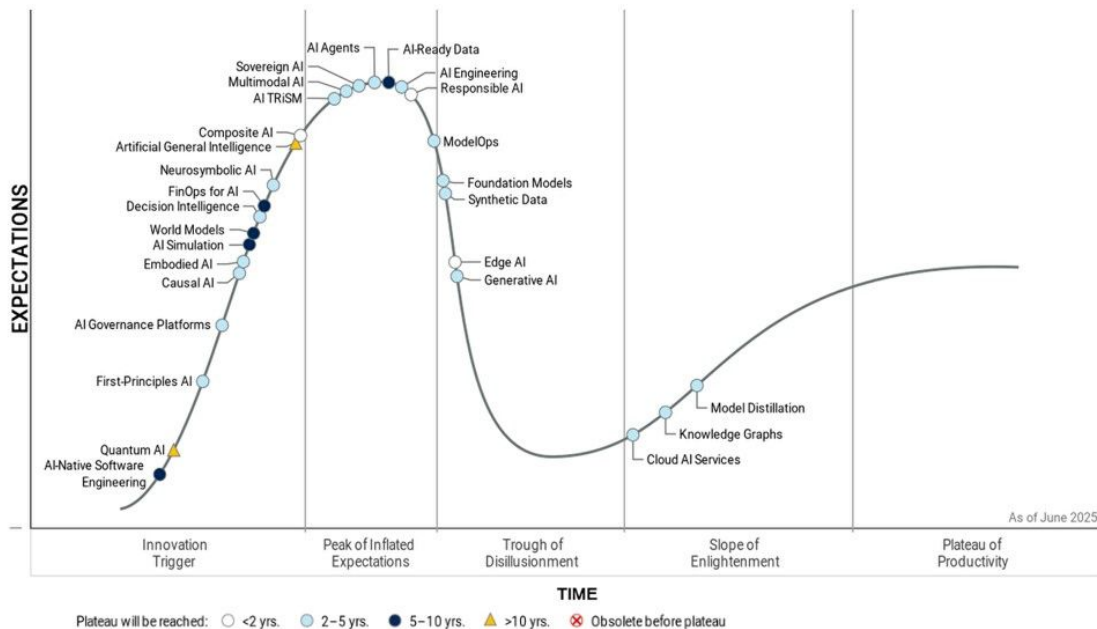
Software

New algorithms, neural network architectures, and open-source frameworks have dramatically improved AI's capabilities and made development more accessible.

Hardware

Advances in GPUs, TPUs, and cloud computing have made it possible to train large AI models faster and more efficiently than ever before.

AI beyond 2025

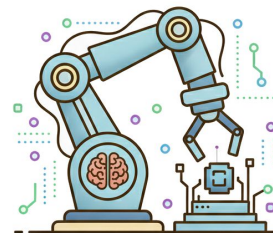


Graphically shows the maturity and adoption of technologies, helping to solve real problems and take advantage of opportunities.

AI beyond 2025

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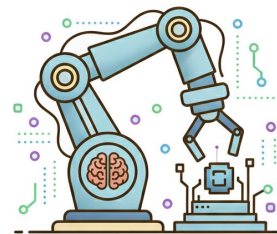
AI Democratization: Making AI tools and knowledge accessible to everyone, lowering barriers for innovation and participation worldwide.



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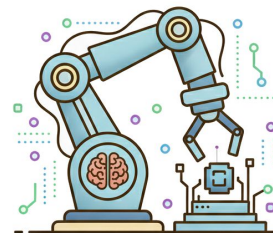


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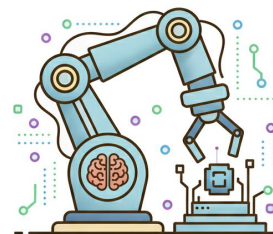
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AI and Human Collaboration: Enhancing creativity and productivity by combining human intuition with machine intelligence.



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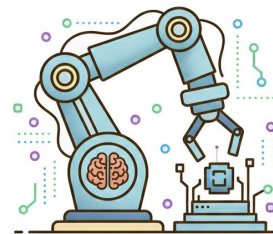
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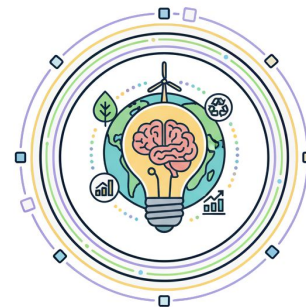
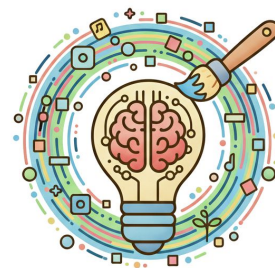
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Autonomous Systems and AI-Powered Robotics: Enabling intelligent automation in transportation, manufacturing, and logistics.



AI beyond 2025

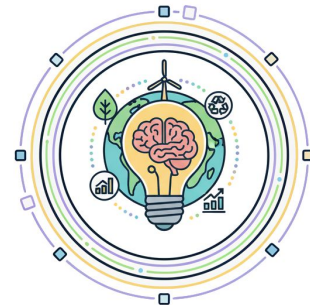
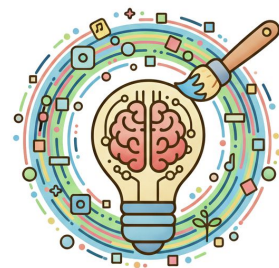
AI in Education: Delivering personalized and adaptive learning experiences for students across all levels.



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Natural Language Processing (NLP) and Conversational AI: Advancing communication between humans and machines through natural, context-aware interactions.

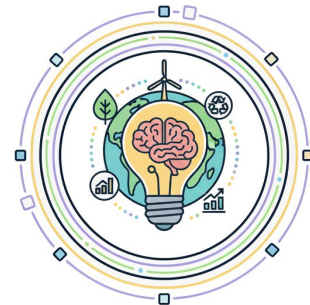
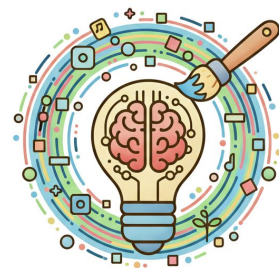


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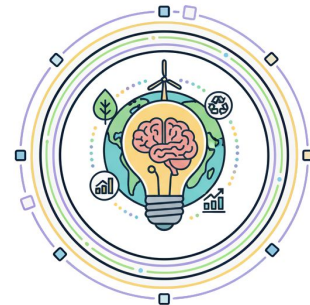
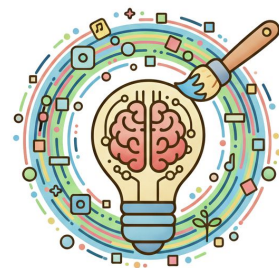
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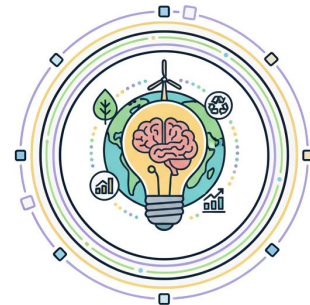
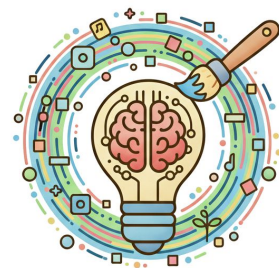
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AI-Driven Creativity: Unlocking new forms of art, design, and innovation through generative models.



AI beyond 2025

5G/6G and Edge AI: Combining ultra-fast connectivity with local AI processing to enable real-time, low-latency intelligence at the edge.



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Neuromorphic Computing: Designing brain-inspired chips for efficient, adaptive AI.



AI beyond 2025

- *Question: What do you think about the future of AI?*



QUESTIONS

AI beyond 2025

AI Market Growth and Impact

Market Growth:

- The global AI market is currently valued at several hundred billion USD and is projected to reach between US \$2–4 trillion by the early-2030s, with annual growth rates (CAGR) in the $\approx 20\%$ to 31% range — depending on the forecast.

AI beyond 2025

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Business Applications:

- According to Gartner, Inc., by 2026 up to 40% of enterprise applications will contain task-specific AI agents (up from less than 5% today).
- They further predict that by 2029, 80% of common customer-service issues will be handled autonomously by what they call “agentic AI” (with little or no human intervention).

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Impact on Businesses & Jobs:

- Business models and job roles are poised to undergo rapid and sometimes unpredictable transformations—driven by autonomous systems, embedded AI in workflows and changing expectations of productivity and capabilities.

AI-Specific Hardware Platforms

- **AI Chips & Processors**
 - **GPUs** (e.g., NVIDIA H100, AMD Instinct MI300) – Still the backbone of AI acceleration.
 - **TPUs** (Google Tensor Processing Units) – Optimized for deep learning workloads.
 - **NPU**s (Neural Processing Units) – Specialized for on-device AI in smartphones and edge devices.
 - **Analog & Optical AI Chips** – Emerging technology for ultra-low-power AI inference.

AI-Specific Hardware Platforms

- **AI Hardware Trends**
 - **Edge AI** – Custom low-power AI chips for real-time processing on IoT devices.
 - **RISC-V AI Processors** – Open-source architecture gaining traction for AI acceleration.
 - **Neuromorphic Computing** – Brain-inspired hardware and algorithms designed for parallel, adaptive, and energy-efficient processing.

AI-Specific Hardware Platforms

- *Question: What do you think about FPGA and AI?*



QUESTIONS

AI-Specific Hardware Platforms

- **FPGA+AI Trends**
 - **AI-Specific FPGA Architectures** – New FPGA models optimized for deep learning (Xilinx Versal AI Core, Intel Stratix 10 NX, and Lattice Avant AI).
 - **Quantum + FPGA Hybrid Computing** – Research into integrating FPGA with quantum acceleration.
 - **FPGA as-a-Service (FaaS)** – Cloud-based FPGA solutions for scalable AI workloads.
 - **Embedded AI & Edge Computing** – FPGAs in IoT & industrial AI, enabling real-time decision-making with ultra-low power.

Edge AI

Edge AI

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On the edge
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On the edge
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Low latency

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Energy efficiency

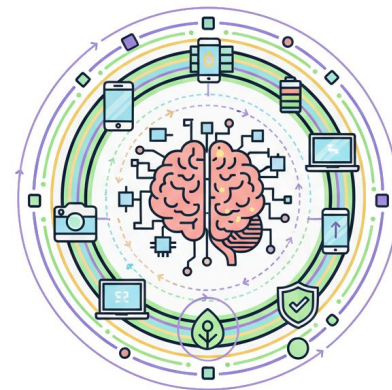
Low latency

Reduced
Bandwidth Usage

Edge AI

Intelligence closer to data

- **Low latency:** Real-time decisions, reducing cloud dependence.
- **Privacy & security:** Data stays on the device.
- **Lower bandwidth use:** Less data sent to the cloud.
- **Energy efficiency:** Optimized local processing.
- **Scalability & reliability:** Devices run autonomously, even offline



Bringing intelligence closer to the data, enabling low-latency, privacy-preserving, and energy-aware AI.

Edge AI Challenges

Hardware & Energy

Limited power

Memory/storage
limits

Computation & Performance

Latency & real-time

Limited compute capacity

Hardware heterogeneity

Data & Deployment

Privacy & security

Network issues



Edge AI

Challenges

- *Question:*

Given all these challenges... how can we make AI models run efficiently on tiny, power-limited devices?



QUESTIONS

Edge AI Challenges

- *Question:*

What if we could combine the strengths of different processors CPUs, GPUs, and FPGAs — to overcome these limits?



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Edge AI

Heterogeneous Computing: A Key Enabler for Edge AI.

- By incorporating CPUs, GPUs, and FPGAs into a single system, **heterogeneous computing** becomes possible.

Edge AI

Heterogeneous Computing: A Key Enabler for Edge AI.

- By incorporating CPUs, GPUs, and FPGAs into a single system, **heterogeneous computing** becomes possible.
- This approach maximizes the strengths of each component, efficiently distributing edge workloads to improve both performance and energy consumption.

Edge AI

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- **CPU:** handles general-purpose tasks like system management, control logic, and lightweight AI inference.

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- **GPU:** accelerates parallelizable tasks such as deep learning inference, image processing, and high-performance computing.

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- **CPU:** handles general-purpose tasks like system management, control logic, and lightweight AI inference.
- **GPU:** accelerates parallelizable tasks such as deep learning inference, image processing, and high-performance computing.
- **FPGA:** provides real-time, ultra-low-latency processing for tasks like sensor fusion, encryption, and custom AI accelerators.

Edge AI based on FPGA

FPGA / SoC-based on FPGA

Edge AI based on FPGA

Low latency

FPGA / SoC-based on FPGA

Edge AI based on FPGA

Low latency

Energy Efficiency

FPGA / SoC-based on FPGA

Edge AI based on FPGA

Low latency

Energy Efficiency

High parallelism

FPGA / SoC-based on FPGA

Edge AI based on FPGA

Low latency

Energy Efficiency

High parallelism

Scalability

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Customizable AI Acceleration

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Edge AI based on FPGA

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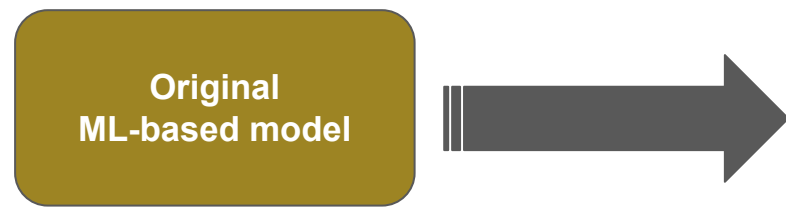
FPGA / SoC-based on FPGA

Resource-constrained devices

Edge AI based on FPGA

Original
ML-based model

Edge AI based on FPGA



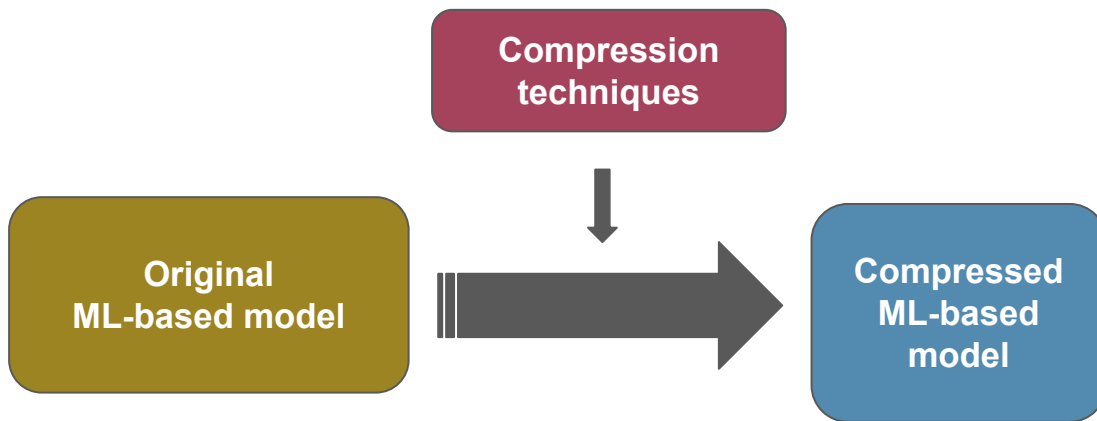
Original
ML-based model

A diagram illustrating the process of edge AI implementation. On the left, a gold-colored rounded rectangle contains the text 'Original ML-based model'. A large, dark gray arrow points from this rectangle to the right, indicating a transformation or deployment process. The arrow has a thick shaft and a triangular head. The background is white, and the slide is framed by dark blue bars at the top and bottom.

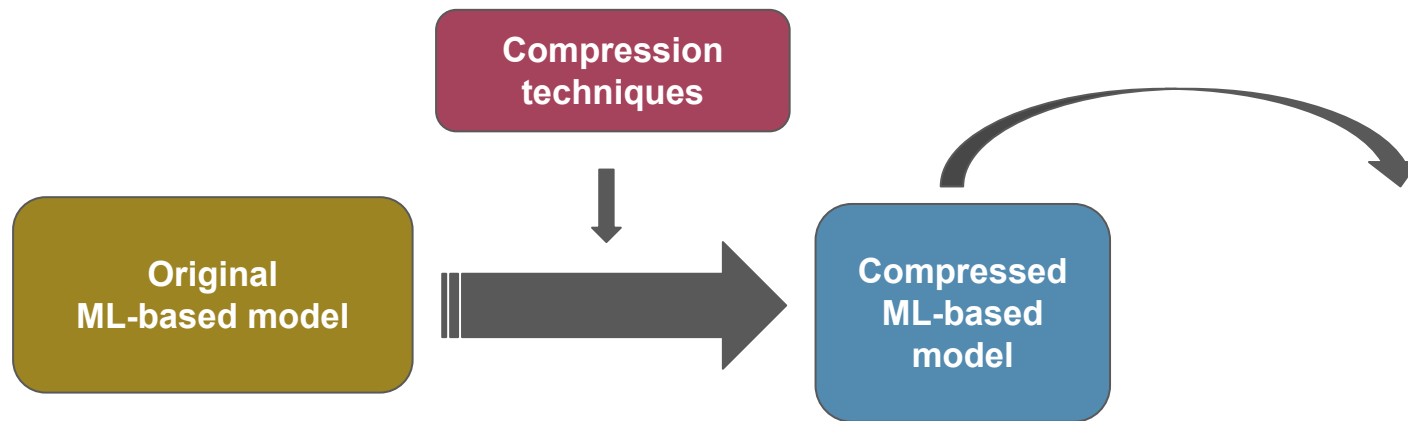
Edge AI based on FPGA



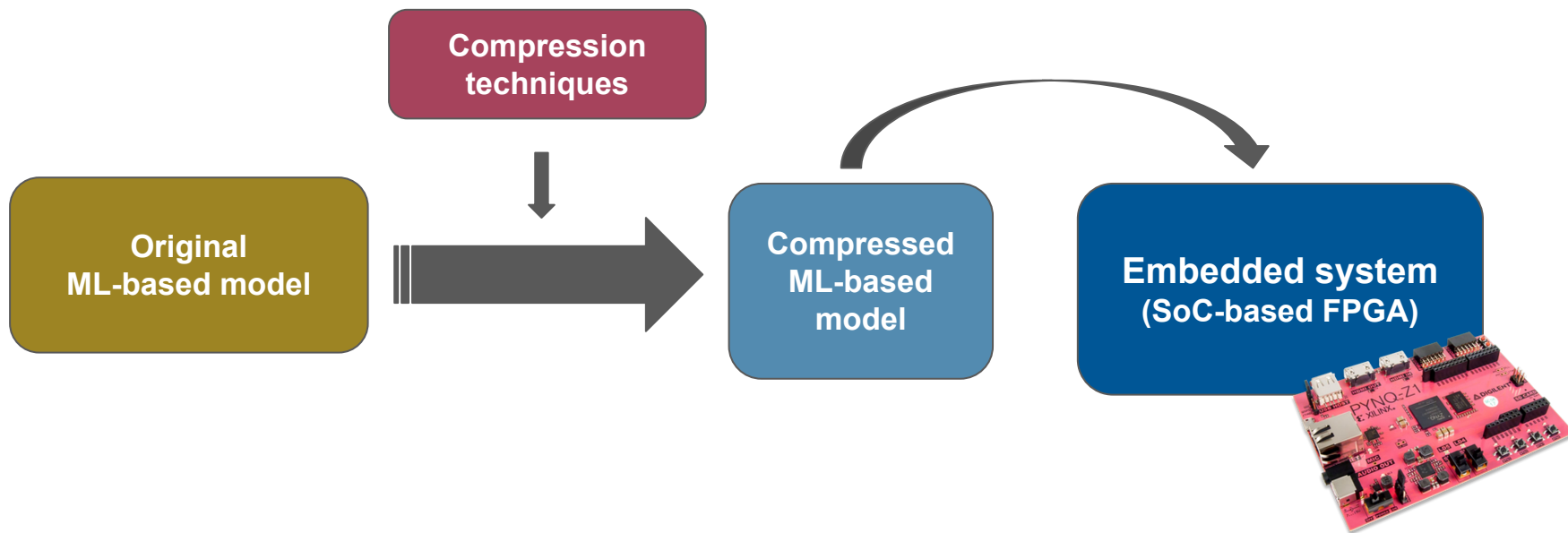
Edge AI based on FPGA



Edge AI based on FPGA



Edge AI based on FPGA



What the Literature Says

What the Literature Says

- **ML on constrained devices is now a major focus**
 - TinyML and on-device inference are growing research areas.
- **Classical state-of-the-art models are being adapted for the edge**
 - MobileNetV2, TinyBERT, and YOLO-Lite show that efficiency is now as important as accuracy.
- **Compression through pruning & quantization dominates optimization**
 - These remain the most used techniques to fit large models into edge hardware.
- **Off-chip memory access is a key bottleneck**
 - Memory transfers can consume more energy than computation.
- **Workflows are still fragmented across tools**
 - Full end-to-end edge pipelines are rare; integration remains an open challenge.

What the Literature Says

**Memory footprint
and latency**

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Productivity

Integrating Every Layer of Edge AI Design

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Optimization is holistic — every phase, from model to hardware, impacts overall performance at the edge.

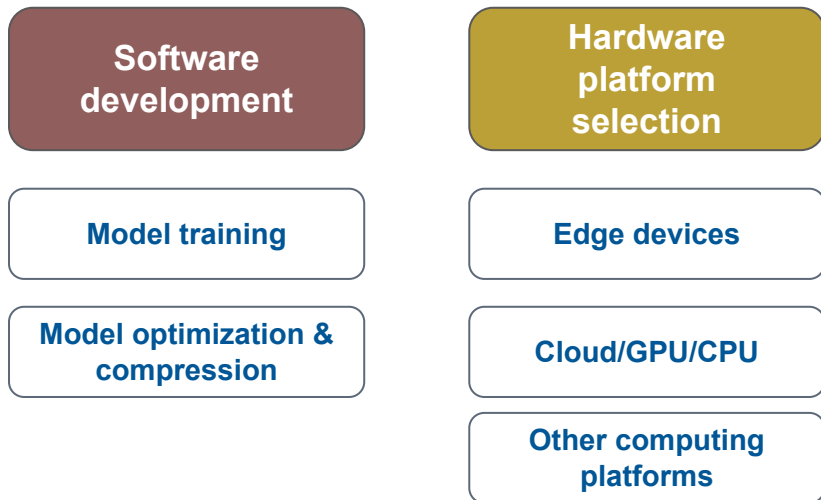
**Software
development**

Model training

**Model optimization &
compression**

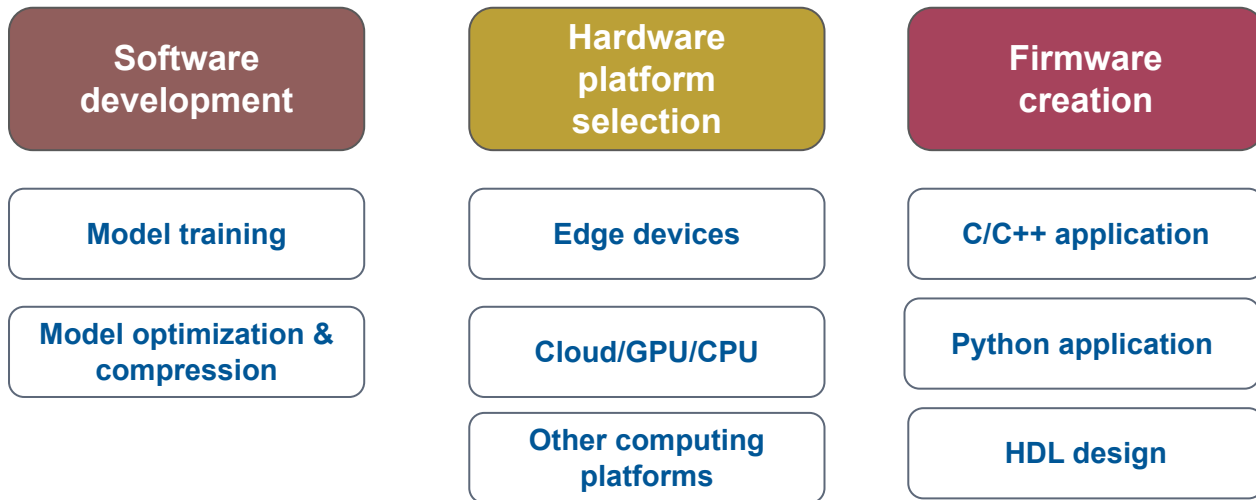
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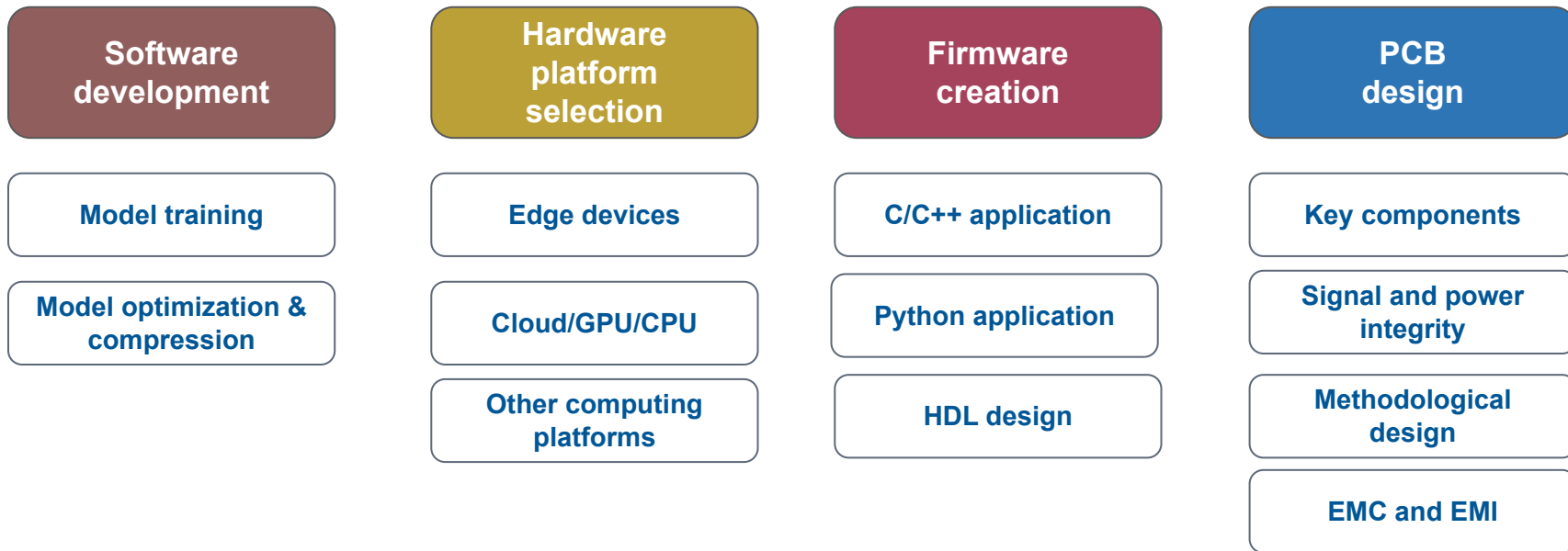
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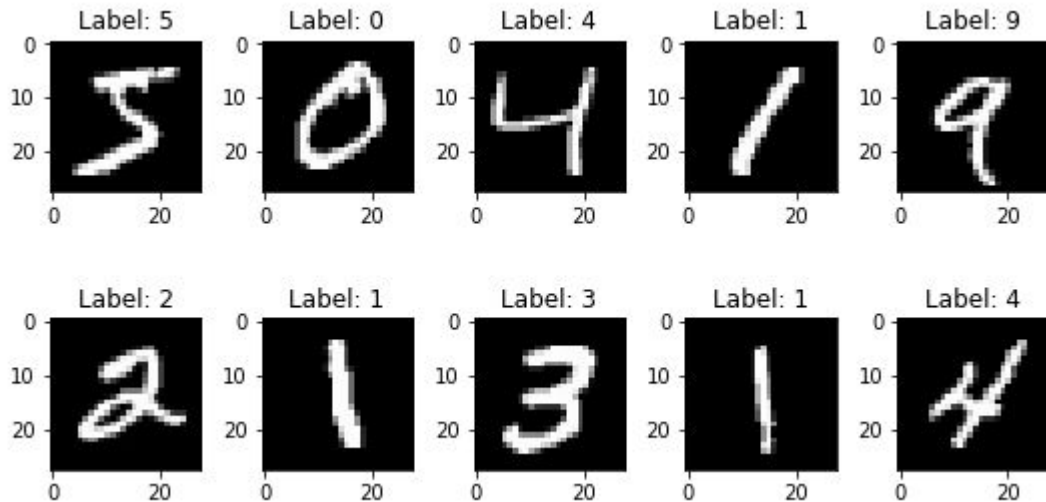


Case Study for FPGA-based Edge AI: MNIST Binary Classification.

ML and model compression techniques for SoC/FPGA

Demo: MNIST-based binary classification

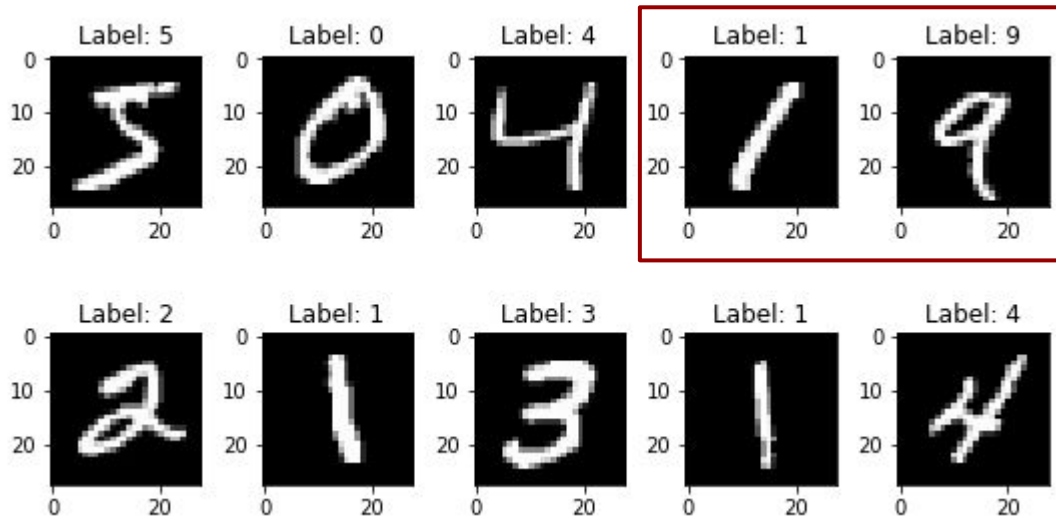
MNIST-based
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MNIST-based binary classification

- **Quantization-Aware Pruning**
 - 8-bits fixed point precision
 - 20% target sparsity
 - QKeras for model definition

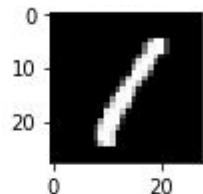
Layer (type)	Output Shape	Param #
fc1_input (QDense)	(None, 5)	3925
relu_input (QActivation)	(None, 5)	0
fc1 (QDense)	(None, 7)	42
relu1 (QActivation)	(None, 7)	0
fc2 (QDense)	(None, 10)	80
relu2 (QActivation)	(None, 10)	0
output (QDense)	(None, 2)	22
sigmoid (Activation)	(None, 2)	0

=====
Total params: 4,069
Trainable params: 4,069
Non-trainable params: 0
=====

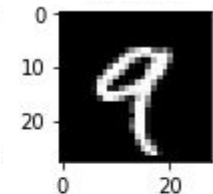
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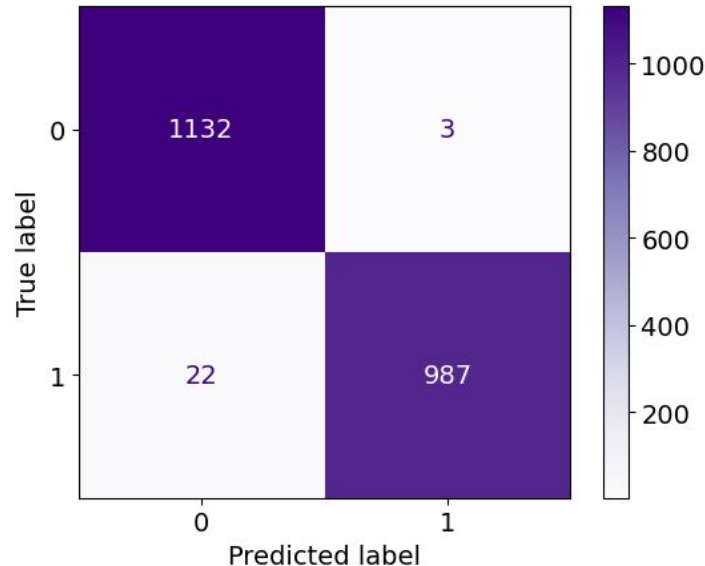
MNIST-based
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Class 0



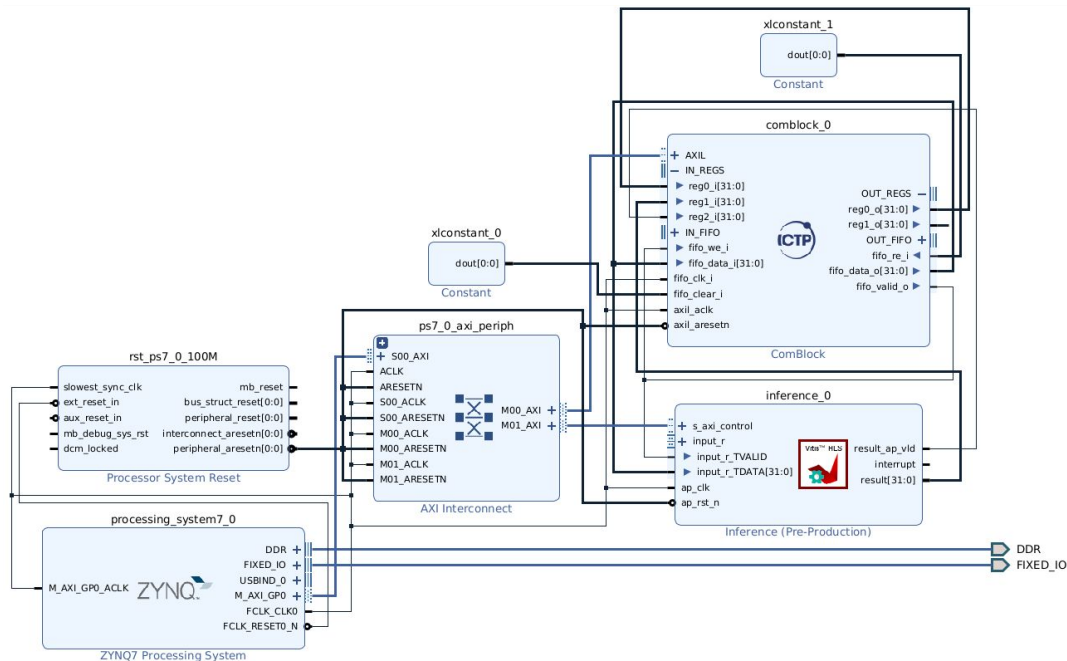
Class 1



ML and model compression techniques for SoC/FPGA

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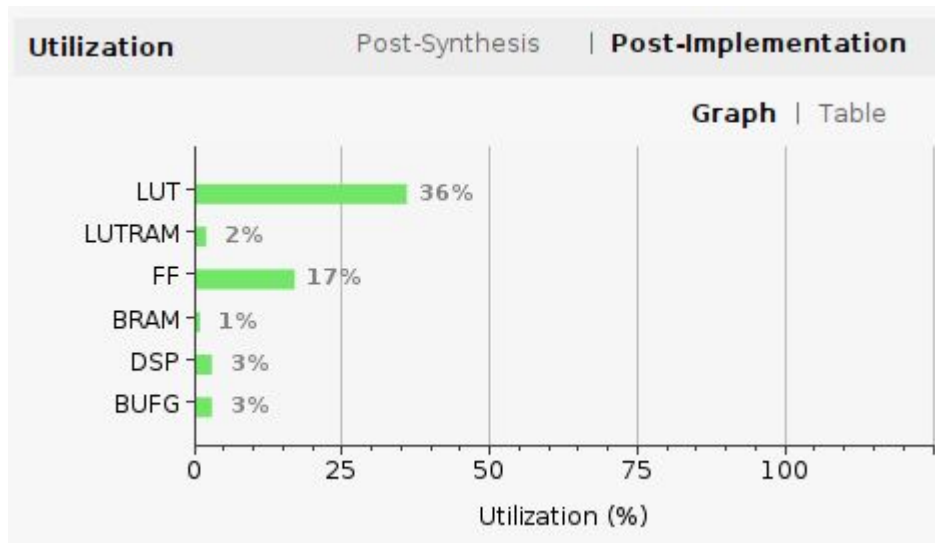
MNIST-based binary classification



ML and model compression techniques for SoC/FPGA

Demo: MNIST-based binary classification

MNIST-based
binary classification



ML and model compression techniques for SoC/FPGA

Demo: MNIST-based binary classification

MNIST-based binary classification

IP core based on ML integrated with PYNQ framework

```
In [ ]: from pynq import Overlay
        from pynq import MMIO
        import comblock as cbc

        import numpy as np
        import matplotlib.pyplot as plt
```

Load Overlay

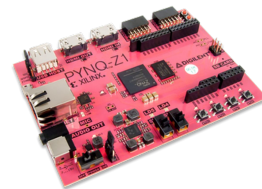
```
In [ ]: # Load the overlay (bitstream) onto the FPGA.

        ol = Overlay("design_1_wrapper.xsa")
```

The information from the **comblock_0** block is read to verify everything that is obtained. Since the object is mapped to AXI Lite, it is noted that the AXI Full address is omitted.

```
In [ ]: ## Overlay information

        ol.ip_dict
```



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Demo: MNIST-based binary classification

MNIST-based binary classification

ComBlock information

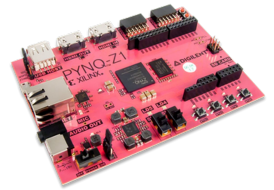
ComBlock for PYNQ: https://github.com/Mballina42/PynQ_ComBlock

For convenience, the `comblock.py` Python script is established which contains useful constants for interacting with the ComBlock.

```
In [ ]: ol.ip_dict['comblock_0']
```

```
In [ ]: # The object is created based on the comblock_0 IP
```

```
cb = ol.comblock_0
```



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Data preparation

[illegible]

```
In [ ]: imageArray = np.array(signal_1)

        image_2d = imageArray.reshape((28, 28))

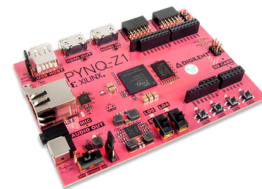
        # Display as an image
        plt.imshow(image_2d, cmap='gray', interpolation='nearest')
        plt.colorbar() # Optional: Show color scale
        plt.show()
```

[illegible]

```
In [ ]: imageArray = np.array(signal_2)

        image_2d = imageArray.reshape((28, 28))

        # Display as an image
        plt.imshow(image_2d, cmap='gray', interpolation='nearest')
        plt.colorbar() # Optional: Show color scale
        plt.show()
```



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Interacting with ComBlock

Signal 1

Write FIFO - Send image to the FPGA

```
In [ ]: cb.write(cbc.OREG1, 1)

# Send data to the ComBlock's FIFO
data_size = 28*28
for i in range(data_size):
    cb.write(cbc.OFIFO_VALUE, signal_1[i])
```

Read registers - Read inference result from the FPGA

```
In [ ]: # Read IREG1 to obtain the result of the inference process
        cb.read(cbc.IREG1)
```

Signal 2

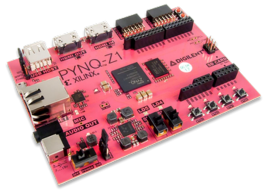
Write FIFO - Send image to the FPGA

```
In [ ]: cb.write(cbc.OREG1, 1)

# Send data to the ComBlock's FIFO
data_size = 28*28
for i in range(data_size):
    cb.write(cbc.OFIFO_VALUE, signal_2[i])
```

Read registers - Read inference result from the FPGA

```
In [ ]: cb.read(cbc.IREG1)
```



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