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Joint ICTP-IAEA School on Detector Signal Processing and Machine Learning for Scientific Instrumentation and Reconfigurable Computing | (smr 4110)

Friday 31 October 2025

- Kastler Lecture Hall (AGH) (09:00-18:00)

time title	presenter
09:00 High-Level Synthesis (HLS) – Part II	FERNANDO RINCON
10:00 Coffee Break	
10:30 Integrating Intelligence in 5G: How ML and Al Are Shaping 5G Networks?	DEJAN VUKOBRATOVIC
11:30 Using FPGAs to Accelerate Machine Learning Algorithms	ROMINA MOLINA
12:30 Lunch Break	
14:00 Edge Al Applications on FPGA-Based Systems	ROMINA MOLINA
15:00 Lab 5.1: Integrating ML Models with HLS4ML for Hardware Synthesis	
16:00 Coffee Break	
16:15 Lab 5.2: Deploying Machine Learning Models on SoC-FPGA	