Outline

❏ Digital CMOS design

- Boolean algebra

- Basic digital CMOS gates

- Combinational and sequential circuits

- Coding - Representation of numbers
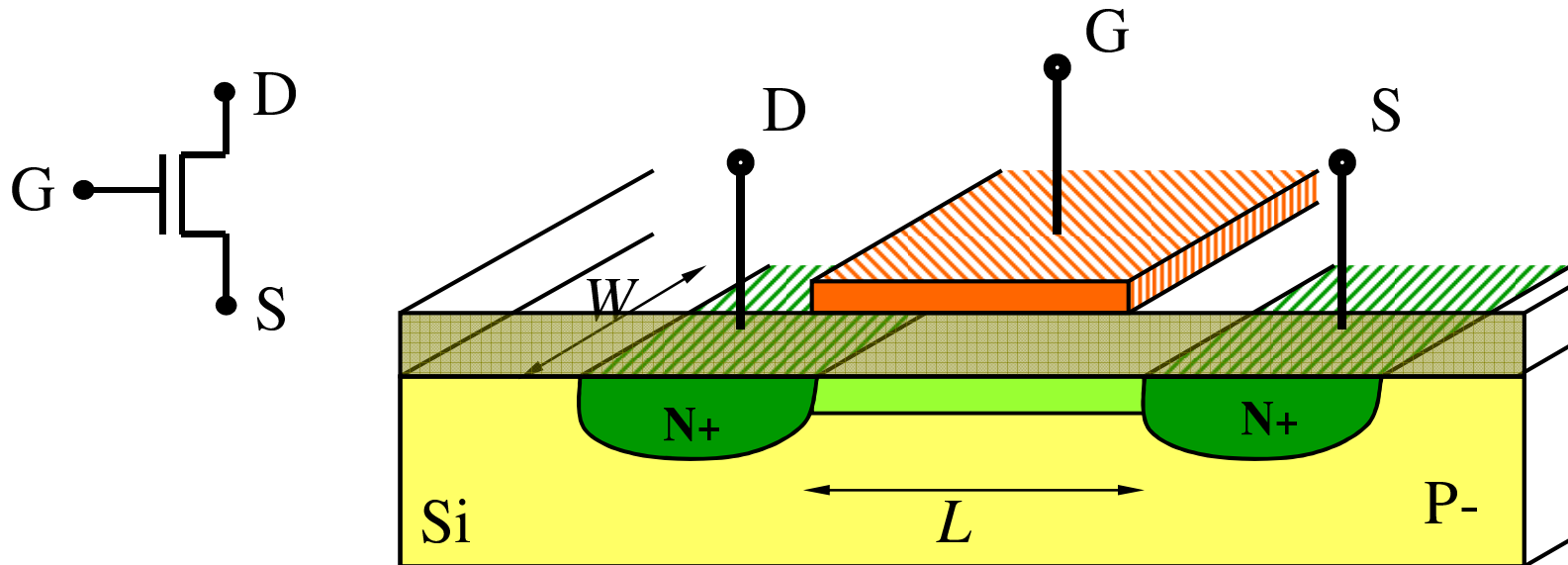
Basic CMOS Gates

How to implement Boolean functions

in CMOS technology ?

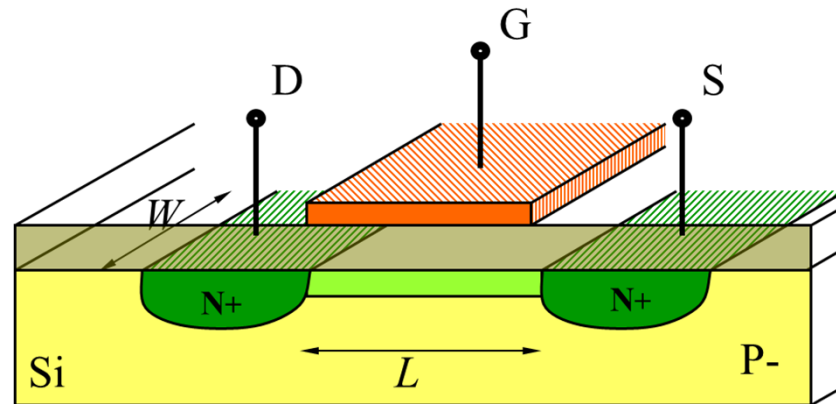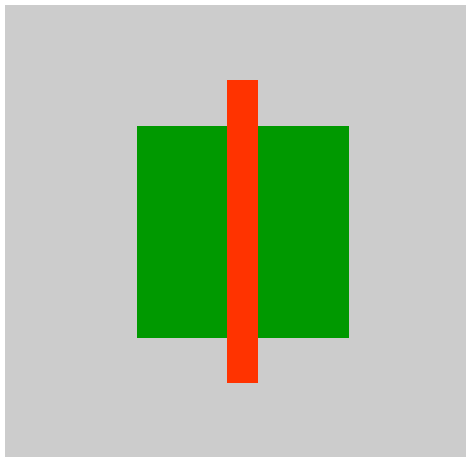Which functionalities are available

Basic CMOS Gates

- N-MOS transistor

G · D

G · S

D

G

S

W

N+   N+

L

Si   P-

Basic CMOS Gates

- N-MOS transistor

Basic CMOS Gates

Ids

Vgs = 1.2 V

Vgs = 1.0 V
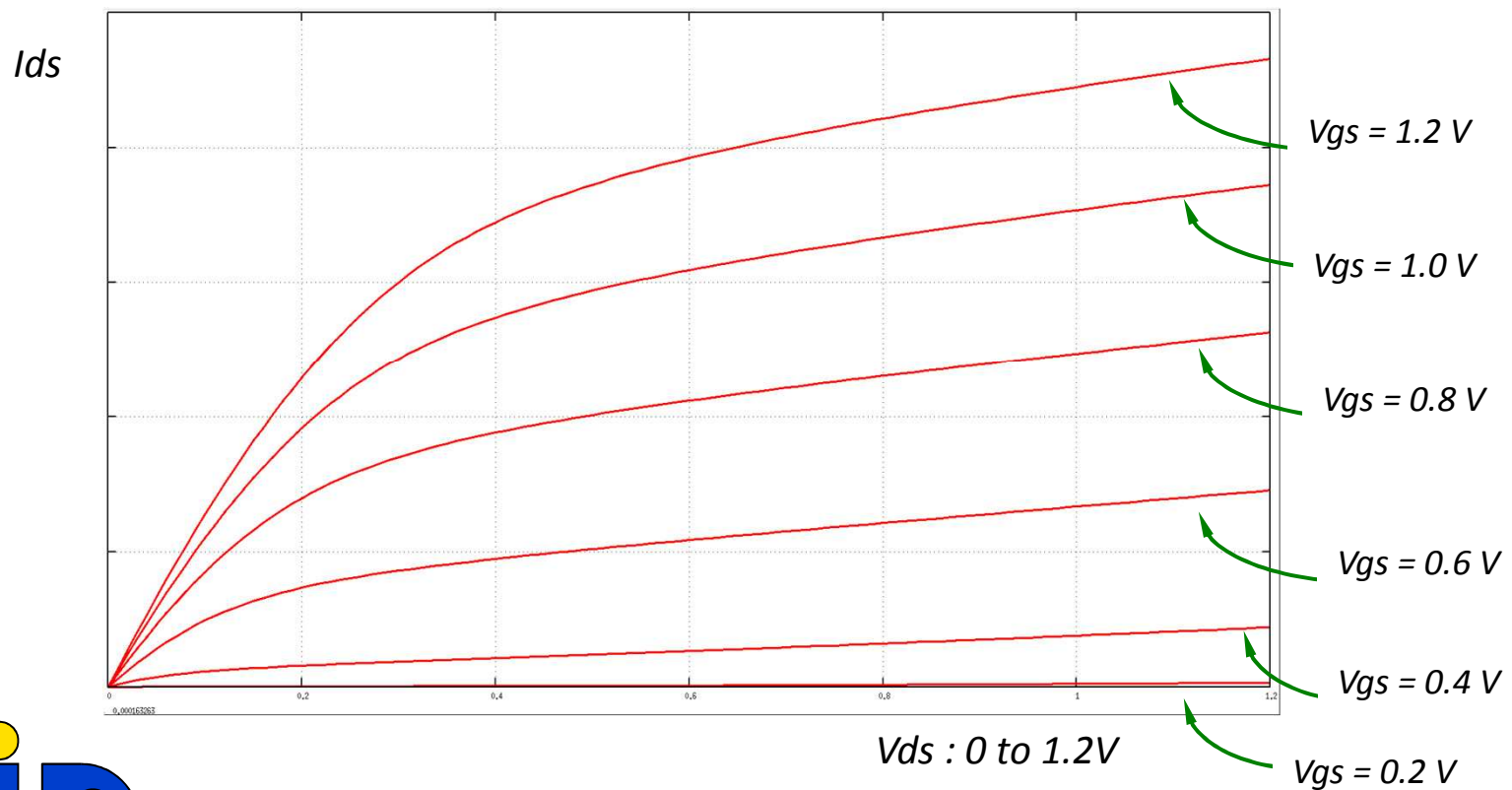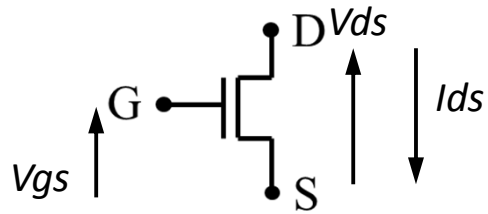
Vgs = 0.8 V

Vgs = 0.6 V

Vgs = 0.4 V

Vds : 0 to 1.2V

Vgs = 0.2 V

Basic CMOS Gates

- P-MOS transistor

Vgs S *Vds*

G *Ids*

D

Ids

Vdd-Vgs = 1.2 V

Vdd-Vgs = 0.2 V

Vds : -1.2 to 0V
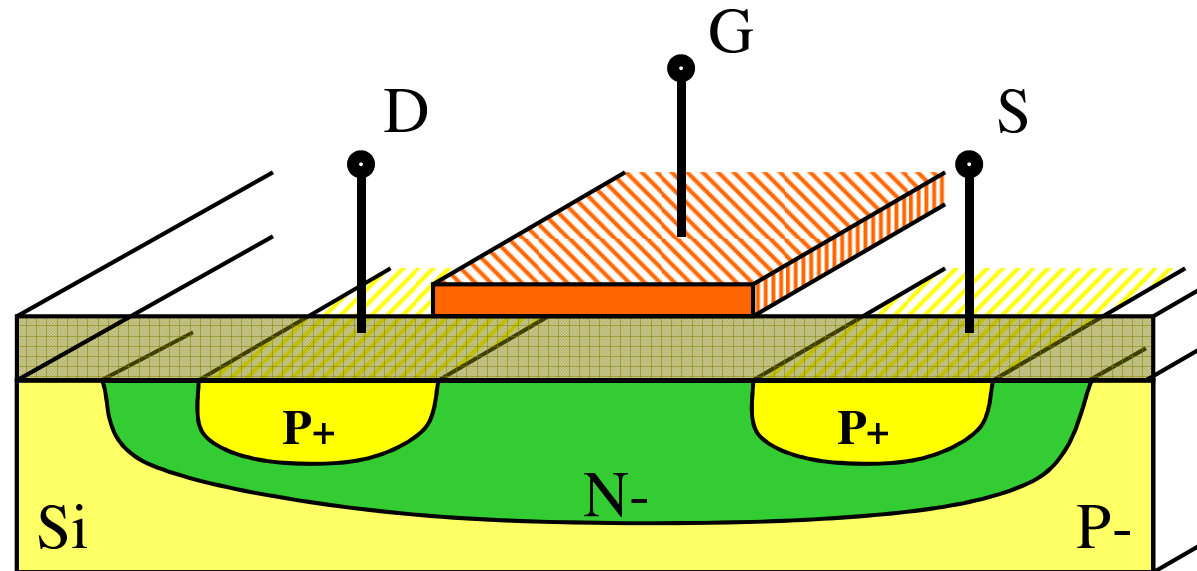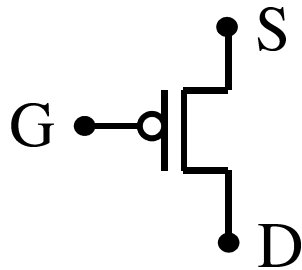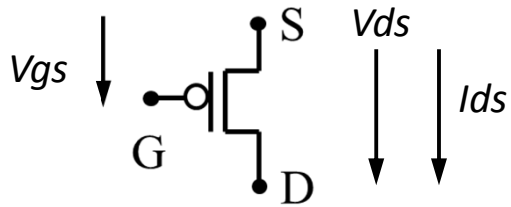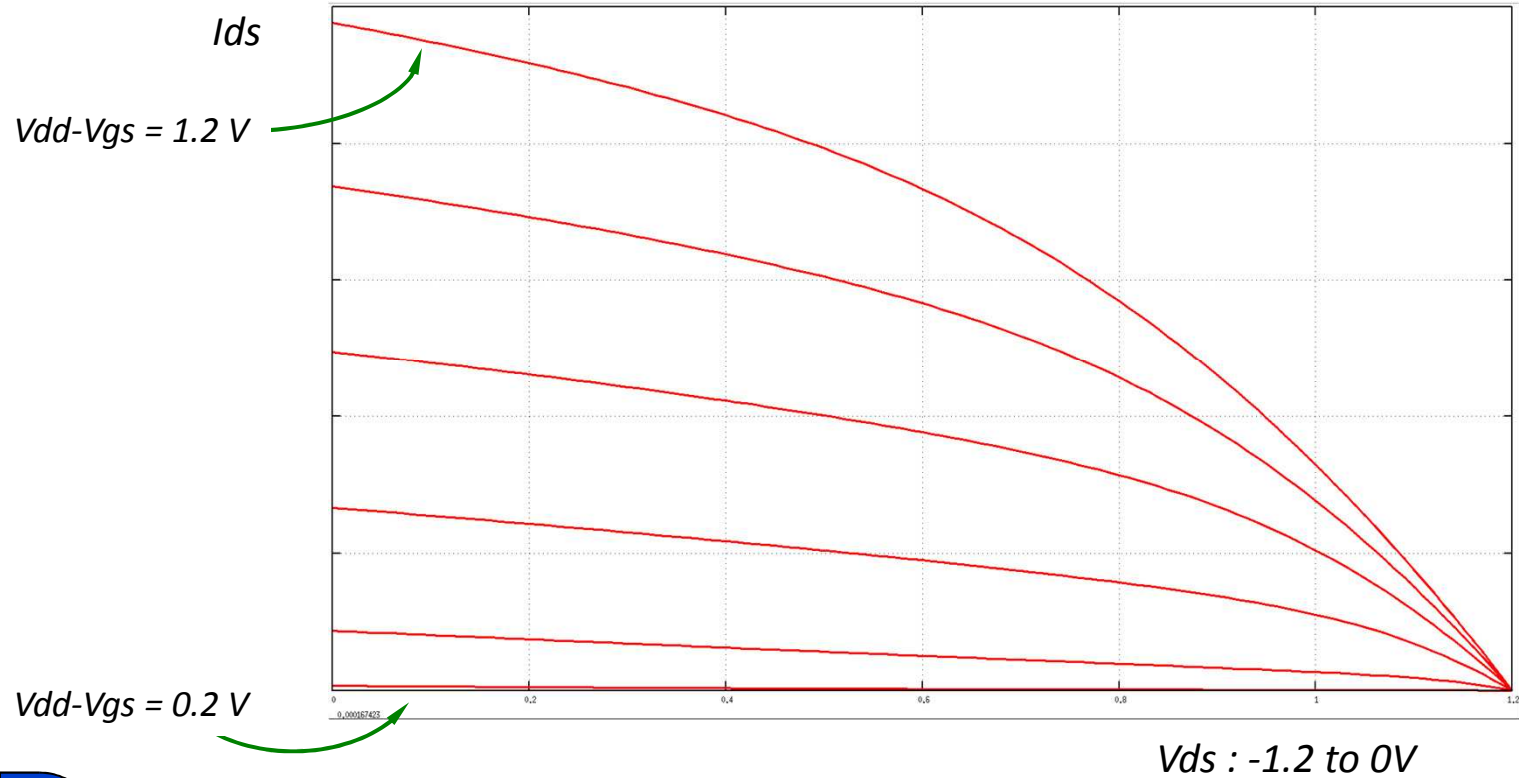
Basic CMOS Gates
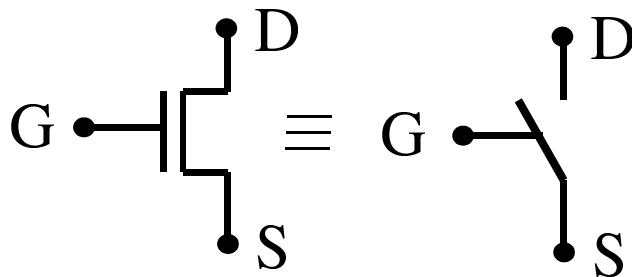
The electrical behavior of a MOS transistor

is very complex

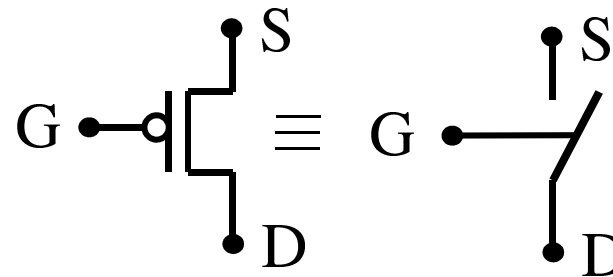Design of a multi-million transistor circuit ?

Basic CMOS Gates

In a digital circuit a MOS transistor can be seen as a Switch

N-MOS

P-MOS

D = S when G = 1

D = S when G = 0

Basic CMOS Gates

When driving, a MOS transistor can be seen as a Resistor

$$Resistance \propto \frac{L}{W} \qquad Conductance \propto \frac{W}{L}$$

For the same size, a P-MOS is twice
more resistive than an N-MOS

Basic CMOS Gates

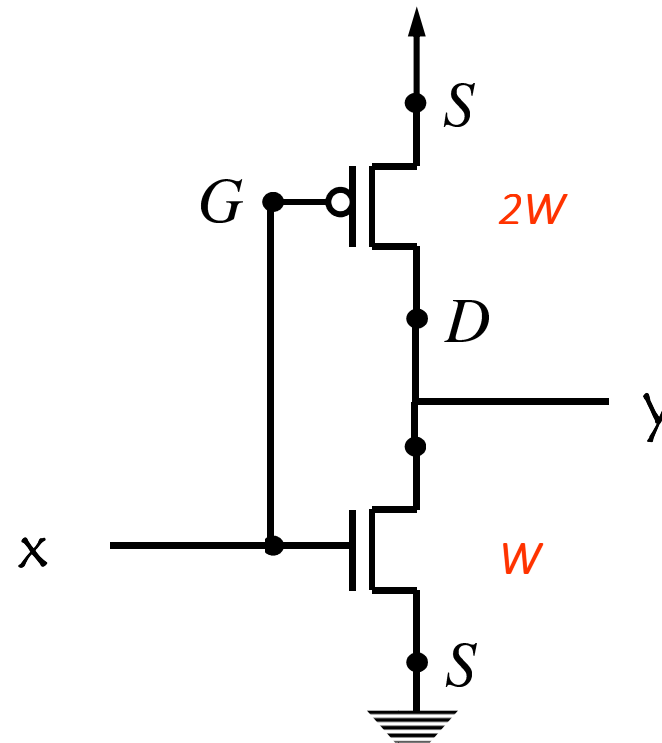The N-MOS and P-MOS are not exactly symmetrical

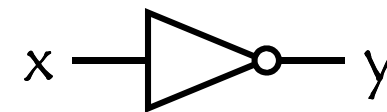A N-MOS is a good transmitter of 0
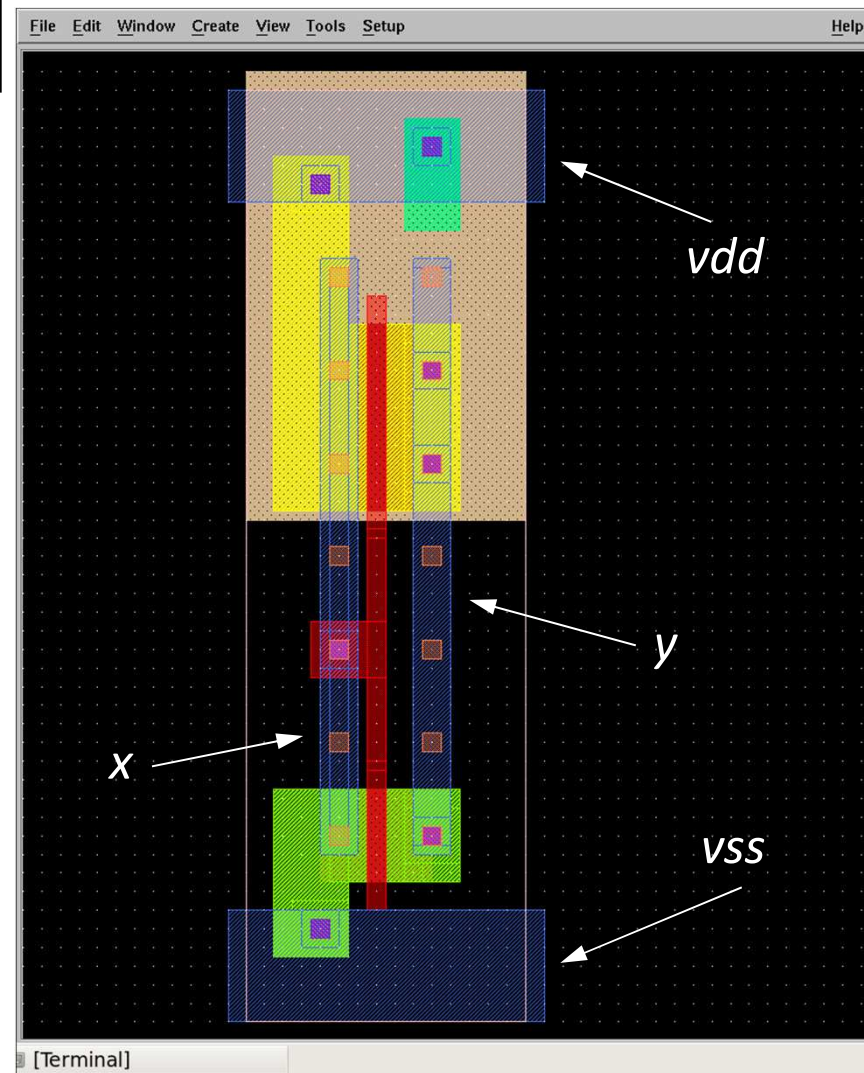
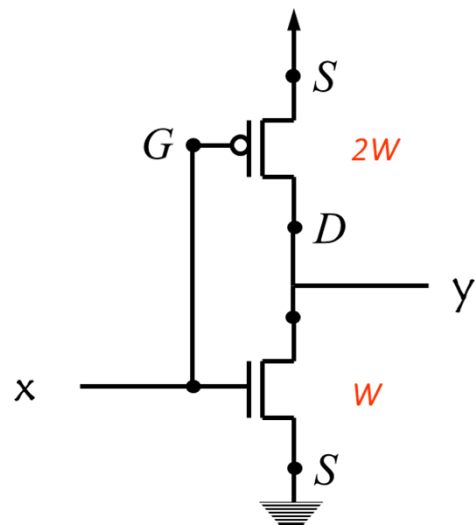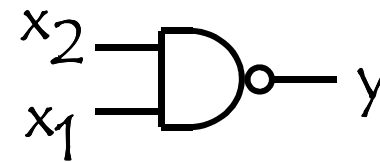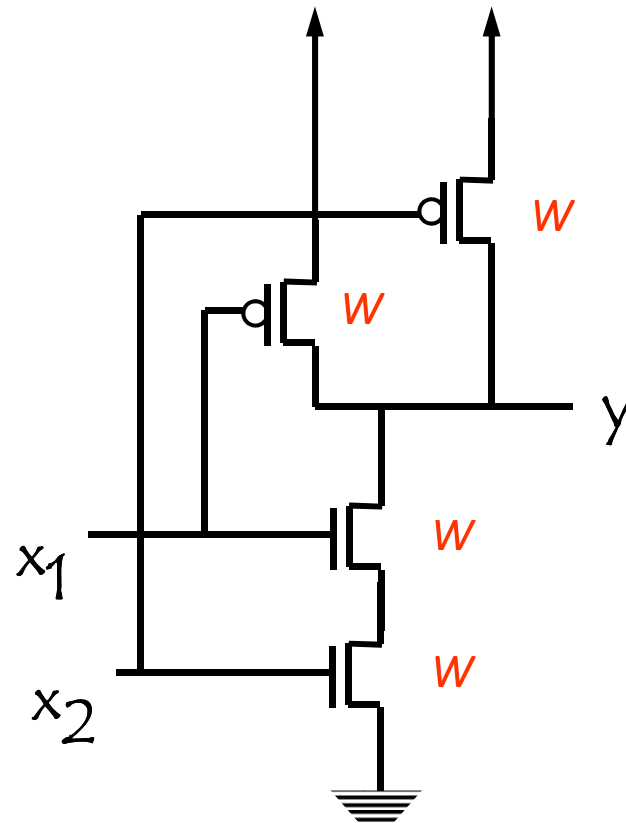A P-MOS is a good transmitter of 1

Basic CMOS Gates

y = *Not* x

Dual CMOS gate

Basic CMOS Gates

Basic CMOS Gates

$$y = \overline{x_1 \cdot x_2}$$

Basic CMOS Gates
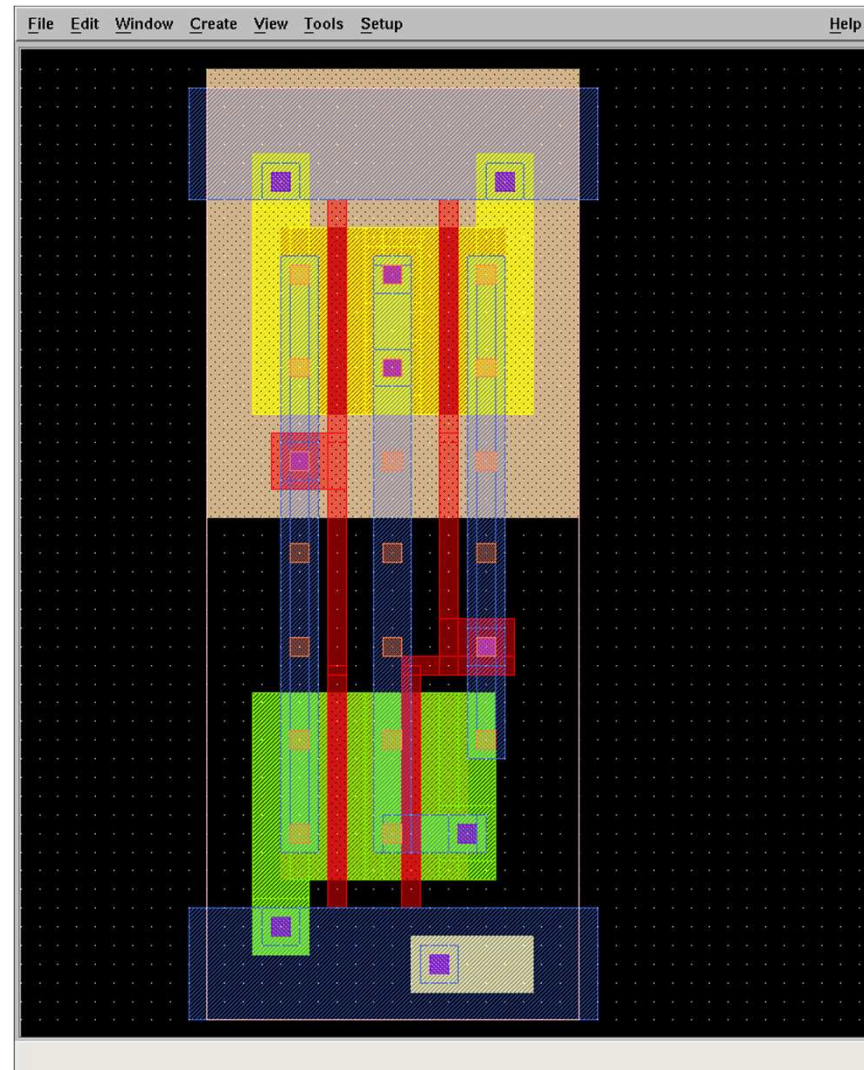
Basic CMOS Gates

Basic CMOS Gates

Design of a dual gate

P network

N network

x_i

y
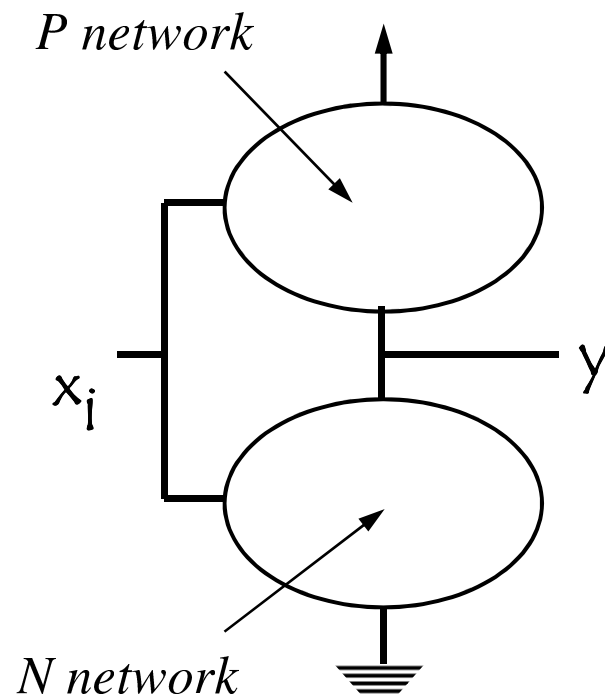
The P-network must be the dual of the N-network

Series $\longrightarrow$ Parallel

Parallel $\longrightarrow$ Series
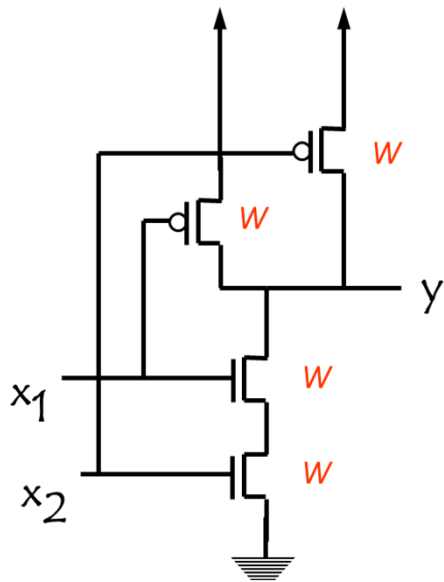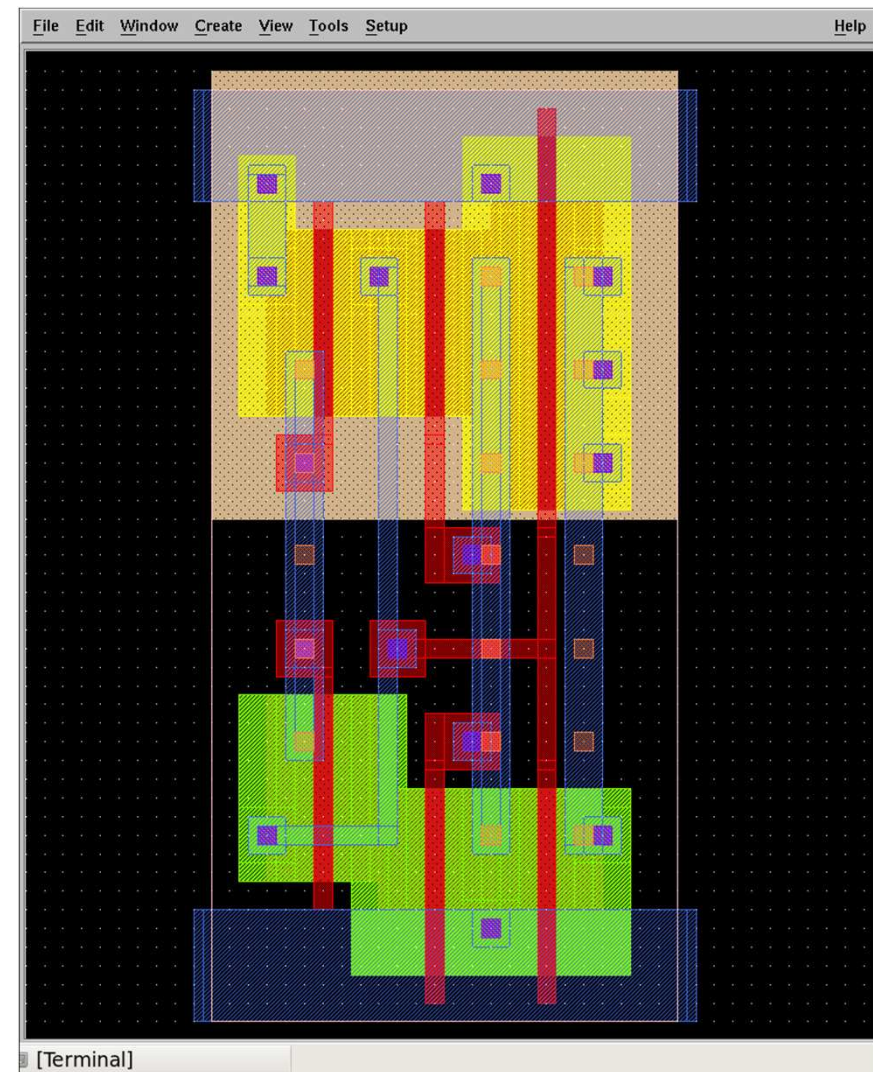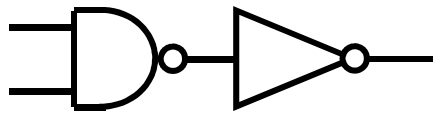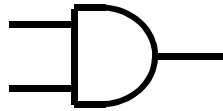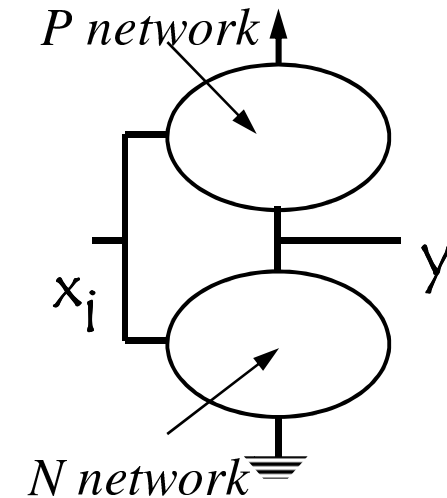
Take care of the size of transistors

Basic CMOS Gates

- To set the output to 0 a path has to be created through the N network

- A series of N-transistor must be conducting

$$\prod x_i = 1$$

P network

x_i

y

N network

Only negative (inverting) functions can be created

Basic CMOS Gates

Implementing a Boolean function with a CMOS gate ?

- The function must be inverting in regard of all the variables

- Put the function in the form of $f = \overline{g}$

- Design the N-network of g

Basic CMOS Gates

Implementing a Boolean function with a CMOS gate ?

○ In the expression of g each ′. ′ are two paths in series

○ In the expression of g each ′+ ′ are two paths in parallel

○ The P-network is the dual network of the N-network

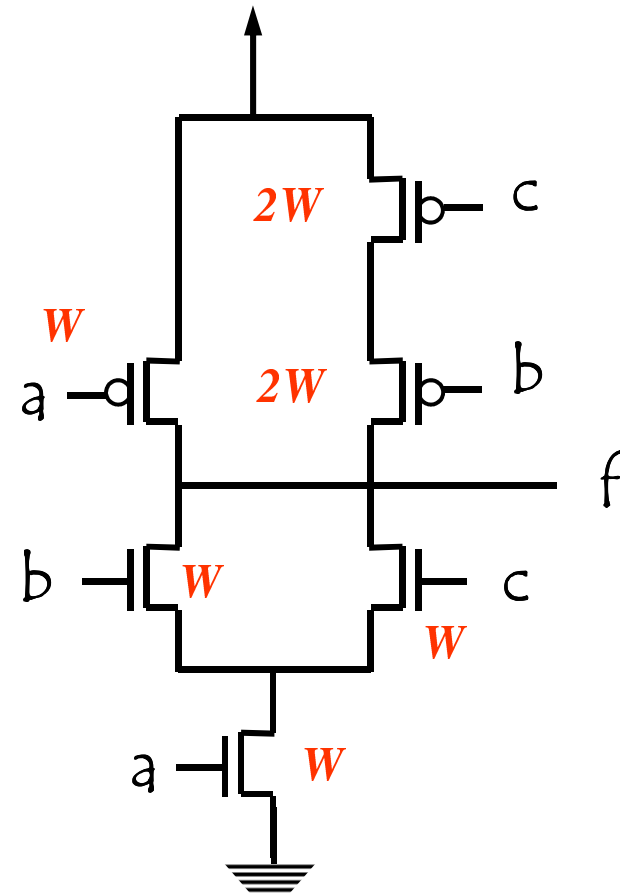○ Avoid putting more than 3 transistors in series

Basic CMOS Gates

Example :

$$f = \overline{a} + (\overline{b}.\overline{c})$$

$$f = \overline{a} + (\overline{b+c})$$
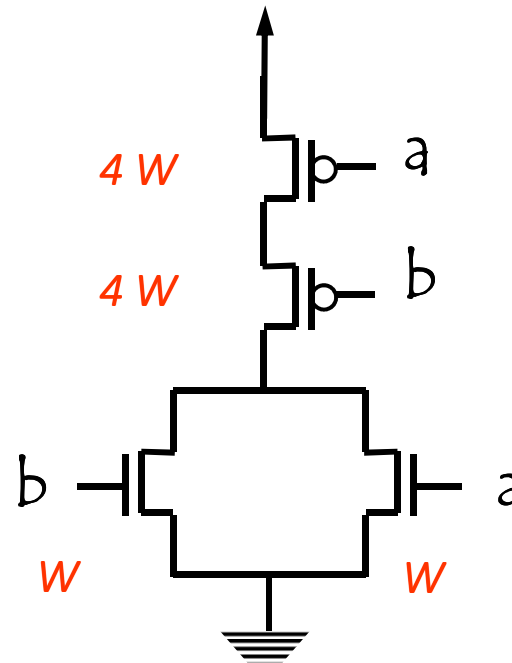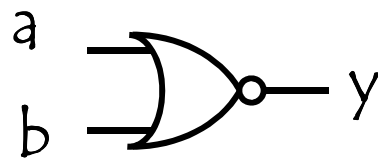
$$f = \overline{a \cdot (b+c)}$$

$$g = a \cdot (b+c)$$

Basic CMOS Gates

Some gates :

Inverter : $f = \overline{a}$

Nand : $f = \overline{a.b}$

Nor : $f = \overline{a+b}$

4 W

4 W

a

b

b

a

W

W

a

b

y

Basic CMOS Gates

Some gates :

Multiplexer :

$$f = \overline{a.s + b.\overline{s}}$$