SoC Based Reconfigurable Virtual Instrumentation (RVI)

Typical Global Architecture

Input/output signals

FPGA

uP

FMC interface

PC

Visualize/ Control/ Computing

uP – PC Communication SW (uP)

FPGA – uP Communication SW (uP)

Application Specific IP

Memory Controller

External DDR

External Hardware (Application specific)

Native or Wishbone interface

uP2FPGA

FIFOs

FPGA2uP

FIFOs

True Dual Port RAMs

Memory Mapped AXI Lite/ AXI Full/ AXI Stream

Registers

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User

Core Logic Design

Control Registers/ FIFOs and True Dual Port RAM

uP – PC Communication SW (uP

User Core Program

External Hardware specific Interface

Native or Wishbone interface

FPGA – uP Communication Block (FPGA)