Pulse Processing in FPGA

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Implementation goals

The aim is the reduction of hardware resources and power consumption

FPGA hardware resources (embedded in FPGA):

- Hardware multipliers (18x18) with high maximal frequencies:
  - Kintex-7, 544 MHz
  - Kintex UltraScale, 631 MHz
  - Virtex UltraScale+, 800-866 MHz
  - Zynq UltraScale+, 820-860 MHz
- Logic elements – adders, subtractors, multiplexers, and LUTs
- RAM memories – 18Kb each

FPGA – power consumption

Strong limitations on power consumption in E61 and HK experiments – 4/10 W

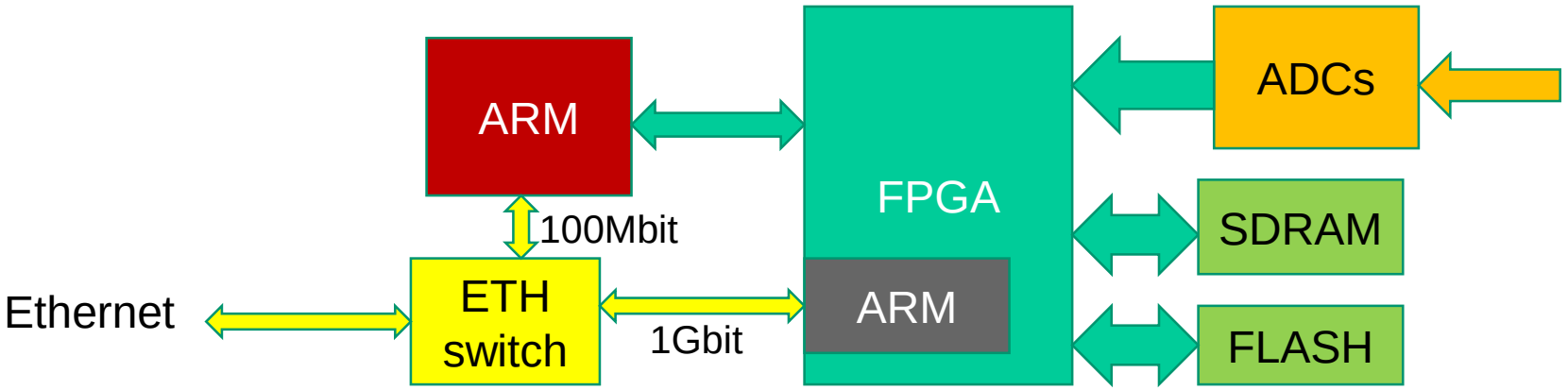
The digital system should include:

- FPGA device – at least 2W
- SDRAM memory – 1W
- External ARM microcontroller – 0.5W - 1W
- DC/DC converters – 0.5W

FPGA size should be as small as possible

Low-power modes should be used when data are not important

1Gbps Ethernet requires switch and more complex FPGA with internal ARM – higher power consumption by 1W-2W -> Decision to limit Ethernet to 100 Mbps

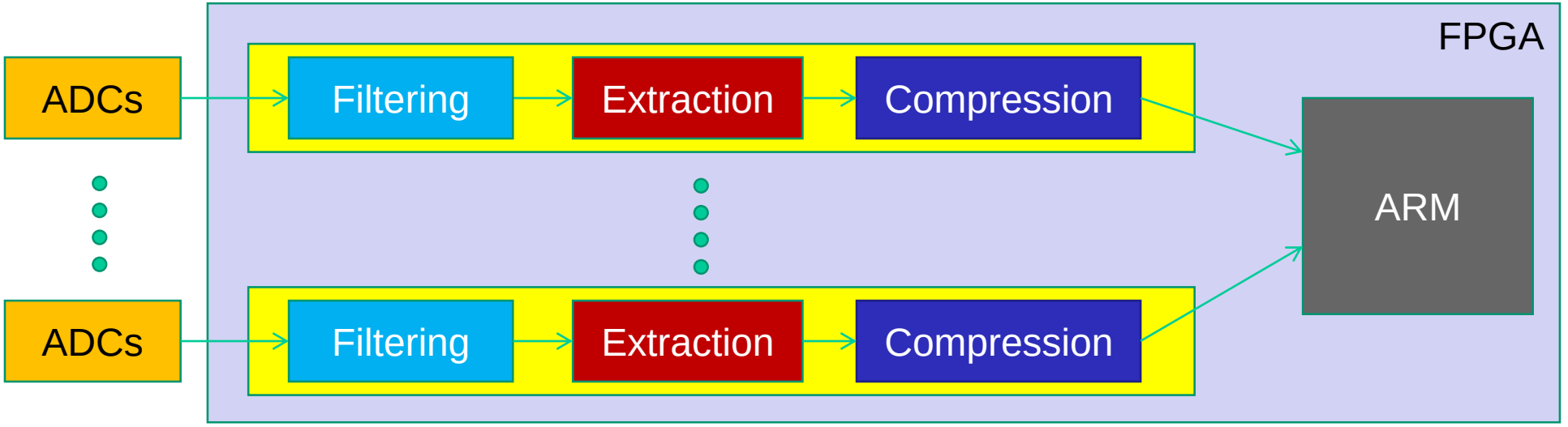


FPGA – architecture

Filtering, Extraction, and Compression in the basic version is not complex

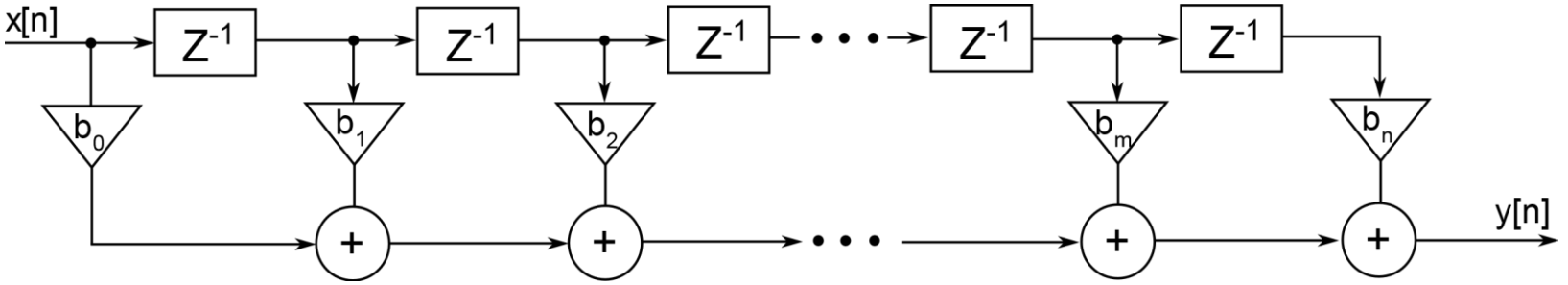
Parallel processing for 19 PMTs in HK significantly increases requirements on resources and power

Resource sharing between channels is useful

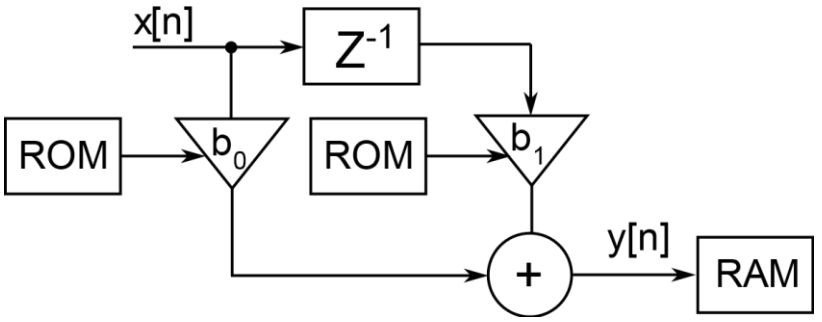


Filter structures

- Direct implementation

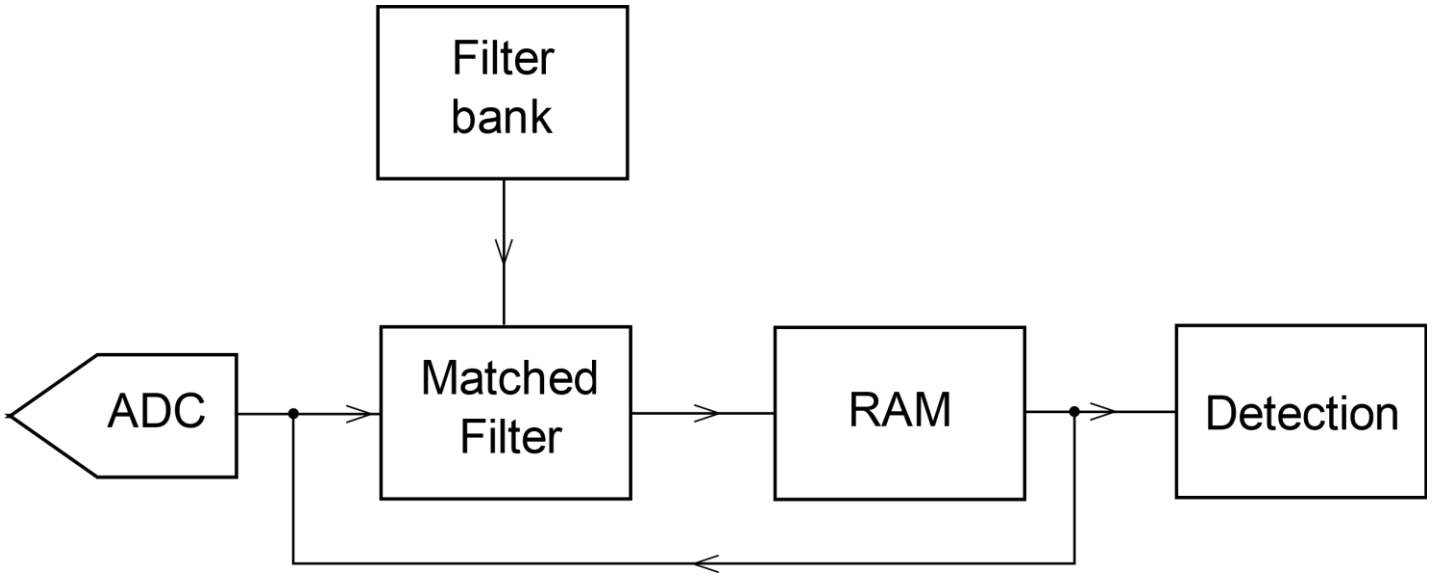


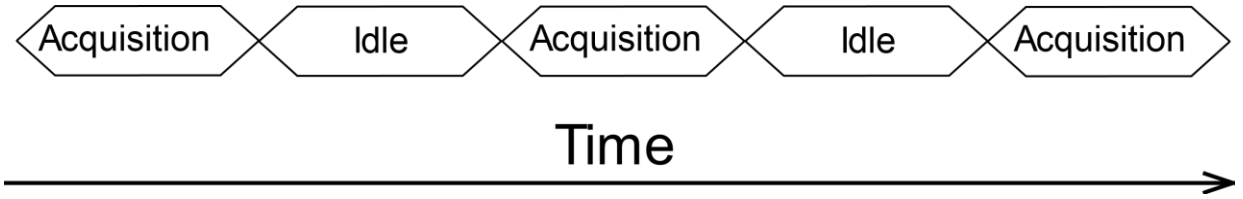
- Sampling frequency usually much smaller than multiplier limitations
  - Several filter cycles are in one sampling cycle,
  - It is possible to reduce the filter complexities around six (630/100) or eight (820/100) times
  - For example, number of multiplications is reduced from 80 to: 13 80/6 ~ 13 or 80/8 = 10



Filter scheduling (1)

- Filter sharing for different coefficients

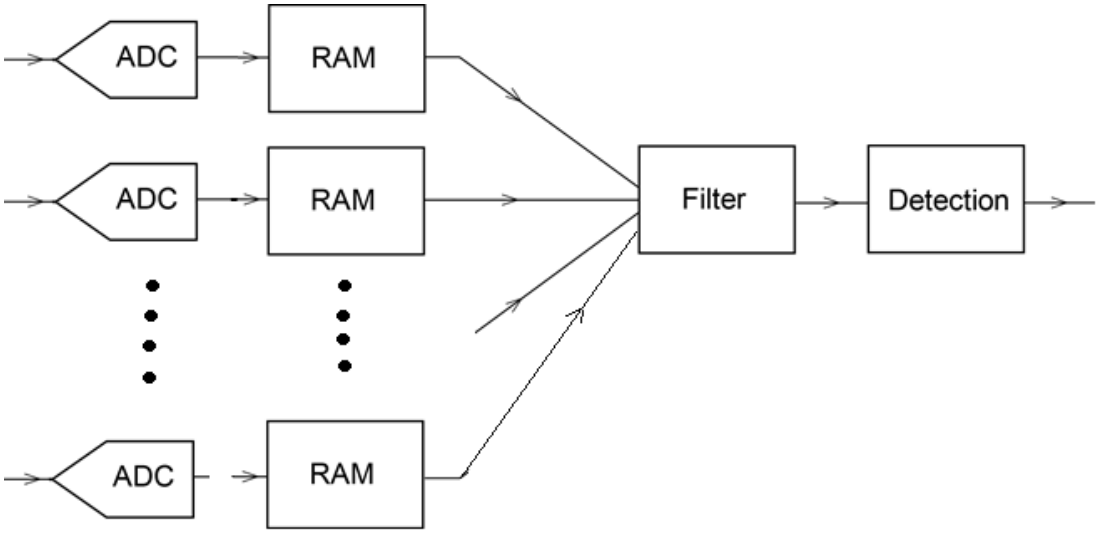


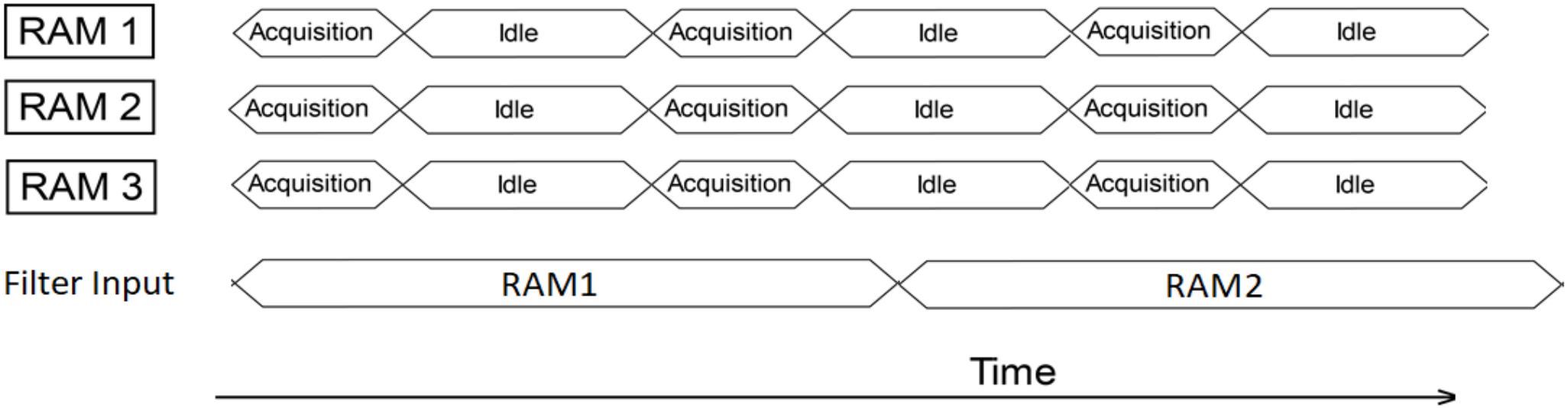


- Input from ADC in acquisition mode and feedback in the idle mode

Filter scheduling (2)

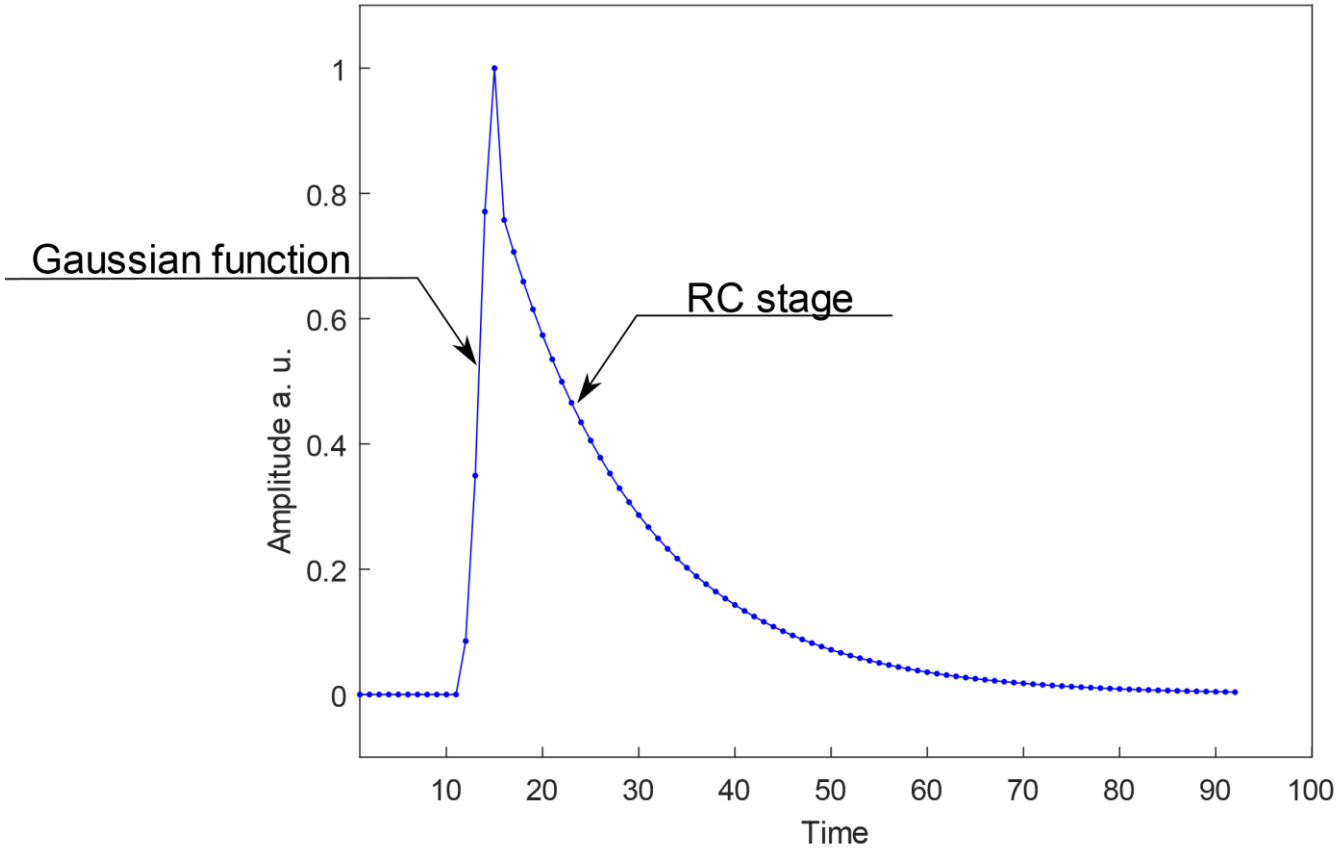
- Filter sharing for several channels





Example detector response

- Sampling frequency 100 Msample/s (10 ns sampling period)
- Fast rising edge like a Gauss function - 4 samples
- Slow falling edge like an RC stage - about 80 samples

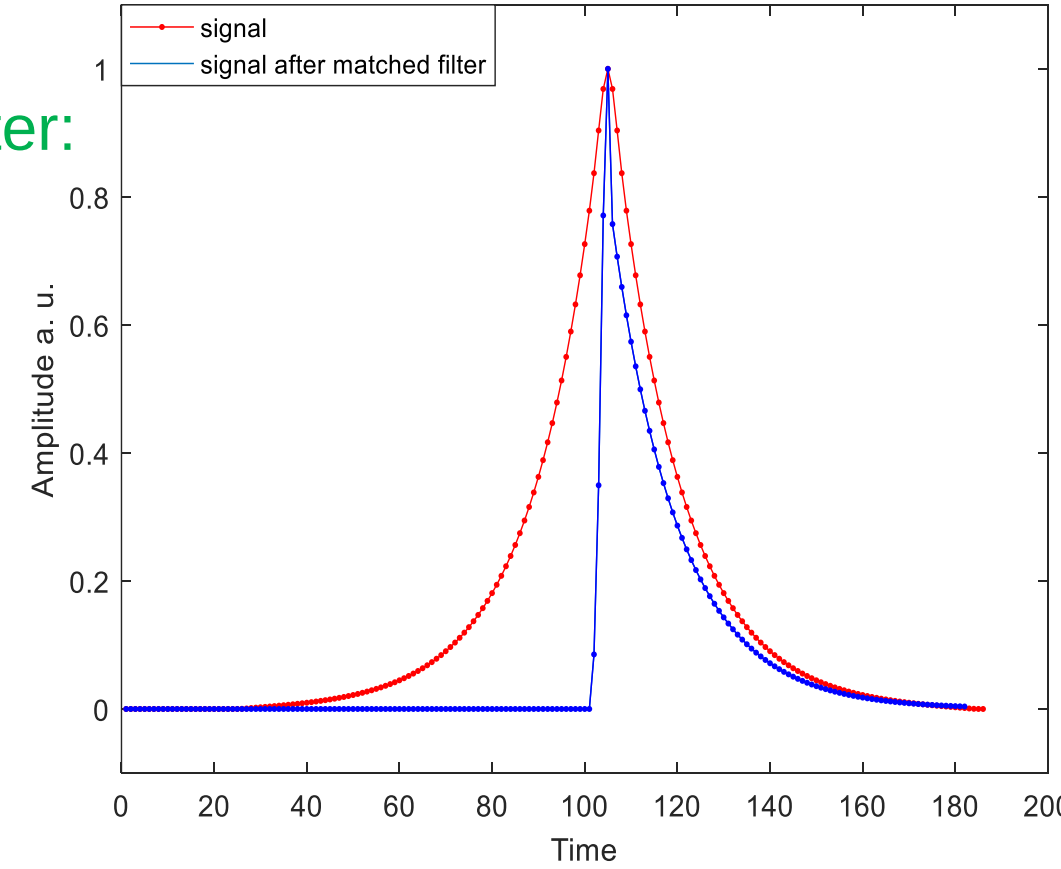


Straightforward filter implementation

- Detector response about 800 ns (80 samples)
- 80 filter coefficients

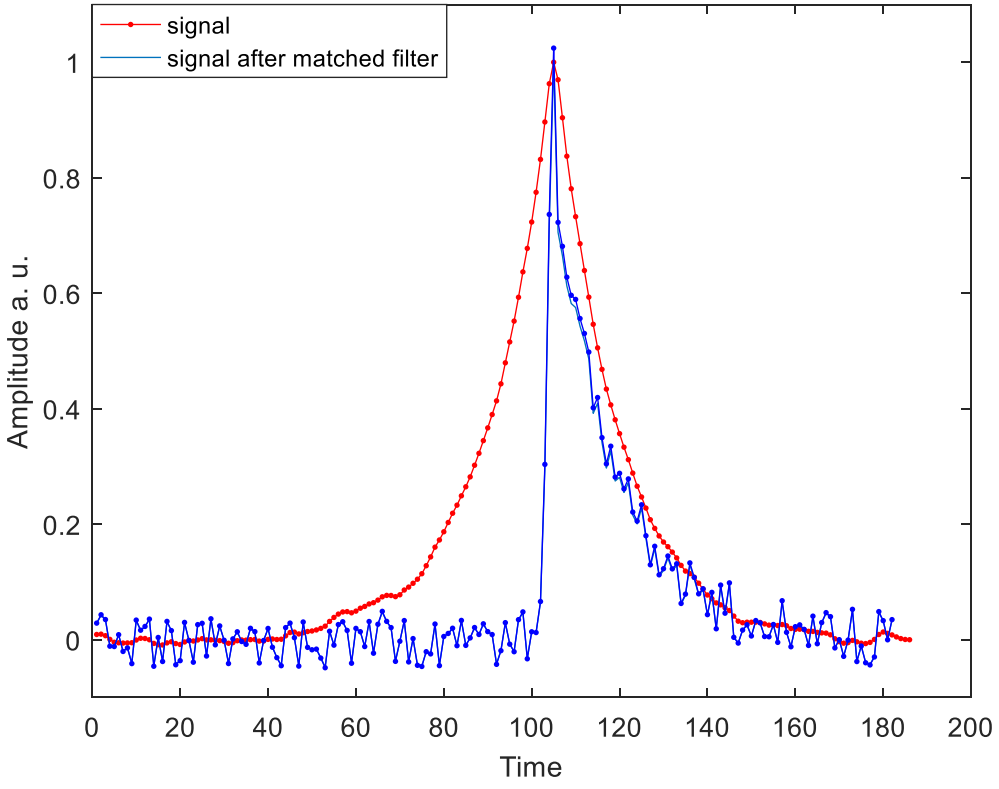
Requirements for the matched filter:

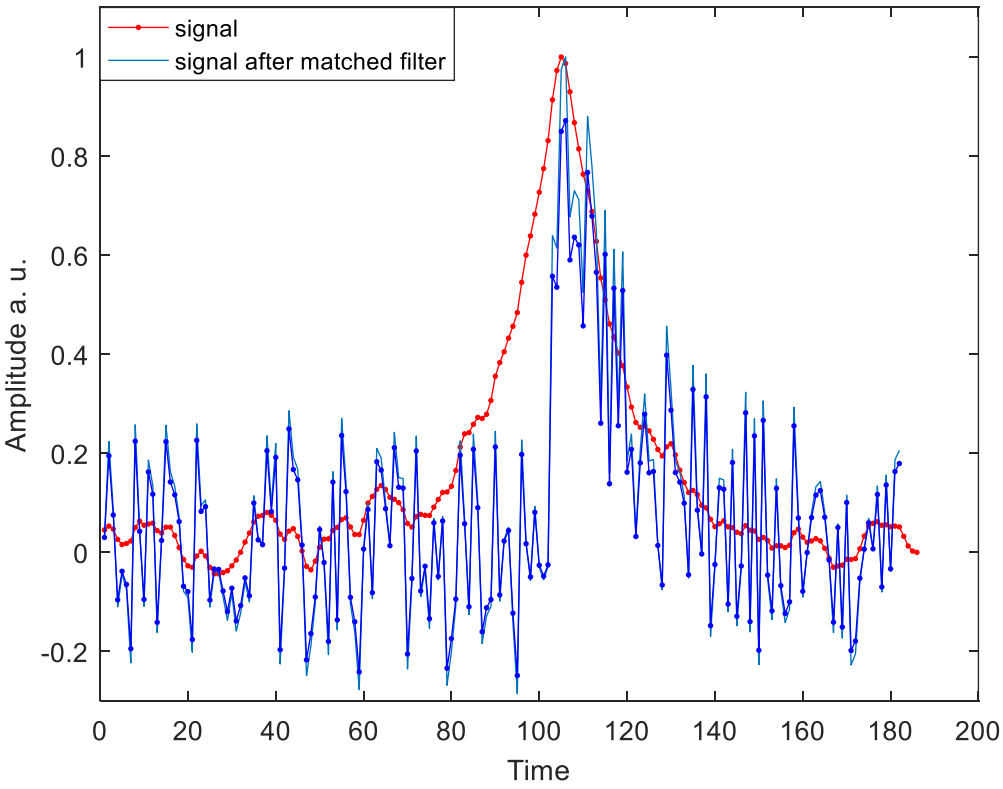
- 80 multiplications
- 80 additions / subtractions



Waveform with noise (1)

- Noise negatively affects time extraction
  - Higher SNR facilitates the design
- Matched filter significantly improves the signal quality
  - Pulse shapes are well-defined

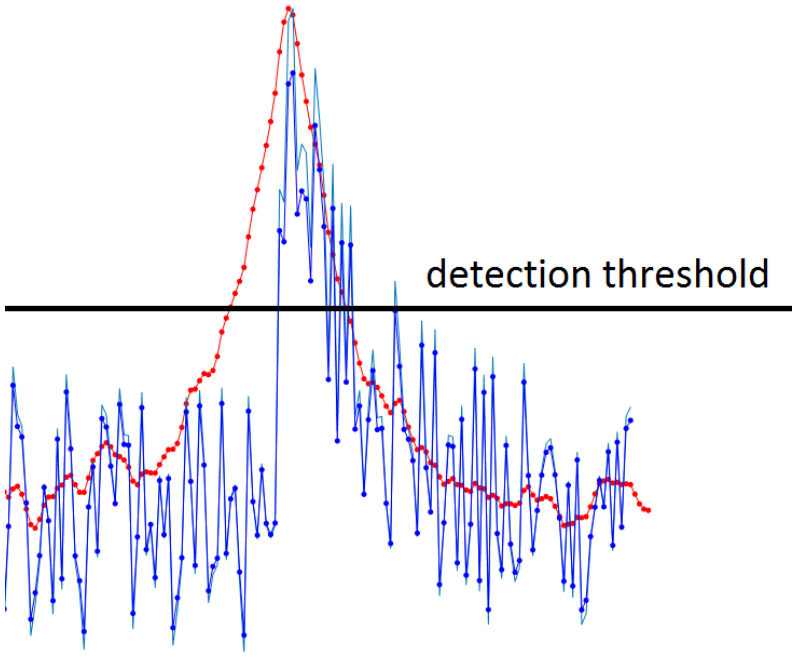




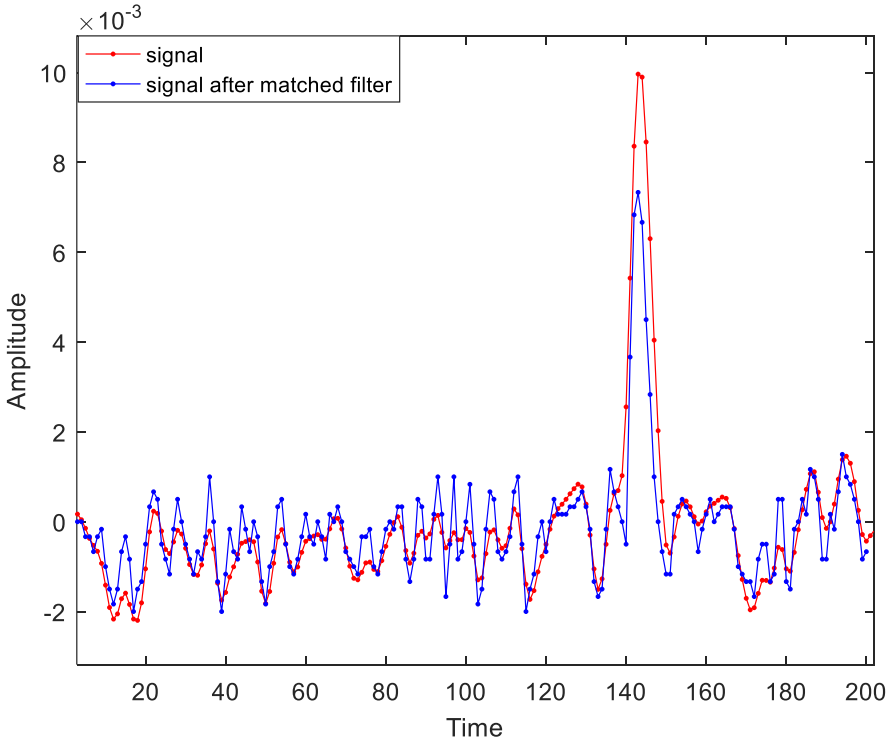
Waveform with noise (2)

- Improved pulse shapes allow signal parameters for detection.
  - The noise on the pulse does not trigger the false detection

Simulation on example waveform

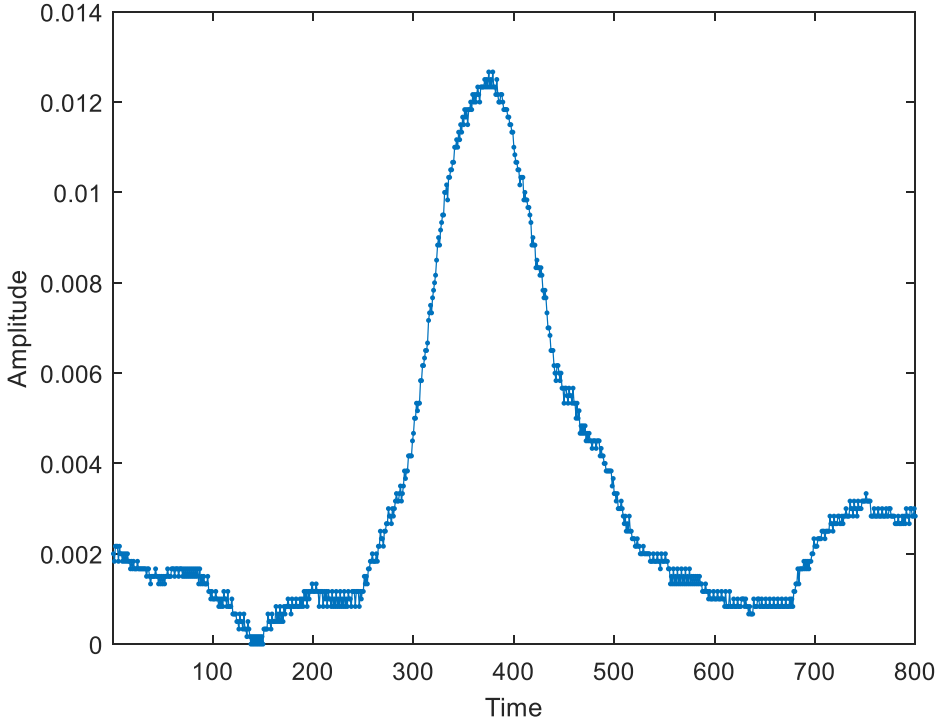


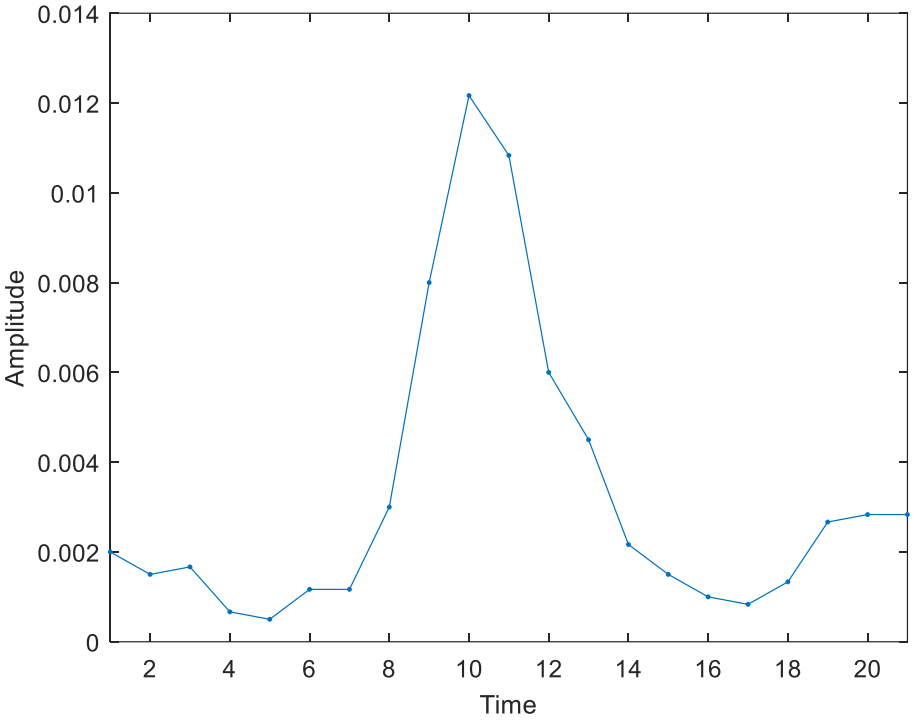
Signal from the SK detector (11 coefficients)



Sampling frequency

What signal accuracy is required?





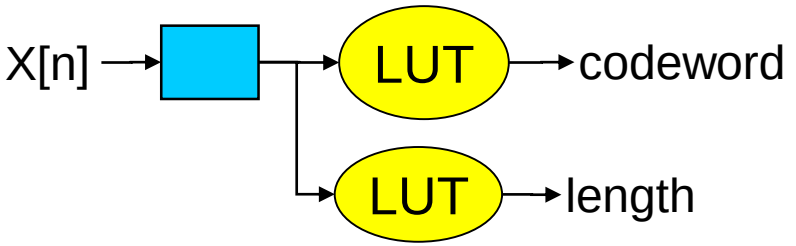
- 4 Gsamle/s -> 450 samples 100 Msamle/s -> 11 samples

Sampling frequency affects:

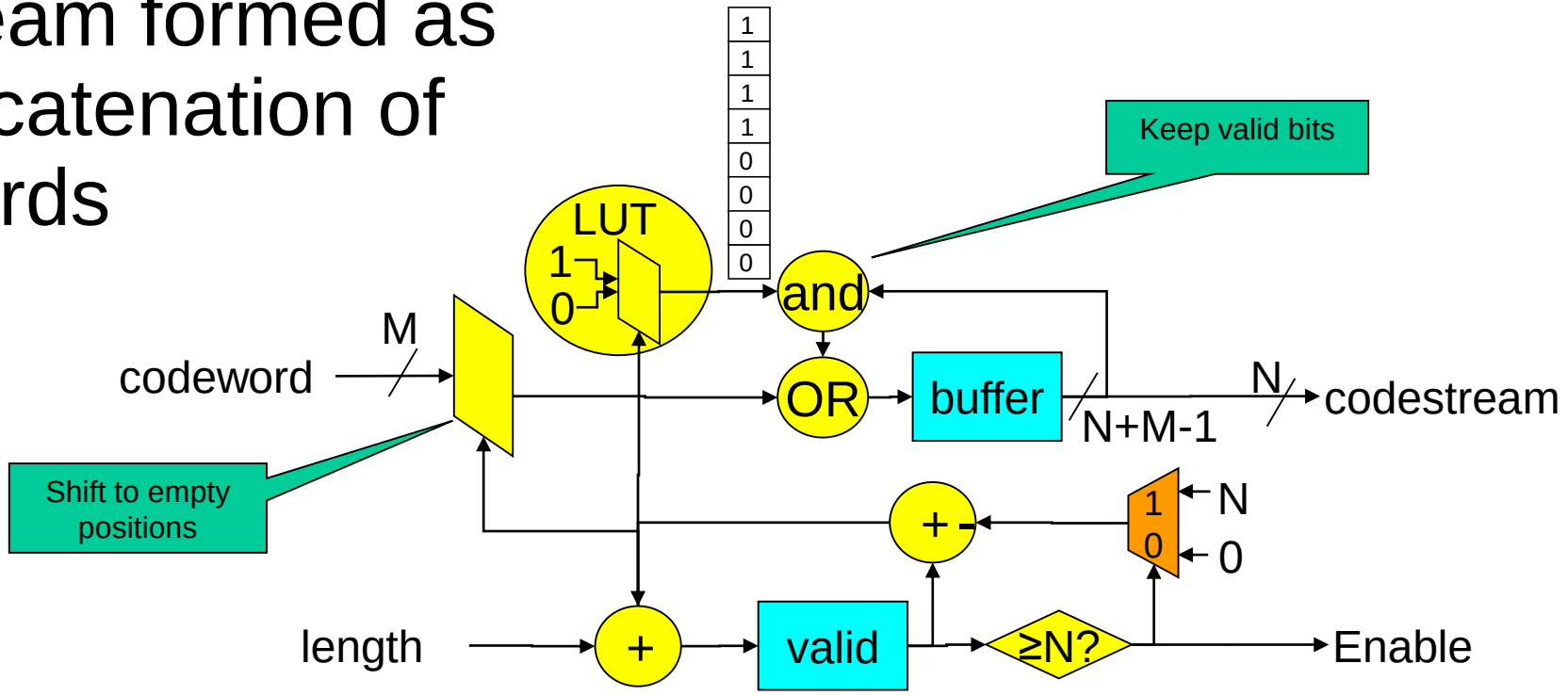
- Matched filter order - the number of taps/coefficients: 450 or 11
- Power consumption

Variable Length Coding(1)

Input value directly mapped to codewords and their lengths

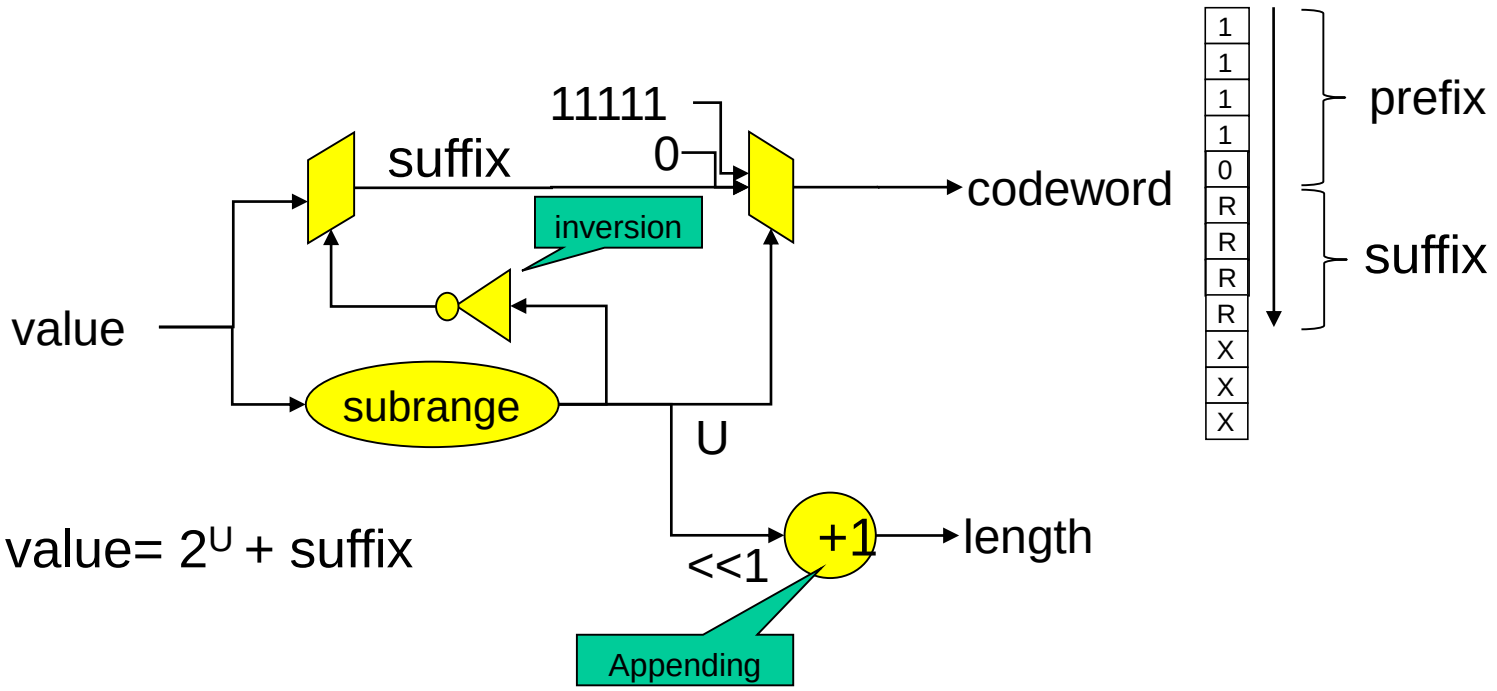


Code-stream formed as the concatenation of codewords



Variable Length Coding(2)

- Some codes are the concatenation of prefix and suffix
- Golomb and Exp-Golomb codes are concatenation of unary and fixed-length codes
- Implementation has a small complexity, suitable for pipelining



Conclusions

- Resources external to FPGA consume power
- Power consumption is proportional to sampling frequencies, filter orders, and channel numbers
- FPGA should be as small as possible (power and price)
- Resource sharing
  - requires higher filter frequencies
  - decrease the amount of resources
  - have small impact on power consumption
  - Is possible for filter taps/coefficients and channels
- Sampling frequency is the tradeoff between the filter order and the accuracy of the parameter extraction
- Variable Length Coding has a small complexity