

Advanced Workshop
on Modern FPGA-
Based Technology for
Scientific Computing



Zynq Architecture

7-Series FPGA Architecture

Cristian Sisterna

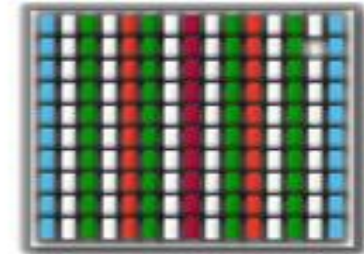
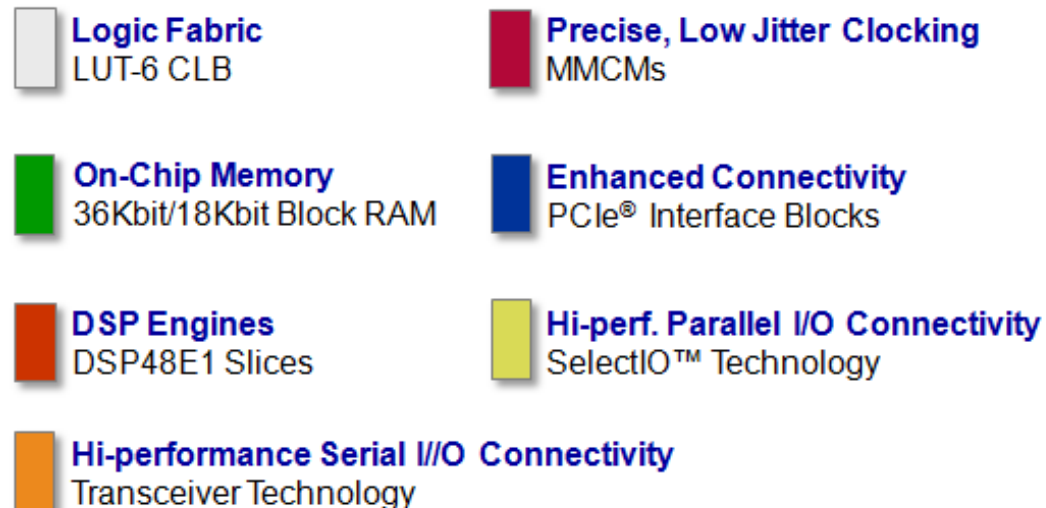
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7-Series FPGA Architecture

7-Series Architecture – Common Elements

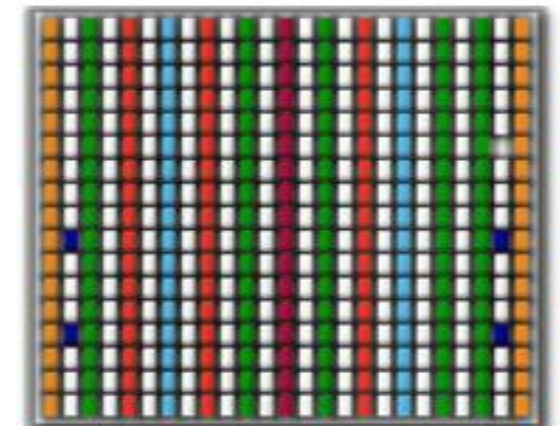
- Common elements enable easy IP reuse for quick design portability across all 7-series families
 - Design scalability from low-cost to high-performance
 - Expanded eco-system support
 - Quickest time to market



Artix-7 FPGA

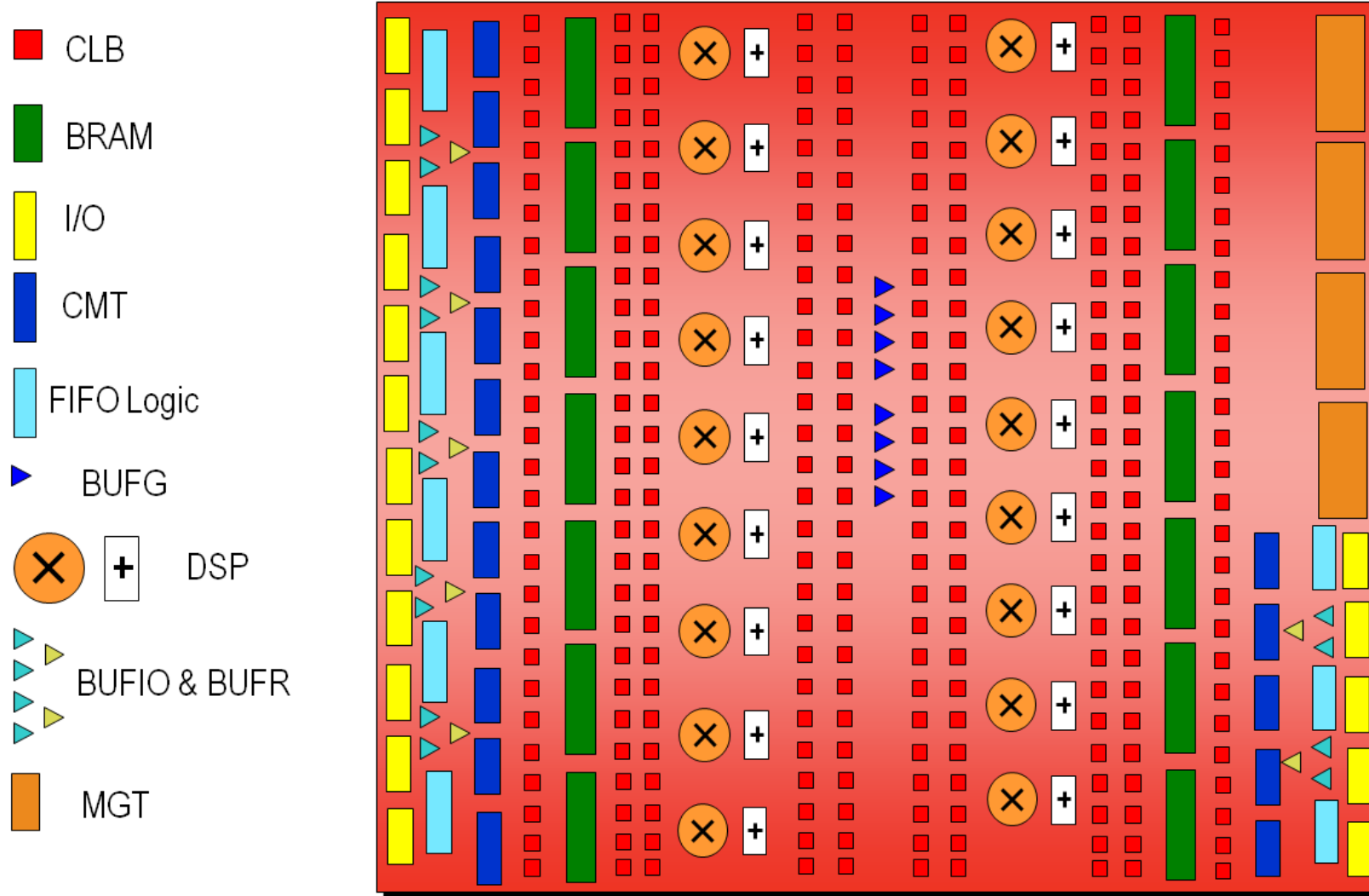


Kintex-7 FPGA



Virtex-7 FPGA

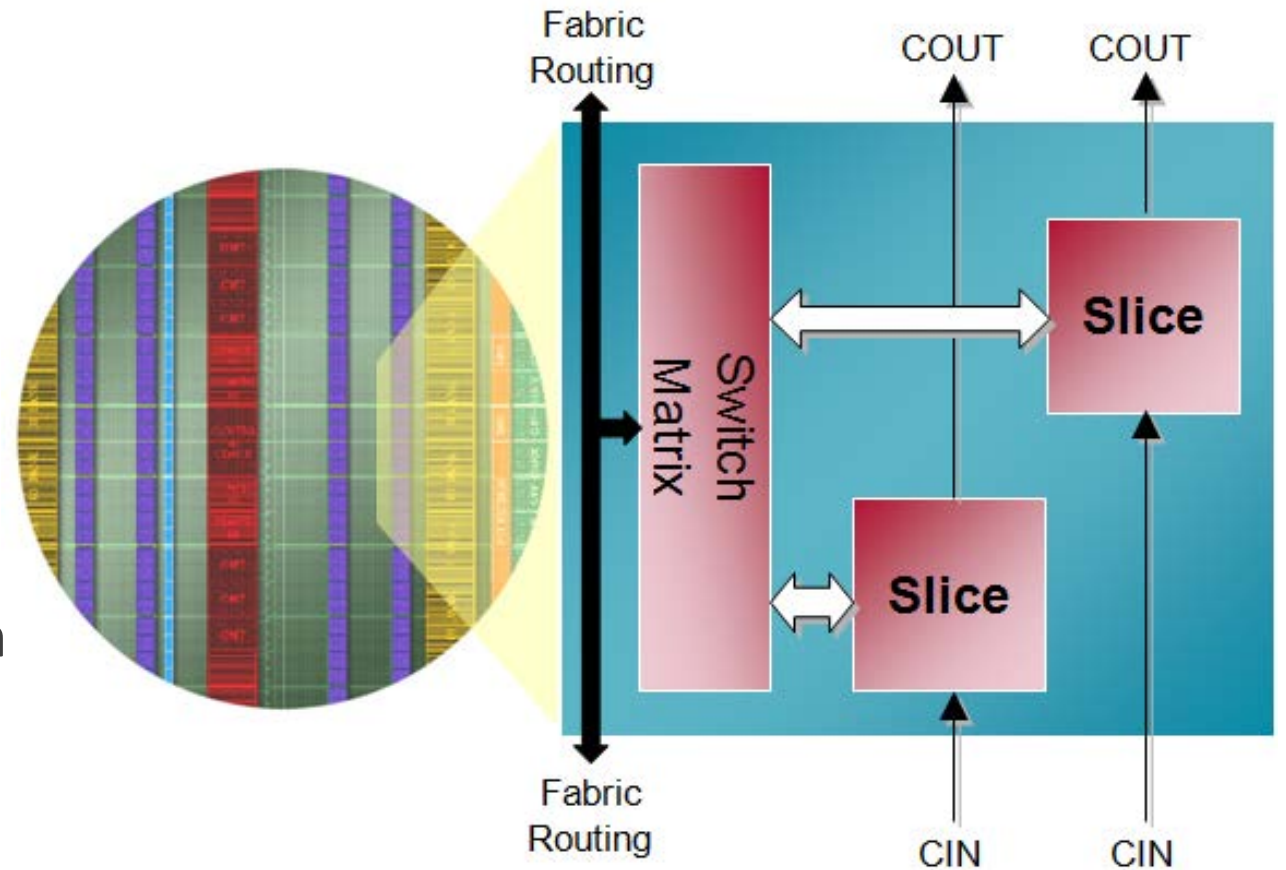
Example of 7-Series Architecture: Artix-7



Logic Resources - CLB

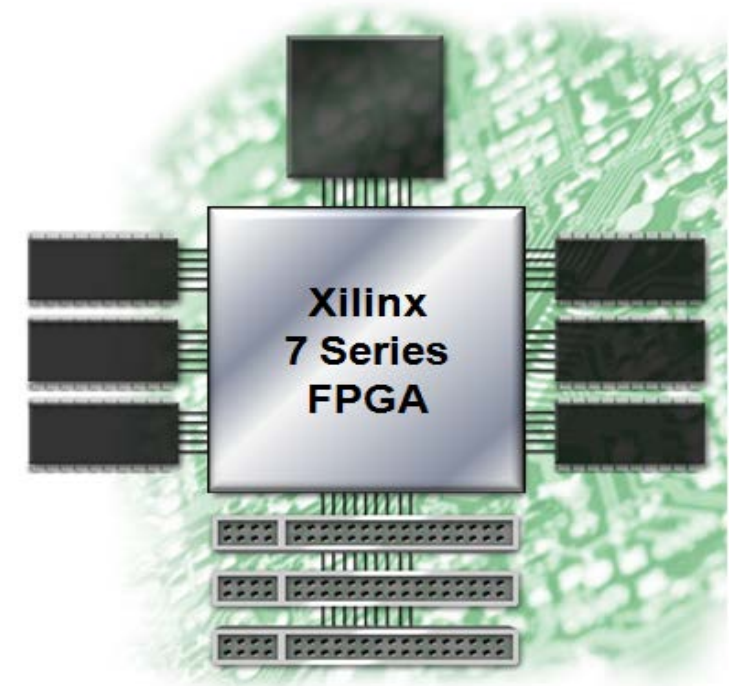
CLB contains two slices

- Primary resource for design
 - Combinatorial functions
 - Flip-flops
- Connected to switch matrix for routing to other FPGA resources
 - Carry chain runs vertically in a column from one slice to the one above



7-Series FPGA Inputs/Outputs

- Wide range of voltages
 - 1.2V to 3.3V operation
- Many different I/O standards
 - Single ended and differential
 - Referenced inputs
 - 3-state support
- Very high performance
 - Up to 1600 Mbps LVDS
 - Up to 1866 Mbps single-ended for DDR3
- Easy interfacing to standard memories
 - Hardware support for QDRII+ and DDR3
- Digitally controlled impedance
- Low power



Input/Output Types

- Two different types of I/O in 7-series FPGAs
 - **High Range (HR)**
 - Supports I/O standards with Vcco voltages up to 3.3V
 - **High Performance (HP)**
 - Supports I/O standards with Vcco voltages up to 1.8V *only*
 - Designed for the highest performance
 - Has ODELAY and DCI capability

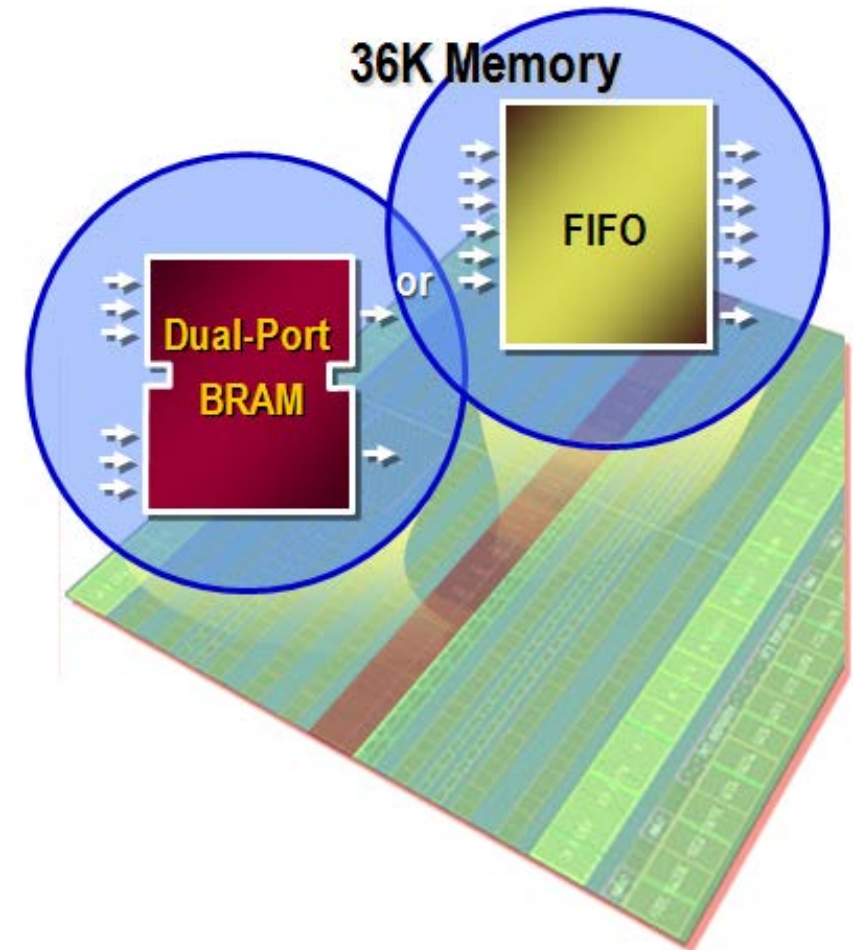
I/O Type	Artix-7 Family	Kintex-7 Family	Virtex-7 Family	Virtex-7 XT/HT/ Family
High Range	All	Most Some		
High Performance		Some	Most	All

Most Common I/Os Standards Available

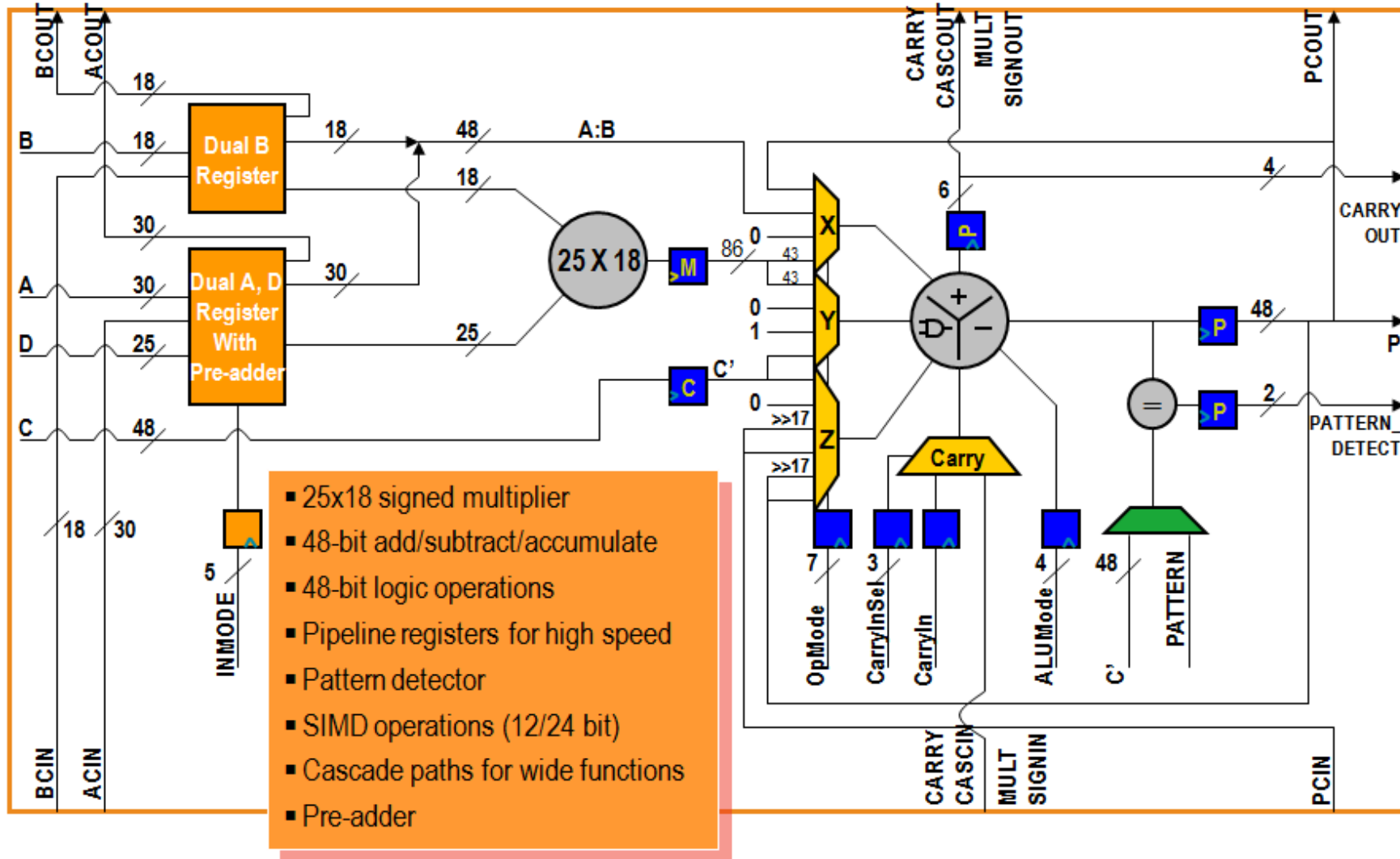
Standard	VCCO	Vref	Application
LVTTTL	3.3	na	Single ended
LVC MOS25, -18, -15	2.5, 1.8, 1.5	na	General Purpose
LVDS33, 25, 18	3.3, 2.5, 1.8	na	Low Voltage Differential
PCI 33/66 MHz, 3.3V	3.3	na	PCI Bus
GTL / GTL+	na	0.80	Back-Plane
HSTL-I, HSTL-III	1.5	0.75	SRAM
SSTL3-I, -II, SSTL2-I	3.3	0.90, 1.5	SDRAM

7-Series Block RAM and FIFO

- All members of the 7-series families have the same Block RAM/FIFO
- Fully synchronous operation
 - All operations are synchronous; all outputs are latched
- Optional internal pipeline register for higher frequency operation
- Two independent ports access common data
 - Individual address, clock, write enable, clock enable
 - Independent data widths for each port
- Multiple configuration options
 - True dual-port, simple dual-port, single-port
- Integrated control for fast and efficient FIFOs



7- Series DSP48E1 Slice



- 25x18 signed multiplier
- 48-bit add/subtract/accumulate
- 48-bit logic operations
- Pipeline registers for high speed
- Pattern detector
- SIMD operations (12/24 bit)
- Cascade paths for wide functions
- Pre-adder

XADC and Analog Mixed Signals (AMS)

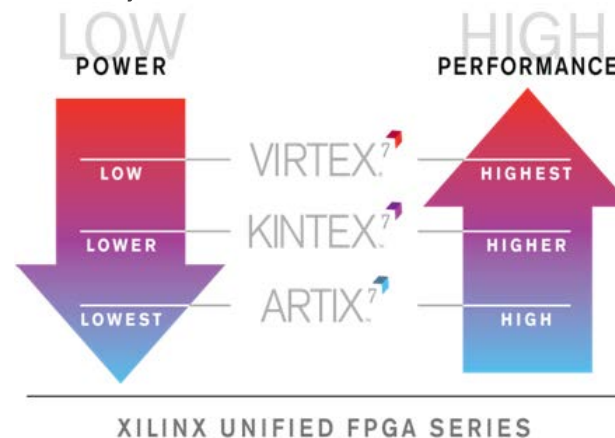
- XADC is a high quality and flexible analog interface new to the 7-series
 - Dual 12-bit 1Msps ADCs, on-chip sensors, 17 flexible analog inputs, and track & holds with programmable signal conditioning
 - 1V input range (unipolar, bipolar and differential)
 - 12-bit resolution conversion
 - Built in digital gain and offset calibration
 - On-chip thermal and Voltage sensors
 - Sample rate of 1 MSPS
- Analog Mixed Signal (AMS)
 - Using the FPGA programmable logic to customize the XADC and replace other external analog functions; for example, linearization, calibration, filtering, and DC balancing to improve data conversion resolution

7-Series FPGA Families

	ARTIX ⁷	KINTEX ⁷	VIRTEX ⁷	ZYNQ ⁷
Maximum Capability	Lowest Power and Cost	Industry's Best Price/Performance	Industry's Highest System Performance	Extensible Processing Platform
Logic Cells	20K – 355K	70K – 480K	285K – 2,000K	30K – 350K
Block RAM	12 Mb	34 Mb	65 Mb	240KB – 2180KB
DSP Slices	40 – 700	240 – 1,920	700 – 3,960	80 – 900
Peak DSP Perf.	504 GMACS	2,450 GMACS	5,053 GMACS	1080 GMACS
Transceivers	4	32	88	16
Transceiver Performance	3.75Gbps	6.6Gbps and 12.5Gbps	12.5Gbps, 13.1Gbps and 28Gbps	6.6Gbps and 12.5Gbps
Memory Performance	1066Mbps	1866Mbps	1866Mbps	1333Mbps
I/O Pins	450	500	1,200	372
I/O Voltages	3.3V and below	3.3V and below 1.8V and below	3.3V and below 1.8V and below	3.3V and below 1.8V and below

7-Series Cost, Power and Performance

- The different families in the 7-series provide solutions to address the different price/performance/power requirements of the FPGA market
 - **Artix™-7** family: Lowest price and power for high volume and consumer applications
 - Battery powered devices, automotive, commercial digital cameras
 - **Kintex™-7** family: Best price/performance
 - Wireless and wired communication, medical, broadcast
 - **Virtex-7** family: Highest performance and capacity
 - High-end wired communication, test and measurement, advanced RADAR, high-performance computing

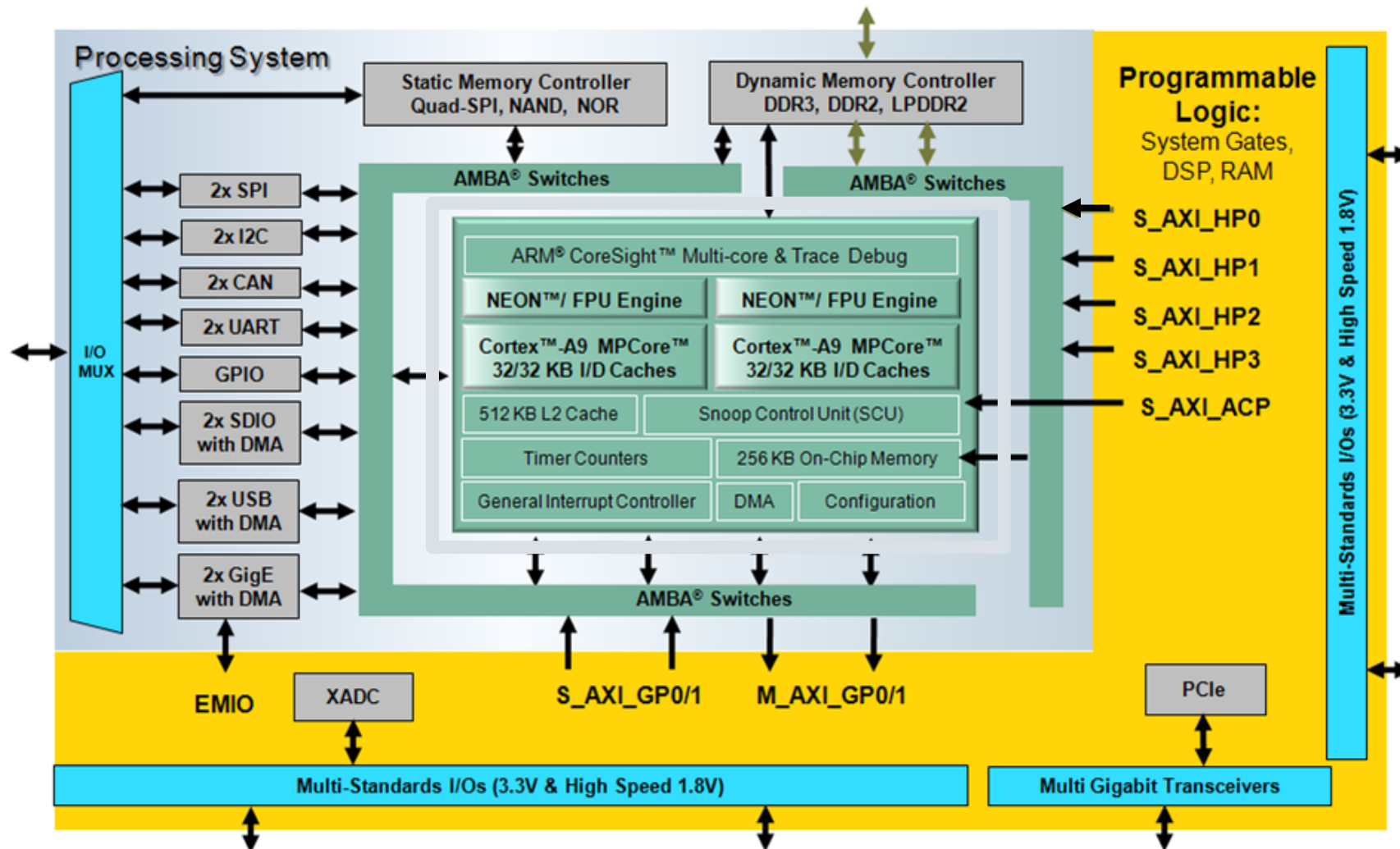


Zynq Architecture

Zynq-7000 Main Features

- **Complete ARM[®]-based processing system**
 - Application Processor Unit (APU)
 - Dual ARM Cortex[™]-A9 processors
 - Caches and support blocks
 - Fully integrated memory controllers
 - I/O peripherals
- **Tightly integrated programmable logic**
 - Used to extend the processing system
 - Scalable density and performance
- **Flexible array of I/O**
 - Wide range of external multi-standard I/O
 - High-performance integrated serial transceivers
 - Analog-to-digital converter inputs

Zynq SoC Block Diagram



PS Main Components

- **Application processing unit (APU)**
- **I/O peripherals (IOP)**
 - Multiplexed I/O (MIO), extended multiplexed I/O (EMIO)
- **Memory interfaces**
- **PS interconnect**
- **DMA**
- **Timers**
 - Public and private
- **General interrupt controller (GIC)**
- **On-chip memory (OCM): RAM**
- **Debug controller: CoreSight**

PL Main Components

- Configurable logic blocks (CLB)
 - 6-input look-up tables (LUTs)
 - Memory capability within the LUT
 - Register and shift register functionality
- 36 Kb BRAM
- DSP48E1 Slice
- Clock management
- Configurable I/Os
- High Speed Serial Transceivers
- Integrated interface for PCI Express

Zynq	FPGA Based Fabric
7z010, 7z015, 7z020	Artix
7z030, 7z035, 7z045, 7z100	Kintex

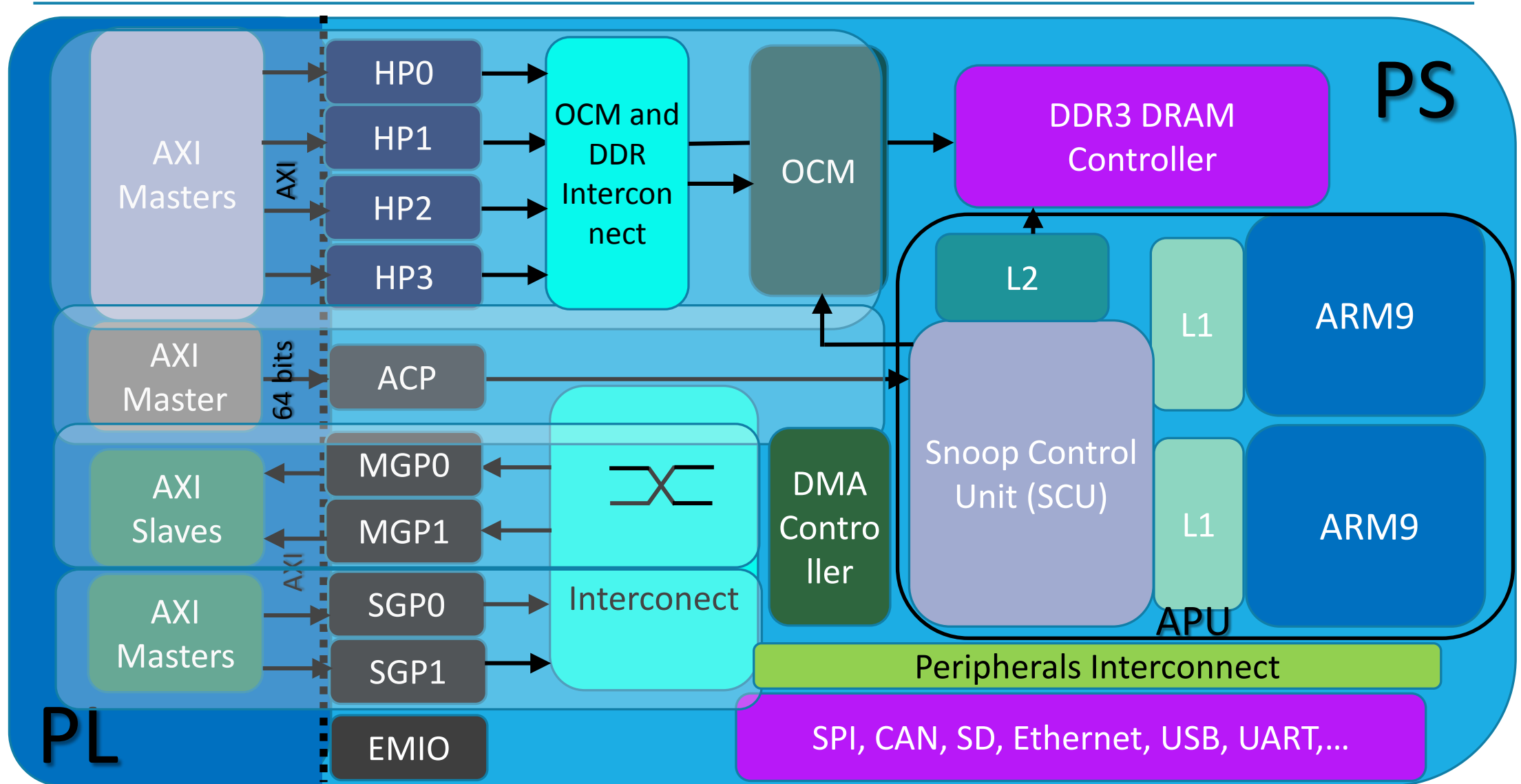
PS-PL Interface

- **AXI high-performance slave ports (HP0-HP3)**
 - Configurable 32-bit or 64-bit data width
 - Access to OCM and DDR only
 - Conversion to processing system clock domain
 - AXI FIFO Interface (AFI) are FIFOs (1KB) to smooth large data transfers
- **AXI general-purpose ports (GP0-GP1)**
 - Two masters from PS to PL
 - Two slaves from PL to PS
 - 32-bit data width
 - Conversion and sync to processing system clock domain

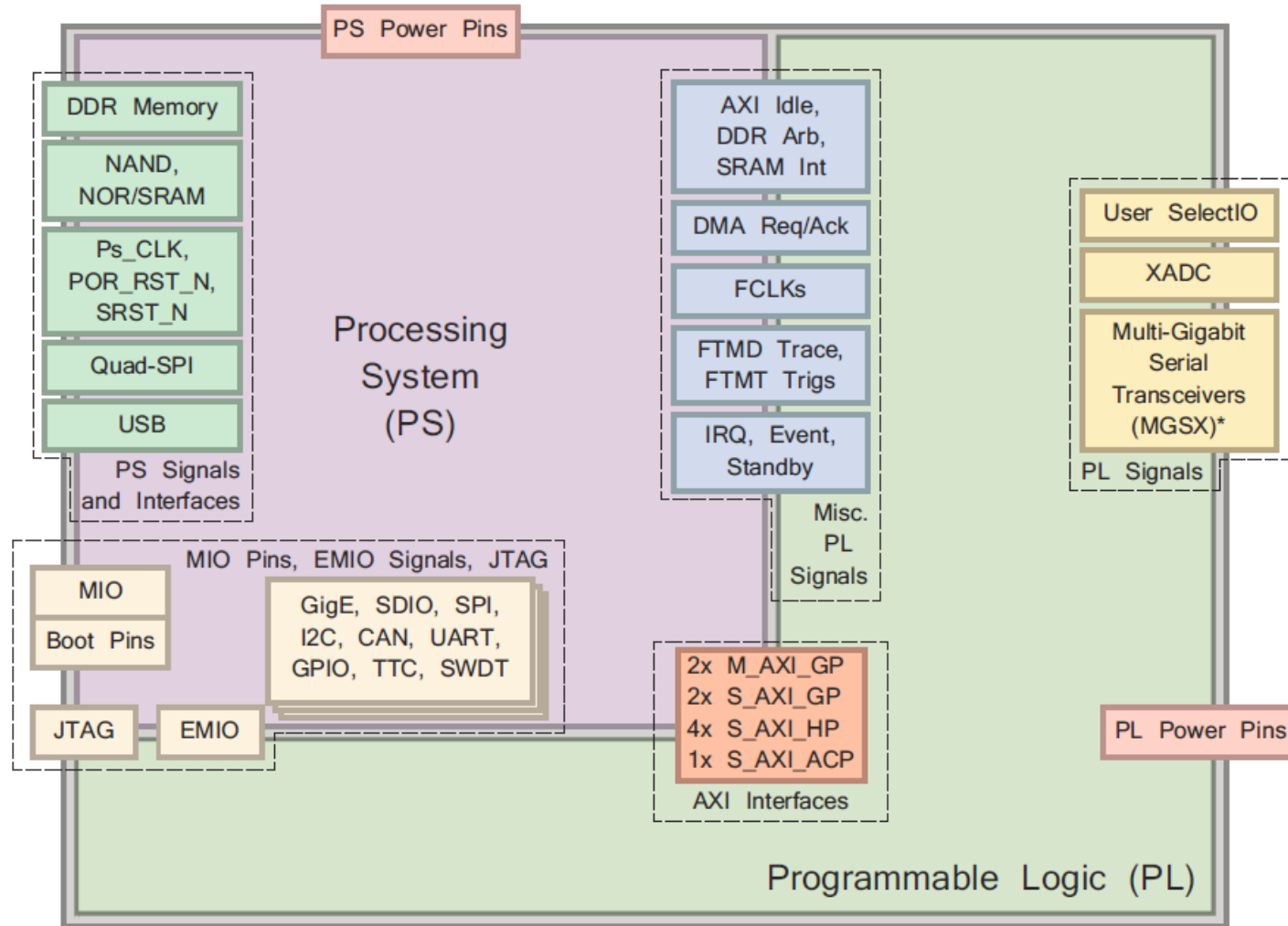
PS-PL Interface

- **One 64-bit accelerator coherence port (ACP) AXI slave interface to CPU memory**
- **DMA, interrupts, events signals**
 - Processor event bus for signaling event information to the CPU
 - PL peripheral IP interrupts to the PS general interrupt controller (GIC)
 - Four DMA channel RDY/ACK signals
- **Extended multiplexed I/O (EMIO) allows PS peripheral ports access to PL logic and device I/O pins**
- **Clock and resets**
 - Four PS clock outputs to the PL with enable control
 - Four PS reset outputs to the PL
- **Configuration and miscellaneous**

Zynq Architecture



PS-PL Interface



*Zynq 7z030, 7x045 & 7z100 only

PS-PL AXI Interfaces

Interface Name	Interface Description	Master	Slave
M_AXI_GP0	General Purpose (AXI_GP)	PS	PL
M_AXI_GP1		PS	PL

PS-PL Interface Performance

Method	Benefits	Drawbacks	Usage	Performance
PL AXI-HP DMA	<ul style="list-style-type: none"> • Highest throughput • Multiple interfaces • Command/Data FIFO 	<ul style="list-style-type: none"> • OC/DDR access only • Complex PL Master design 	<ul style="list-style-type: none"> • HP DMA for large datasets 	1.200 MB/s (per interface)
PL AXI-ACP DMA	<ul style="list-style-type: none"> • - Highest throughput - Lowest latency - Optional cache coherency 	<ul style="list-style-type: none"> • Large burst might cause cache trashing • Shares CPU interconnect bandwidth • Complex PL Master design 	<ul style="list-style-type: none"> • HP DMA for smaller coherent datasets • Medium granularity CPU offload 	1.200 MB/s
PL AXI-GP DMA	<ul style="list-style-type: none"> • Medium throughput 	<ul style="list-style-type: none"> • More complex PL Master design 	<ul style="list-style-type: none"> • PL to PS control functions • PS I/O Peripheral access 	600 MB/s
CPU Programmed I/O	<ul style="list-style-type: none"> • Simple Sw • Least PL resources • Simple PL Slave 	<ul style="list-style-type: none"> • Lowest throughput 	<ul style="list-style-type: none"> • Control functions 	< 25 MB/s

PS-PL Miscellaneous Signals

- PL Clocks and Resets
- PL Interrupts to PS
- IOP Interrupts to/from the PL
- Events
- Idle AXI, DDR, ARB, SRAM Interrupt
- DMA Controller
- EMIO Signals

PS Peripherals and Connections

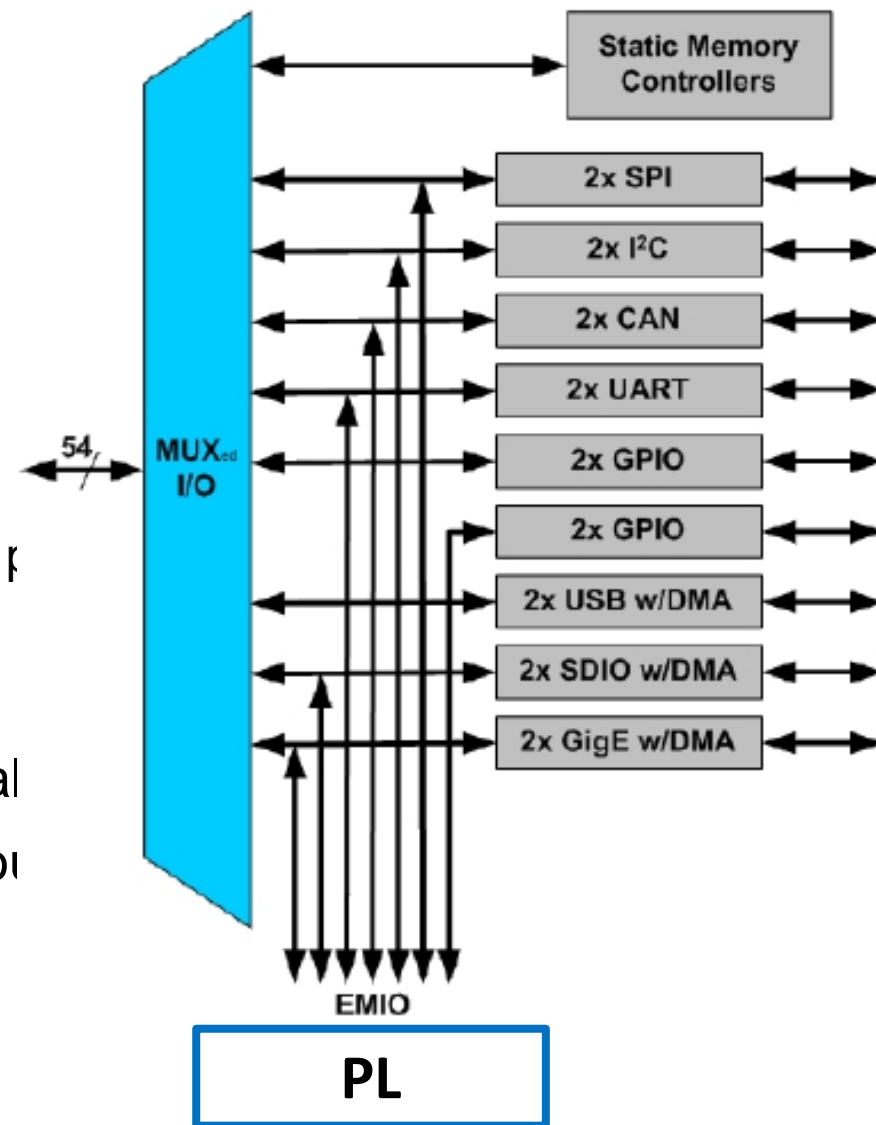
Multiplexed I/O – Internal / External

❖ Multiplexed input/output (MIO)

- ❖ Multiplexed output of peripheral and static memories
- ❖ Two I/O banks; each selectable: 1.8V, 2.5V, or 3.3V
- ❖ Configured using configuration
- ❖ Dedicated pins are used
 - ❖ User constraints (LOC) should not be present
 - The BitGen process will throw errors if LOC constraints are present

❖ Extended MIO

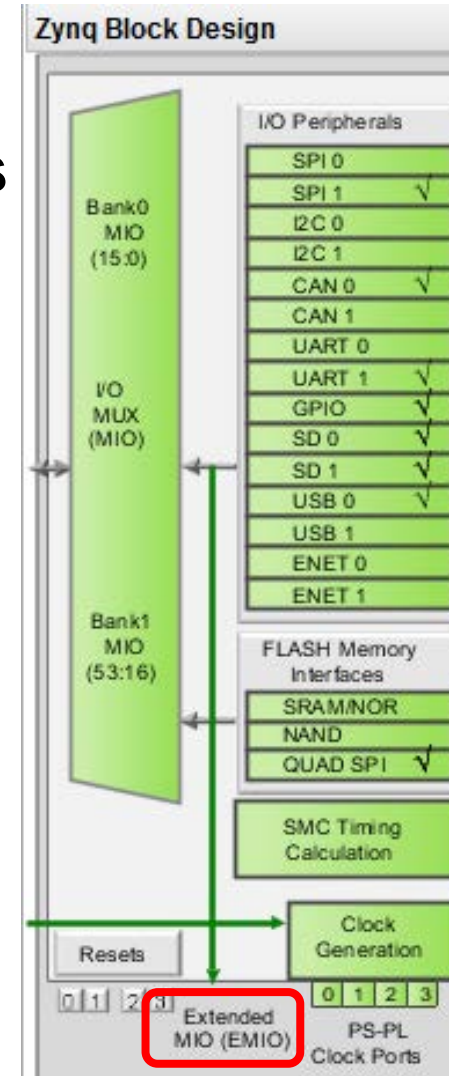
- ❖ Enables use of the SelectIO™ interface with PS peripheral
- ❖ User constraints must be present for the signals brought out to the SelectIO pins
 - ❖ The BitGen process will throw errors if LOC constraints are not present



Extended Multiplexed I/O (EMIO)

Extended interface to PL I/O peripheral ports

- ❖ EMIO: Peripheral port to PL
- ❖ Alternative to using MIO
- ❖ Mandatory for some peripheral ports
- ❖ Facilitates
 - ❖ Connection to peripheral in programmable logic
 - ❖ Use of general I/O pins to supplement MIO pin usage
 - ❖ Allows additional signals for many of the peripherals
 - ❖ Alleviates competition for MIO pin usage



Multiplexed I/O (MIO)

The screenshot shows the 'Peripheral I/O Pins' configuration window for a ZYNQ7 Processing System (5.3). The interface is divided into a left-hand menu and a main grid area. The left-hand menu includes sections for 'Zynq Block Design', 'PS-PL Configuration', 'Peripheral I/O Pins' (highlighted), 'MIO Configuration', 'Clock Configuration', 'DDR Configuration', 'SMC Timing Calculation', and 'Interrupts'. The 'Peripheral I/O Pins' section lists various peripherals with checkboxes for their configuration. The main grid area shows the mapping of these peripherals to specific pins across two banks: Bank 0 (LVC MOS 3.3V) and Bank 1 (LVC MOS 1.8V). The grid is organized into rows and columns, with each cell representing a pin and its assigned peripheral. The peripherals shown include Quad SPI Flash, SRAM/NOR Flash, NAND Flash, Ethernet 0, Ethernet 1, USB 0, USB 1, SD 0, SD 1, SP 0, SP 1, UART 0, UART 1, I2C 0, I2C 1, CAN 0, CAN 1, TTC 0, TTC 1, SWD, PJTAG, Trace, and GPIO MIO. The GPIO MIO and GPIO EMIO options are also visible in the left-hand menu.

MIO Port Configuration

ZYNQ7 Processing System (5.5)

Documentation Presets IP Location Import XPS Settings

Page Navigator << Zynq Block Design PS-PL Configuration Peripheral I/O Pins **MIO Configuration** Clock Configuration DDR Configuration SMC Timing Calculation Interrupts

MIO Configuration [Summary Report](#)

Bank 0 I/O Voltage: LVCMOS 3.3V Bank 1 I/O Voltage: LVCMOS 1.8V

Search: Q

Peripheral	IO	Signal	IO Type	Speed	Pullup	Dir...	Polarity
Memory Interfaces							
I/O Peripherals							
<input checked="" type="checkbox"/> ENET 0	EMIO						
<input type="checkbox"/> ENET 1							
<input type="checkbox"/> USB 0							
<input type="checkbox"/> USB 1							
<input checked="" type="checkbox"/> SD 0							
<input checked="" type="checkbox"/> SD 1	MIO 22 .. 27						
<input type="checkbox"/> UART 0							
<input checked="" type="checkbox"/> UART 1	MIO 48 .. 49						
<input type="checkbox"/> Modem signals							
<input type="checkbox"/> UART 1	MIO 48	tx	LVCMOS 1.8V	slow	disabled	out	
<input type="checkbox"/> UART 1	MIO 49	rx	LVCMOS 1.8V	slow	disabled	in	
<input type="checkbox"/> I2C 0							
<input type="checkbox"/> I2C 1							
<input checked="" type="checkbox"/> SPI 0							
<input checked="" type="checkbox"/> SPI 1	EMIO						

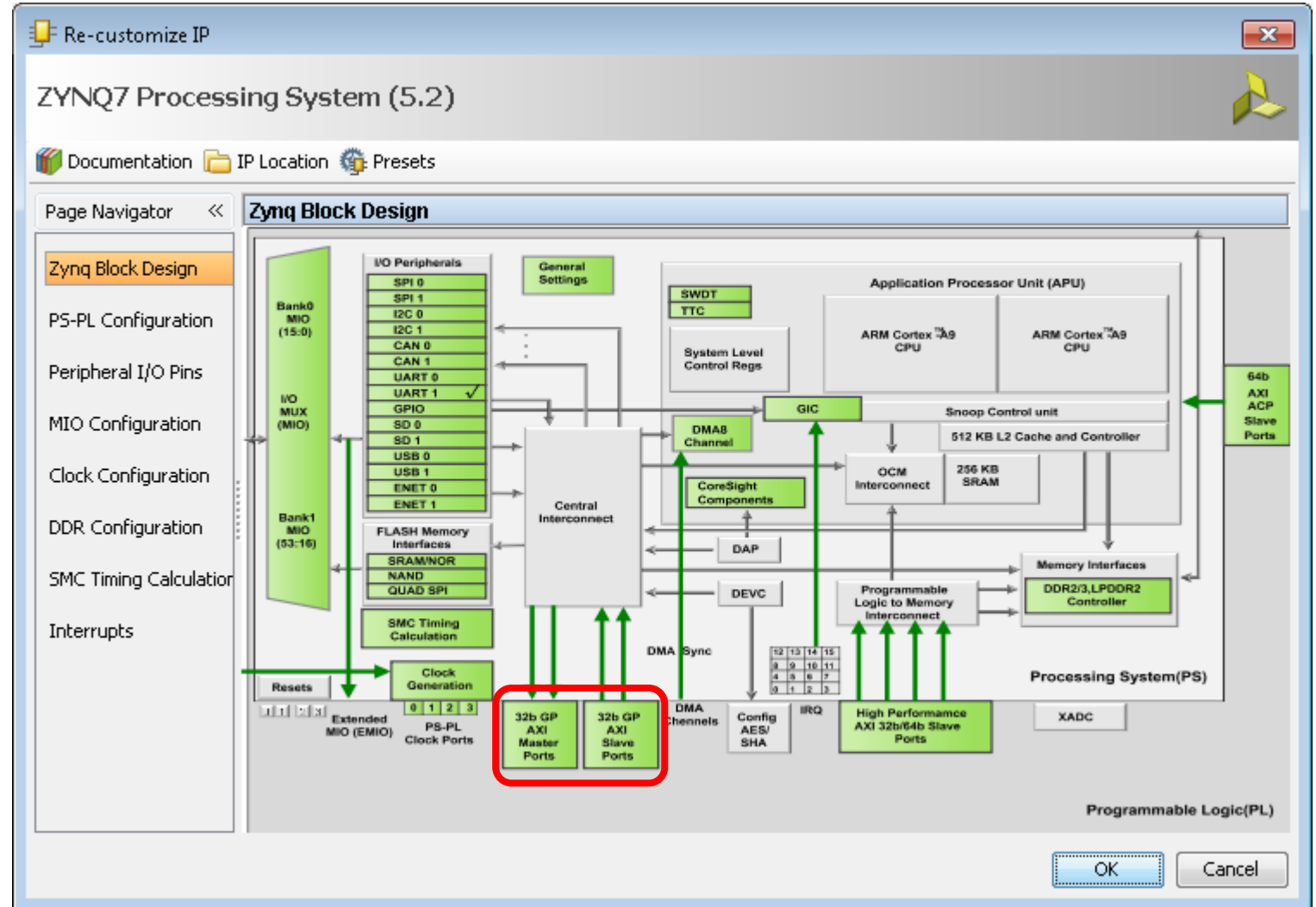
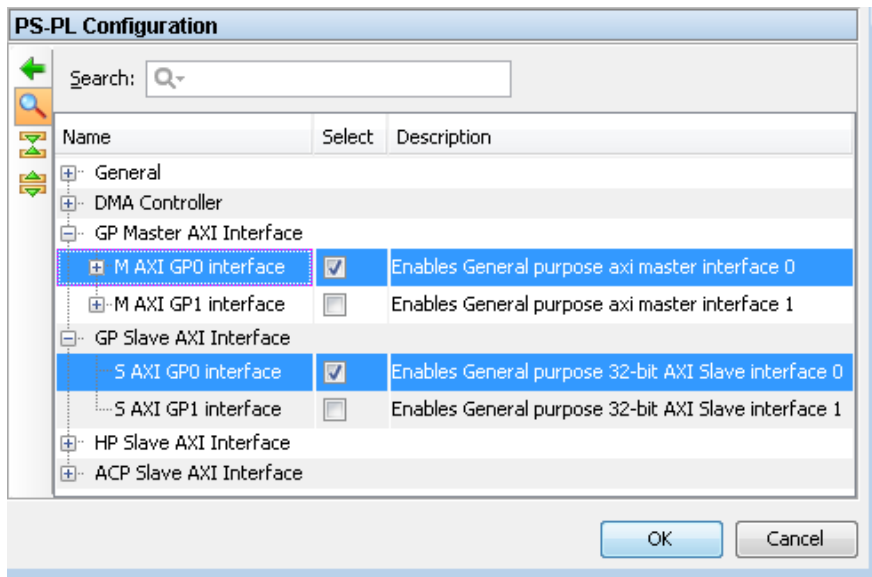
OK Cancel

PS Available Peripherals

PS Peripheral	Description
SPI (x2)	Serial Peripheral Interface, either master or slave mode.
I2C (x2)	I ² C bus. Supports master and slave modes.
CAN (x2)	Controller Area Network. CAN 2.0A and CAN 2.0B.
UART (x2)	Universal Asynchronous Receiver Transmitter. One UART is used for terminal connections to a host PC.
GPIO	General purpose Input/Output. There are four GPIO banks, each of 32 bits.
SD (x2)	SD card memory controller
USB (x2)	Universal Serial Bus. Host or OTG (in-the-go) modes.
GigE (x2)	Gigabit Ethernet MAC peripheral, supports 10Mbps, 100MBps and 1Gbps.

GP0/1 Ports Configuration for PS-PL Interface

- Click on the menu or green GP Blocks to configure

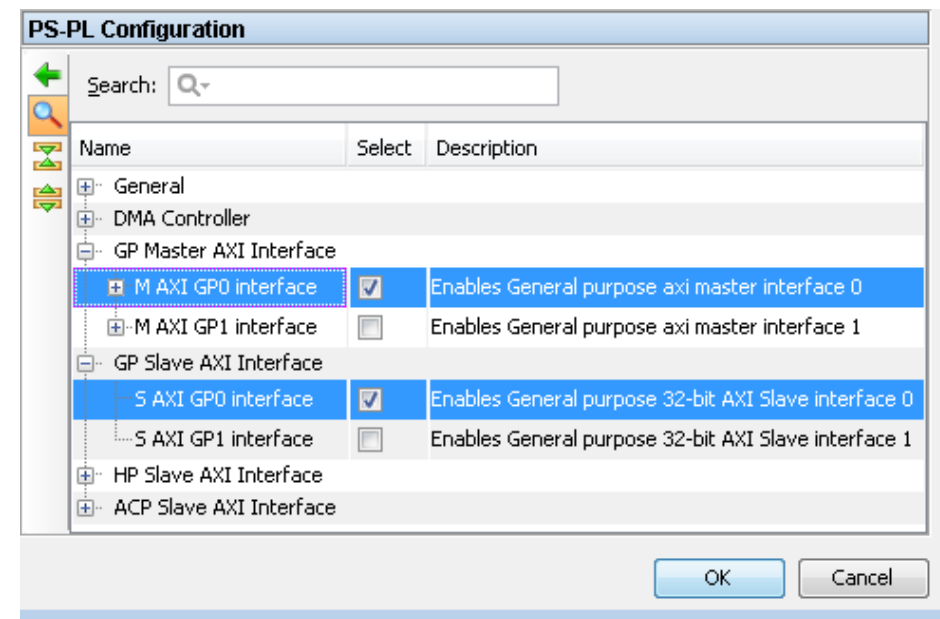


GP 0/1 Ports

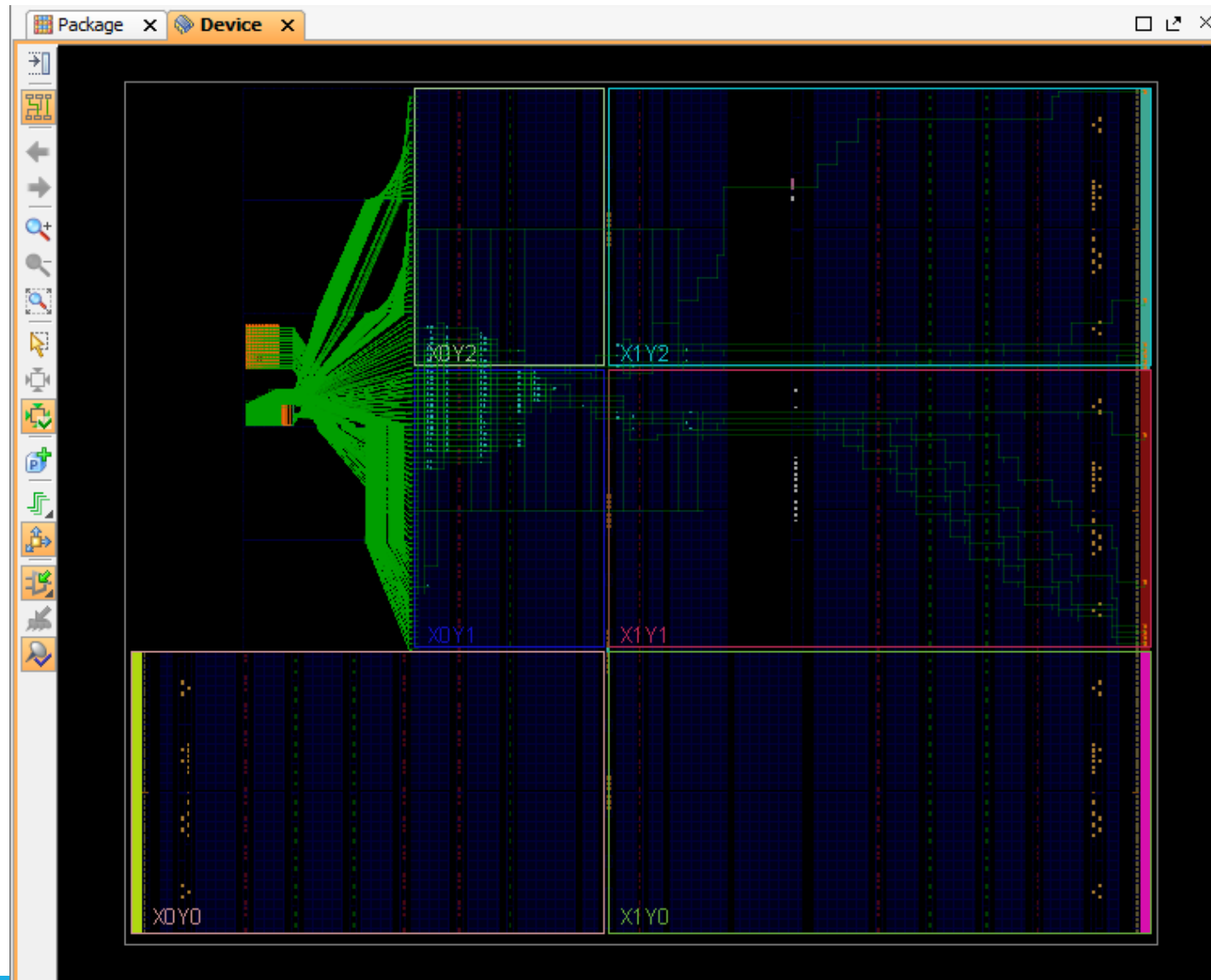
- By default, GP Slave and Master ports are disabled



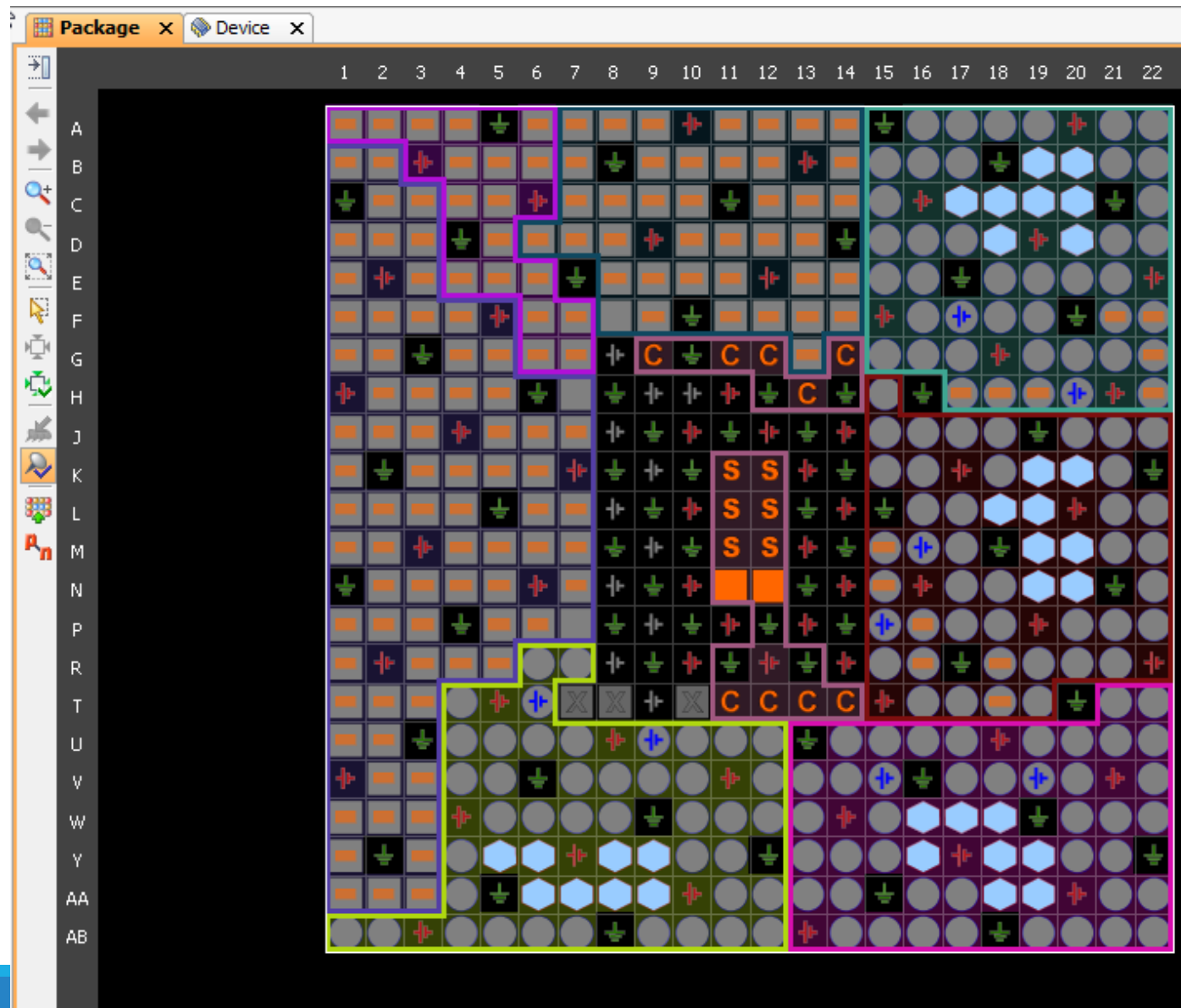
- Enable GP Master and/or Slave ports depending on whether a slave or a master peripheral is going to be added in PL
- axi_interconnect block is required to connect IP to a port with different protocols
 - Automatically convert Protocols
 - Can be automatically added when using Block Automation in Vivado IP



Zynq – Internal Device View



Zynq – Package View



Apendix

PS I/O Peripherals

I2C

- I²C bus specification version 2
- Programmable to use normal (7-bit) or extended (10-bit) addressing
- Programmable rates: fast mode (400 kbit/s) , standard (100 kbits/s), and low (10 kbits/s)
 - Rates higher than 400 kbits/sec are not supported
- Programmable as either a master or slave interface
- Capable of clock synchronization and bus arbitration
- Fully programmable slave response address
- Reversible FIFO operation supported
- 16-byte buffer size
- Slave monitor mode when set up as master
- I²C bus hold for slow host service
- Slave timeout detection with programmable period
- Transfer status interrupts and flags

CAN

- Up to 24-MHz CAN_REF clock as system clock
- 64 message-deep receiver and transmitter buffer
- Full CAN 2.0B compliant; conforms to ISO 11898-1
- Maximum baud rate of 1 Mb/s
- Four message filters required for buffer mode
- Listen-only mode for test and debug
- External PHY I/O
- “Wake-on-message”
- Time-stamping for receive messages
- TX and RX FIFO watermarking
- Exception: no power-down mode

SD-SDIO

- Support for version 2.0 of SD Specification
- Full-speed (4 MB/s) and low-speed (2 MB/s) support
 - Low-speed clock (400 KHz) used until bandwidth negotiated
- 1-bit and 4-bit data interface support
- Host mode support only
- Built-in DMA controller
- Full-speed clock (0-50 MHz) with maximum throughput at 25 MB/s
- 1 KB data FIFO interface
- Support for MMC 3.31 card at 52 MHz
- Support for memory, I/O, and combo cards
- Support for power control modes and interrupts

SPI

- Master or slave SPI mode
- Four wire bus: MOSI, MISO, SCK, nSS
- Supports up to three slave select lines
- Supports multi-master environment
- Identifies an error condition if more than one master detected
- Software can poll for status or function as interrupt-driven device
- Programmable interrupt generation
- 50-MHz maximum external SPI clock rate
- Selectable master clock reference
- Integrated 128-byte deep read and write FIFOs
- Full-duplex operation offers simultaneous receive and transmit

UART

- Two UARTs
- Programmable baud rate generator
- 64-byte receive and transmit FIFOs
- 6, 7, or 8 data bits and 1, 1.5, or 2 stop bits
- Odd, even, space, mark, or no parity with parity, framing, and overrun error detection
- "Line break" generation and detection
- Normal, automatic echo, local loopback, and remote loopback channel modes
- Interrupts generation
- Support 8 Mb/s maximum baud rate with additional reference clock or up to 1.5 Mb/s with a 100-MHz peripheral bus clock
- Modem control signals: CTS, RTS, DSR, DTR, RI, and DCD (through EMIO)
- Simple UART: only two pins (TX and RX through MIO)

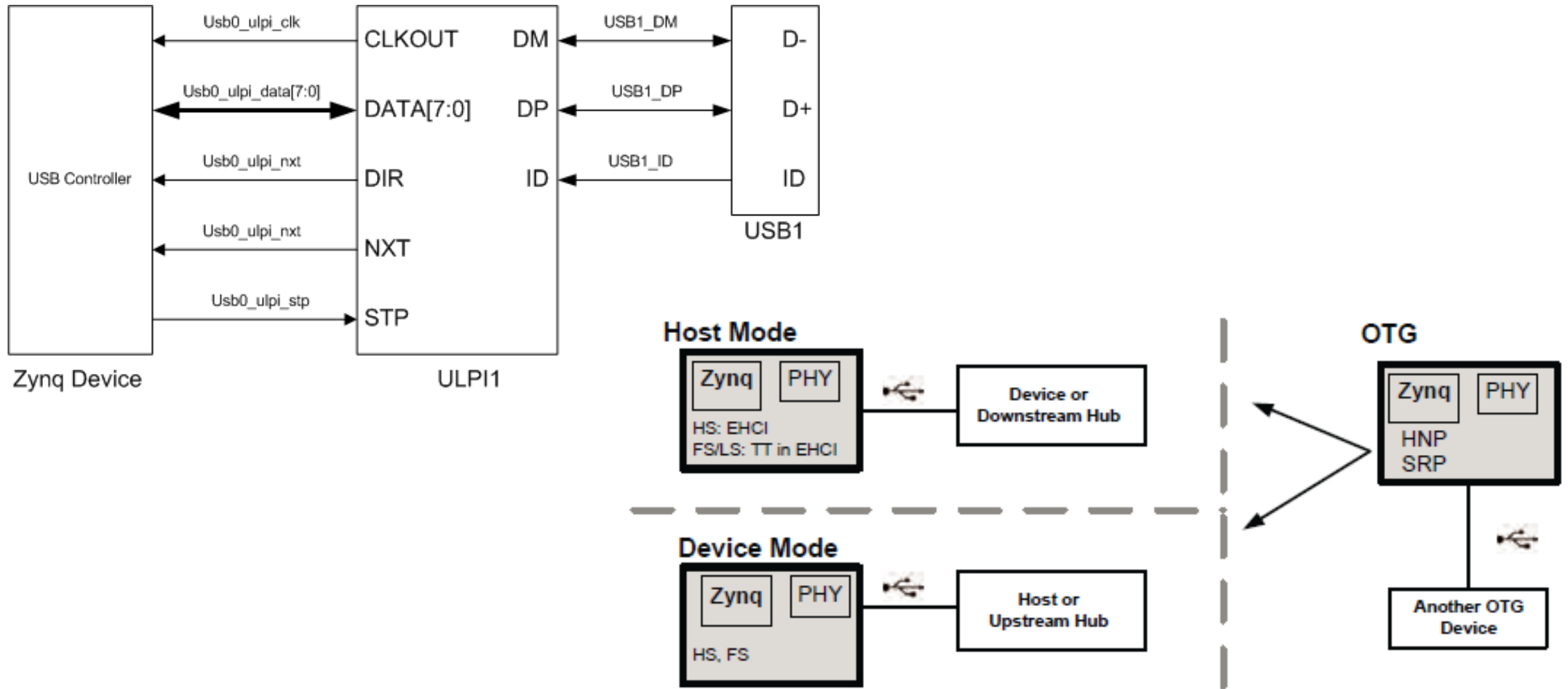
USB

- Two USB 2.0 hardened IP peripherals per Zynq device
 - Each independently controlled and configured
- Supported interfaces
 - High-speed USB 2.0: 480 Mbit/s
 - Full-speed USB 1.1: 12 Mbit/s
 - Low-speed USB 1.0: 1.5 Mbit/s
 - Communication starts at USB 2.0 speed and drops until sync is achieved
- Each block can be configured as host, device, or on-the-go (OTG)
- 8-bit ULPI interface
- All four transfer types supported: isochronous, interrupt, bulk, and control
- Supports up to 12 endpoints per USB block in the Zynq device
 - Running in host mode
- Source-code drivers

USB 2.0 OTG

- Control and configuration registers for each USB block
- Software-ready with standalone and OS linux source-code delivered drivers
- EHCI compliant host registers
- USB host controller registers and data structures compliant to Intel EHCI specifications
- Internal DMA
- Must use the MIO pins

USB 2.0 Usage Example

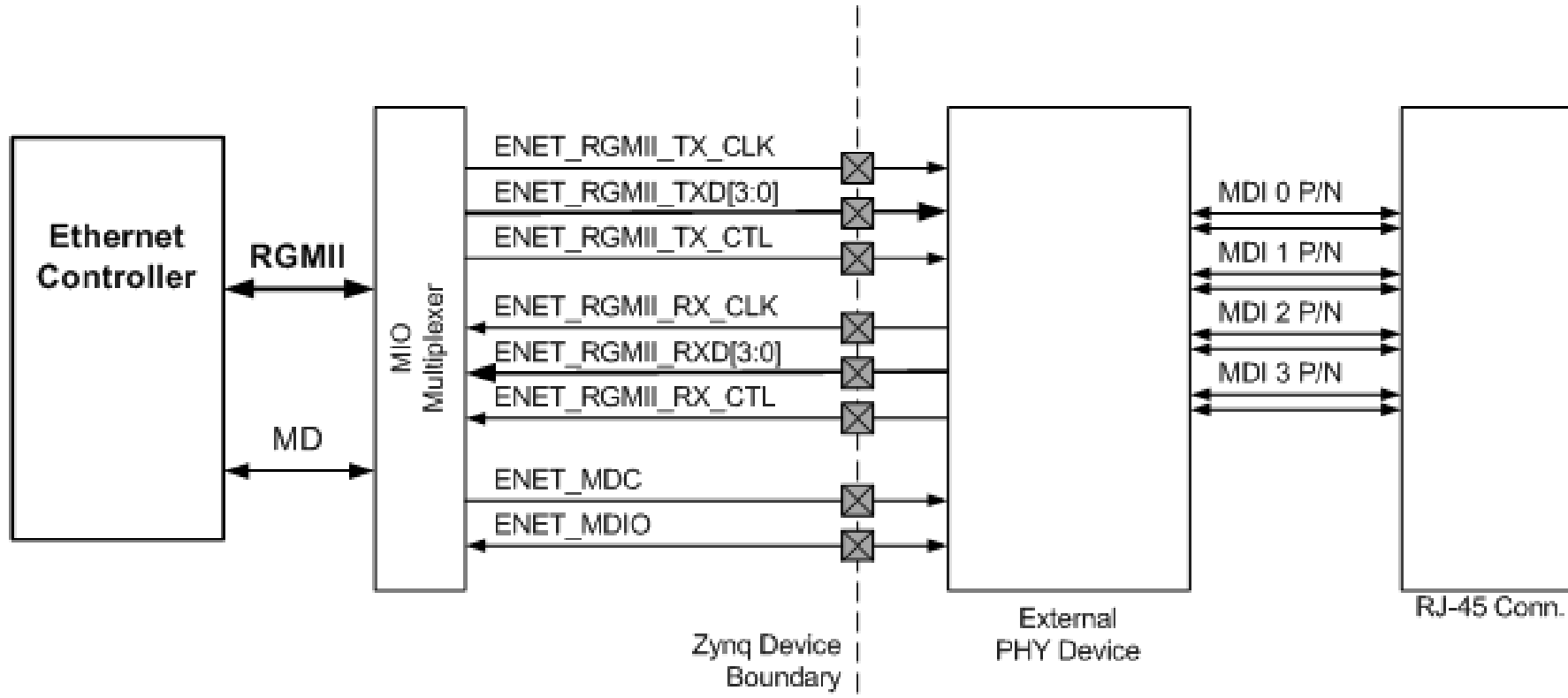


UG585_c15_30_030712

Gigabit Ethernet Controller

- Tri-mode Ethernet MAC (10/100/1G) with native GMII interface
- IEEE1588 rev 2.0
 - Time stamp support
 - 1 us resolution
- IEEE802.3
- RGMII v2.0 (HSTL) interface to MIO pins
 - Need MIO set at 1.8V to support RGMII speed
 - Need to use large bank of MIO pins for two Ethernets
- MII/GMII/SGMII/RGMII ver1.3 (LVCMOS) and ver2.0 (HSTL) interface available through EMIO (programmable logic I/O)
- TX/RX checksum offload for TCP and UDP
- Internal DMA and wake on LAN

Gigabit Ethernet Controller

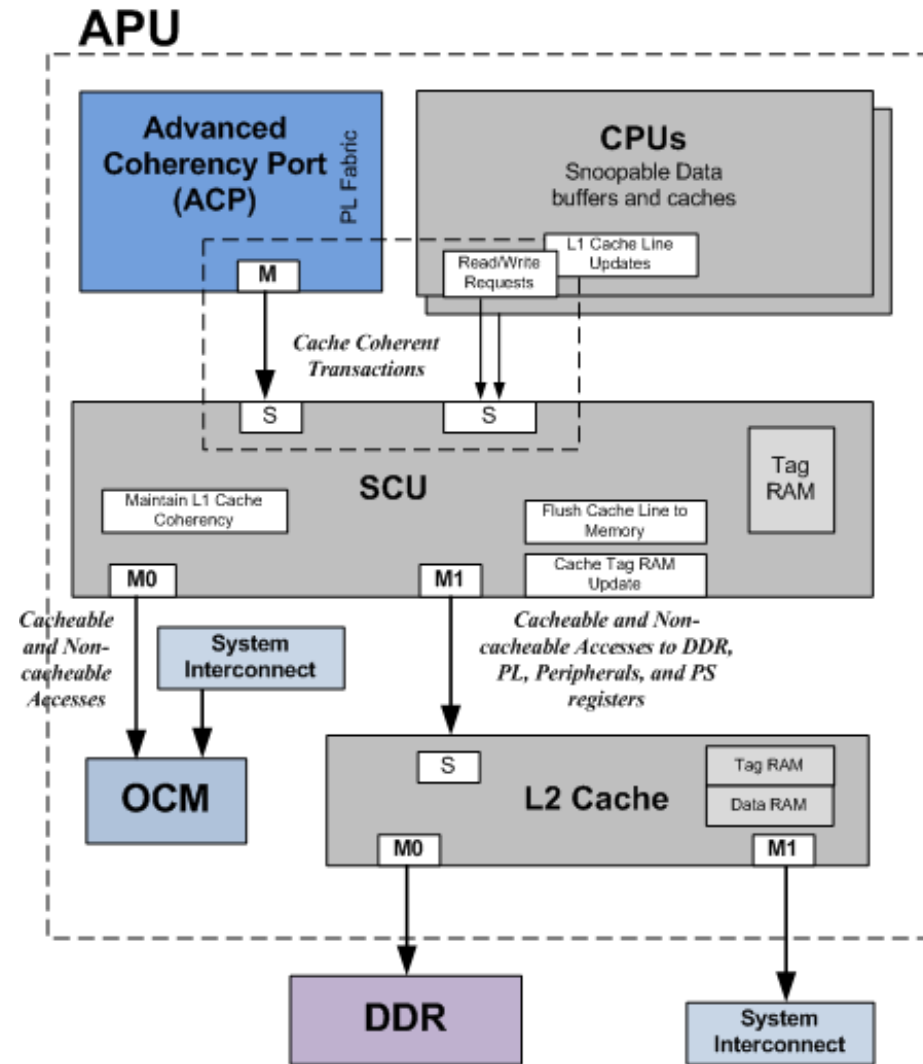


Application Processor Unit (APU)

ARM Processor Architecture

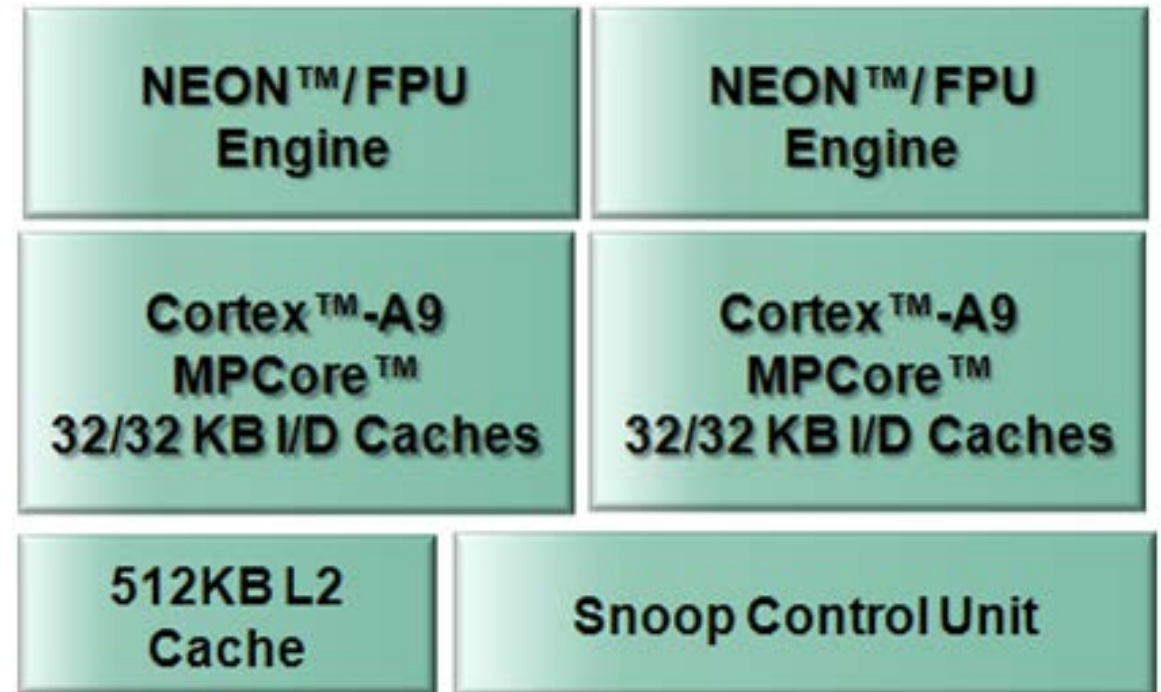
- **ARM Cortex-A9 processor implements the ARMv7-A architecture**
 - ARMv7 is the ARM Instruction Set Architecture (ISA)
 - Thumb instructions: 16 bits; Thumb-2 instructions: 32 bits
 - NEON: ARM's Single Instruction Multiple Data (SIMD) instructions
 - ARMv7-A: Application set that includes support for a Memory Management Unit (MMU)
 - ARMv7-R: Real-time set that includes support for a Memory Protection Unit (MPU)
 - ARMv7-M: Microcontroller set that is the smallest set
- **ARM Advanced Microcontroller Bus Architecture (AMBA[®]) protocol**
 - AXI3: Third-generation ARM interface
 - AXI4: Adding to the existing AXI definition (extended bursts, subsets)
- **Cortex is the new family of processors**
 - ARM family is older generation; Cortex is current; MMUs in Cortex processors and MPUs in ARM

APU



APU Components

- Dual ARM[®] Cortex[™]-A9 MPCore with NEON extensions
 - Up to 800-MHz operation
 - 2.5 DMIPS/MHz per core
 - Separate 32KB instruction and data caches
- Snoop Control Unit (SCU)
 - L1 cache snoop control
 - Accelerator coherency port
- Level 2 cache and controller
 - Shared 512 KB cache with parity



APU Sub-Components

- General interrupt controller (GIC)
- On-chip memory (OCM): RAM and boot ROM
- Central DMA (eight channels)
- Device configuration (DEVCFG)
- Private watchdog timer and timer for each CPU
- System watchdog and triple timer counters shared between CPUs
- ARM CoreSight debug technology

APU Address Map

- All registers for both CPUs are grouped into two contiguous 4KB pages
 - Accessed through a dedicated internal bus
- Fixed at 0xF8F0_0000 with a register block size of 8 KB
 - Each CPU uses an offset into this base address

0x0000-0x00FC	SCU registers
0x0100-0x01FF	Interrupt controller interface
0x0200-0x02FF	Global timer
0x0600-0x06FF	Private timers and watchdog timers
0x1000-0x1FFF	Interrupt distributor

NEON Main Features

- NEON is the ARM codename for the vector processing unit
 - Provides multimedia and signal processing support
- FPU is the floating-point unit extension to NEON
 - Both NEON and FPU share a single set of registers
- NEON technology is a wide single instruction, multiple data (SIMD) parallel and co-processing architecture
 - 32 registers, 64-bits wide (dual view as 16 registers, 128-bits wide)
 - Data types can be: signed/unsigned 8-bit, 16-bit, 32-bit, 64-bit, or 32-bit float

L1 Cache Features

- Separate instruction and data caches for each processor
- Caches are four-way, set associative and are write-back
- Non-lockable
- Eight words cache length
- On a cache miss, critical word first filling of the cache is performed followed by the next word in sequence

L2 Cache Features

- 512K bytes of RAM built into the SCU
 - Latency of 25 CPU cycles
 - Unified instruction and data cache
- Fixed, 256-bit (32 words) cache line size
- Support for per-master way lockdown between multiple CPUs
- Eight-way, set associative
- Two AXI interfaces
 - One to DDR controller
 - One to programmable logic master (to peripherals)

On-Chip Memory (OCM)

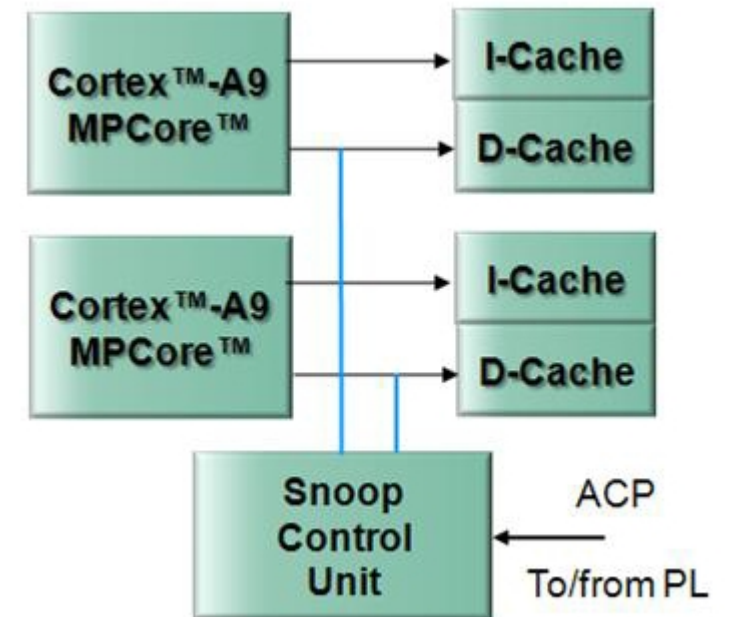
- The on-chip memory (OCM) module contains 256 KB of RAM and 128 KB of ROM (BootROM).
- It supports two 64-bit AXI slave interface ports, one dedicated for CPU/ACP access via the APU snoop control unit (SCU), and the other shared by all other bus masters within the processing system (PS) and programmable logic (PL).
- The BootROM memory is used exclusively by the boot process and is not visible to the user.

Snoop Control Unit (SCU)

- Shares and arbitrates functions between the two processor cores
 - Data cache coherency between the processors
 - Initiates L2 AXI memory access
 - Arbitrates between the processors requesting L2 accesses
 - Manages ACP accesses
 - A second master port with programmable address filtering between OCM and L2 memory support

Cache Coherency Using SCU

- High-performance, cache-to-cache transfers
- Snoop each CPU and cache each interface independently
- Coherency protocol is MESI
 - M: Cache line has been modified
 - E: Cache line is held exclusively
 - S: Cache line is shared with another CPU
 - I: Cache line is invalidated
- Uses Accelerator Coherence Port (ACP) to allow coherency to be extended to PL



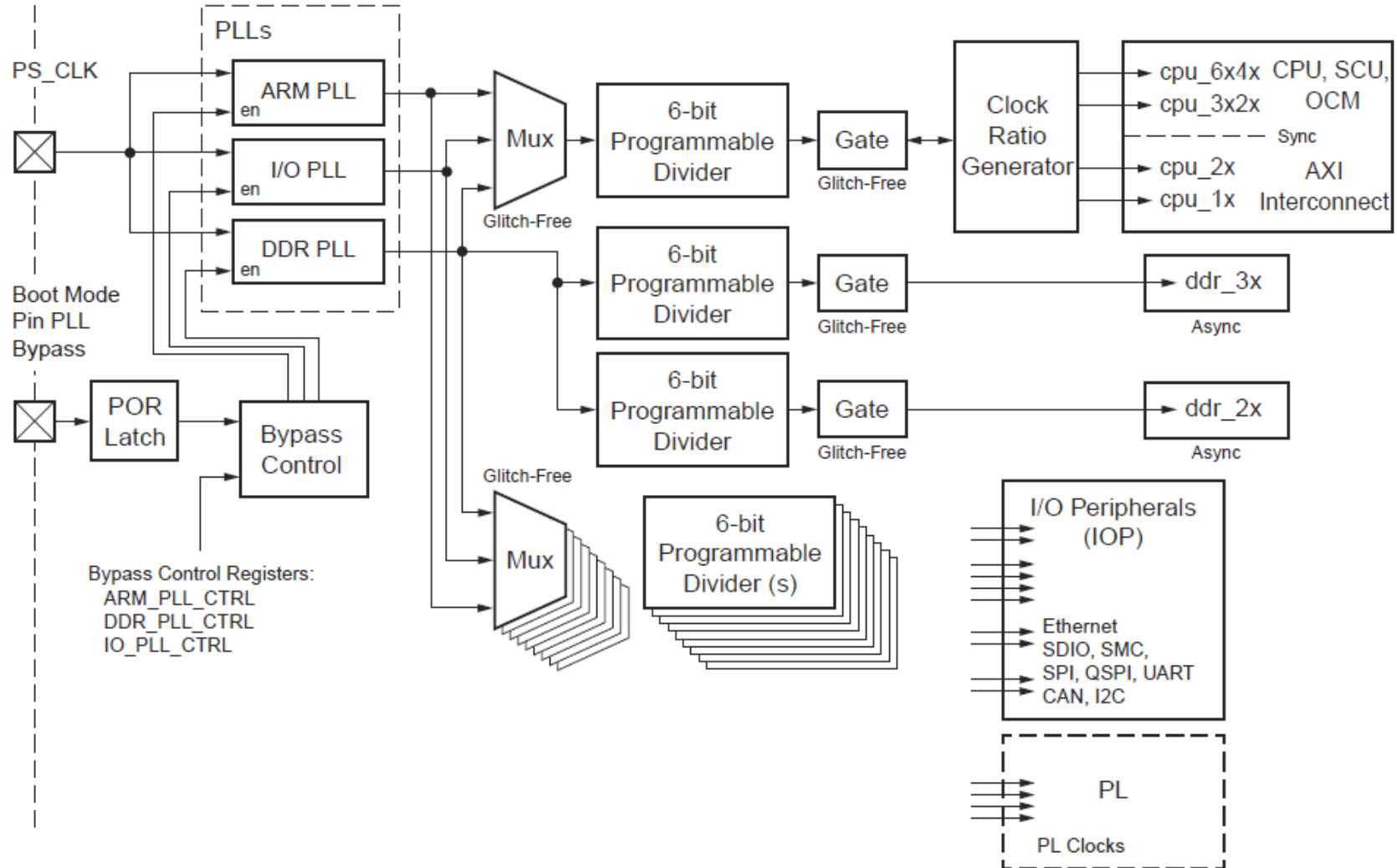
System Level Control Register (SLCR)

- A set of special registers in the APU used to configure the PS
 - Power and clock management
 - Reset control
 - MIO/EMIO management
- Accessible through software
 - Standalone BSP support

SLCR Categories	
System clock and reset control/status registers	TrustZone control register
APU control registers	SoC debug control registers
DMA initialization registers	MIO/IOP control/status registers
DDR control registers	Miscellaneous control registers
PL reset registers	RAM and ROM control registers

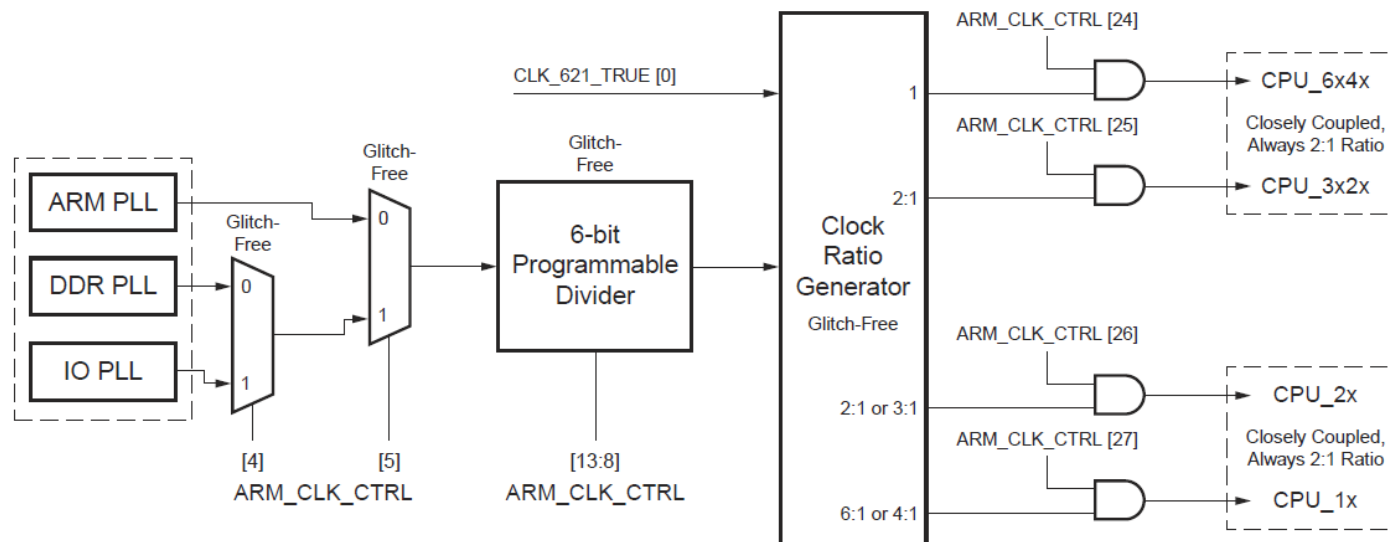
Zynq Clocks

System Clocks



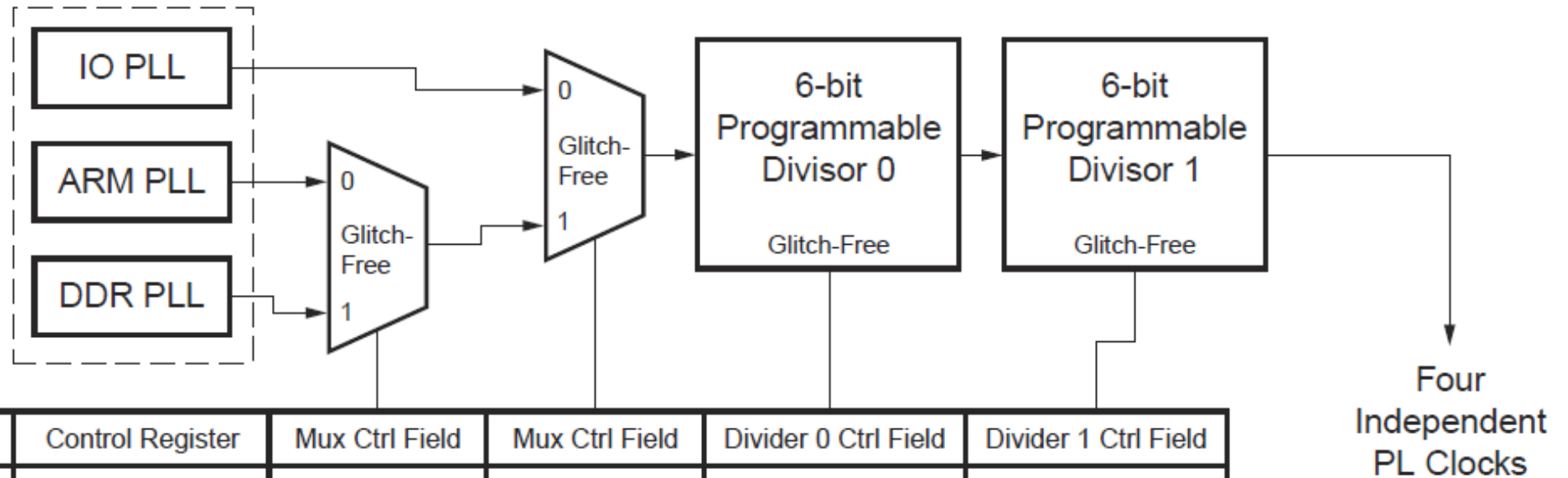
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CPU Clock

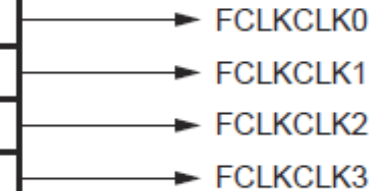


CPU Clock	6:2:1	4:2:1	Clock Domain Modules
CPU_6x4x	800 MHz (6 times faster than CPU_1x)	600 MHz (4 times faster than CPU_1x)	CPU clock freq, SCU, OCM arbitrator, NEON and L2 Cache
CPU_3x2x	400 MHz (3 times faster than CPU_1x)	300 MHz (2 times faster than CPU_1x)	APU Timers
CPU_2x	266MHz (2 times faster than CPU_1x)	300 MHz (2 times faster than CPU_1x)	IOP, central interconnect, master interconnect, slave interconnect and OCM RAM
CPU_1x	133 MHz	150 MHz	IOP, AHB and APB interface busses

PL Clocks



PL FCLK Clock	Control Register	Mux Ctrl Field	Mux Ctrl Field	Divider 0 Ctrl Field	Divider 1 Ctrl Field
PL FCLK 0	FPGA0_CLK_CTRL	SRCSEL, 4	SRCSEL, 5	DIVISOR 0, 13:8	DIVISOR 1, 25:20
PL FCLK 1	FPGA1_CLK_CTRL	SRCSEL, 4	SRCSEL, 5	DIVISOR 0, 13:8	DIVISOR 1, 25:20
PL FCLK 2	FPGA2_CLK_CTRL	SRCSEL, 4	SRCSEL, 5	DIVISOR 0, 13:8	DIVISOR 1, 25:20
PL FCLK 3	FPGA3_CLK_CTRL	SRCSEL, 4	SRCSEL, 5	DIVISOR 0, 13:8	DIVISOR 1, 25:20



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