Front-end Electronics and Data Acquisition in Particle Physics

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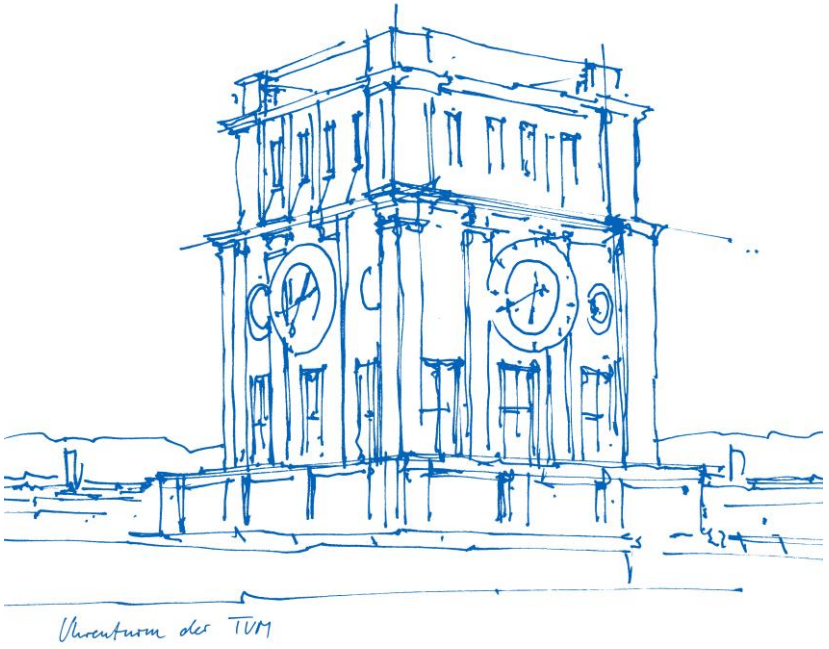
Joint ICTP-IAEASchool on FPGA-based SoC

and its Applications for

Nuclear and Related

Instrumentation

25 January – 19 February



Overview

DAQ and front-end electronics

FPGA-based Time-to-Digital Converter

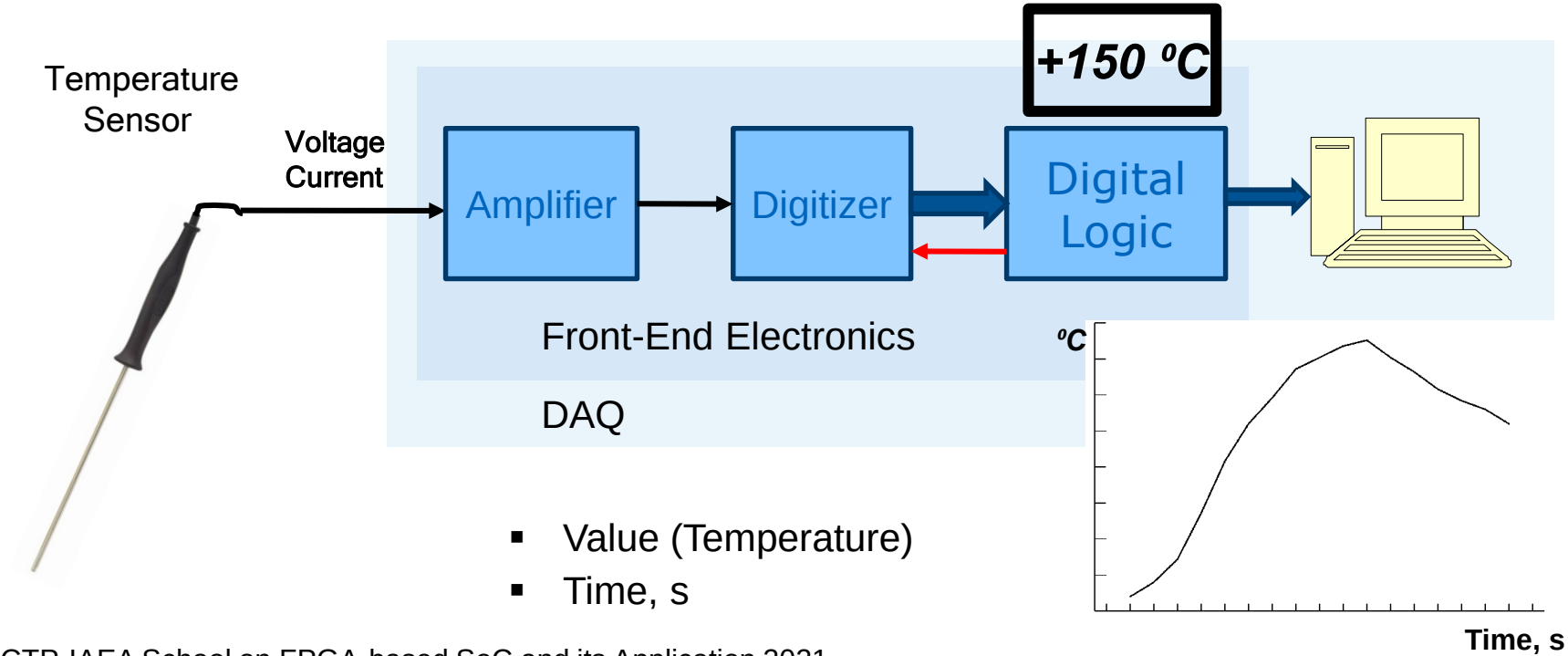
Preprocessing Detector Signal in FPGA

FPGA Technology

- Digital Logic
- Programmable
- Parallel
- DSPs
- Serial links

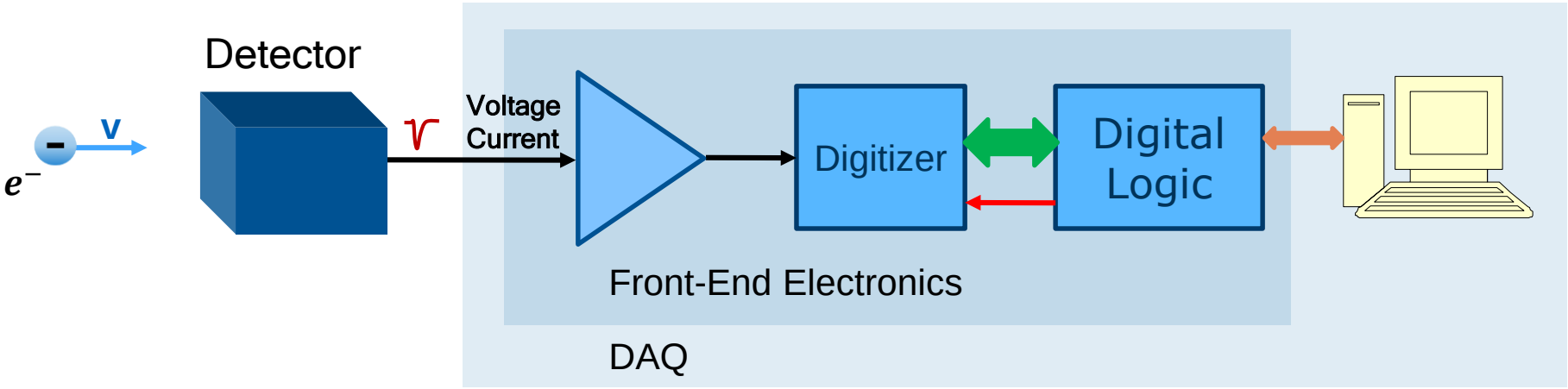
Data Acquisition System

- The process of sampling detector signals
- Conversion to digital form
- Data processing
- Transmission to PC for further processing, visualization, and storage



- Value (Temperature)
- Time, s

Data Acquisition System



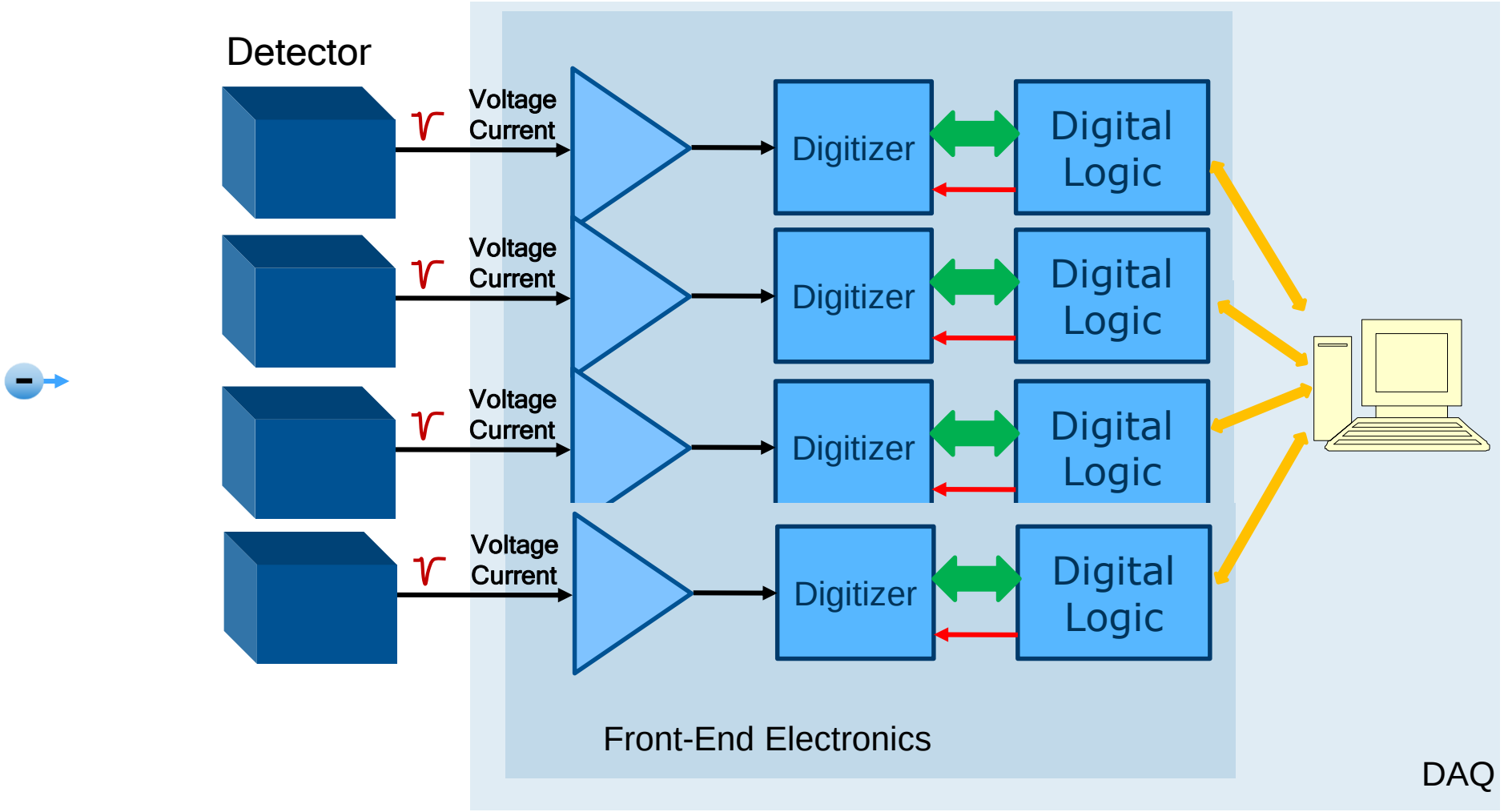
Amplitude - amount of energy released in Detector

Time - when particle crossed Detector

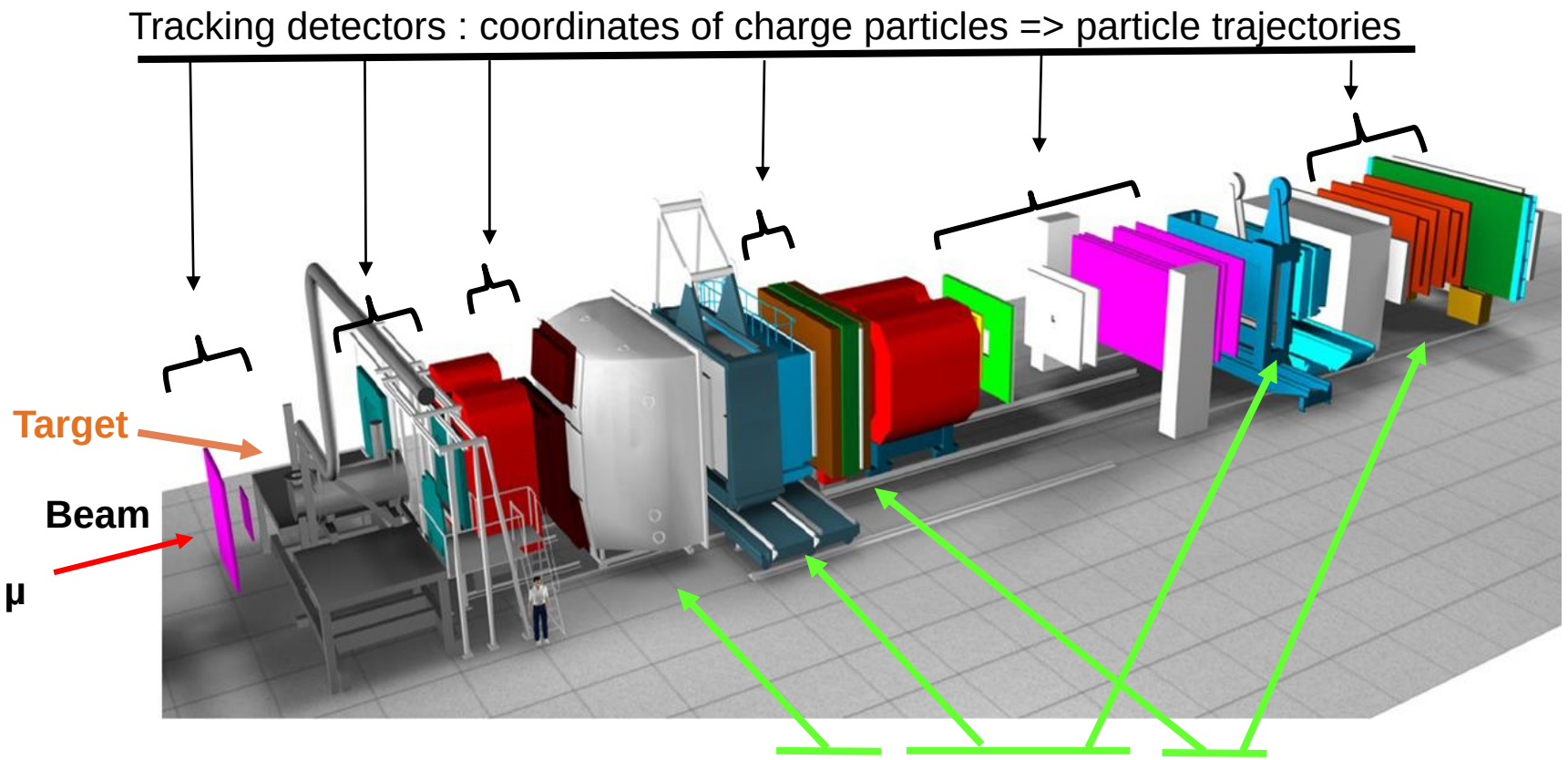
FPGA functionalities :

- **Glue Logic** – custom logic, slow interfaces: SPI, I2C, JTAG, LVDS …
- **Control and synchronization**
- **Data processing – noise suppression, data size reduction, conversion**
- **Serial links to Computer – Ethernet, PCIE, USB…**

Multi Channel System

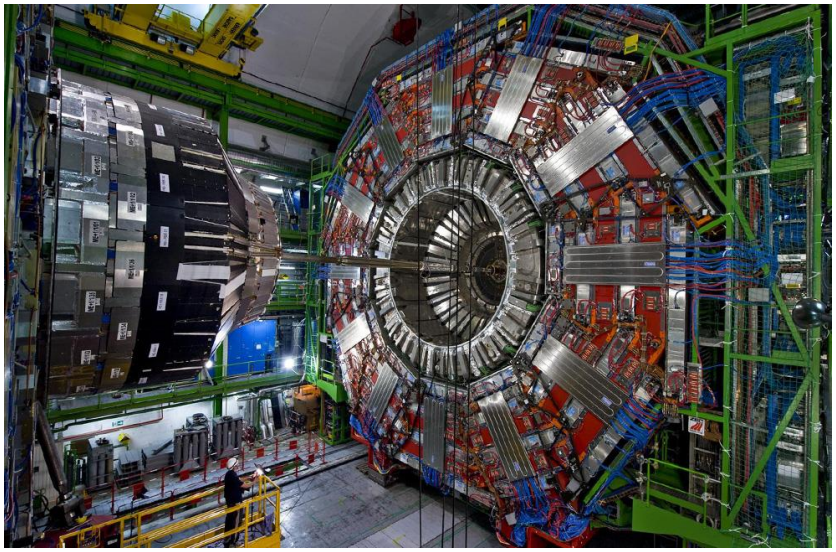


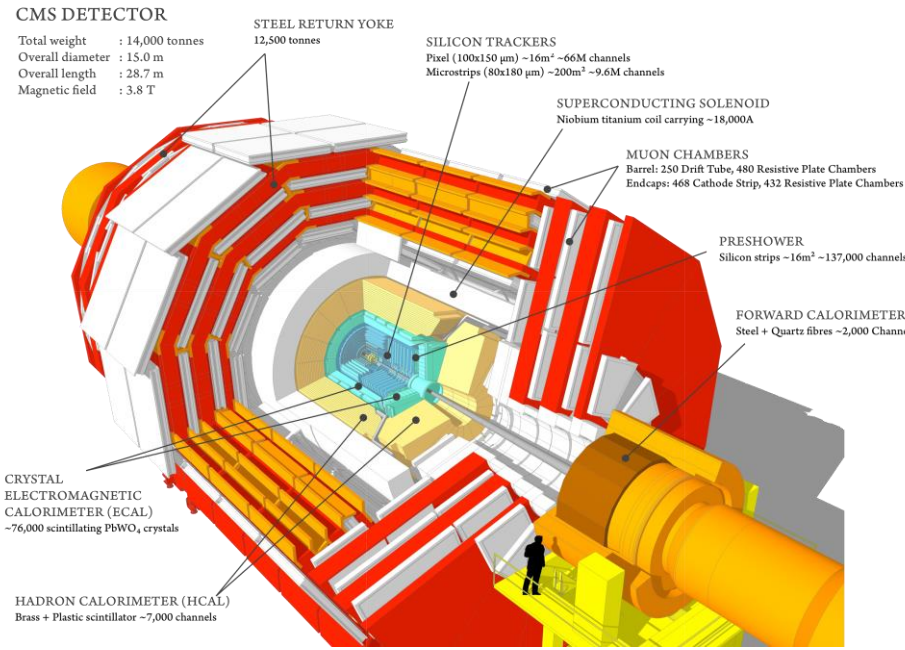
Particle Physics Experiment (COMPASS)



300 000 detector channels

LHC Experiments (CMS Experiment)





3 other LHC experiments

- ATLAS
- LHCb
- ALICE

Number of channels > 10^7

FPGAs in High-Energy Physics

1. Detector Front-End Electronics (FEE)

Data Reduction Steps

TDC

- Time measurement
- Zero Suppression
- Time stamp assignment
- Data Sorting

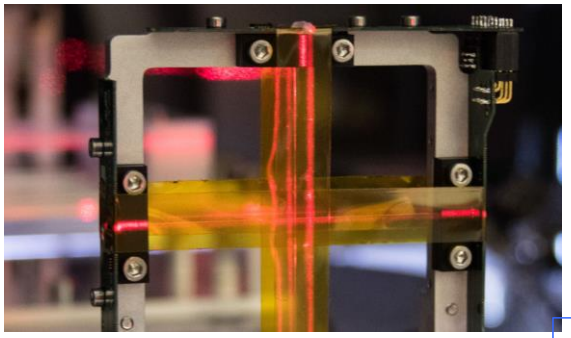
ADC

- Pedestal Calculation
- Signal detection
- Feature Extraction
  - Signal Amplitude
  - Signal Time

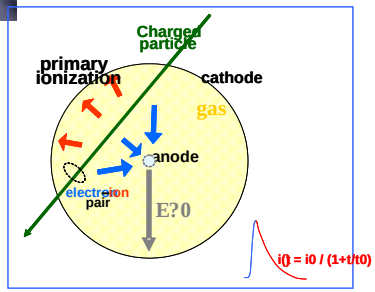
2. Data Acquisition and (Sub-)Event Building

3. Trigger Logic

FEE: Detector Readout



SciFi detector



Drift tube

Time-to-Digital Converters

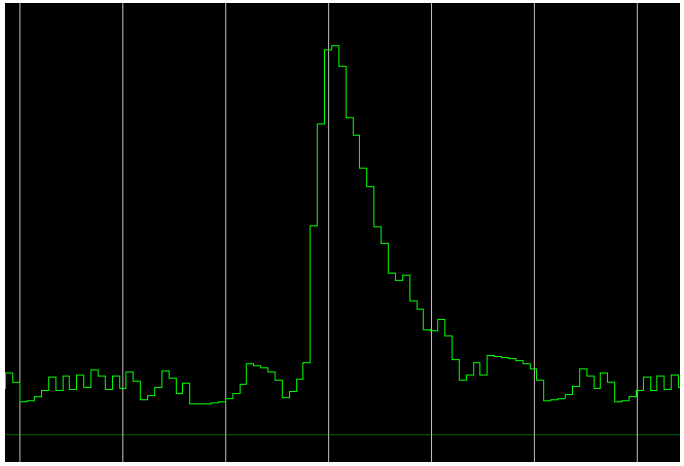
- **Time information only**:
  - **Scintillation detectors**
    - light emission
  - **Many types of wire detectors**
    - Ionization of gas by charged particle

Special circuit : Time-to-Digital-Converter (TDC)

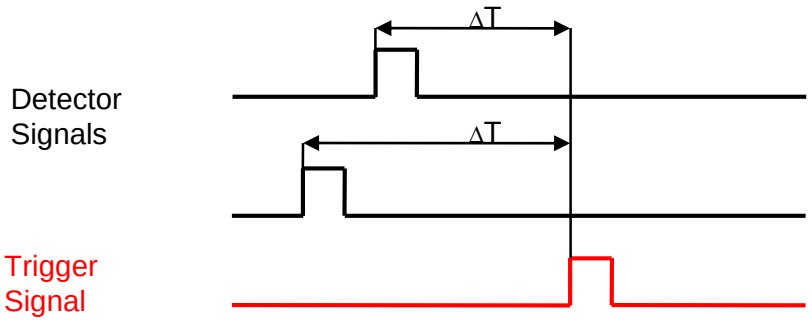
Analog-to-Digital Converters

- **Signal Amplitude and Time of signal arrival**
- **Energy loss measurement**
  - **Calorimeters**
  - **Silicon detectors**

Sampling Analog-to-Digital Converter (ADC)

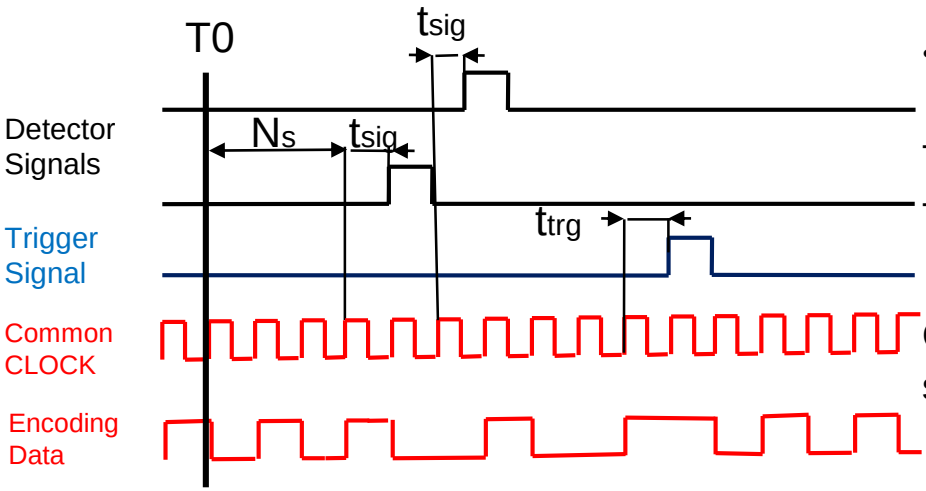


How to Measure Time



Classical method:

- TRIGGER is a reference
- SIGNAL time is measured respectively to TRIGGER signal



Alternative method for big experiments:

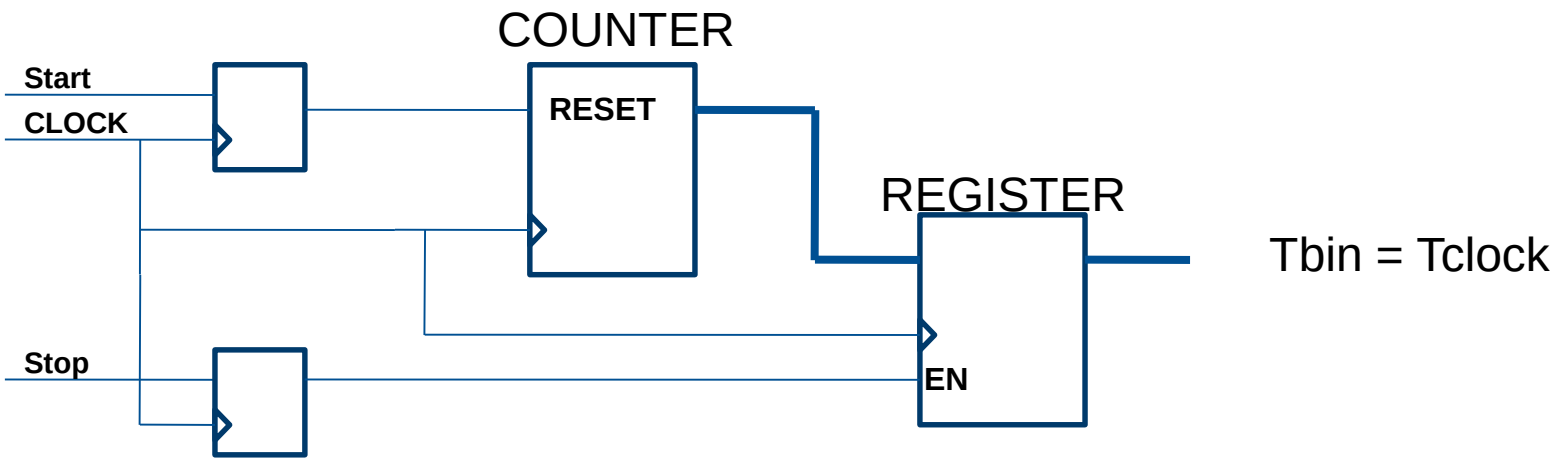
- Distribute CLOCK , why clock?
  - Easier to distribute with very low jitter
- Measure absolute time respectively to CLOCK phase

$T_{sig} = N_s\ T_{clk} + t_{sig}$

$T_{trg} = N_t\ T_{clk} + t_{trg}$

Clock and Data are encoded and transmitted from single source to multiple destinations

Counter-based TDC

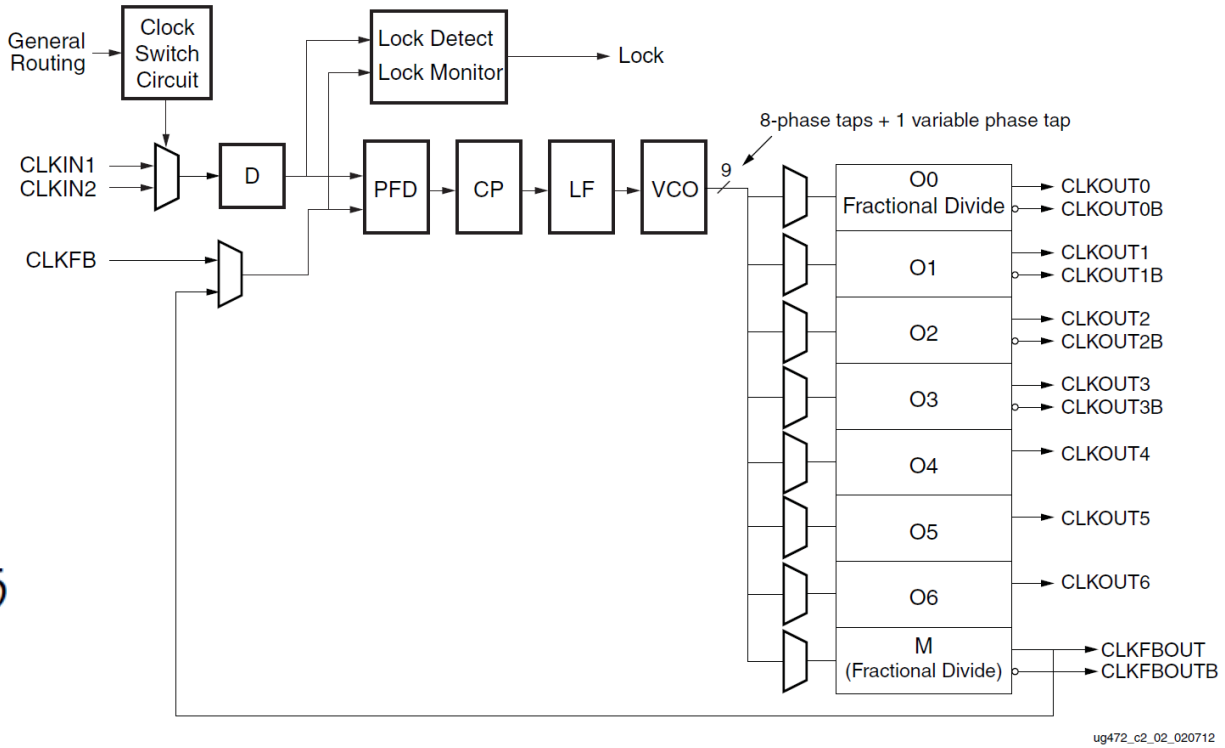


System Clock
Maximum Clock frequency is limited

FPGA Features : Clock Management Tile

PLL consists of

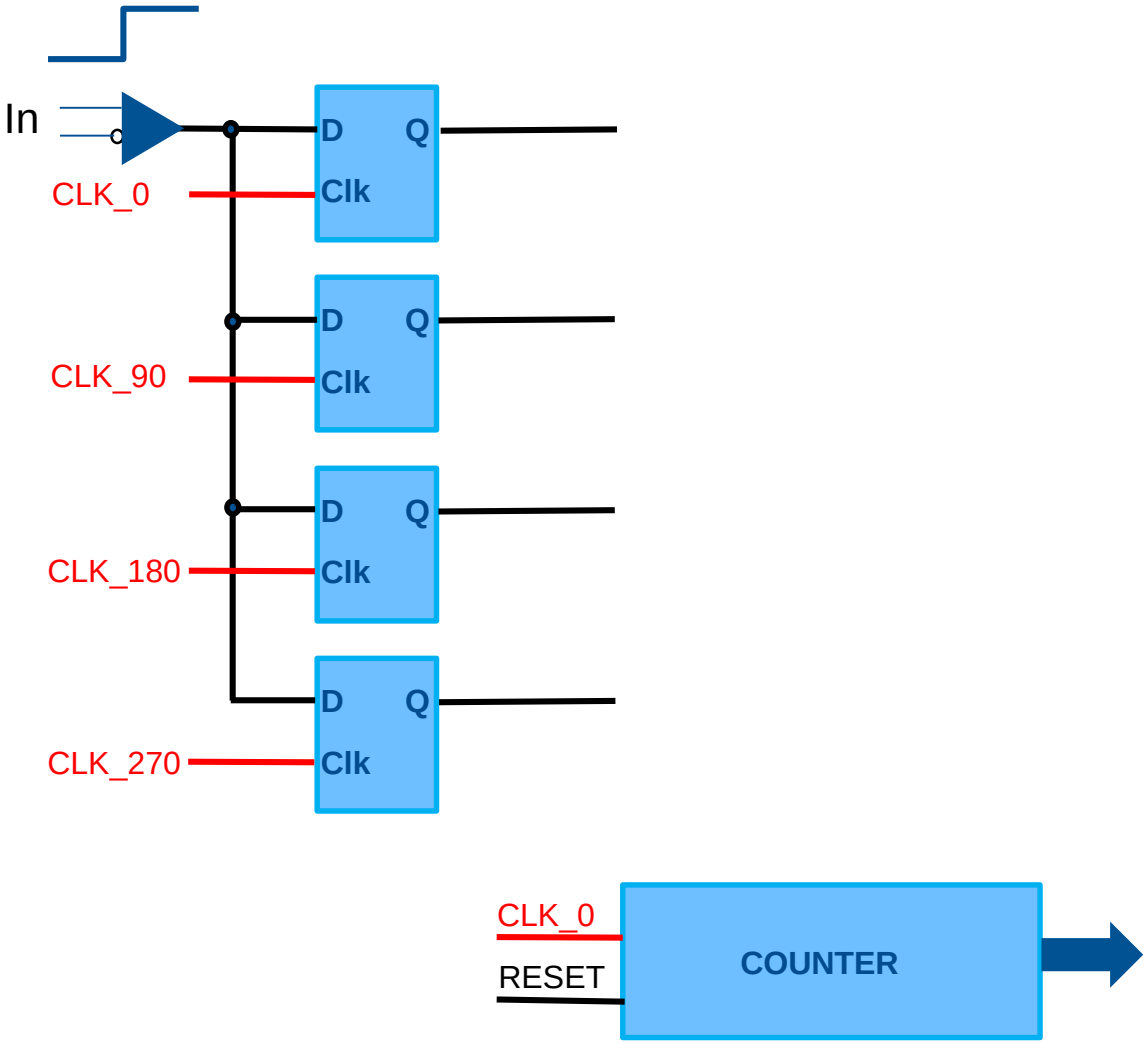
- **Phase detector** (PFD)
- **Charge pump** (CP)
- **Loop filter with defined time properties** (LF)
- **Voltage controlled oscillator** (VCO)



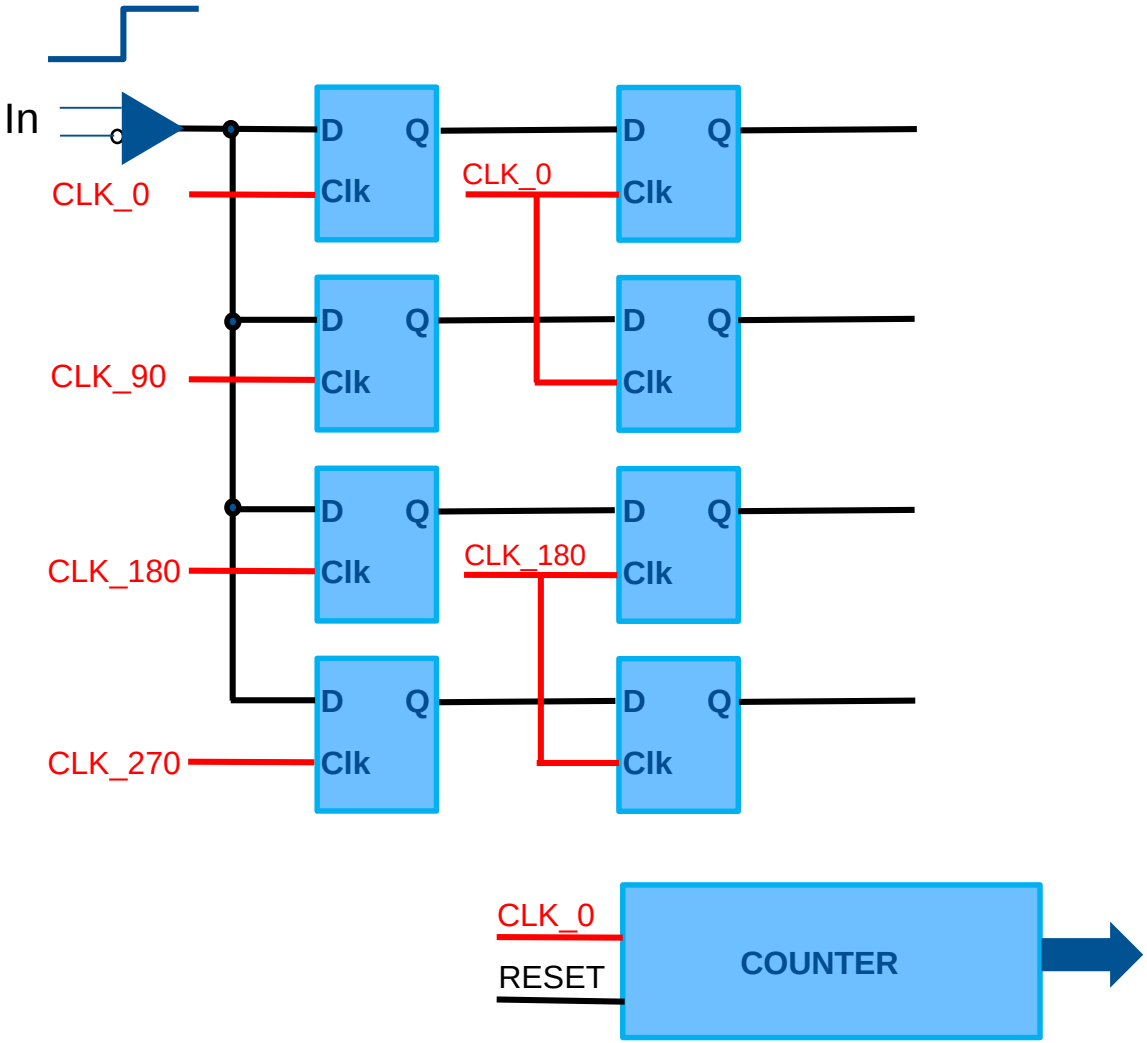
$$F_{VCO} = F_{CLKIN} \times \frac{M}{D}$$

$$F_{OUT} = F_{CLKIN} \times \frac{M}{D \times O}$$

FPGA-based TDCs. Multiple Clock Phases



FPGA-based TDCs. Multiple Clock Phases



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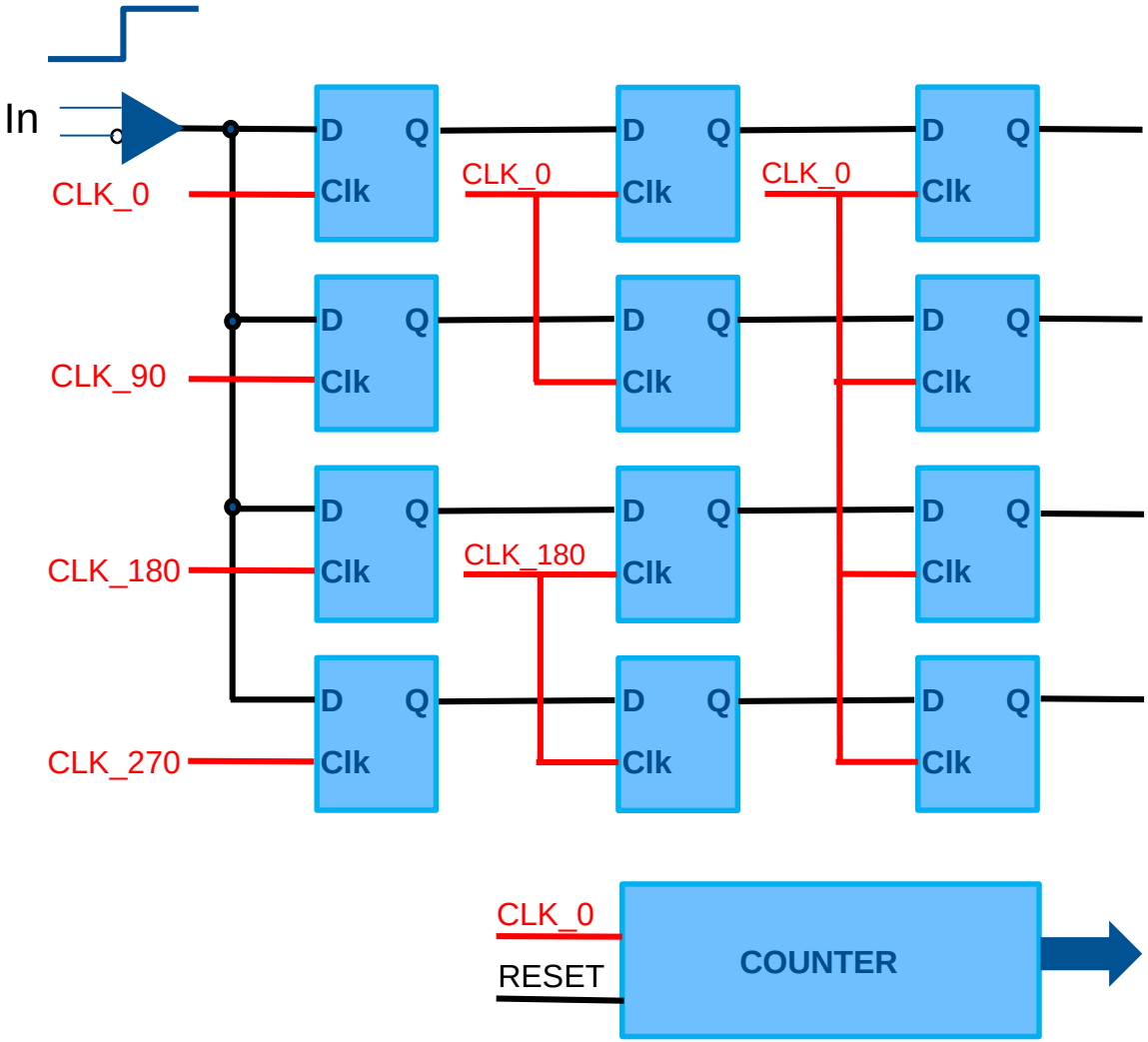
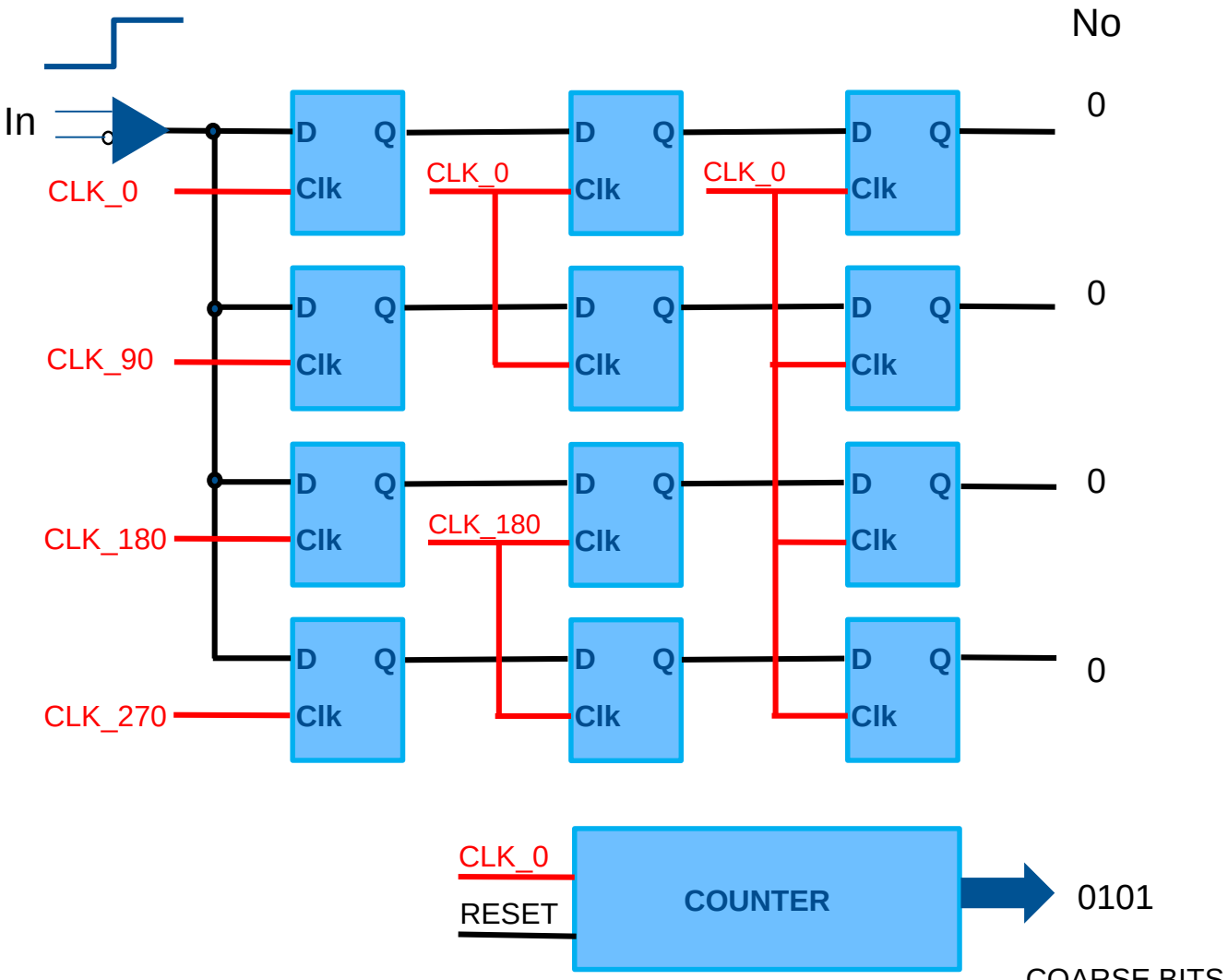


FPGA-based TDCs. Multiple Clock Phases



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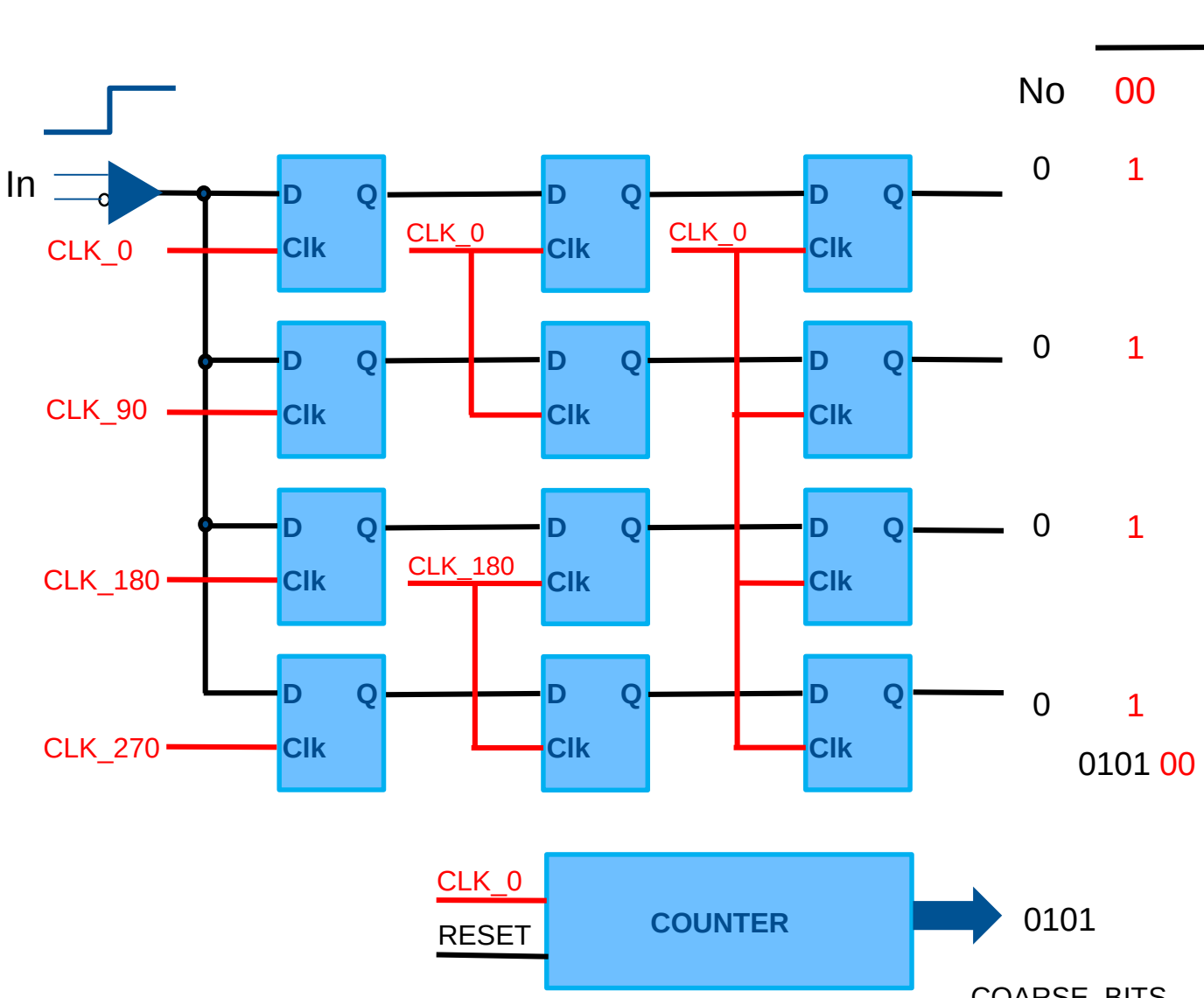
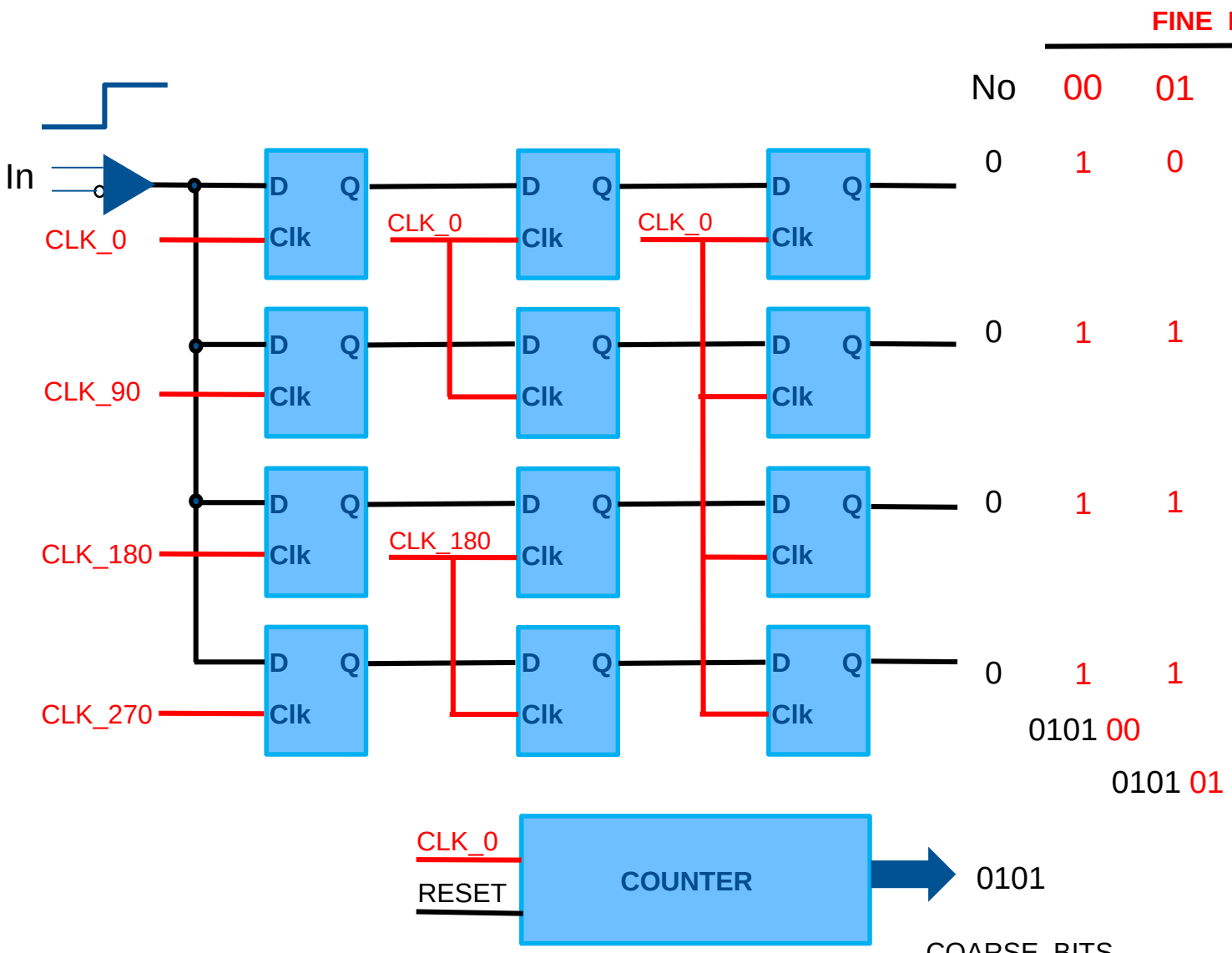
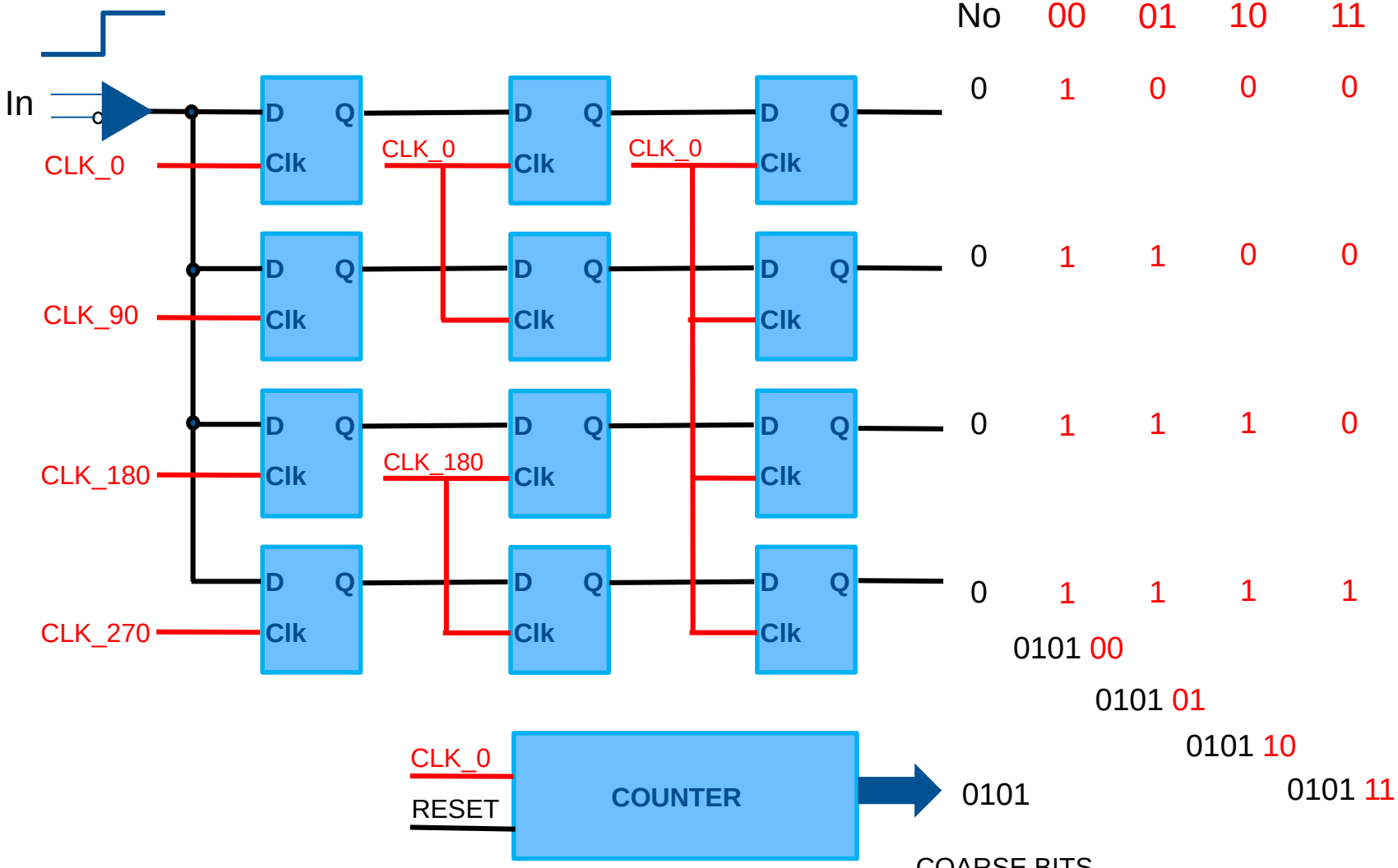


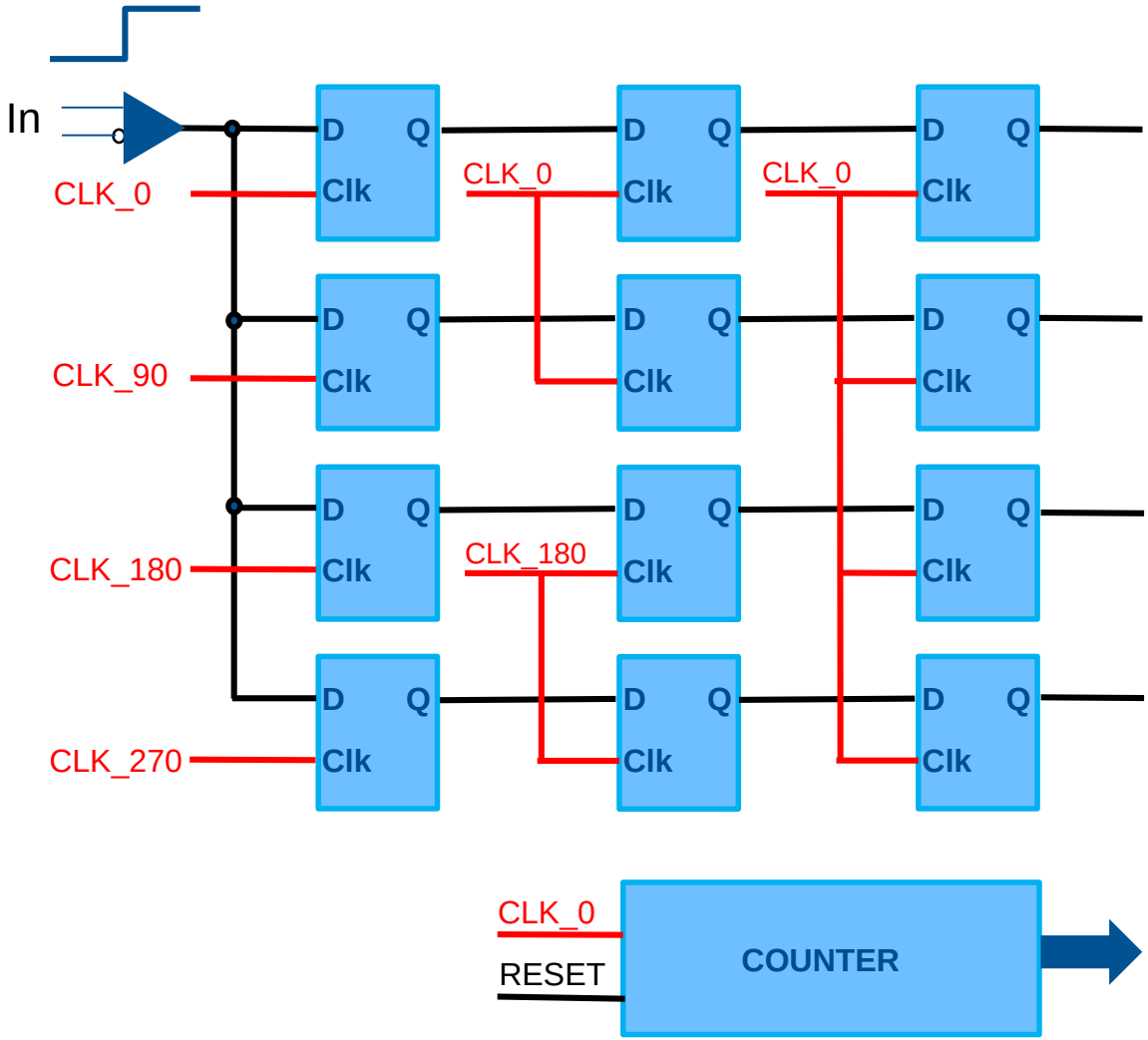
FPGA-based TDCs. Multiple Clock Phases



FPGA-based TDCs. Multiple Clock Phases



FPGA-based TDC. Multiple Clock Phases



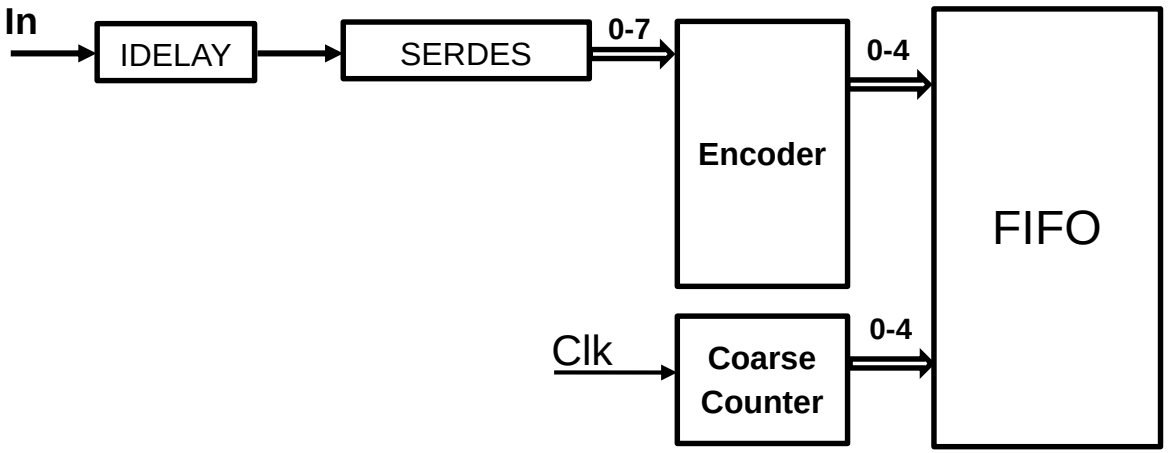
Performance :

CLK_0	Bin size	Resolution
100 MHz	2.5 ns	720 ps
250 MHz	1 ns	290 ps
500 MHz	500 ps	144 ps

FPGA-based TDC. SERDES

IO Blocks of modern FPGAs :

- IO delay, programmable with step 50-70 ps
- SERDES – serializer/deserializer, speed 0.8 – 1.2 Gbps



Performance : 1 Gbps => bin size 1 ns => resolution 290 ps

SERDES : improved circuit for FF metastability problem !

FPGA-based TDC. SERDES

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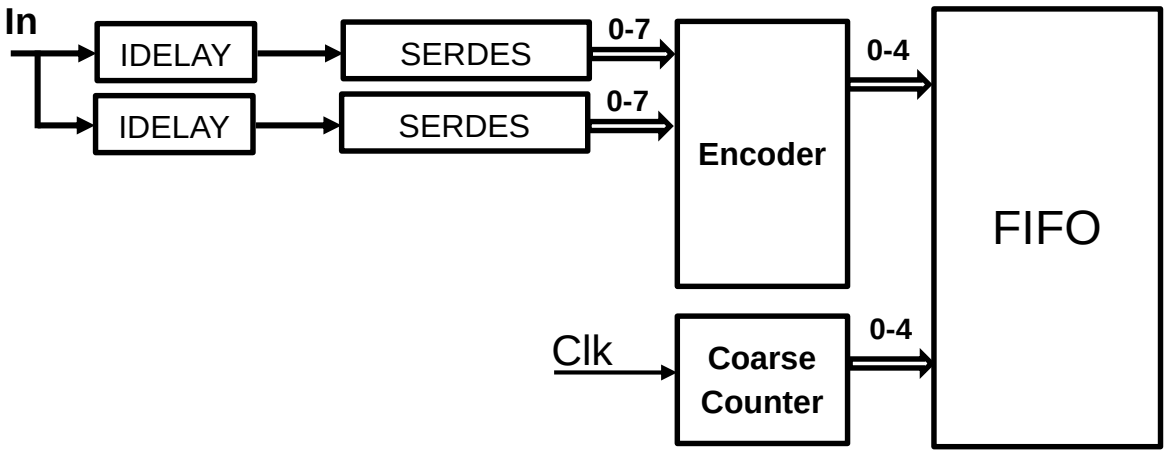
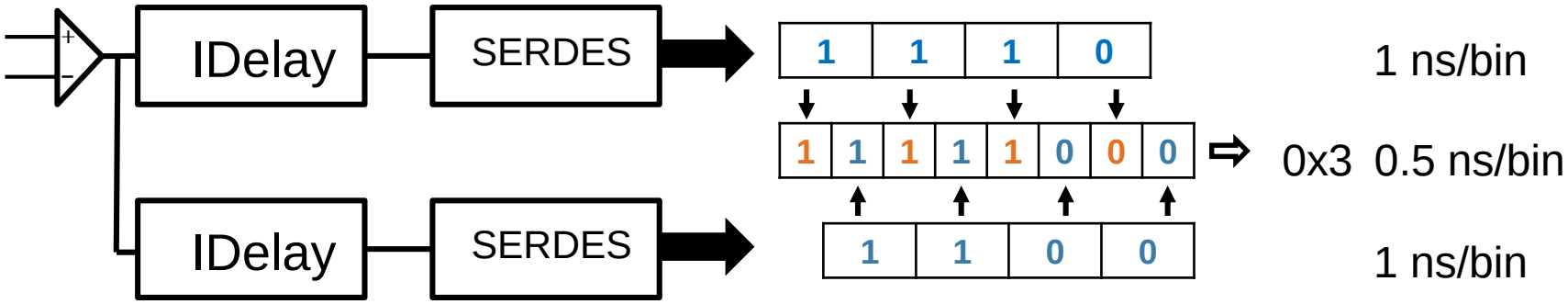
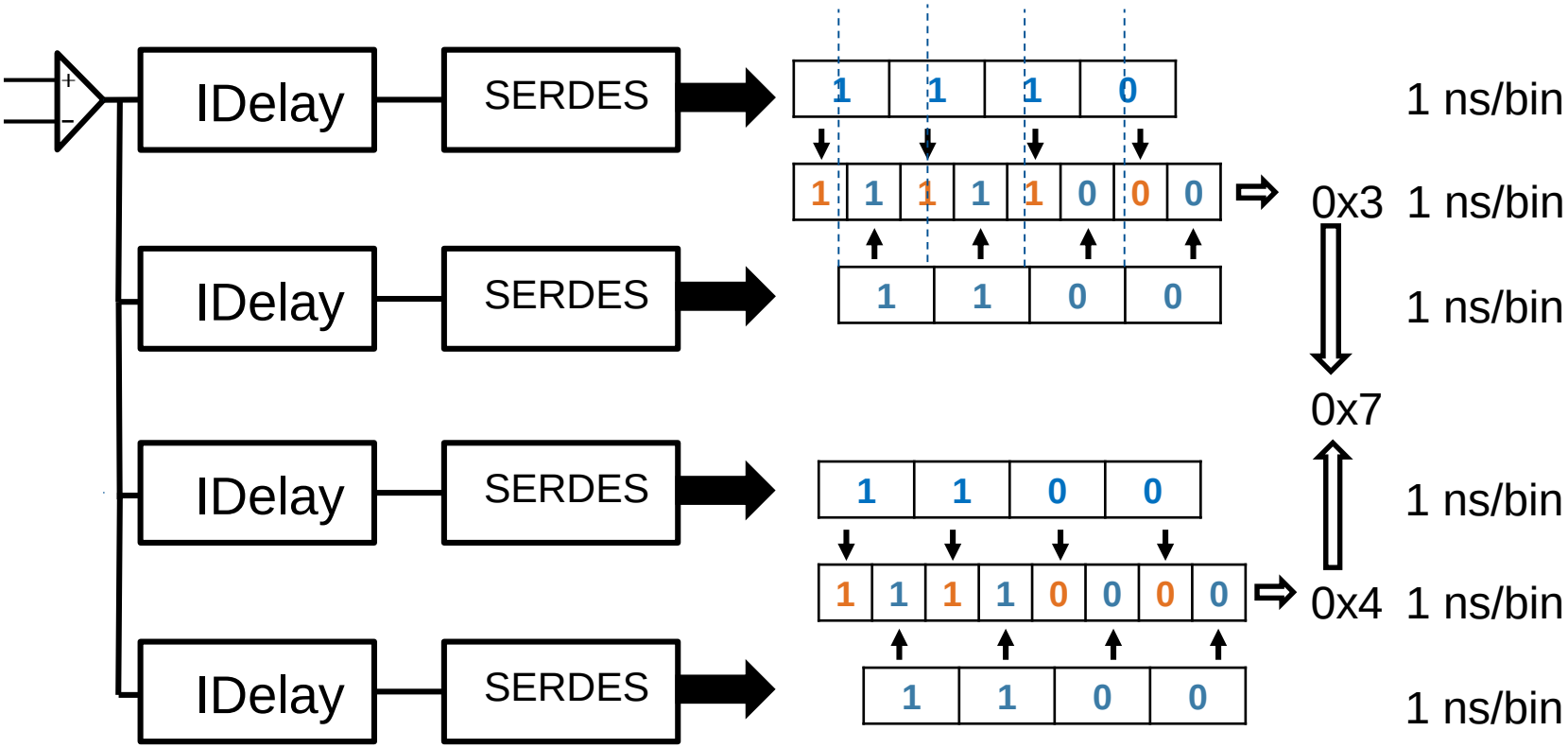


Performance : 1 Gbps => bin size 0.5 ns => resolution 144 ps

SERDES : improved circuit for FF metastability problem !


IDelay
SERDES
IDelay
SERDES
1 1 1 0
1 1 1 1 1 0 0 0
1 1 0 0
0x3
1 ns/bin
0.5 ns/bin
1 ns/bin


IDelay
SERDES
IDelay
SERDES
IDelay
SERDES
IDelay
SERDES
1 1 1 0
1 1 1 1 1 0 0 0
1 1 0 0
1 1 1 1 0 0 0 0
1 1 0 0
1 1 0 0
1 ns/bin
0x3
1 ns/bin
1 ns/bin
0x7
1 ns/bin
0x4
1 ns/bin
1 ns/bin

FPGA-based TDC. SERDES

IO Blocks of modern FPGAs :

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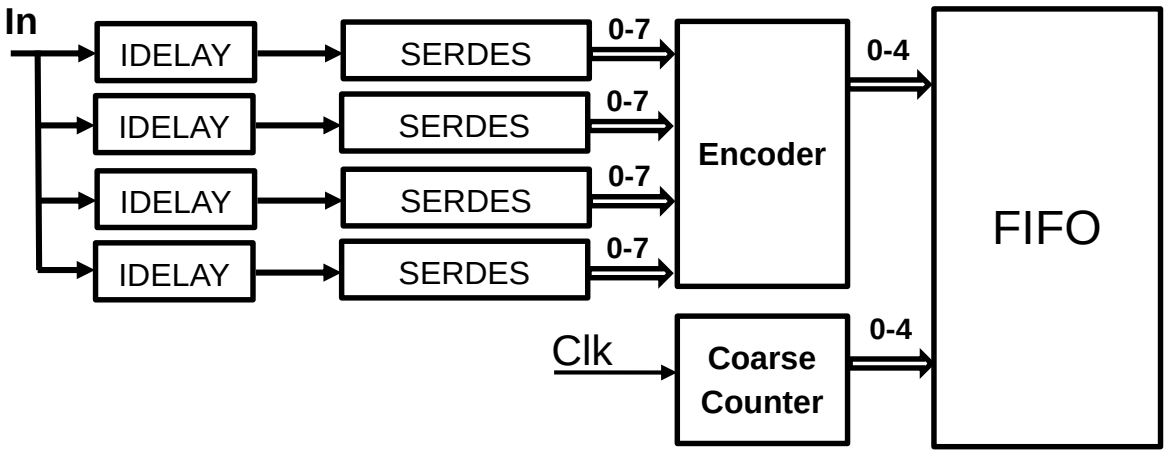
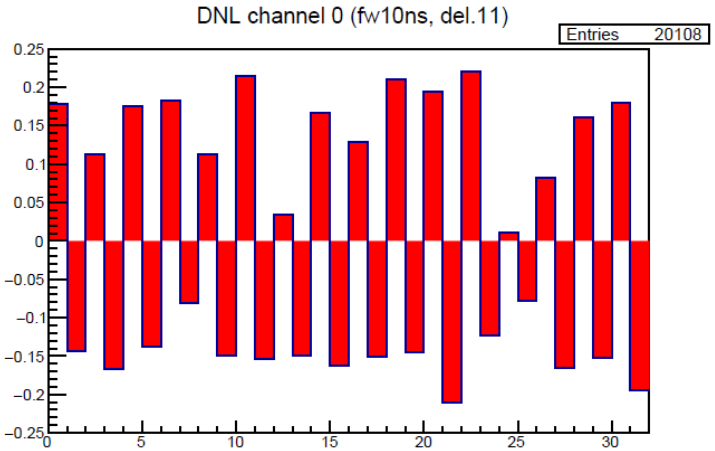
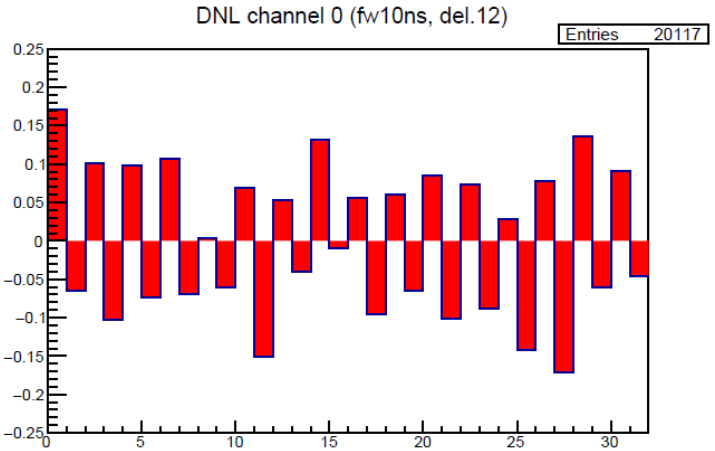


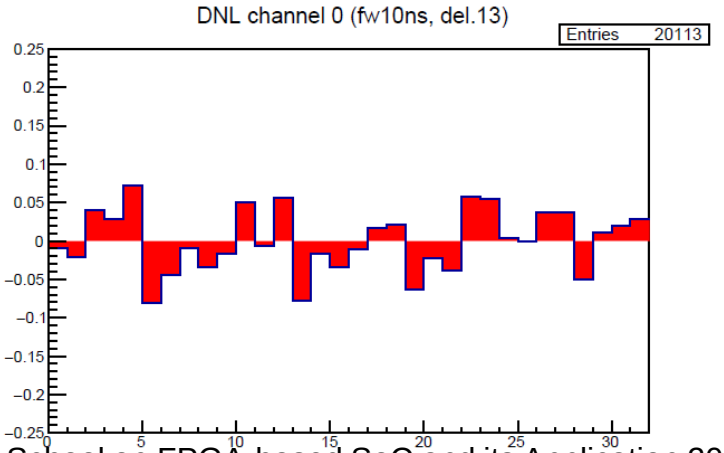
Performance : 1 Gbps => bin size 0.25 ns => resolution 72 ps

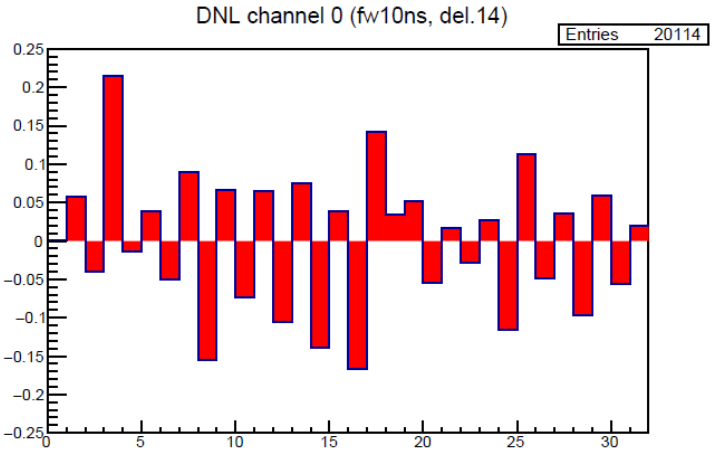
TDC : Differential Non-Linearity

Scan of IDELAY

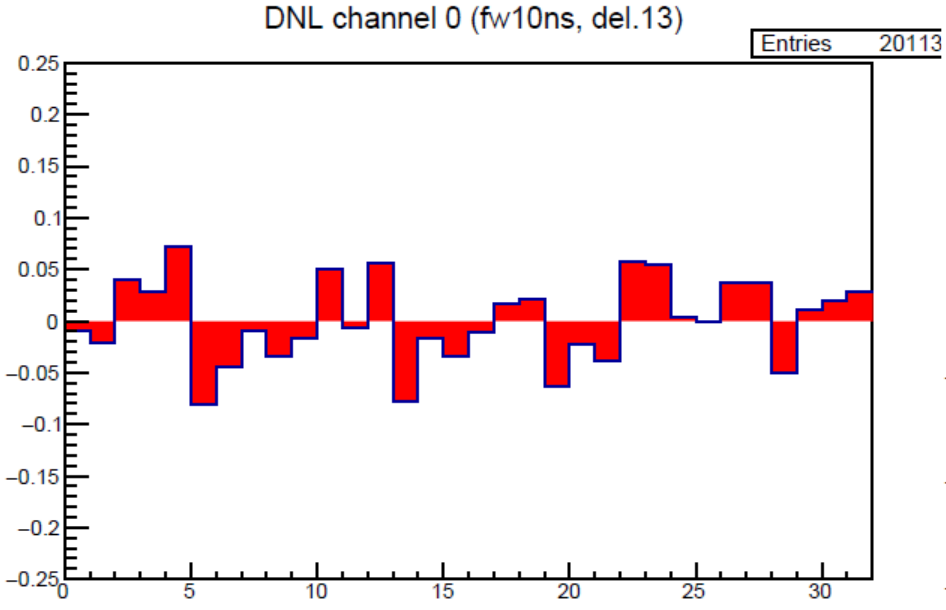




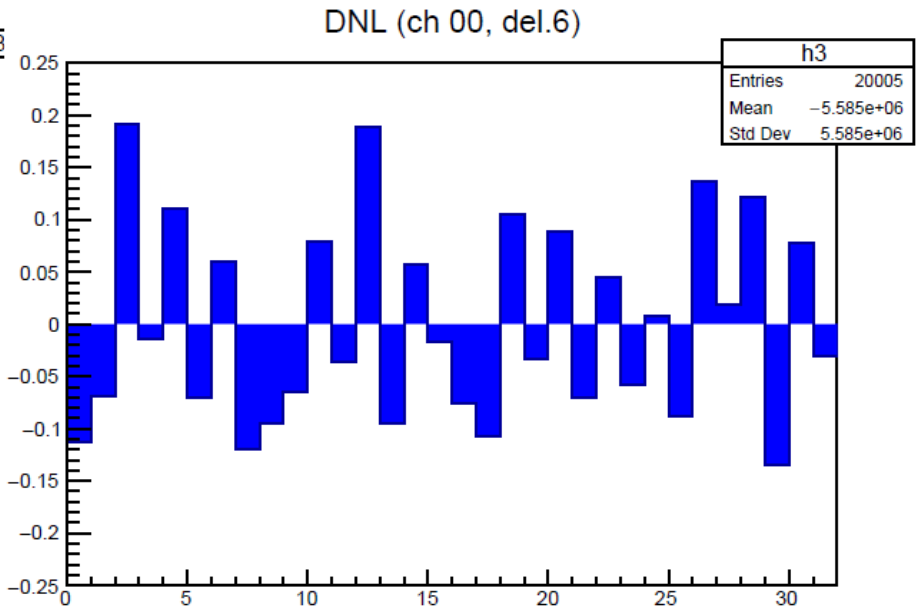




TDC. Differential Non-Linearity



1 ns bin size

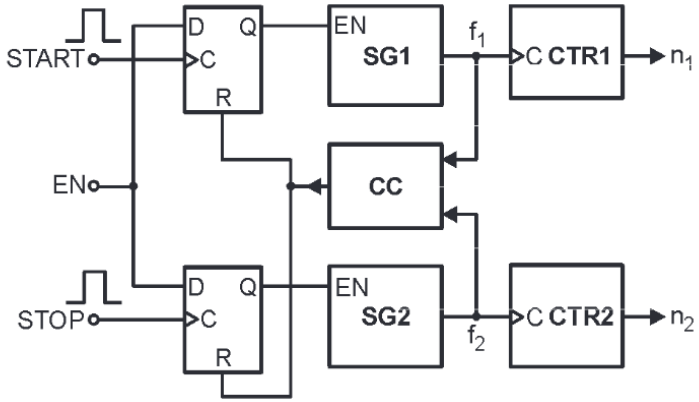


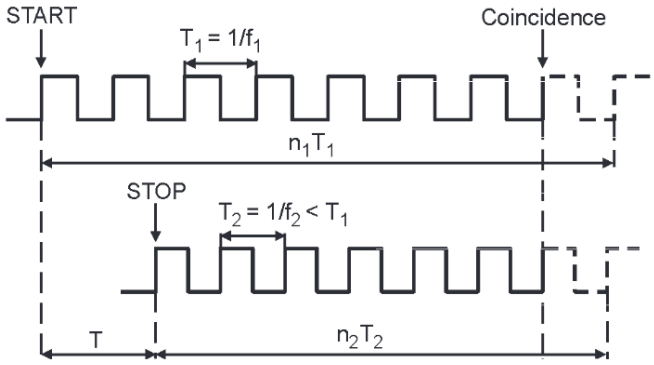
0.5 ns bin size

Limits of SERDES

IDELAY quantization and DNL degradation limits TDC resolution to ~50ps

Vernier Converter





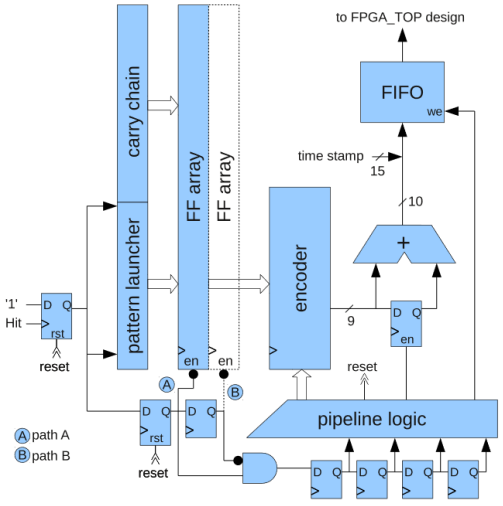
$$T = T1 \cdot (n1-1) - T2 \cdot (n2-1)$$

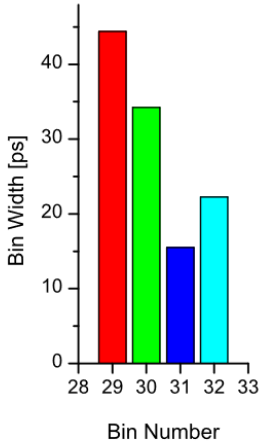
Metrologia41(2004) 17–32PII: S0026-1394(04)70012-2
Review of methods for time intervalmeasurements with picosecond resolution
J´ozef Kalisz

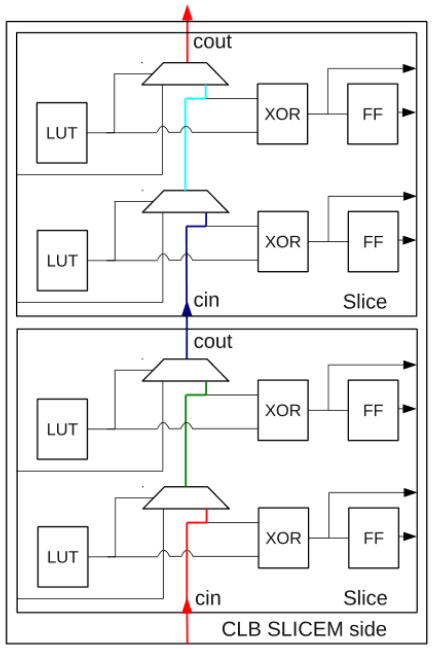
Taped Delay Line TDC

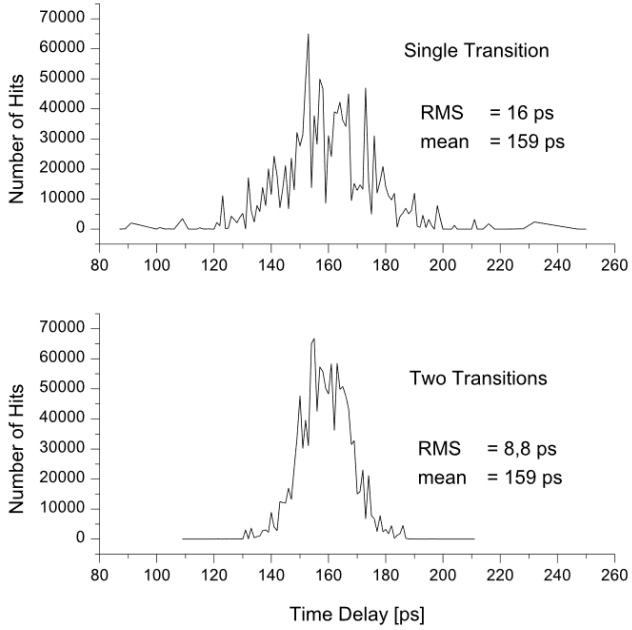
Big variation of bin sizes
Solutions :

- Two TDLs for one measurement
- Combine both measurements
- Precision improvements by factor 1.8





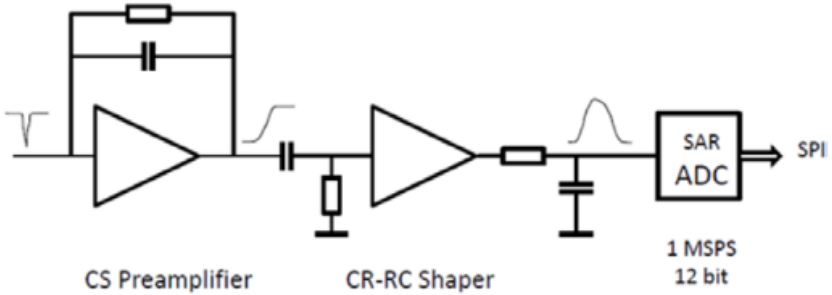




High Res. TDC
E. Bayer and M. Traxler
GSI

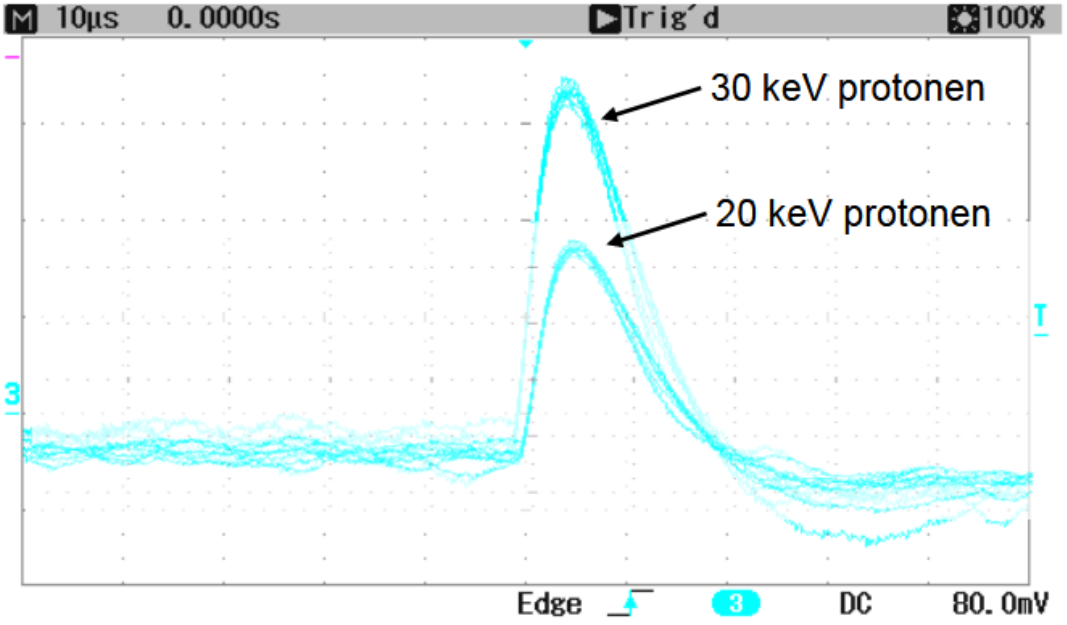
ADC Front-End Data Processing

ADC readout – Preamplifier and Shaper

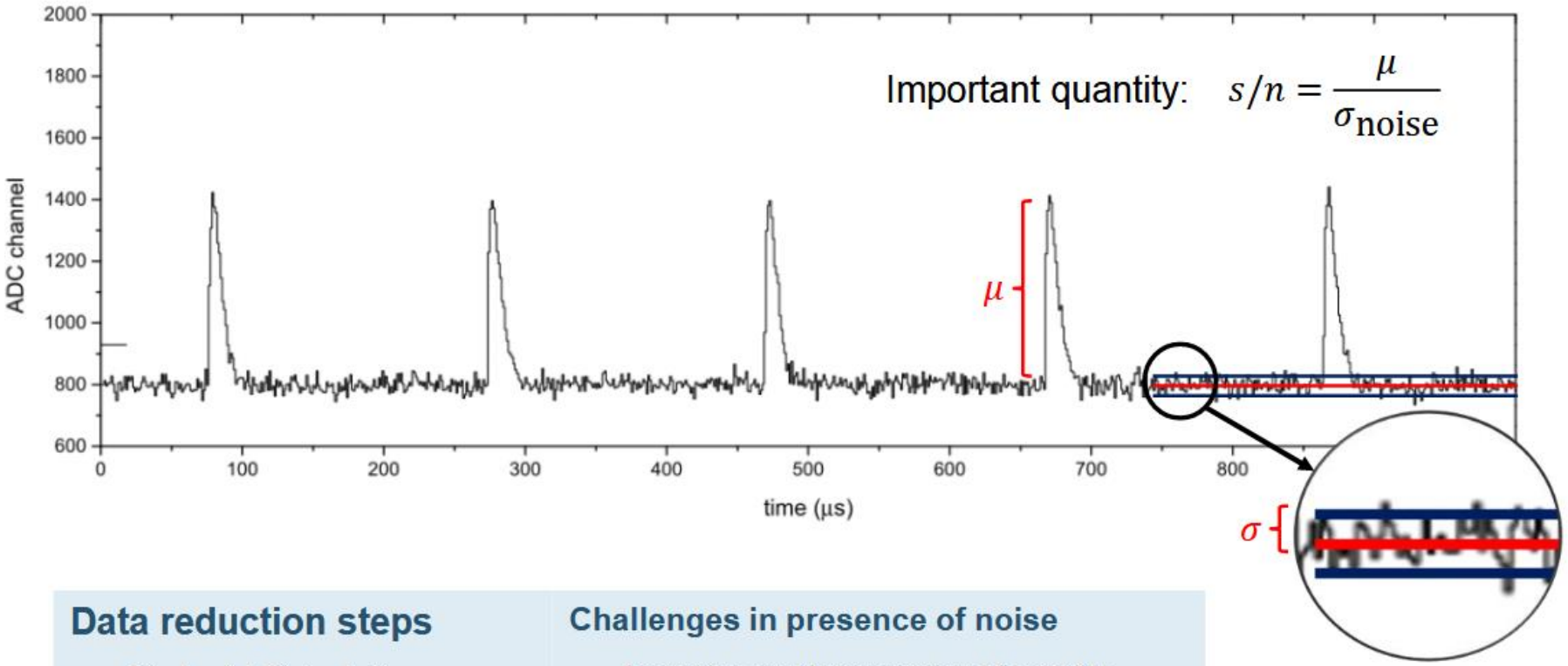


Created charge proportional to energy deposit
=> Amplitude measurement

- Charge-sensitive (CS) preamplifier
- Shaping: CR differentiator and RC integrator
- 12-bit ADC (AD7450) with $f_{\text{sample}} = 1\ \text{MHz}$



Noise on Signals



Data reduction steps

- Pedestal Calculation
- Signal detection
- Feature Extraction

Challenges in presence of noise

- Averaging over large number of samples
- Discrimination between signals and noise (signal-to-noise ratio)
- Precise determination of amplitude or signal shape

Pedestal Calculation

- Pedestal

$$\bar{S} = \frac{\sum_{k=0}^{N-1} s_k}{N}$$

$s_k = \{a_{11}\ a_{10}\ a_9\ a_8\ a_7\ a_6\ a_5\ a_4 a_3\ a_2\ a_1\ a_0\}$ – bit vector

a_{11}	a_{10}	a_9	a_8	a_7	a_6	a_5	a_4	a_3	a_2	a_1	a_0

  - Tip
    - N = 2^m => Integer DIVISION is shift by m bits

If m = 7

$\sum_{k=0}^{6} s_k =$

a_{18}	a_{17}	a_{16}	a_{15}	a_{14}	a_{13}	a_{12}	a_{11}	a_{10}	a_9	a_8	a_7	a_6	a_5	a_4	a_3	a_2	a_1	a_0

Shift

$\bar{S} = \frac{\sum_{k=0}^{N-1} s_k}{N} =$

a_{18}	a_{17}	a_{16}	a_{15}	a_{14}	a_{13}	a_{12}	a_{11}	a_{10}	a_9	a_8	a_7	a_6	a_5	a_4	a_3	a_2	a_1	a_0

$\bar{S} = \frac{\sum_{k=0}^{N-1} s_k}{N} =$

a_{11}	a_{10}	a_9	a_8	a_7	a_6	a_5	a_4	a_3	a_2	a_1	a_0

Noise Calculation

Standard deviation : $\sigma^2 = \frac{1}{N-1}\sum_{i=0}^{N-1}(s_i - \bar{s})^2$ (1),

where $\bar{S} = \frac{\sum_{k=0}^{N-1} s_k}{N}$

Equation (1) is not convenient for moving statistics calculations

Therefore equation (1) is converted to : $\sigma^2 = \overline{S^2} - \bar{S}^2$ (2),

where $\overline{S^2} = \frac{\sum_{k=0}^{N-1} {s_k}^2}{N}$ and $\bar{S} = \frac{\sum_{k=0}^{N-1} s_k}{N}$

σ^2 - called variance

Baseline Follower

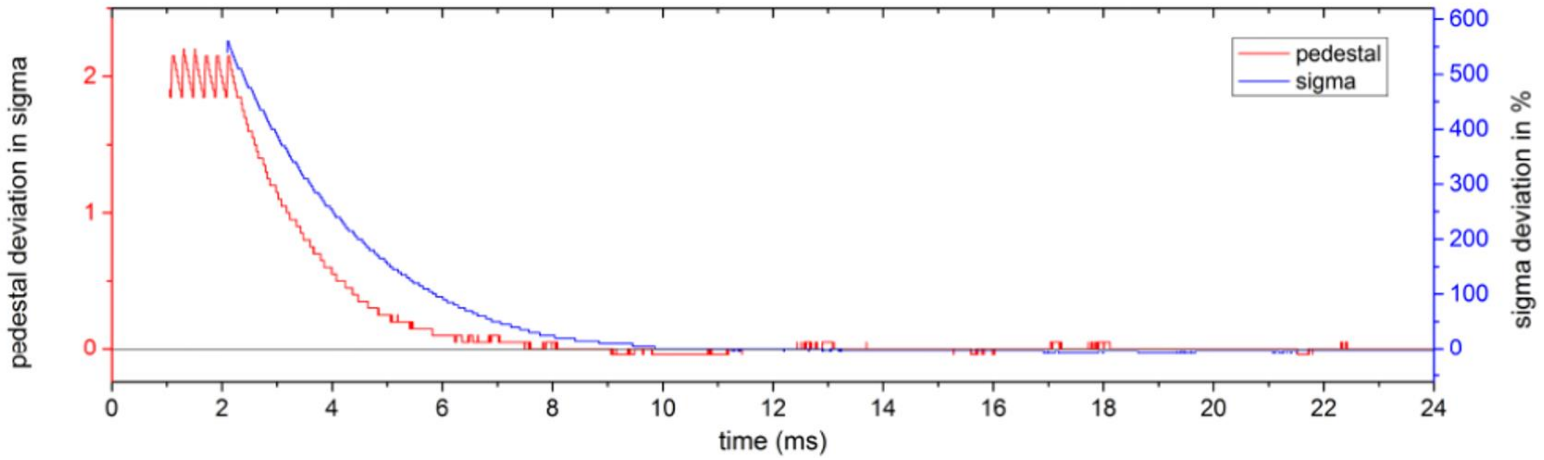
- Continuous calculation of pedestal with limited number of samples N

$\sum_{Ped}$ = $\sum_{Ped}$ - $\bar{S}$ + s_i, where $\bar{S} = \frac{\sum_{Ped}}{N}$ and used instead of s_{i-N}

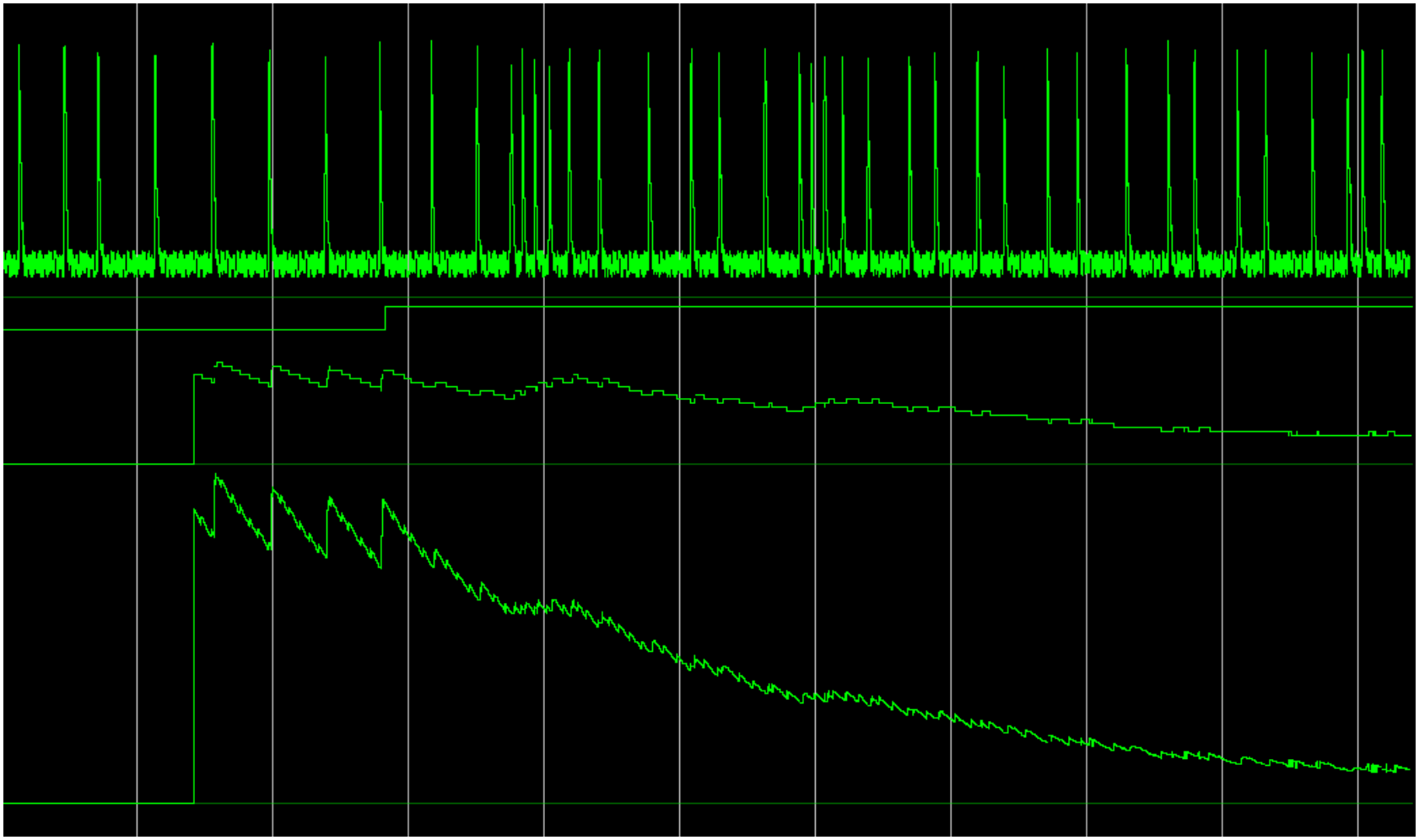
- Continuous variance calculation

$\overline{S^2} = \overline{S^2} - \frac{\overline{S^2}}{N} + \frac{{s_i}^2}{N}$ $\sum_{sqr} = \mathrm{N} \cdot \overline{S^2} = \mathrm{N} \cdot \overline{S^2} - \overline{S^2} + {s_i}^2$ (3)

$\sigma^2 = \frac{\sum_{sqr}}{N} - (\frac{\sum_{Ped}}{N})^2$ (4)



Simulation of Pedestal and Variance Calculation



Moving Average Filter

New sample $v_i = \sum_{j=0}^{M-1} s_{i+j}/M$, noise : $\sigma = \frac{\sigma}{\sqrt{M}}$

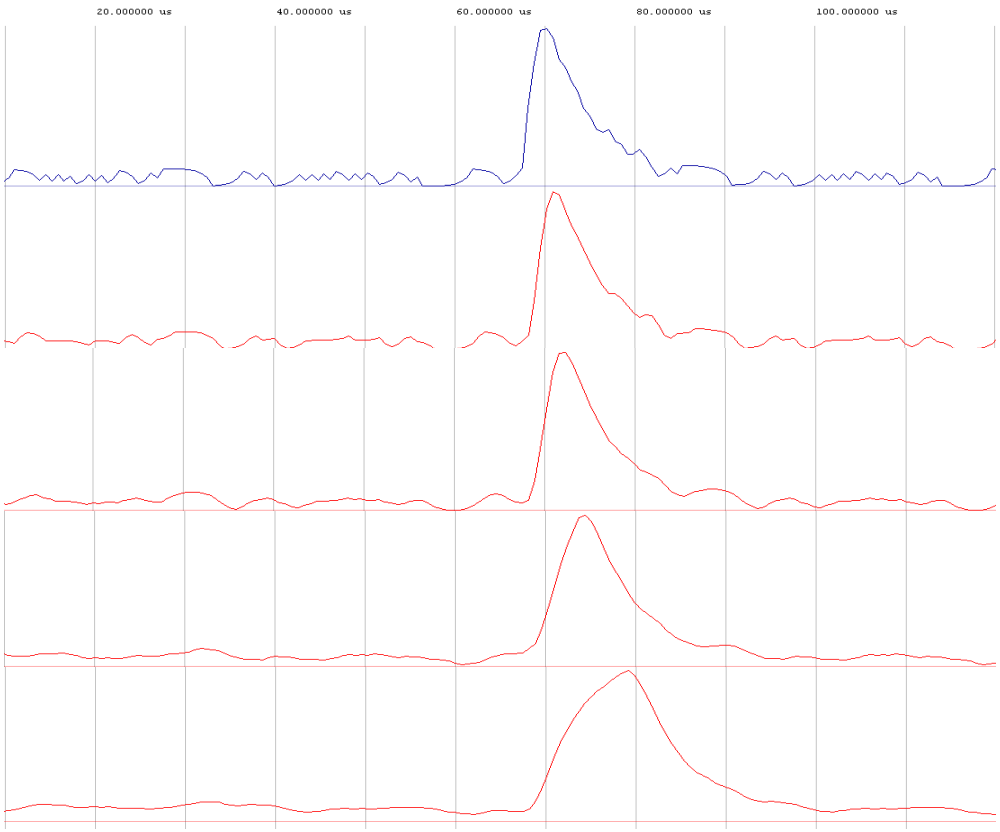
M=1 $\sigma = \sigma$

M=2 $\sigma = \frac{\sigma}{\sqrt{2}}$

M=4 $\sigma = \frac{\sigma}{2}$

M=8 $\sigma = \frac{\sigma}{\sqrt{8}}$

M=16 $\sigma = \frac{\sigma}{4}$



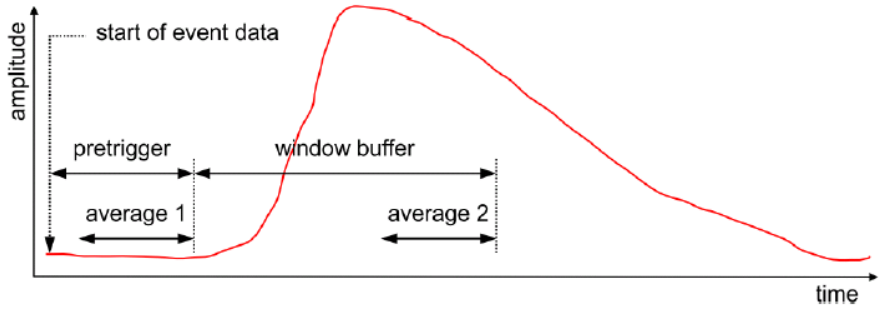
Signal Detection

Different algorithms :

1. Amplitude over threshold: $s_i > \text{thr}$
2. Window over threshold: $\sum \frac{s_i}{N} > \text{thr}$

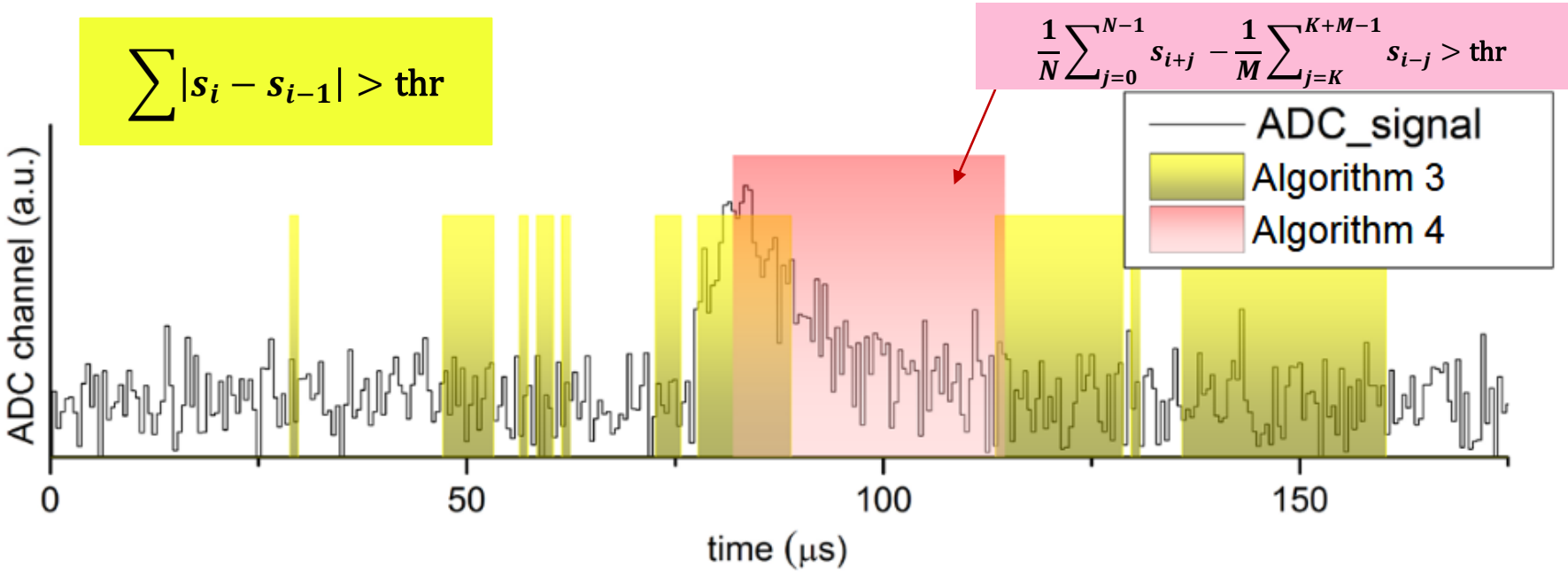
3. Difference between consecutive samples over threshold:
$$\sum |s_i - s_{i-1}| > \text{thr}$$

4. Window over baseline:



5. For baseline follower and continuous sigma calculation:
$$(|s_i - \bar{s}| > x \cdot \sigma) \wedge (|s_{i+1} - \bar{s}| > x \cdot \sigma) \wedge (|s_{i+2} - \bar{s}| > x \cdot \sigma) \wedge \cdots \wedge (|s_{i+n} - \bar{s}| > x \cdot \sigma)$$

Comparison Between Algorithms



Areas where trigger condition is fulfilled are highlighted. S/N = 6

Parameter for algorithm 3: N = 15

Parameter for algorithm 4: length of averaging windows = 16, distance = 30

Signal Feature Extraction

What we want to know about signal for further analysis?

Signal Amplitude – energy released in detector => energy lost by particle

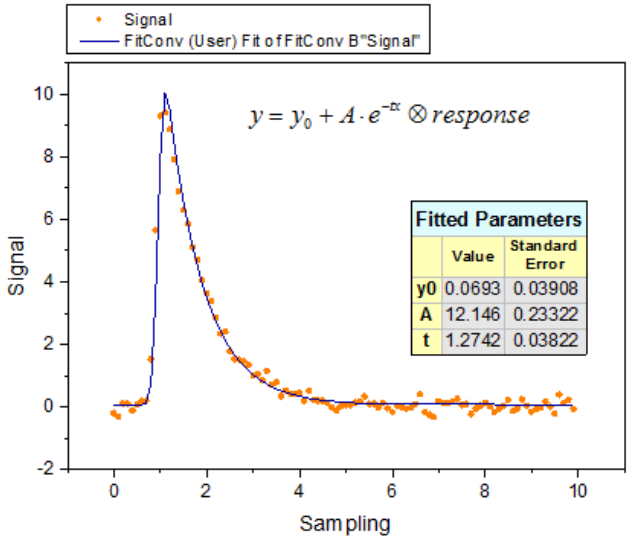
Signal Time – when signal occurred => to synchronize with other detectors

Motivation

- Instead of signal samples transmit Signal Amplitude and Signal Time
- Reduce amount of data for transmission

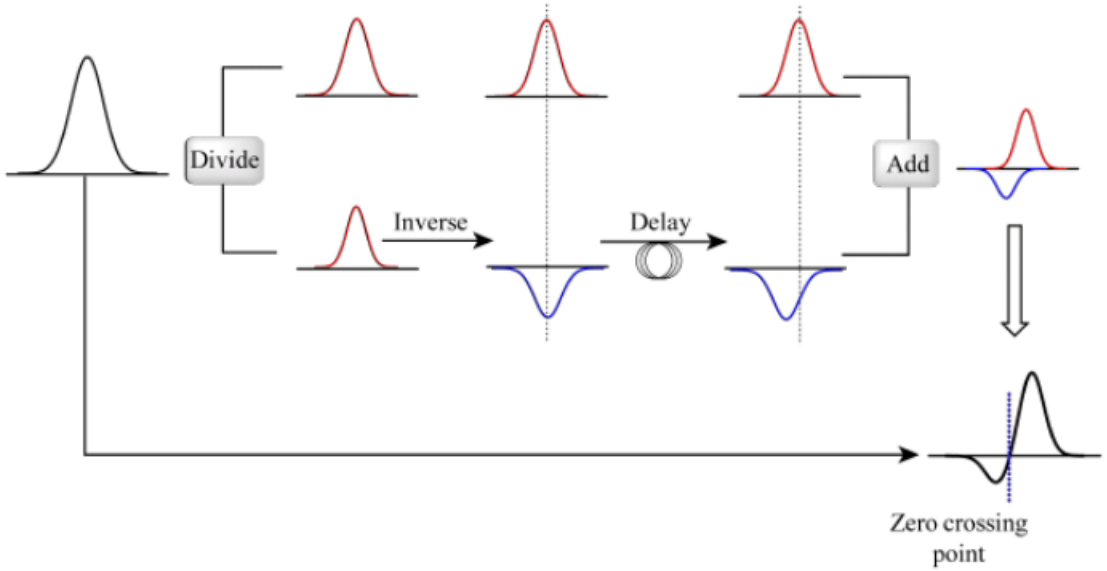
Amplitude Extraction algorithms:

- Sample with maximum amplitude
- Signal integral : $\sum(s_i - \bar{S})$
- Function fit
  - Most precise but requires a lot of resources
- Advanced digital filters FFT, FIR



Signal Time Extraction – Constant Fraction Discriminator

- Difference of two signals B_i
  - Scaled samples $f \cdot s_i$
  - Delayed samples s_{i-t}
- Zero crossing defines signal time
  - Coarse time = i if $B_i < 0$ and $B_{i+1} > 0$
  - Fine time $dt = \frac{B_i}{B_i - B_{i+1}} \cdot t_{clk}$



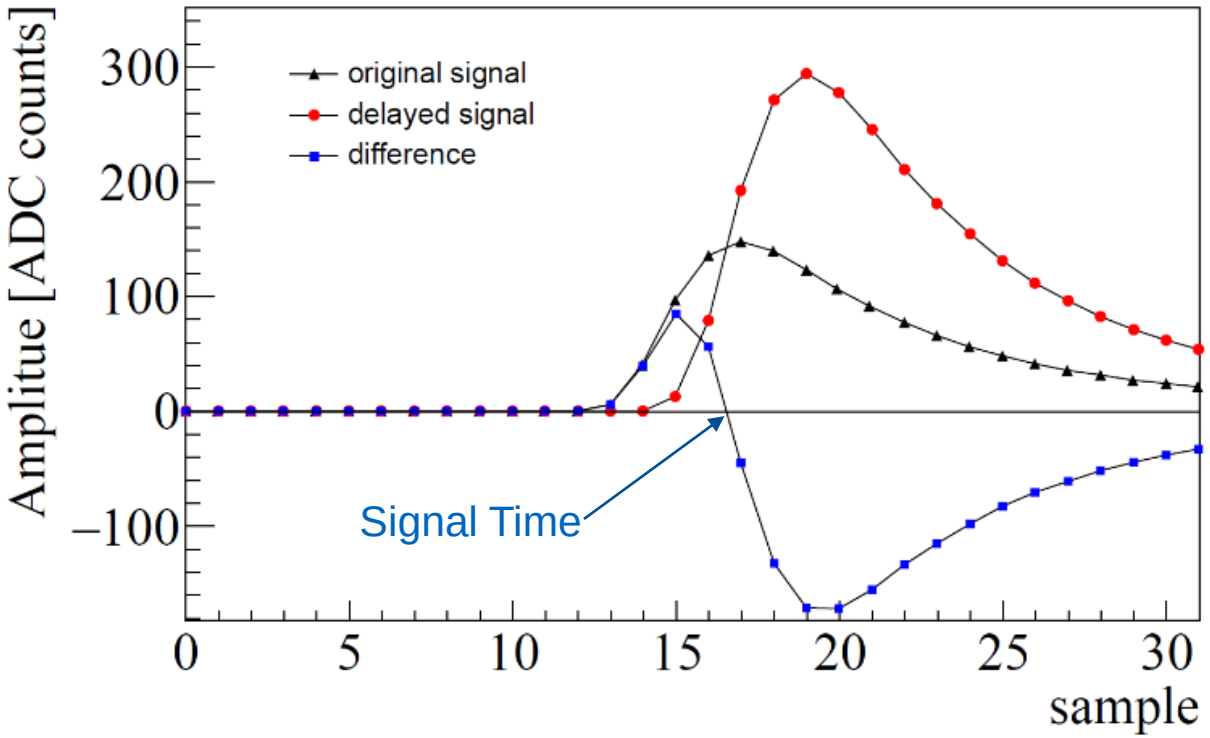
Digital Constant Fraction Discriminator

Additional signal compared to original:

- Delay of 2 samples
- scaled

Time measurement:

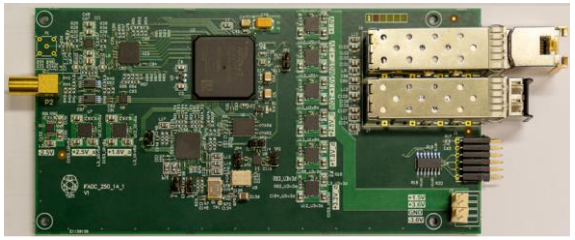
- Subtraction of delayed signal from original
- Interpolation of zero crossing



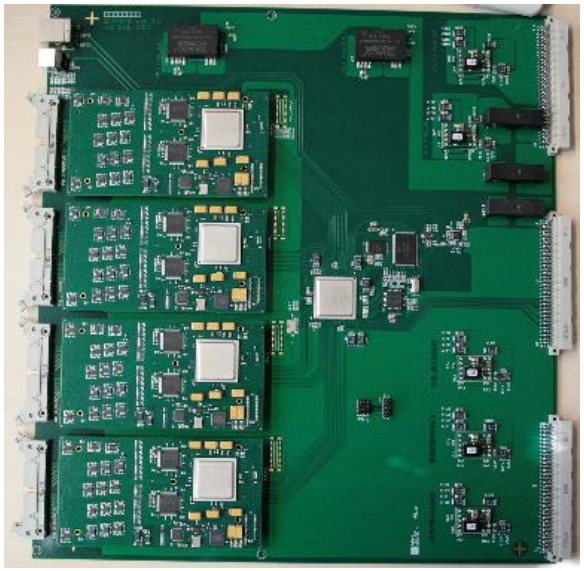
Commercial and Custom ADC and TDC Modules

64ch 200ps, 32ch 100 ps

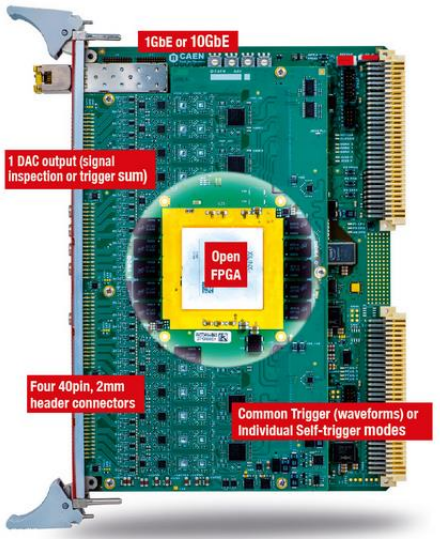
1ch , 14b 250 MHz



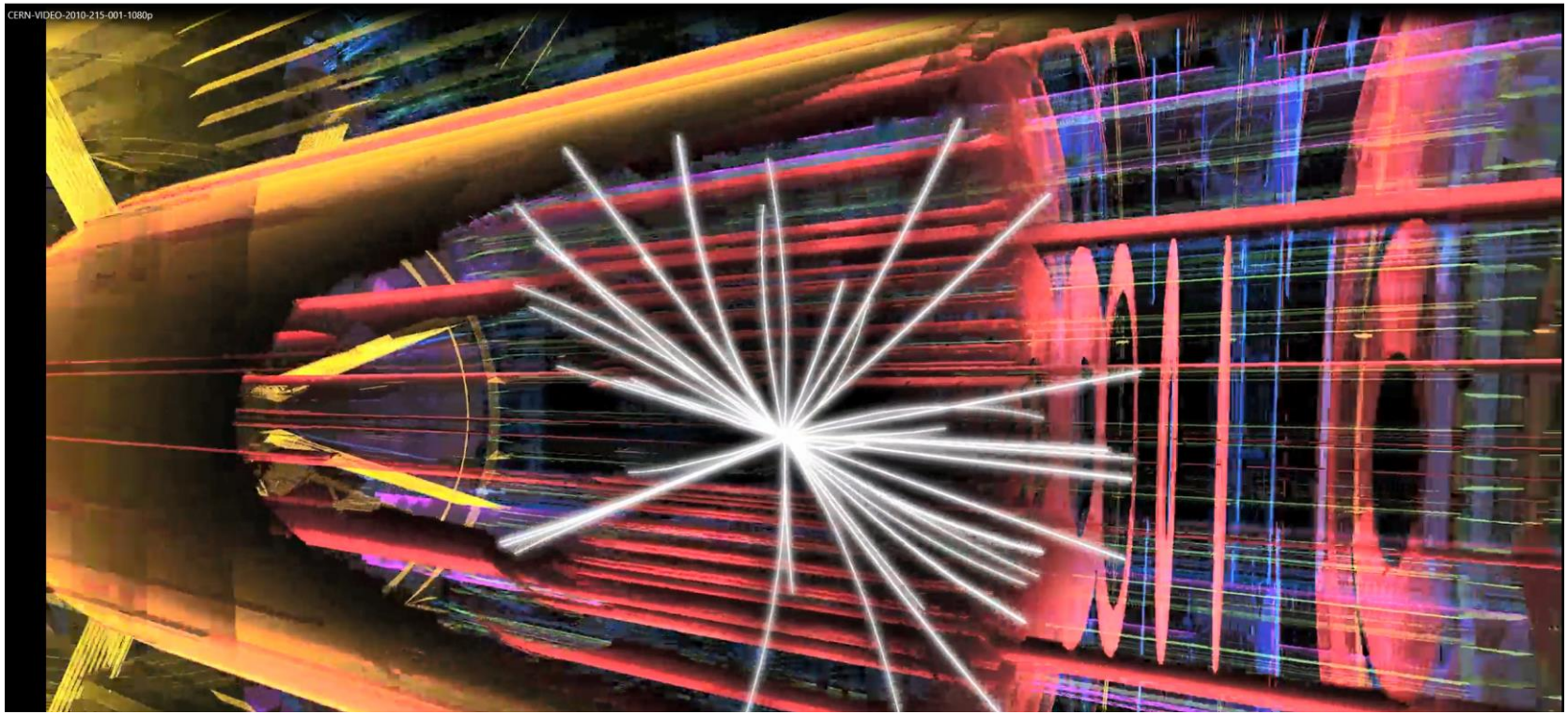
64ch , 12b 80 MHz



64ch , 16b 125 MHz



Z Boson decay



Screenshot of CERN video

https://home.cern/resources/video/physics/z-e-e-collision-event-animation
https://home.cern/resources/video/experiments/cms-event-collision-simulation-13-tev