Contribution ID : **595** Type : **not specified**

Lab activities with tutors: Embedded processor design on the FPGA-based hardware platform (part II)

Thursday, 11 February 2021 14:00 (3:00)

Content

Summary

Presenter(s) : MLADEN BOGOVAC (IAEA, Austria); VLADIMIR RAJOVIC (University of Belgrade, Serbia); NIKOLA JOVALEKIC (TTTech Computertechnik AG, Austria)

Session Classification : Session 28: Laboratory Activities