

Joint ICTP-IAEA School on FPGA-based SoC and its Applications for Nuclear and Related Instrumentation



25 January - 19 February 2021
An ICTP-IAEA Virtual Meeting
Trieste, Italy

Further information:
<http://indico.ictp.it/event/9443/>
smr3562@ictp.it

Marija Chaushevskaja
Jozef Stefan Institute – Ljubljana, Slovenia

Zynq Processing System

- Complete ARM – based PS
- Combines a dual-core ARM Cortex-A9 with a traditional (FPGA).
- Two hard processors
- Programmable logic (PL)
- PS Main components:
 - I/O peripherals
 - Memory interfaces
 - Timers
 - DMA
 - General Interrupt Controller

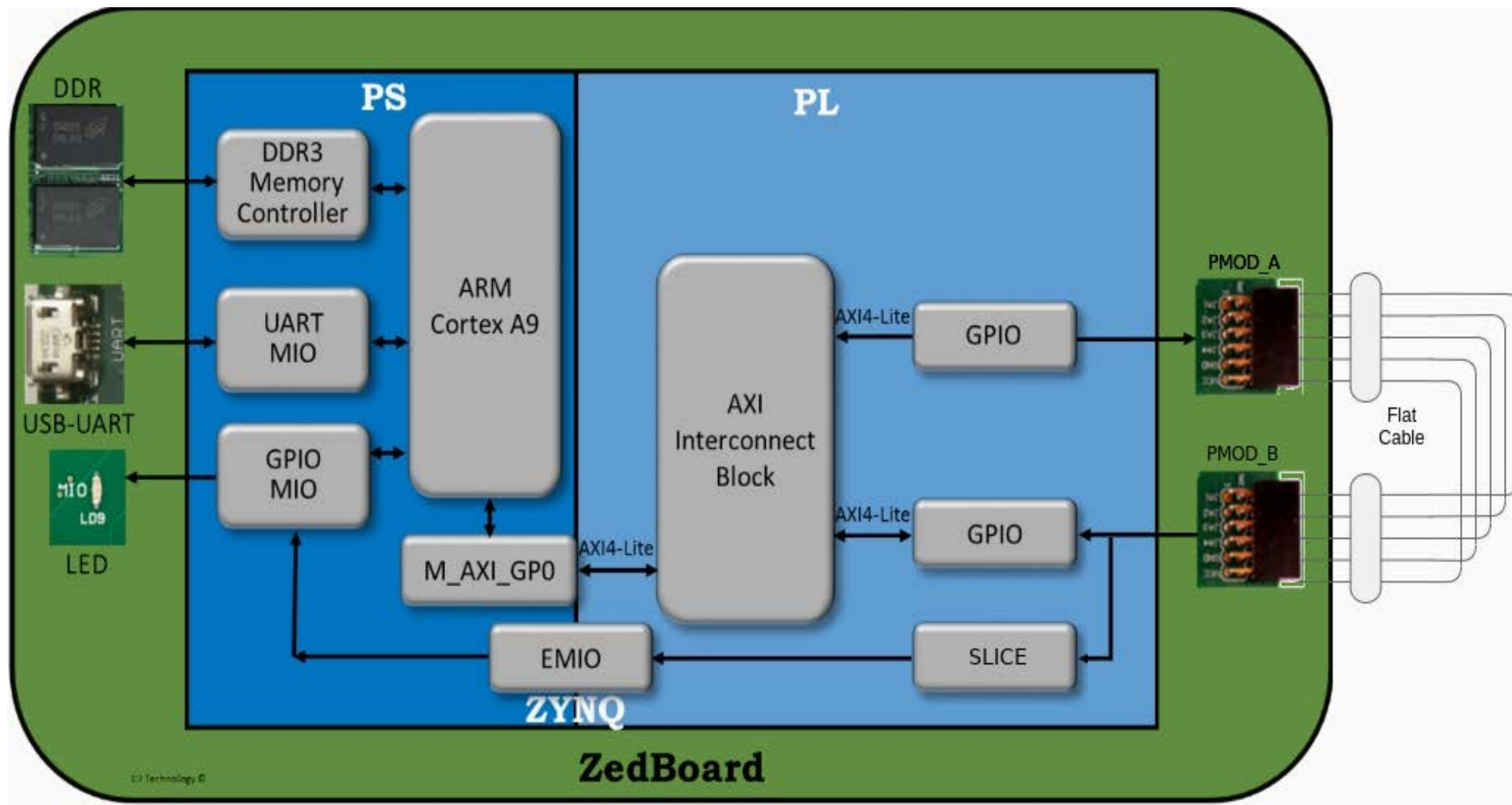


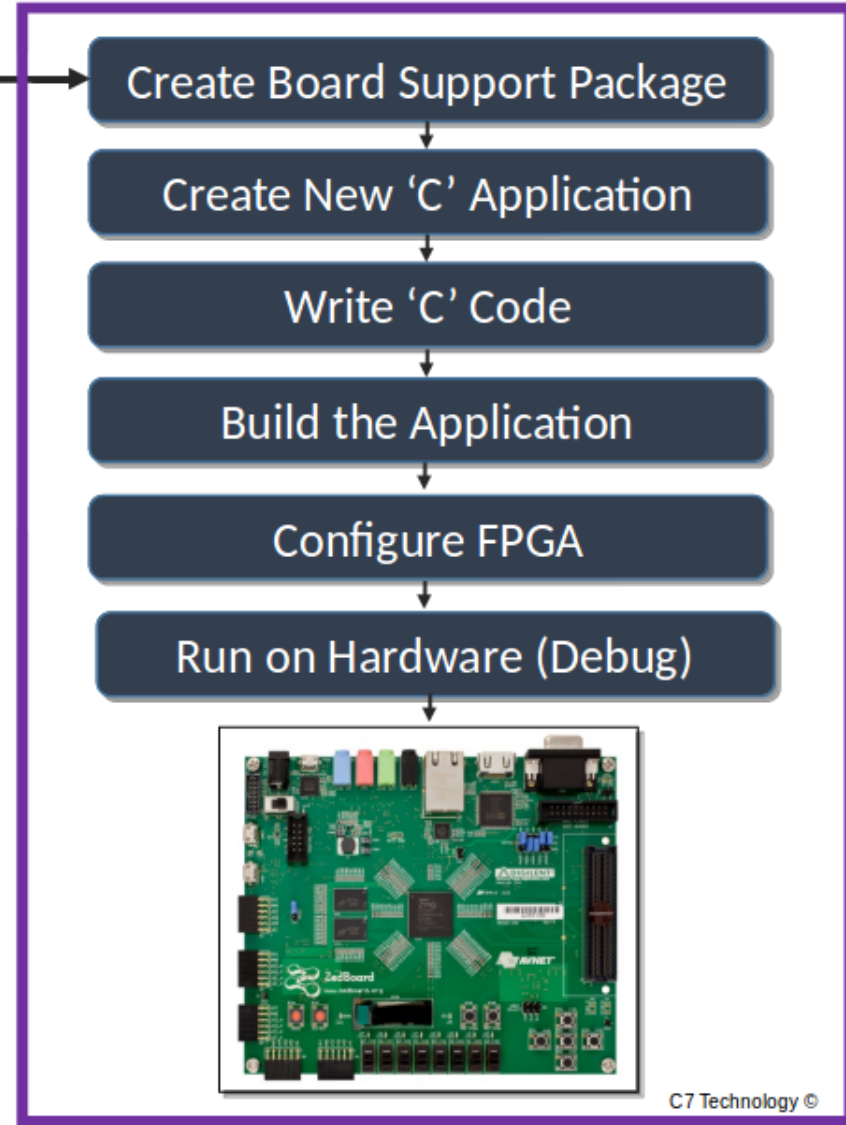
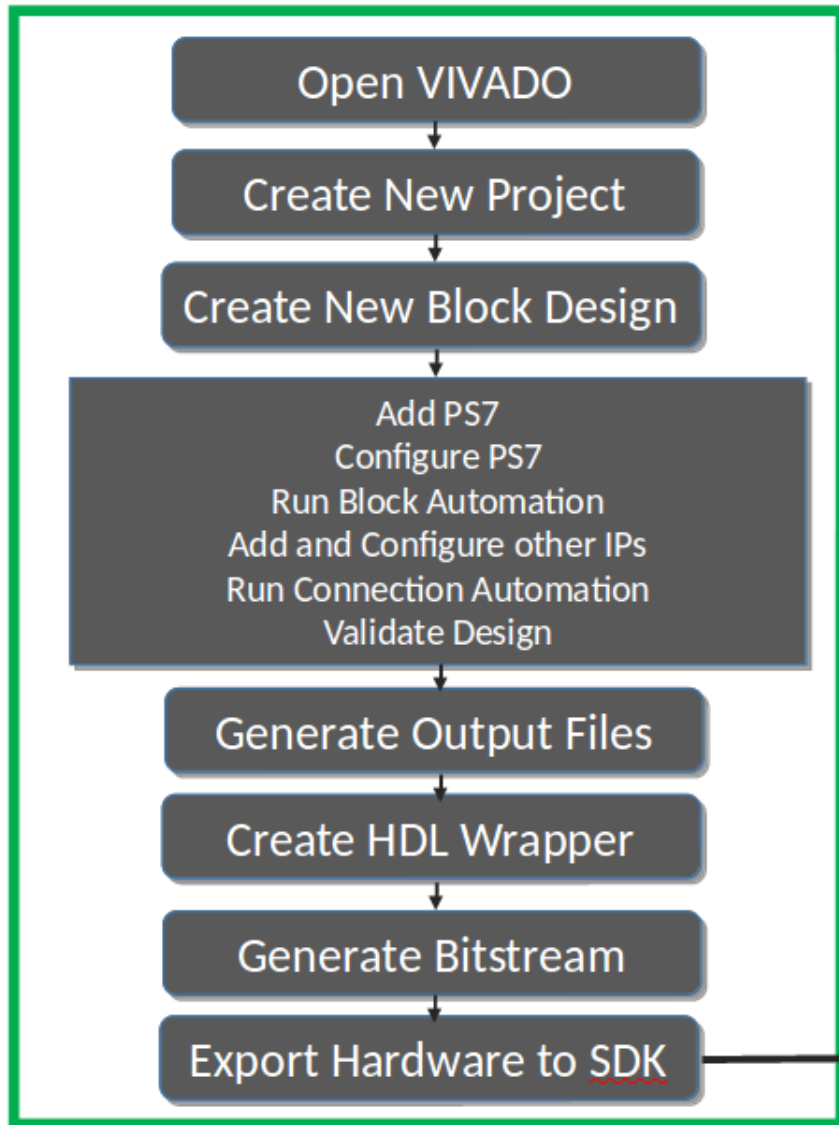
Laboratory 2: GPIO IP Cores



Lab2 guide:

- Create a system with two GPIOs IP Cores
- One GPIO IP -> output
 - Output -> PMOD-A Header of ZedBoard
- One GPIO IP -> input
 - Input -> PMOD-B Header of ZedBoard
- Write an application in 'C' code in the SDK environment
- To run in PS





Thank you for your attention !