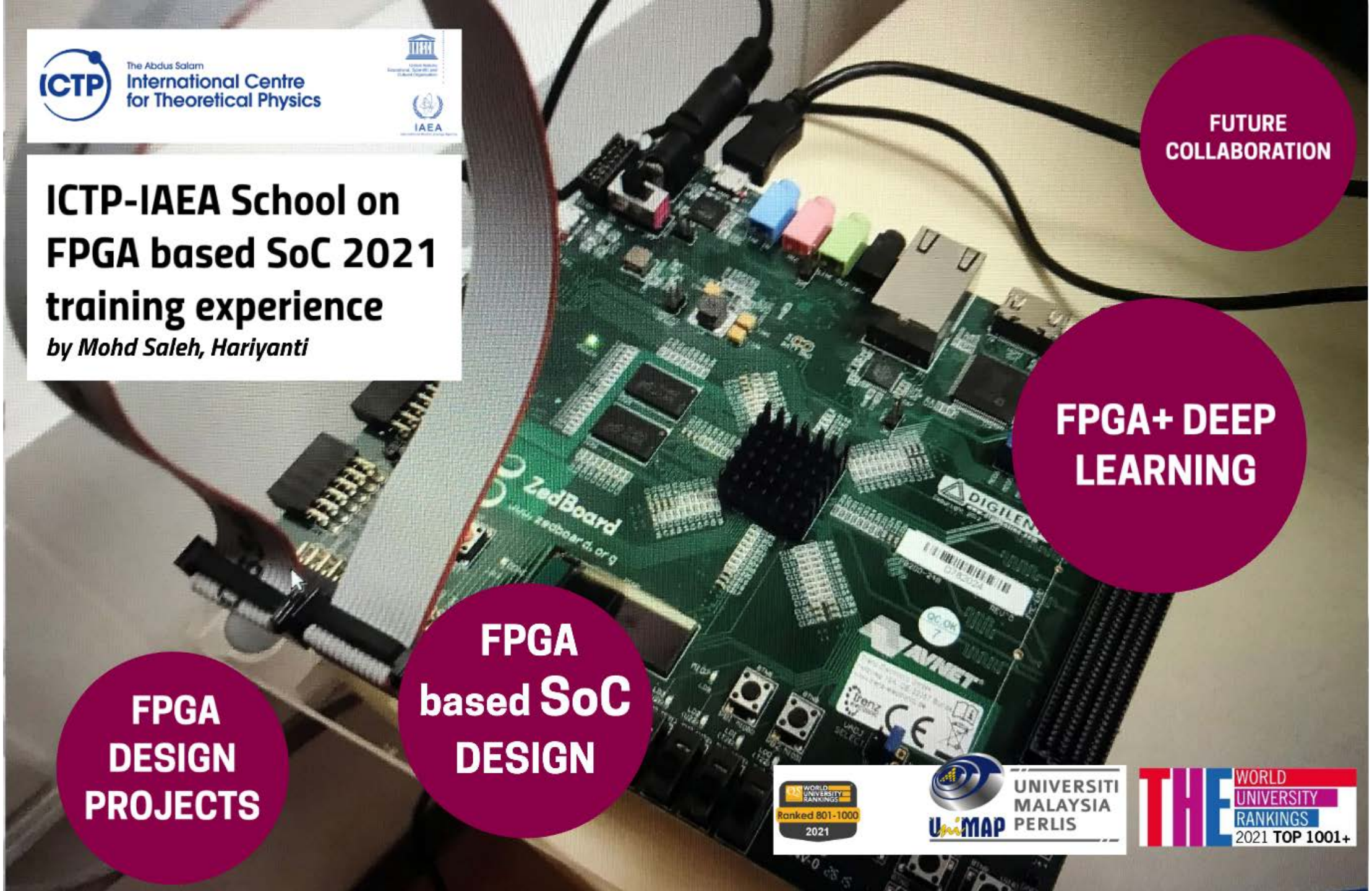


The Abdus Salam International Centre for Theoretical Physics

IAEA

# ICTP-IAEA School on FPGA based SoC 2021 training experience

*by Mohd Saleh, Hariyanti*

Ranked 801-1000 2021

UNIVERSITI MALAYSIA PERLIS

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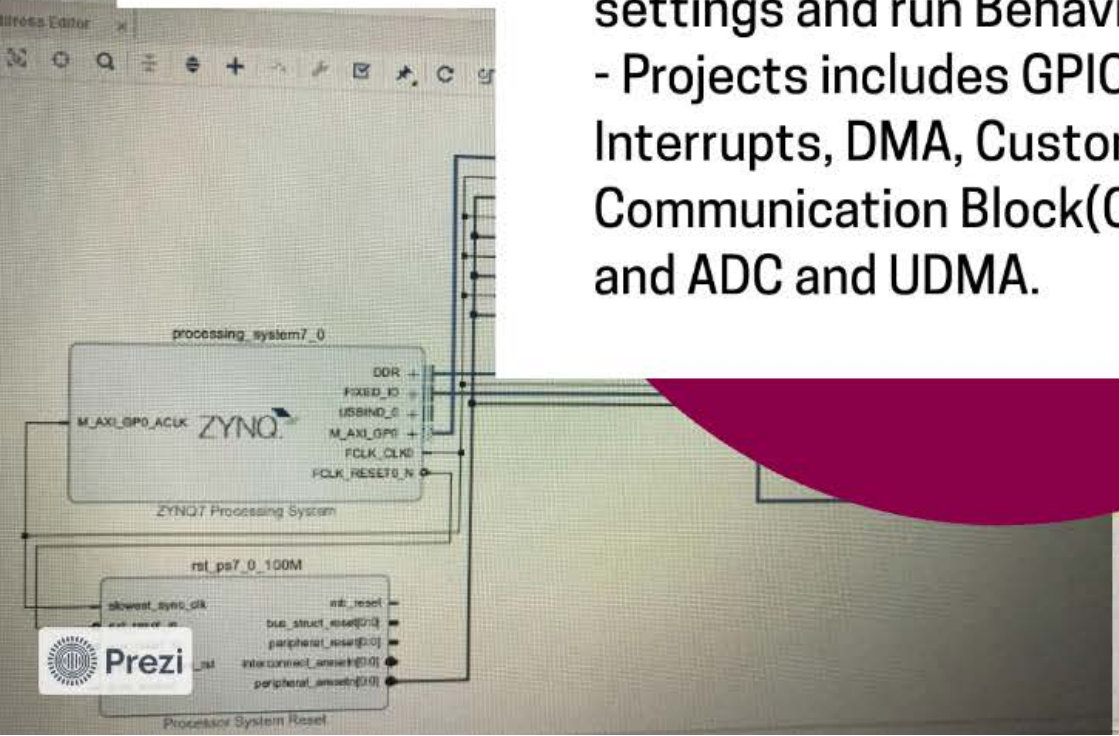
THE WORLD UNIVERSITY RANKINGS 2021 TOP 1001+

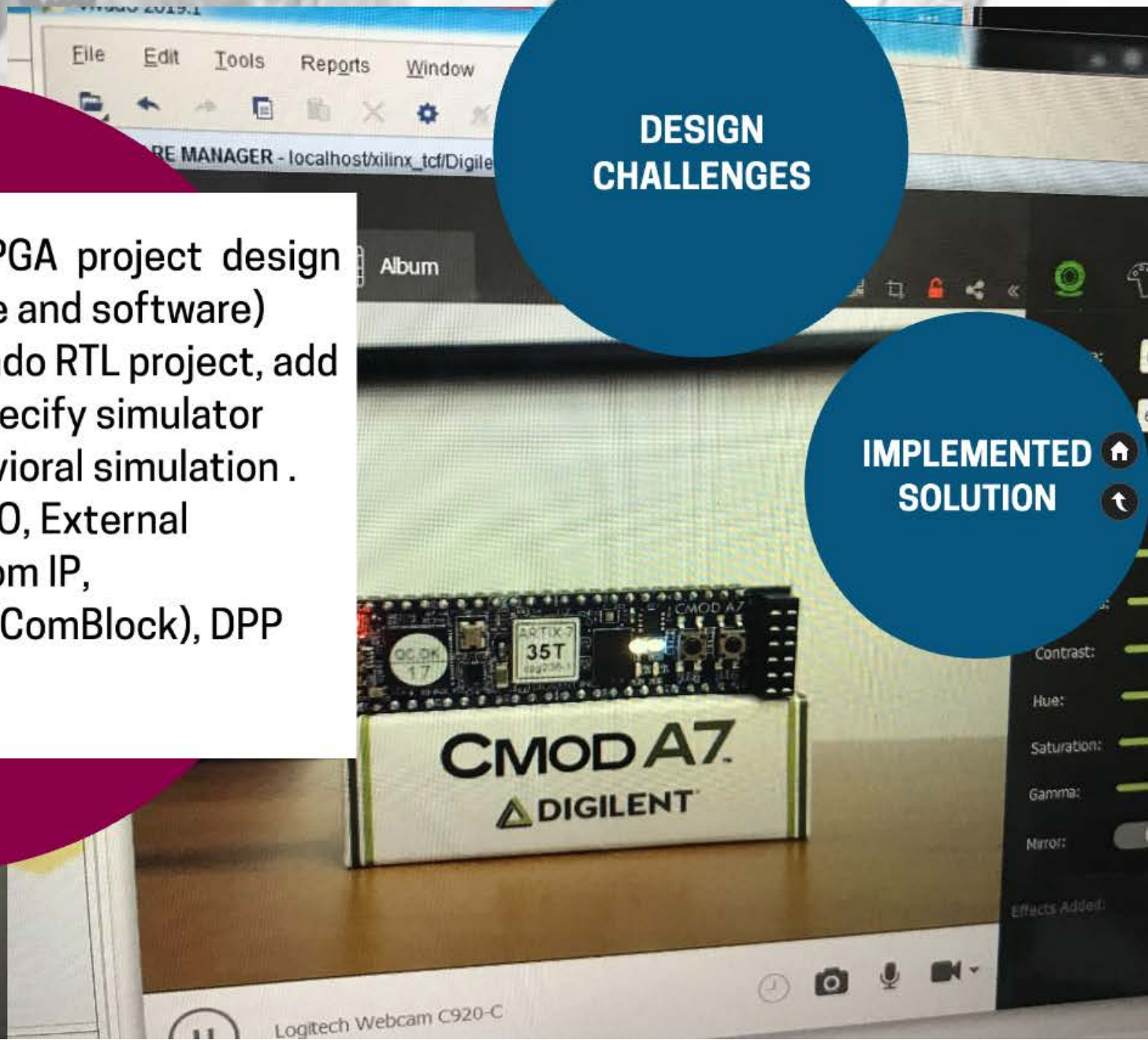
# FPGA DESIGN PROJECTS

- We have learned FPGA project design using vivado.(hardware and software)
- We have created Vivado RTL project, add simulation sources, specify simulator settings and run Behavioral simulation .
- Projects includes GPIO, External Interrupts, DMA, Custom IP, Communication Block(ComBlock), DPP and ADC and UDMA.

DESIGN CHALLENGES

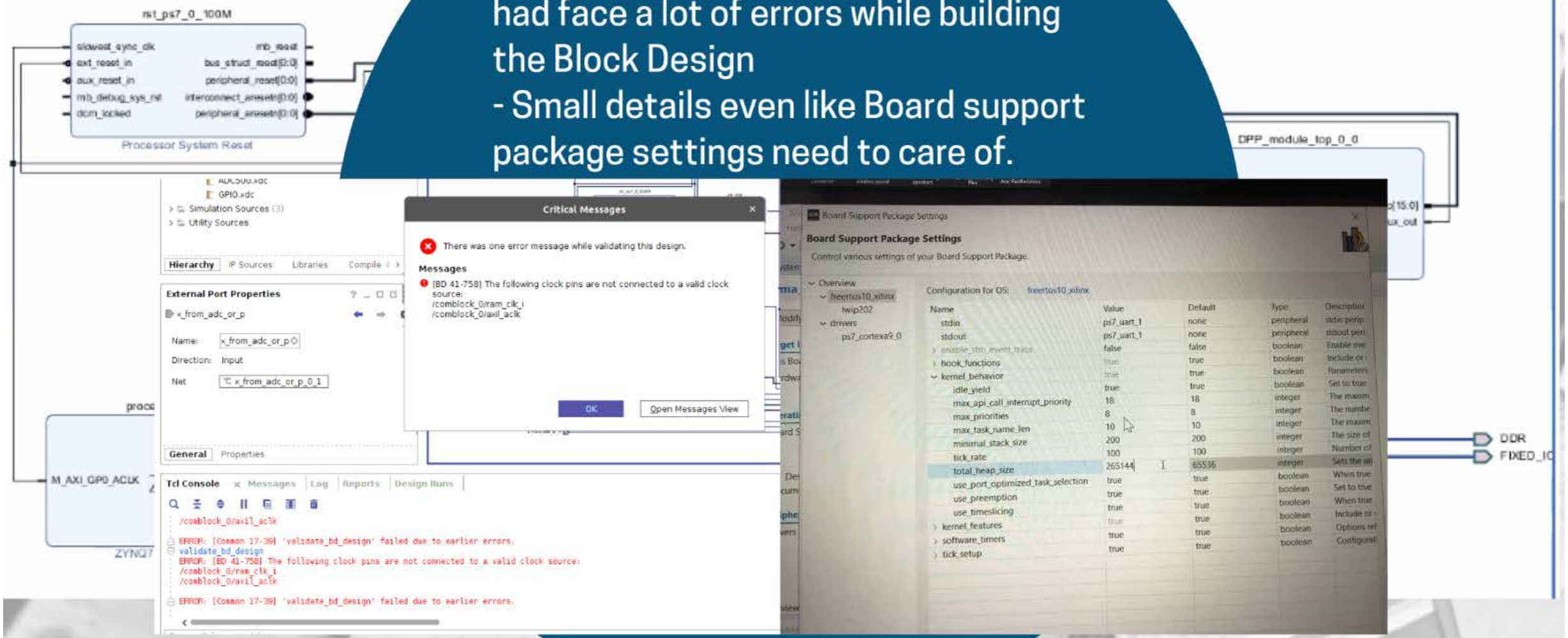
IMPLEMENTED SOLUTION



## DESIGN CHALLENGES

- Not aware of block connection and had face a lot of errors while building the Block Design
- Small details even like Board support package settings need to care of.

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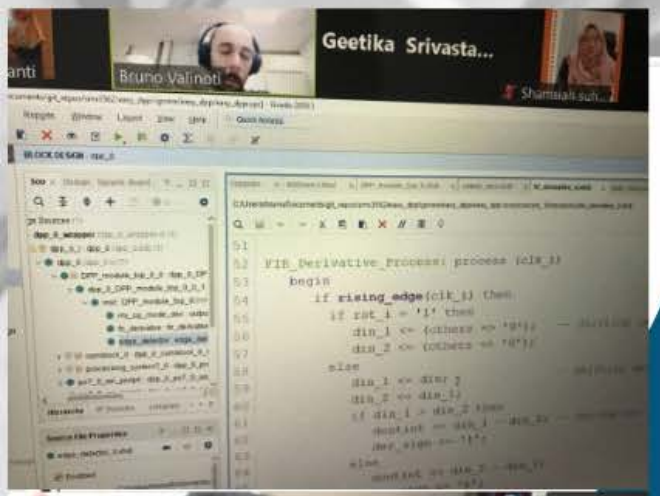
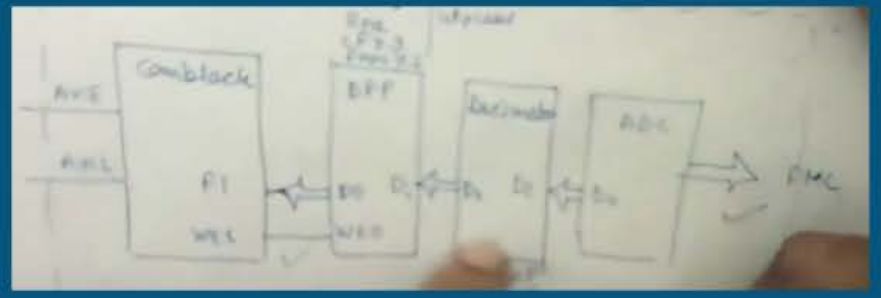
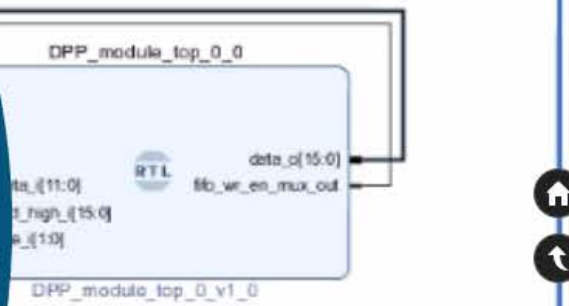


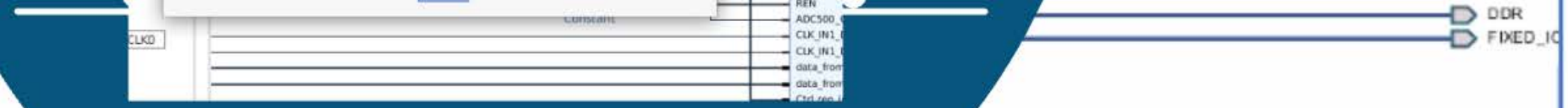

## SOLUTION

- Understand the block design
- Validate Design and get instructor help



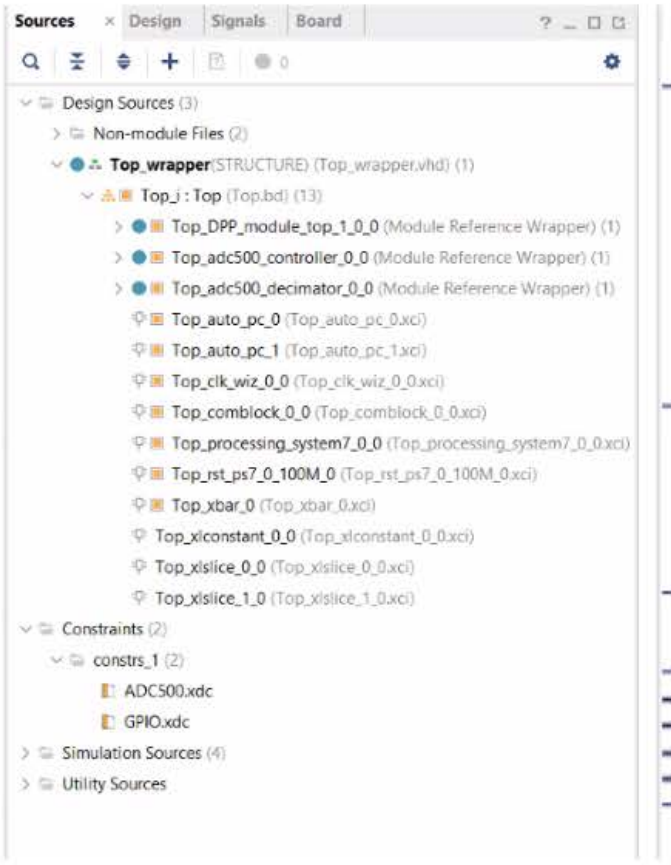


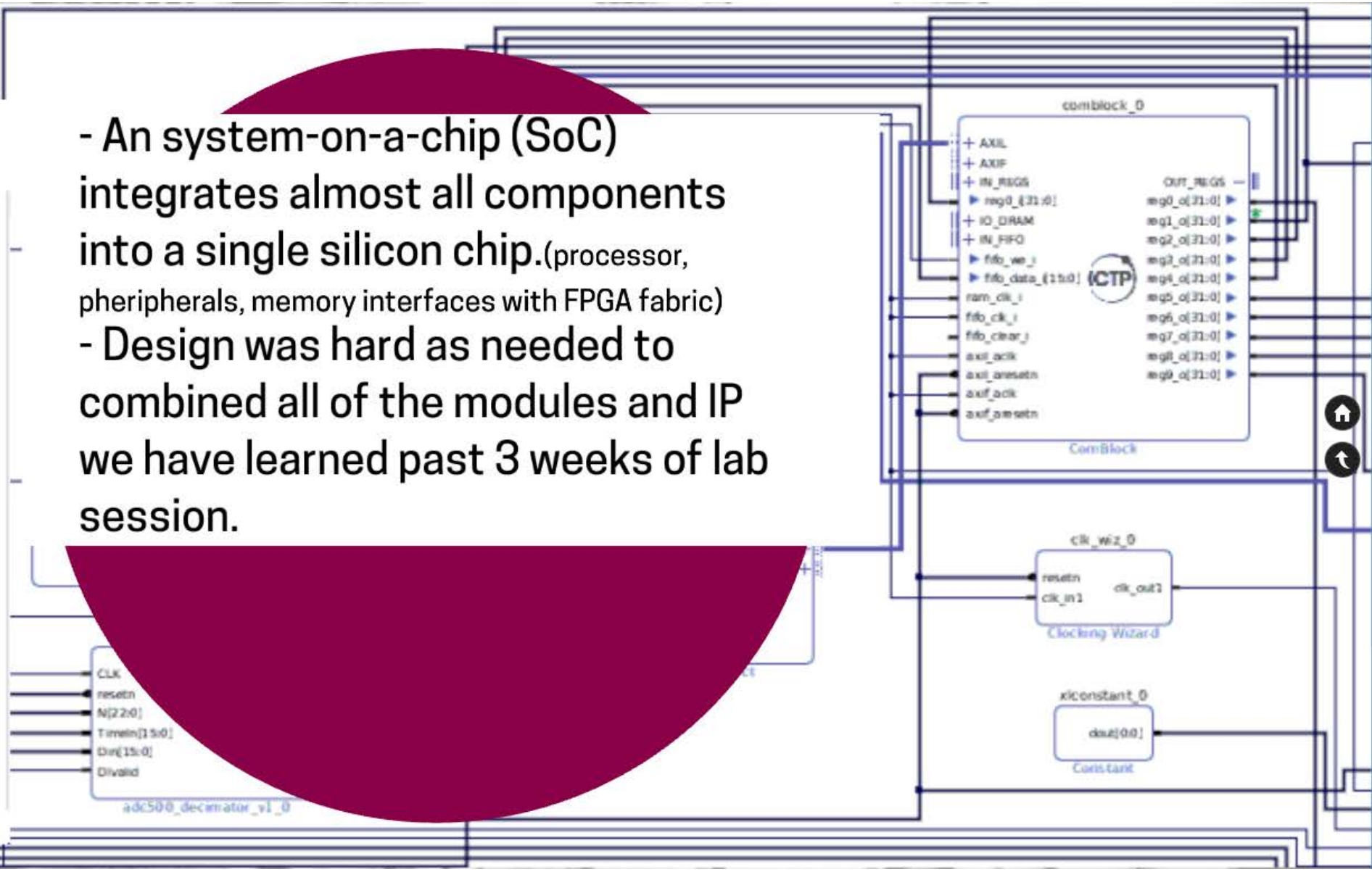


# FPGA based SoC Design

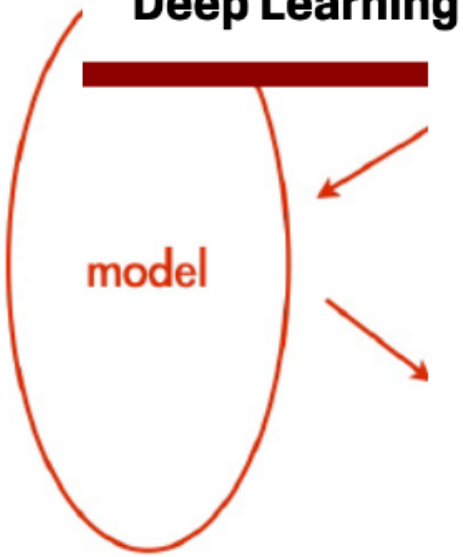
- An system-on-a-chip (SoC) integrates almost all components into a single silicon chip.(processor, pheripherals, memory interfaces with FPGA fabric)
- Design was hard as needed to combined all of the modules and IP we have learned past 3 weeks of lab session.



# hls4ml

**FPGA+**
**Deep Learning**




Usual machine le
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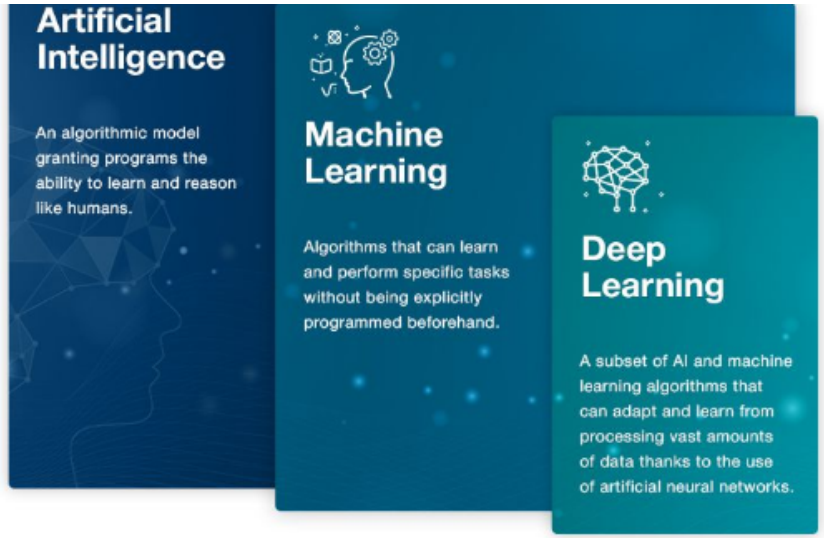
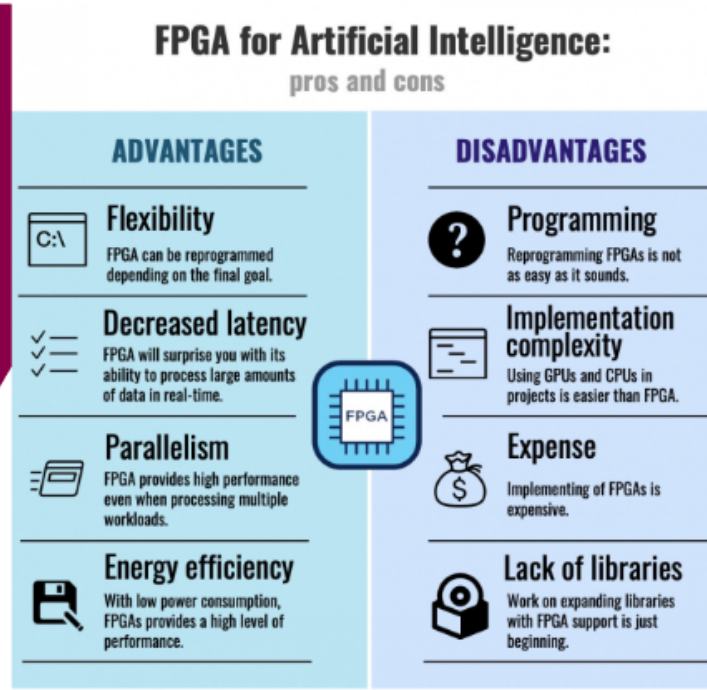
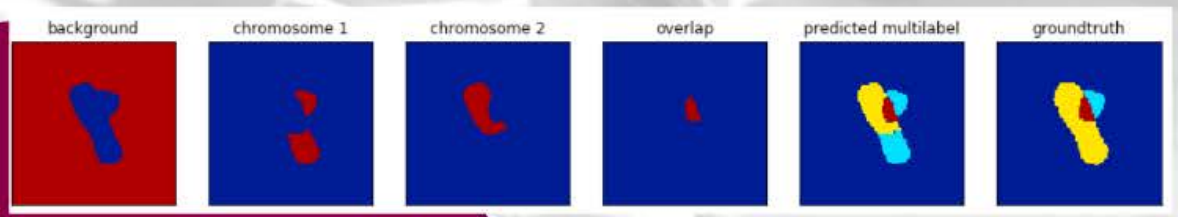
- The biggest potential of FPGAs is in the area of deep learning due to its:
  - >FLEXIBILTY
  - >DECREASED LATENCY
  - >PARALLELISM
  - >ENERGY EFFICIENCY
- Deep Learning can break complex patterns into simpler ones.

on
pipeline




## FUTURE COLLABORATION

- My research area: Medical Imaging using Deep Learning Algorithm
- Contact me for collaboration on FPGA+ Deep Learning
- email: hariyanti@unimap.edu.my

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