



The Abdus Salam
International Centre
for Theoretical Physics



ICTP-IAEA School on FPGA based SoC 2021 training experience

by Mohd Saleh, Hariyanti

**FUTURE
COLLABORATION**

**FPGA+ DEEP
LEARNING**

**FPGA
DESIGN
PROJECTS**

**FPGA
based SoC
DESIGN**

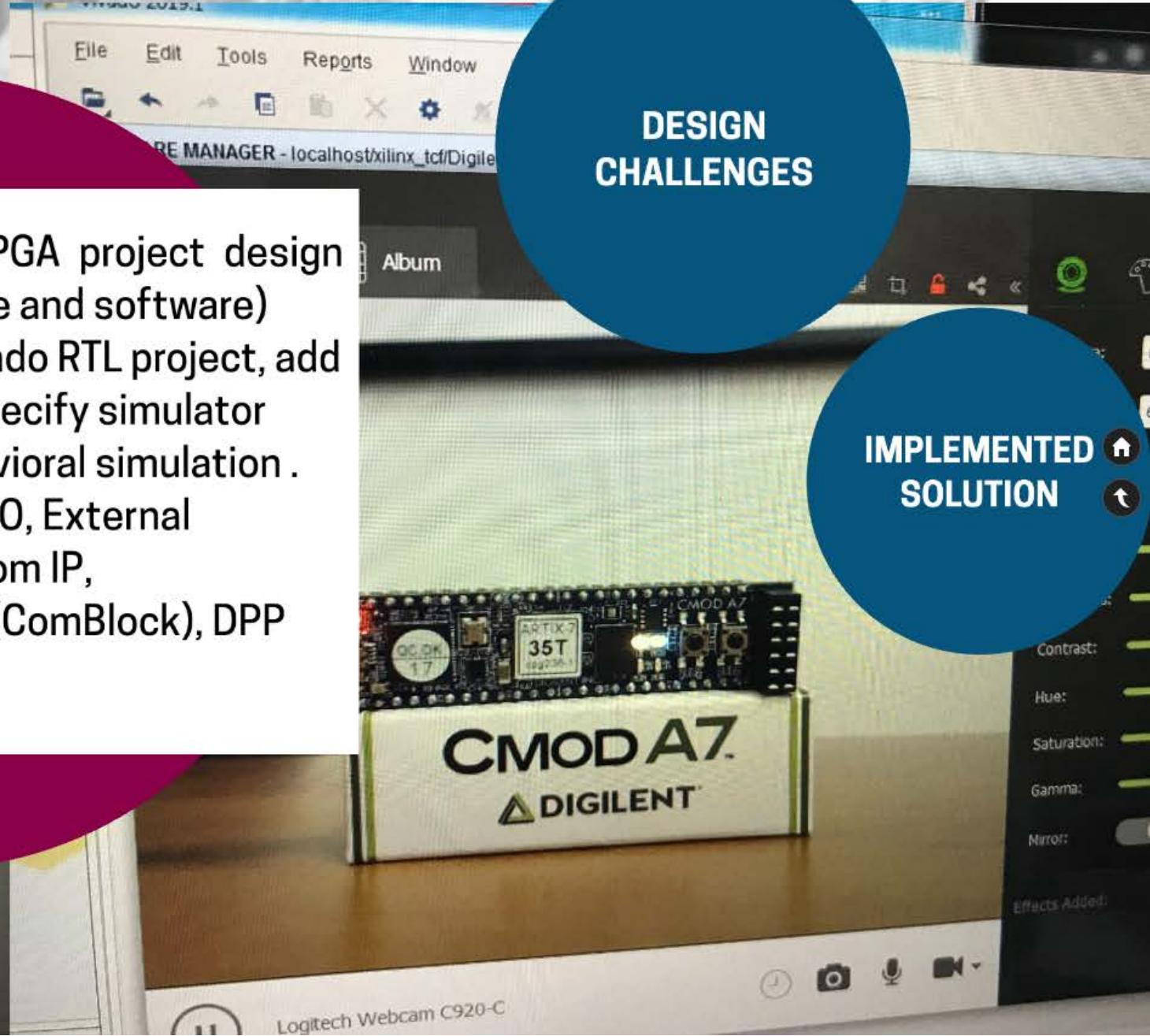
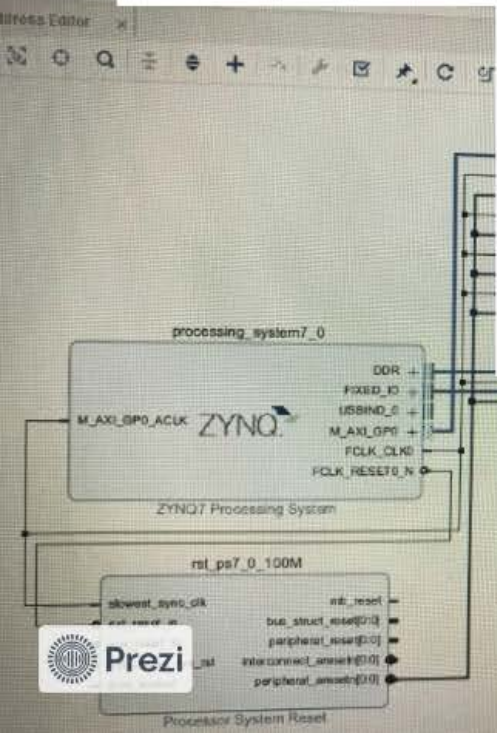


FPGA DESIGN PROJECTS

- We have learned FPGA project design using vivado.(hardware and software)
- We have created Vivado RTL project, add simulation sources, specify simulator settings and run Behavioral simulation .
- Projects includes GPIO, External Interrupts, DMA, Custom IP, Communication Block(ComBlock), DPP and ADC and UDMA.

DESIGN
CHALLENGES

IMPLEMENTED
SOLUTION



DESIGN CHALLENGES

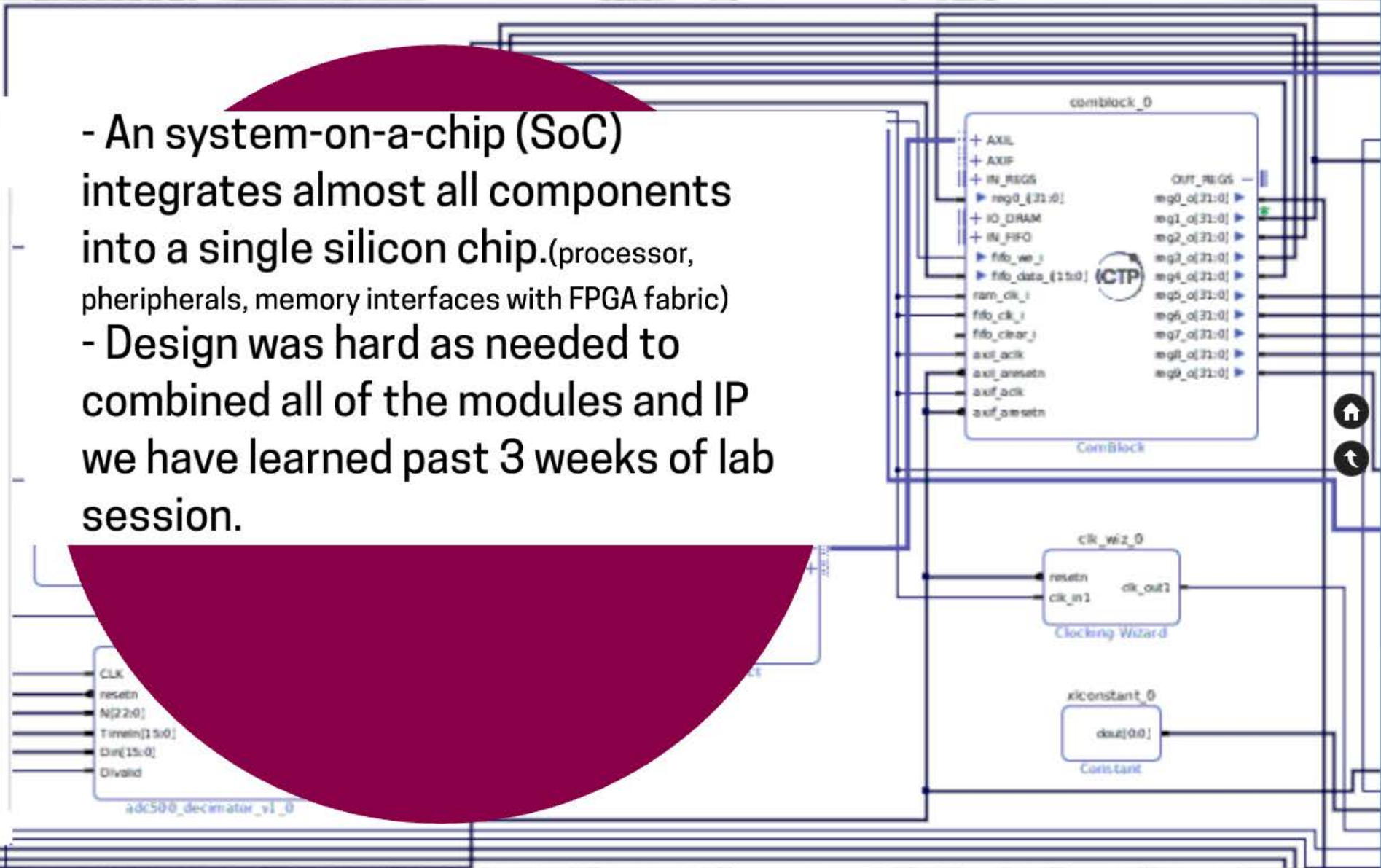
- Not aware of block connection and had face a lot of errors while building the Block Design
- Small details even like Board support package settings need to care of.

The screenshot displays the Xilinx Vivado IDE interface. At the top, a block diagram shows the 'rst_ps7_0_100M' block connected to various signals like 'slowest_sync_clk', 'ext_reset_in', and 'aux_reset_in'. Below this, the 'Processor System Reset' block is visible. The 'External Port Properties' window shows the configuration for 'x_from_adc_or_p_0'. The 'Tcl Console' at the bottom shows error messages: 'ERROR: [Common 17-39] 'validate_bd_design' failed due to earlier errors. validate_bd_design ERROR: [BD 41-758] The following clock pins are not connected to a valid clock source: /comblock_0/rst_clk_1 /comblock_0/axi1_aclk'. A 'Critical Messages' dialog box is open, displaying the error message: 'There was one error message while validating this design. Messages [BD 41-758] The following clock pins are not connected to a valid clock source: /comblock_0/rst_clk_1 /comblock_0/axi1_aclk'. On the right, the 'Board Support Package Settings' window is open, showing configuration for OS: 'freertos10_xilinx'. The table below lists various settings:

Name	Value	Default	Type	Description
stdin	ps7_uart_1	none	peripheral	stdio perip
stdout	ps7_uart_1	none	peripheral	stdio perip
enable_str_event_trace	false	false	boolean	Enable true
hook_functions	true	true	boolean	Include or
kernel_behavior	true	true	boolean	Parameters
idle_yield	true	true	boolean	Set to true
max_api_call_interrupt_priority	18	18	integer	The maxim
max_priorities	8	8	integer	The number
max_task_name_len	10	10	integer	The size of
minimal_stack_size	200	200	integer	The size of
tick_rate	100	100	integer	Number of
total_heap_size	265144	65536	integer	Sets the all
use_port_optimized_task_selection	true	true	boolean	When true
use_preemption	true	true	boolean	Set to true
use_timeslicing	true	true	boolean	When true
kernel_features	true	true	boolean	When true
software_timers	true	true	boolean	Include or
tick_setup	true	true	boolean	Options rel

FPGA based SoC Design

- An system-on-a-chip (SoC) integrates almost all components into a single silicon chip.(processor, peripherals, memory interfaces with FPGA fabric)
- Design was hard as needed to combined all of the modules and IP we have learned past 3 weeks of lab session.



hls4ml

FPGA+ Deep Learning

model

Usual machine learning software workflow

Keras
TensorFlow

- The biggest potential of FPGAs is in the area of deep learning due to its:
 - > FLEXIBILITY
 - > DECREASED LATENCY
 - > PARALLELISM
 - > ENERGY EFFICIENCY
- Deep Learning can break complex patterns into simpler ones.

Artificial Intelligence

An algorithmic model granting programs the ability to learn and reason like humans.



Machine Learning

Algorithms that can learn and perform specific tasks without being explicitly programmed beforehand.



Deep Learning

A subset of AI and machine learning algorithms that can adapt and learn from processing vast amounts of data thanks to the use of artificial neural networks.

FPGA for Artificial Intelligence: pros and cons

ADVANTAGES



Flexibility

FPGA can be reprogrammed depending on the final goal.



Decreased latency

FPGA will surprise you with its ability to process large amounts of data in real-time.



Parallelism

FPGA provides high performance even when processing multiple workloads.



Energy efficiency

With low power consumption, FPGAs provides a high level of performance.



DISADVANTAGES



Programming

Reprogramming FPGAs is not as easy as it sounds.



Implementation complexity

Using GPUs and CPUs in projects is easier than FPGA.



Expense

Implementing of FPGAs is expensive.



Lack of libraries

Work on expanding libraries with FPGA support is just beginning.



FUTURE COLLABORATION

- My research area: Medical Imaging using Deep Learning Algorithm
- Contact me for collaboration on FPGA+ Deep Learning
- email: hariyanti@unimap.edu.my

