



ICTP-IAEA project presentation

By

Gisele Beatrice Sonfack, PhD in Electronics Post-doc Reseacher,
Polytechnics Orléns, France

Lecturer at Unniversity of Douala, Cameroon

Outline

1. why did i apply for this school?
2. What have I learned?
3. My expectations



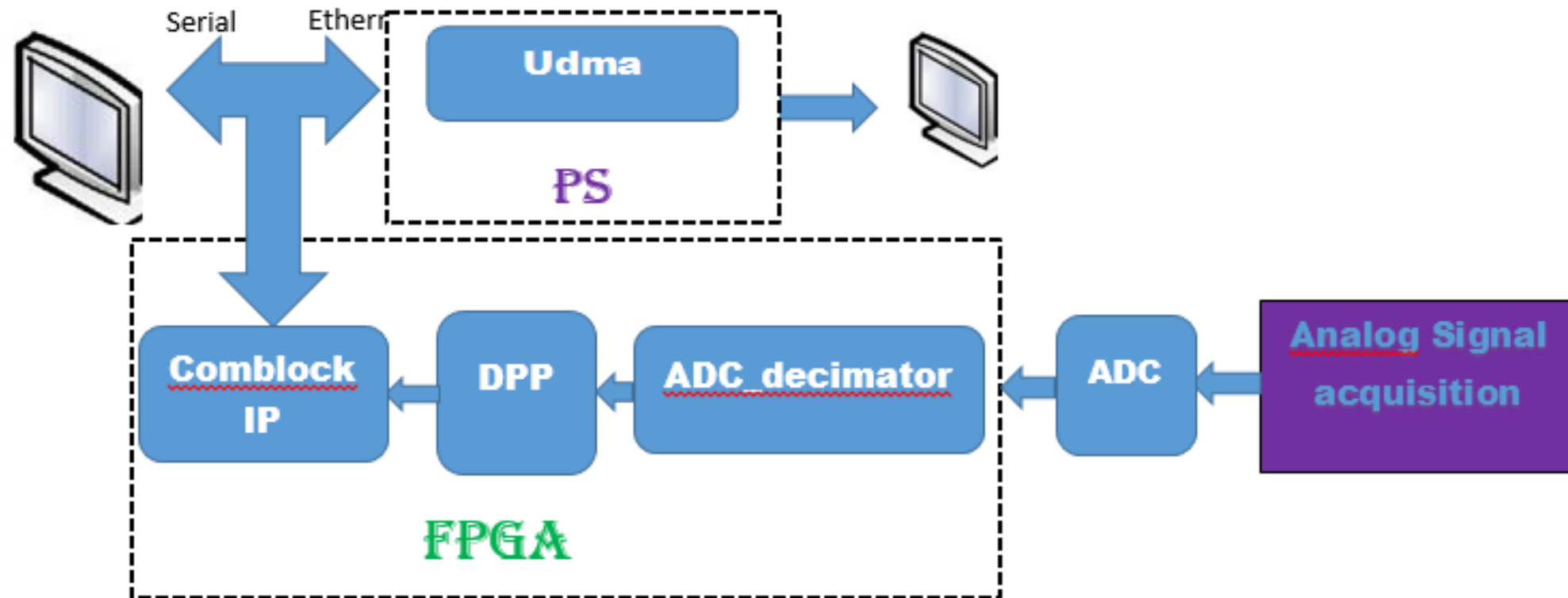
Why did i apply for this opportunity?

Previous work and Current projects

- ▶ PhD thesis: new technique of analog-to-digital conversion (ADC), based on FPGA-assisted optimal duty cycle modulation (ODCM).
- ▶ Current work (post-doc) : Electric signal analysis and processing (identification of the consumers on the electricity network)

What i have learned

➤ FPGA-based real time data acquisition

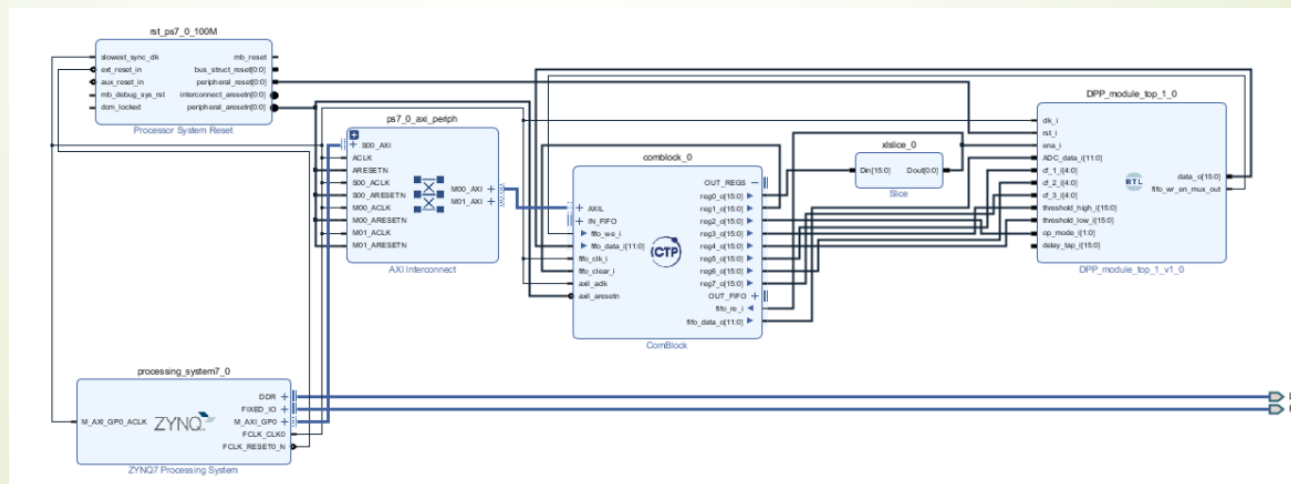


What i have learned

Digital pulse processing

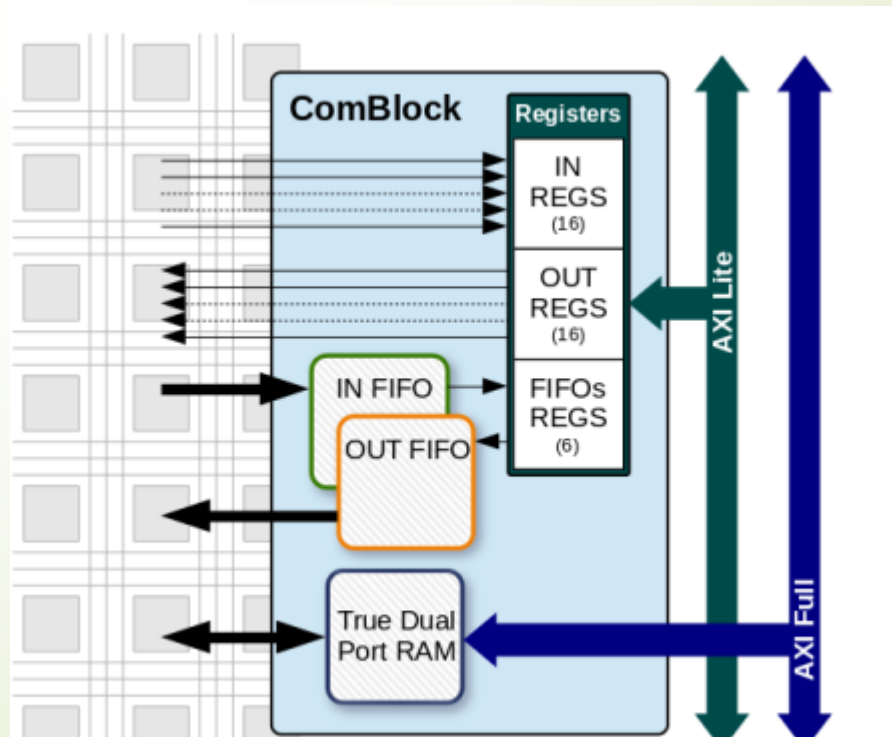
The development of the dpp implementation has been driven by the following considerations: utilizing data parallelism and allowing application specific specialization while keeping functional flexibility and minimizing power consumption

Block diagram



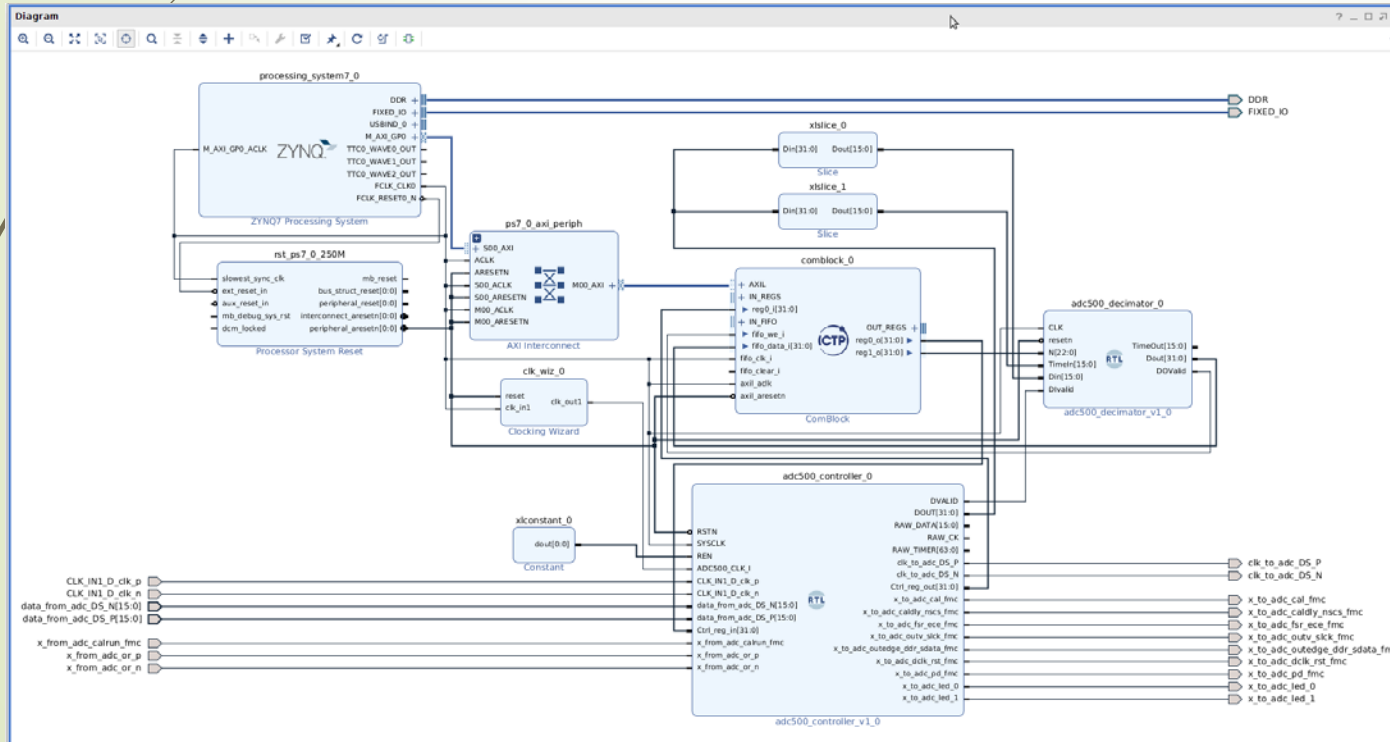
Comblock IP

- It is the communication block created to provide known interfaces such as registers, RAM, FIFO...to a user of the Programmable Logic, avoiding the complexity of the bus provided by the Processor System
- In this part, we have how to add a new IP core in the repository and use it in the block design



Adc_500 decimator/controller

- The adc_500 is a high speed ADC based in ADC08500 with a 500Mhz sampling frequency
- The method here for increasing the effective resolution of the ADC is oversampling and decimation. This technique involves oversampling of the input signal so that a number of samples can be used to compute a virtual result with greater accuracy than a single real sample can provide.





To summarize

- After this 4 weeks workshops i can:
- Develop the main IP core using VHDL;
- Configure any IP core in Vivado;
- Using Vivado for designing, simulating and implementing;
- Emulating an operation using Zedboard;
- Writing and reading in the registers and FIFO;
- Doing data acquisition using Zedboard



My expectations

- **Collaborate with ICTP and IAEA team after this school to develop RVI based on FPGA for my Lab and other Universities in my country**
- **Collaborate with other participants on different projects**
- **Applying what I have learned to improve my current work**

Thank you for the whole ICTP and IAEA team

A special Thanks to the tutors for their technical assistance and their patience

Thanks for giving me the chance to be a part of this amazing workshop