ICTP Project

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and its Applications for Nuclear and Related Instrumentation

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PROJECT ACTIVITIES

• Project 1	DPP
• Project 2	ADC500
• Project 3	UDMA
• Project Integration	INTEGRATION OF DPP, ADC AND UDMA

Project 1

DPP

- ❑ DPP top module :

1. Output mux
2. Fir derivative
3. Edge detector

Generate using vivado (Zedboard) with comblock IP Core

- ❑ Generate bit stream and open the SDK

IMPLEMENTED SOLUTION

- ➢Print the value of Pulses
- ➢By changing the threshold in the C code, the pulses produced will be changing based on initial input given.

Project 2

ADC500

- ADC500 module
  1. decimator module
  2. clocking wizard

Generate using vivado (Zedboard) with comblock IP Core

- Create ports match with the ones in the constraint files.
- Generate bit stream and open the SDK

IMPLEMENTED SOLUTION

- Import the file from sdk folder which is adc500.h
- Program the FPGA, and Produce Waveform
- The setting waveform output can be modified from GUI waveform
- Data acquisition can be produced using the SerialPlot software

Project 3

UDMA

- Combination between FPGA and microprocessor

Generate using vivado (Zedboard) with comblock IP Core

- This project is using FreeRTOS and LwIP

- Create Boot Image

IMPLEMENTED SOLUTION

- By using terminal, clone the repository and connect the board.
- By typing help command in the terminal, we can test the system and see how it works
- It shows that we can transfer the information given

Project Integration

DPP ,ADC500, UDMA

SoC –FPGA

- ❑ FPGA:
- ❖ DPP,ADC500 (Programmable Logic)
- ❑ Microprocessor
- ❖ UDMA – FreeRTOS and LwIP

Generate using vivado (Zedboard) with comblock IP Core

IMPLEMENTED SOLUTION

- ❑ It shows that the combination between data acquisition and digital pulse processing will produce the Digital Pulse Processor based on SoC-FPGA for Particle Detectors

PREFERABLE PROJECT : DPP

DPP

- This project generates the output using vivado (Zedboard) with comblock IP Core
- Produce simulation waveform
- The step concept of the design is almost like any FPGA application design

CRYPTOGRAPHY

key

Plaintext → Cryptographic chiper → chipertext

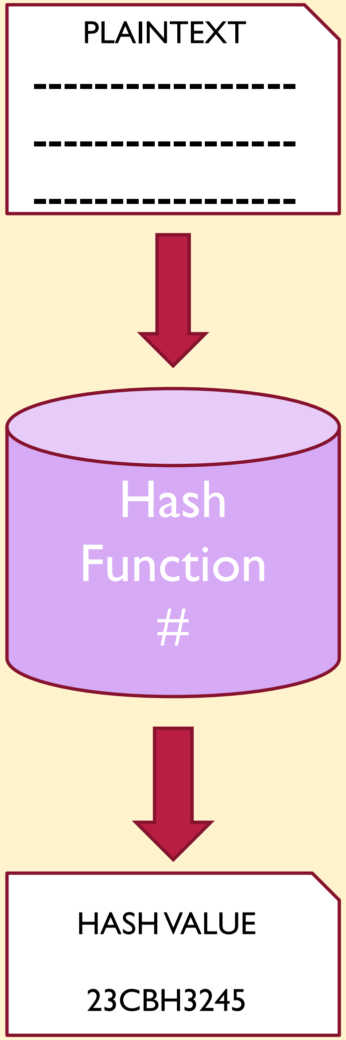
Hide actual data

SYMMETRIC CRYPTOGRAPHY – USE SINGLE KEY

ASYMMETRIC CRYPTOGRAPHY – USE TWO KEYS

HASH FUNCTION (ONE-WAY CRYPTOGRAPHY) – NO KEY

WHAT IS HASH FUNCTION?



TRANSFORMATION

- Take a variable size input, m and return a fixed-size string, hash value, h

BASIC REQUIREMENT

- Input can be any length
- Output has a fixed length
- One-way function – infeasible to find an input message x

GENERAL TYPES OF HASH FUNCTIONS

- MD5, SHA-1, RIPEMD160,SHA-224, SHA-256, SHA-384, SHA-512 and others

NEW TOPICS LEARNED

- Vivado, SDK, Gitlab, ILA, HLS, Access Memory etc
- C and VHDL for embedded system design
- New Idea of the FPGA application design

DIFFICULTIES AND CHALLENGES

Time constraint

Create IP core in the future design

PERSONAL IMPROVEMENT TO THE IMPLEMENTED SOLUTION

THANK YOU