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B.S. Electronics, LETI, Russia

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FPGA Background

- Taught a semester special course in Logic Synthesis with VHDL.

- Proposal to NASA: implement FPGA for improved time resolution and precision time tracking in lidar remote sensing for Jupiter Europa Orbiter (JEO), Jupiter Icy Moons Explorer (JUICE)

ICTP-IAEA School Objectives

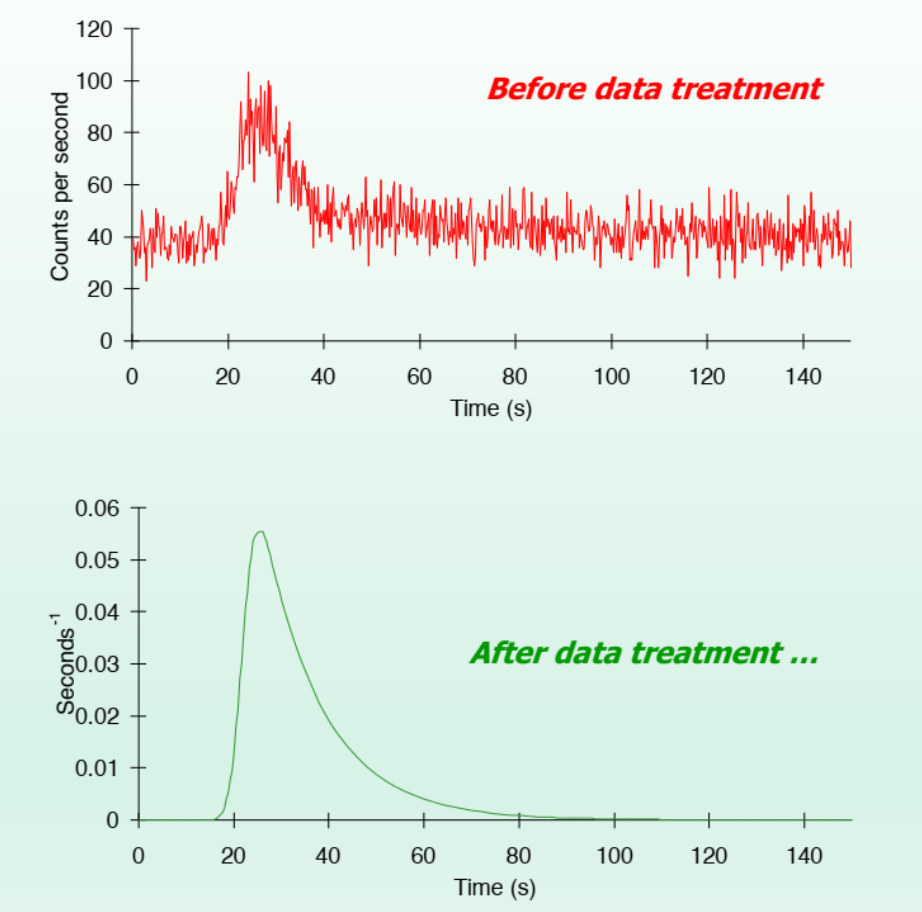
Learn New Topics and Applications in FPGA Implementation in Scientific Instrumentation.

Forge Research Collaboration with Researchers at School on developing VHDL code and Circuit Design in Applications of Common Interest – Examples: precision time-tracking, pulse processing.

Interest Project at Joint ICTP-IAEA School

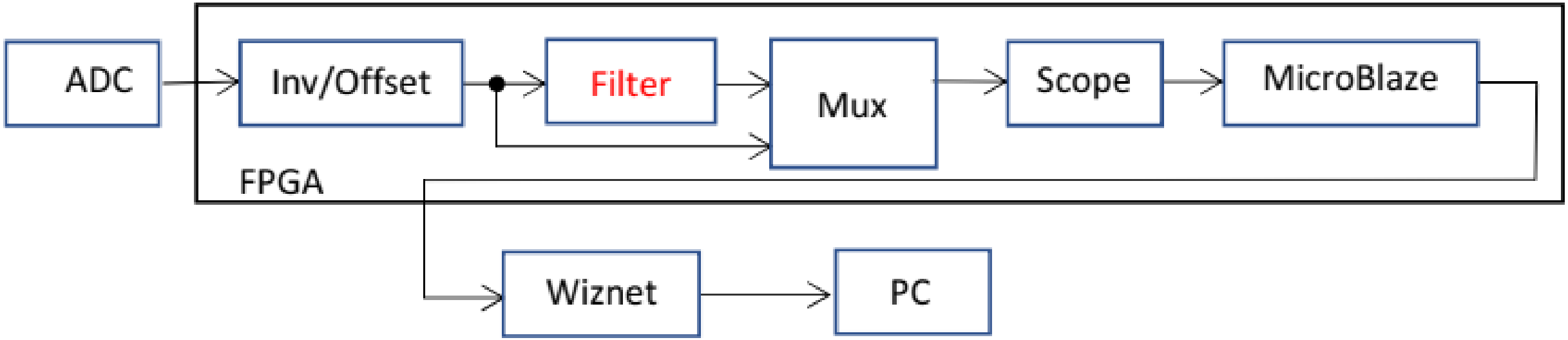
FPGA-Implementation of a Digital Filter to Improve S/N Ratio of Detected Signal in Radiotracer Techniques in Industrial and Environmental Applications

Apply smoothing and noise removal to acquired signal with digital filters in CMOD-A7 (< 100 $).



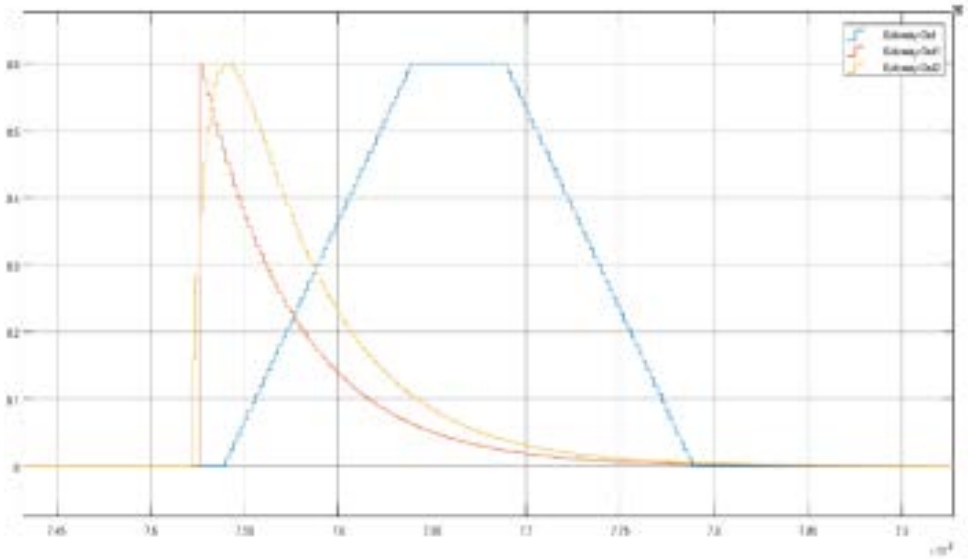
The constant zero offset in treated signal is due to DC stabilization and baseline restoration.

Block Diagram of Circuit in IAEA Lab



Filter is custom IP called Shaper in IAEA Lab

IAEA Lab: Five Stage Trapezoidal Filter



Blue – trapezoid filter
Red – filtered signal

Filter Stages: i) second-pole correction ii) impulse deconvolver; ii) moving window; iii) moving average; iv) normalization

Digital Filter Research Ambitions

- Optimal choice of filter stages

- Implement operations with minimal/reduced cost, e.g. convolution operation is far more computationally expensive than operations in frequency domain – Discrete Fourier Transform (DFT), Fast Fourier Transform (FFT).

Lab Obstacles

- Technical Faults in Vivado – Broken Clock Wizard Had to be Fixed by resetting environmental variables of ICTP computer.
- A few setbacks with remote transfer between computers, e.g. between ICTP Linux and IAEA Windows machines.

Result of Faults – Delayed lab, project work.

Propose:

i) Major software (Vivado) should be well tested on working computers before school.

ii) Remote connections should be established in advance.

ICTP-IAEA School Learning Experience

My FPGA experience was limited to logic synthesis with VHDL followed by verification of code with functional and timing simulation.

In Joint ICTP-IAEA School: Used applications not only for logic synthesis but for communicating with synthesized logic through a processor or microcontroller, and with a personal computer.

THANKS

TO

ORGANIZERS, SPEAKERS, TUTORS