Outline

- Digital CMOS design
  - Boolean algebra
  - Basic digital CMOS gates
  - Combinational and sequential circuits
  - Coding - Representation of numbers

CMOS Circuits

How to implement Boolean functions in CMOS technology ?

- A complex function cannot be implemented using a single gate
- Use a network of gates

Boolean network

CMOS Circuits

Example :

x	y	z	f
0	0	0	0
0	0	1	0
0	1	0	0
0	1	1	1
1	0	0	1
1	0	1	1
1	1	0	0
1	1	1	1

$f = \bar{x}.y.z + x.\bar{y}.\bar{z} + x.\bar{y}.z + x.y.z$

$f = (x+y+z) \,.\, (x+y+\bar{z}) \,.$

$(x+\bar{y}+z) \,.\, (\bar{x}+\bar{y}+z)$

$f = x.(yz+\bar{y}) + \bar{x}.(y.z)$

$f = \bar{x}.y.z + x.\bar{y}.\bar{z} + x.z$

$f = x.\bar{y} + y.z$

There is not a unique expression

CMOS Circuits

Example :

x	y	z	f
0	0	0	0
0	0	1	0
0	1	0	0
0	1	1	1
1	0	0	1
1	0	1	1
1	1	0	0
1	1	1	1

Which gates should I use ?

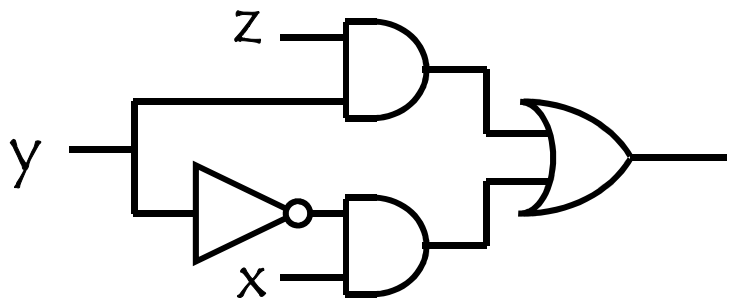
Cell library

$f = x.\overline{y} + y.z$

CMOS Circuits

Example :

x	y	z	f
0	0	0	0
0	0	1	0
0	1	0	0
0	1	1	1
1	0	0	1
1	0	1	1
1	1	0	0
1	1	1	1



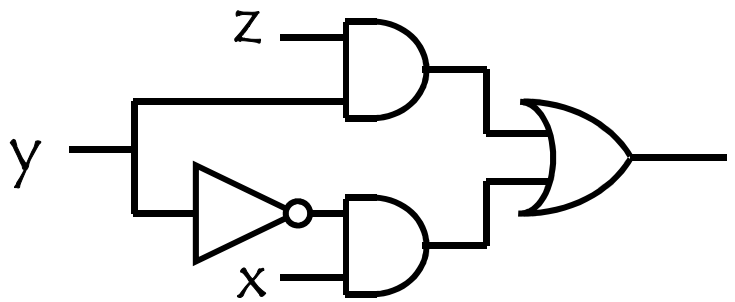
In VLSI, non-inverting gates do NOT exist

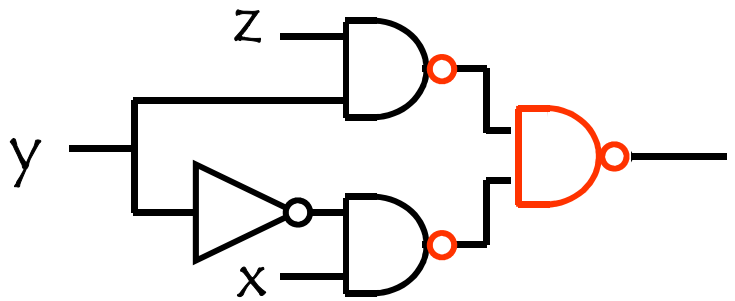
$f = x.\overline{y} + y.z$

CMOS Circuits

Example :

x	y	z	f
0	0	0	0
0	0	1	0
0	1	0	0
0	1	1	1
1	0	0	1
1	0	1	1
1	1	0	0
1	1	1	1





CMOS Circuits

Example :

$$f = (\overline{x} + y) \oplus x$$

$$f = \overline{(\overline{x} + y)} \oplus \overline{x}$$

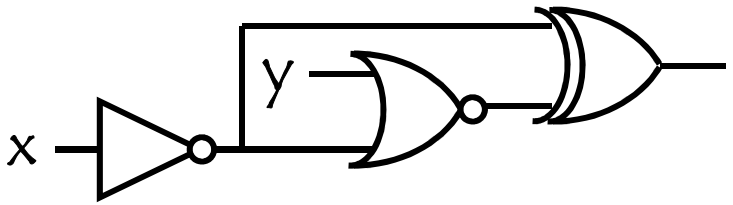
$$f = (\overline{x} + y) \,.\, \overline{x} + \overline{(\overline{x} + y)} \,.\, x$$

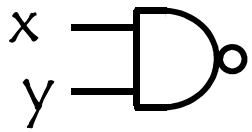
$$f = \overline{x} + y.\overline{x} + x.\overline{y}$$

$$f = \overline{x} + x.\overline{y}$$

$$f = \overline{x} + \overline{y}$$

$$f = \overline{x \,.\, y}$$





CMOS Circuits

How to implement Boolean functions with a gate network ?

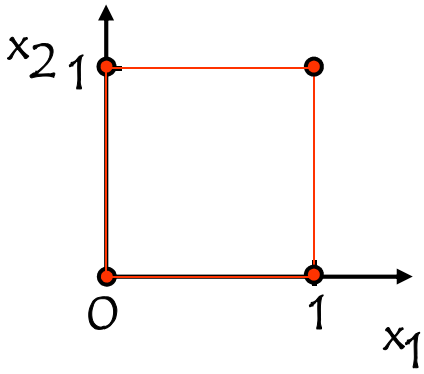
- Which expression ?

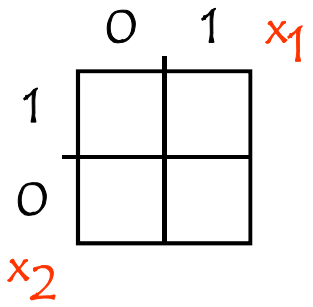
CMOS Circuits

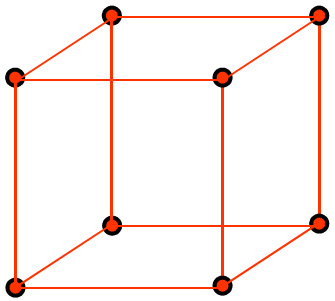
A function can be defined by its Truth table

- Karnaugh representation gives a minimal expression

Representation of the function in a space of dimension n



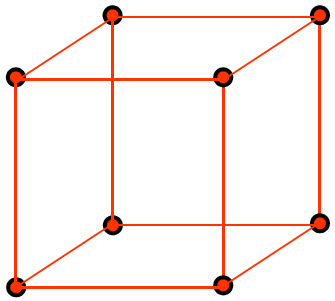


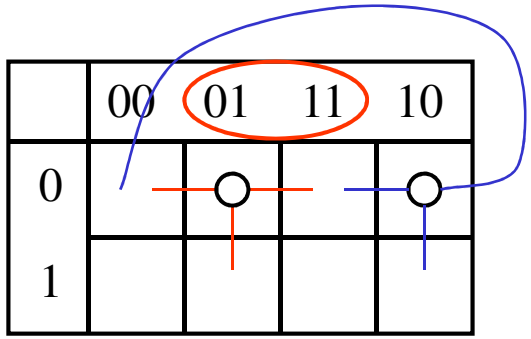


Representation of vectors' adjacency

CMOS Circuits

A Karnaugh table is represented in a flat 2-dimension table





vectors' adjacency

CMOS Circuits

Example :

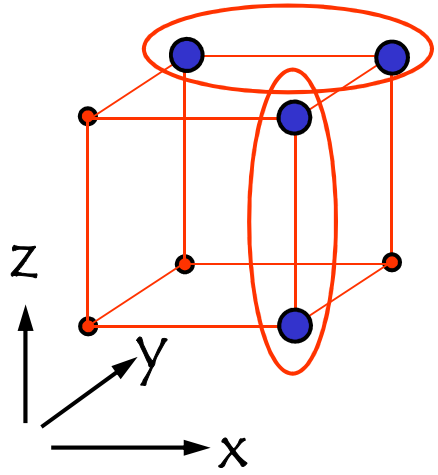
x	y	z	f
0	0	0	0
0	0	1	0
0	1	0	0
0	1	1	1
1	0	0	1
1	0	1	1
1	1	0	0
1	1	1	1

	00	01	11	10	xy
0	0	0	0	1	
1	0	1	1	1	

z

CMOS Circuits

Example :



	00	01	11	10
0	0	0	0	1
1	0	1	1	1

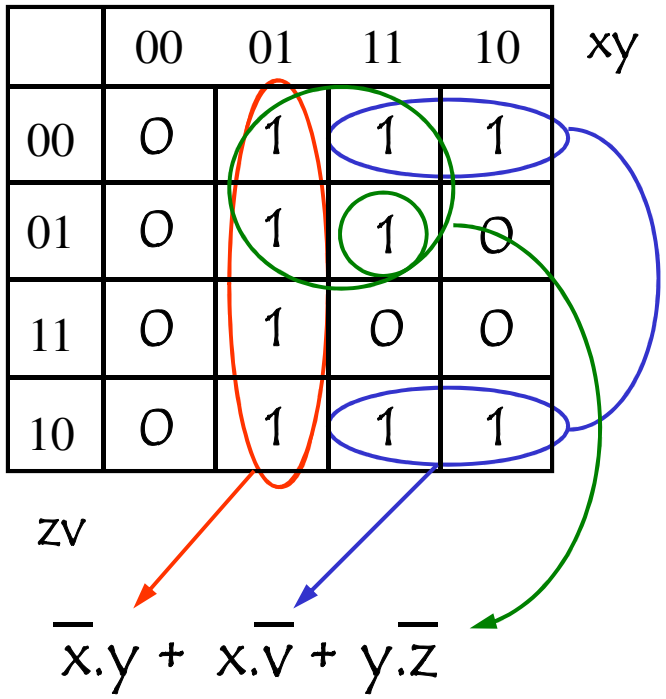
xy

z

$f = x.\overline{y} + yz$

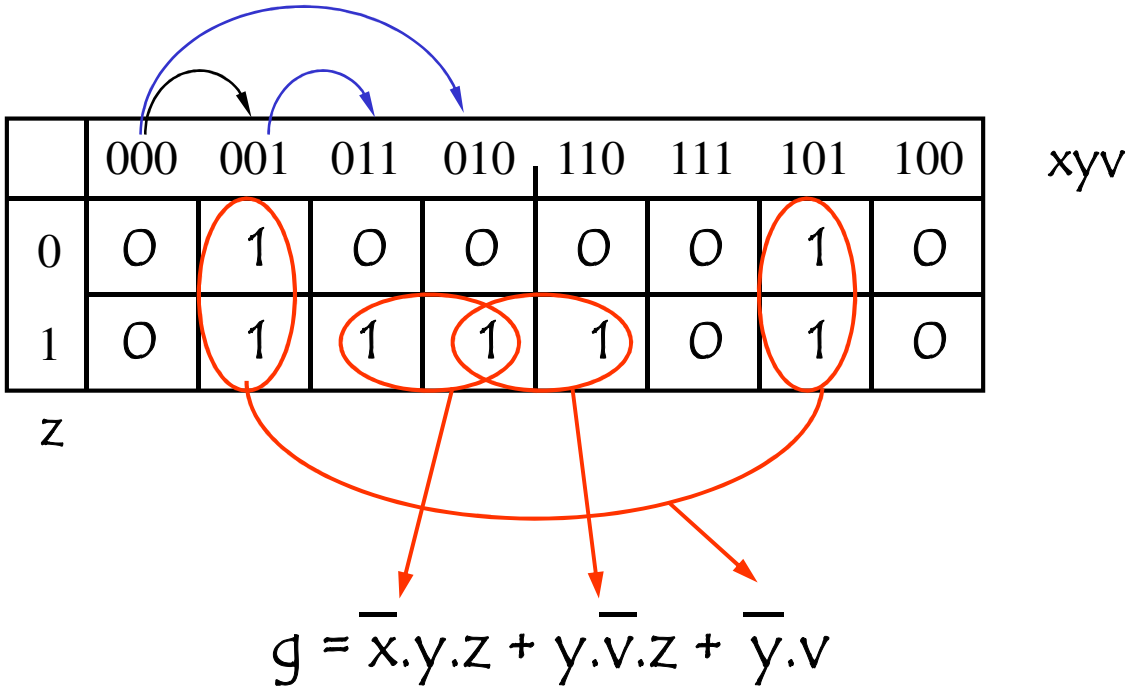
CMOS Circuits

Example :



CMOS Circuits

Example :



$$g = \overline{x}.y.z + y.\overline{v}.z + \overline{y}.v$$

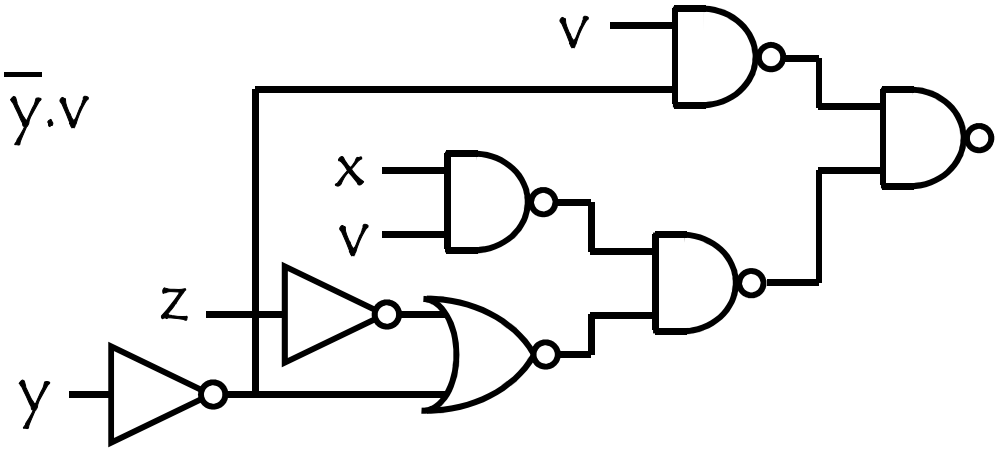
CMOS Circuits

Example :

$$g = \overline{x}.y.z + y.\overline{v}.z + \overline{y}.v$$

$$g = y.z.(\overline{x}+\overline{v}) + \overline{y}.v$$

$$g = \overline{(\overline{y}+\overline{z})}.\overline{(x.v)} + \overline{y}.v$$



CMOS Circuits

How to implement Boolean functions with a gate network ?

- Local optimization using Karnaugh tables

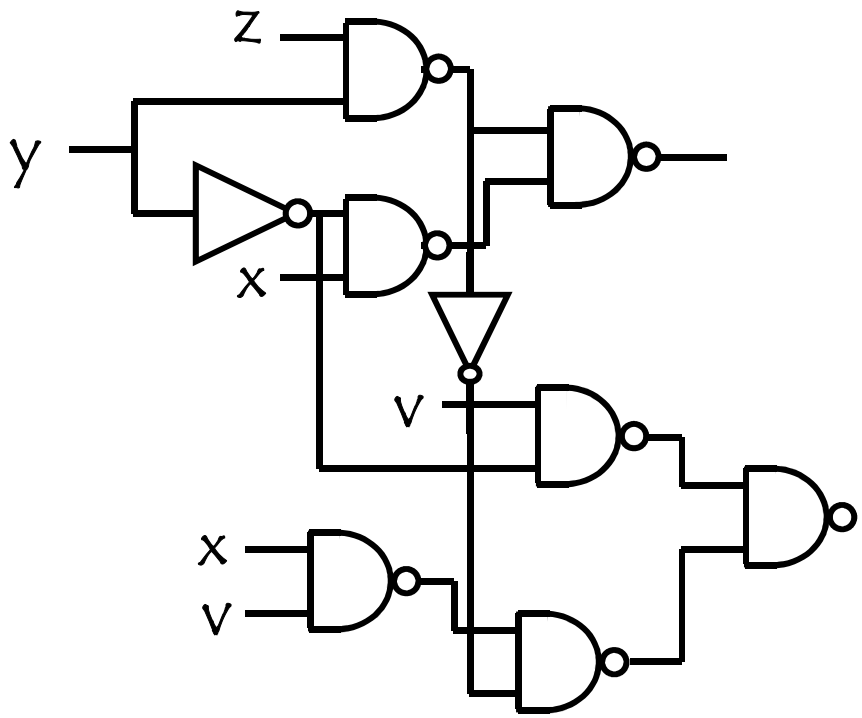
A design includes several Boolean functions

CMOS Circuits

Example :

$$g = \overline{\overline{(y+z)}.\overline{(x.v)}} + \overline{y}.v$$

$$f = x.\overline{y} + y.z$$



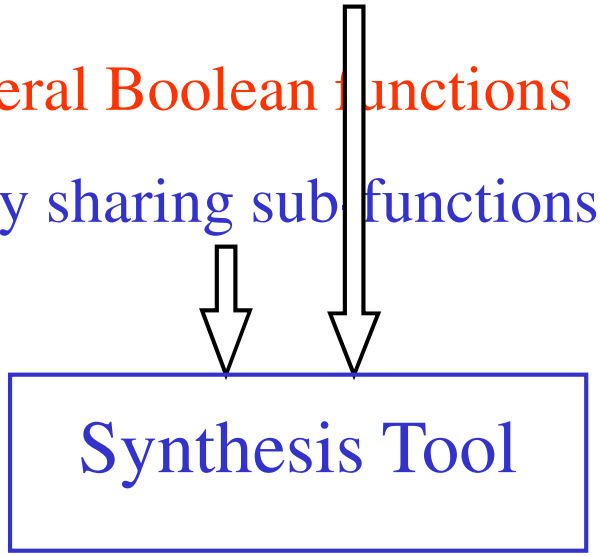
CMOS Circuits

How to implement Boolean functions with a gate network ?

- Local optimization using Karnaugh tables

A design includes several Boolean functions

- Global optimization by sharing sub-functions



CMOS Circuits

- ## Combinational logic

  The value of the output can be determined knowing the value of the inputs

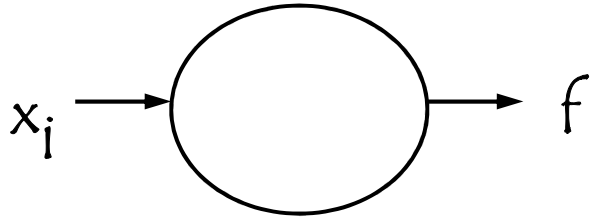
- ## Sequential logic

  The value of the output depends on the value of the inputs and the history

Notion of memory

CMOS Circuits

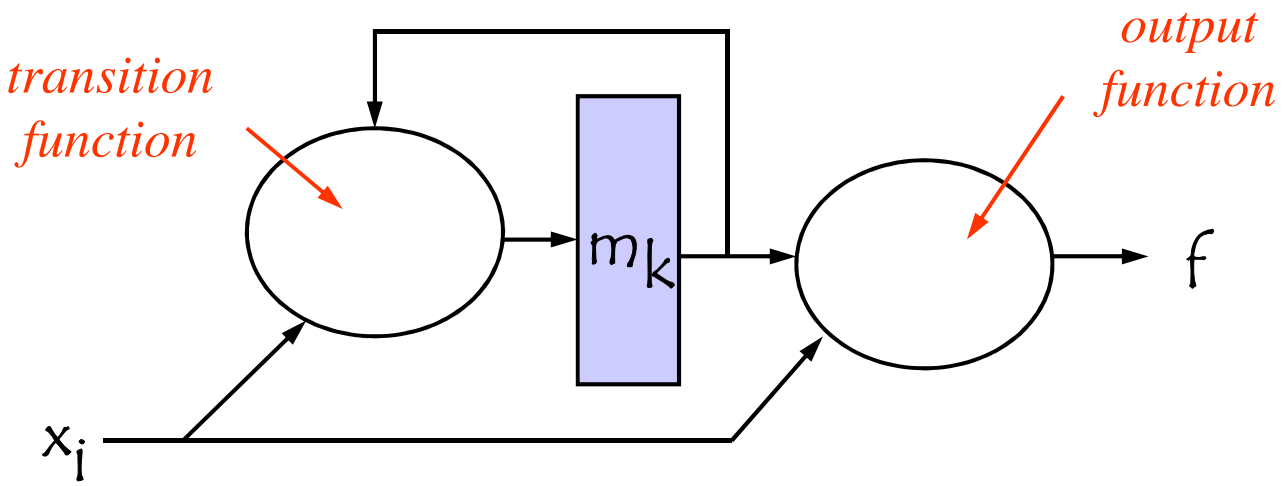
- Sequential logic



$$f(x_1, \ldots, x_i, \ldots, x_n , m_1, \ldots, m_k, \ldots, m_p)$$
$$m_k(x_1, \ldots, x_i, \ldots, x_n , m_1, \ldots, m_k, \ldots, m_p)$$

CMOS Circuits

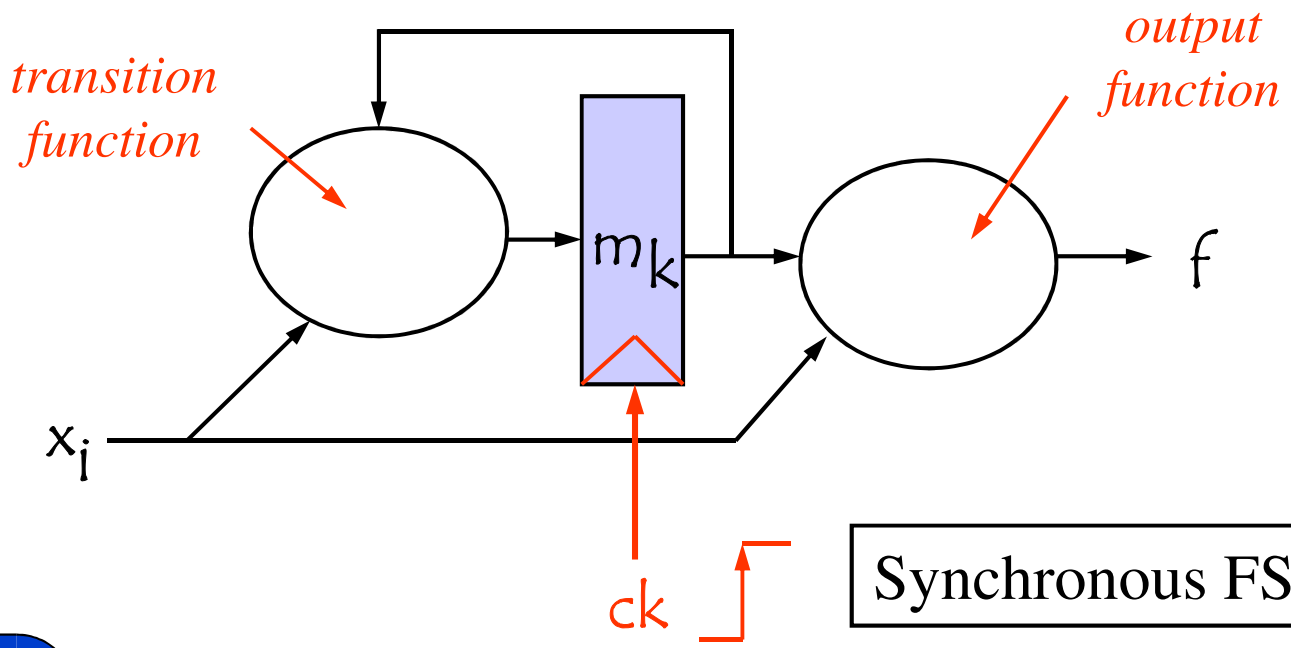
- Sequential logic



Finite State Machine (FSM)

CMOS Circuits

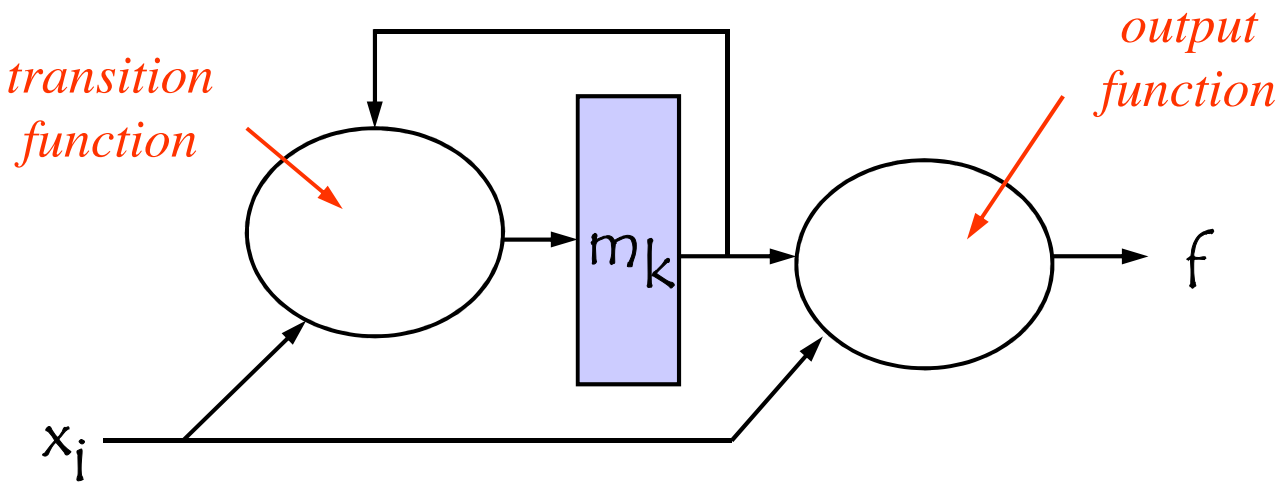
Finite State Machine



Synchronous FSM

CMOS Circuits

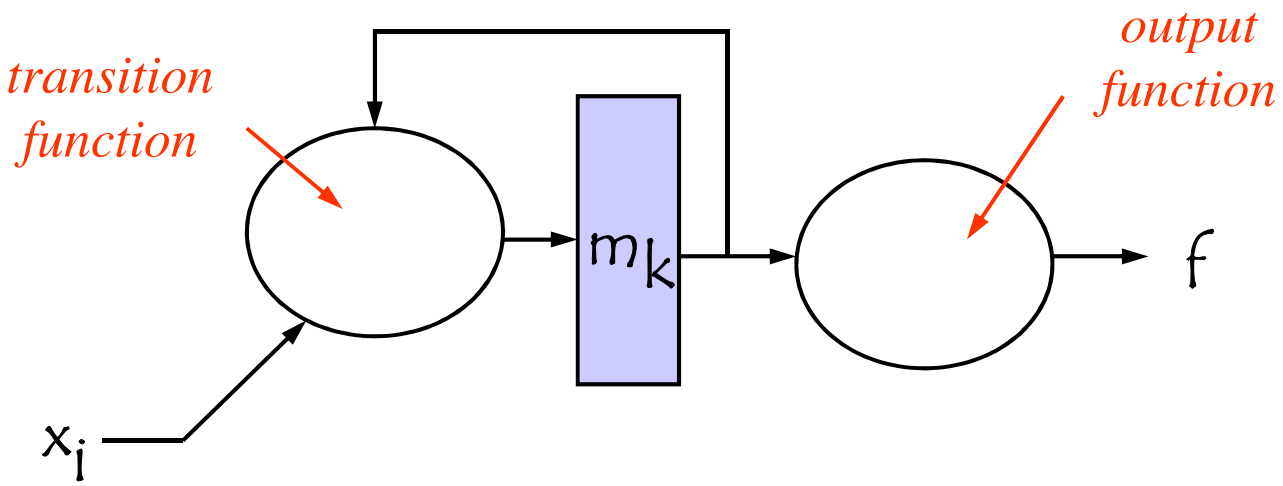
- Finite State Machine



Mealy FSM

CMOS Circuits

- Finite State Machine



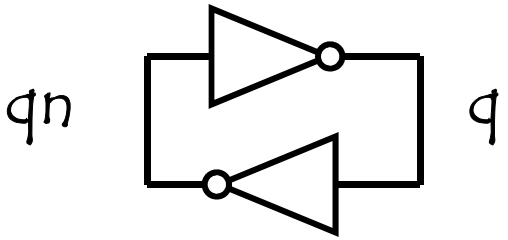
Moore FSM

CMOS Circuits

Memory :

Hold a data (0 or 1)

Write a data (0 or 1)

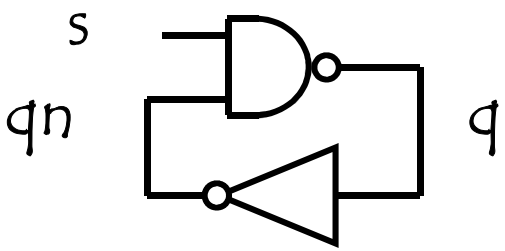


CMOS Circuits

Memory :

Hold a data (0 or 1)

Write a data (0 or 1)



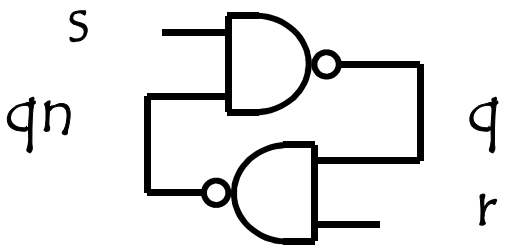
s	q	qn
0	1	0
1	$\overline{qn}$	$\overline{q}$

CMOS Circuits

Memory :

Hold a data (0 or 1)

Write a data (0 or 1)

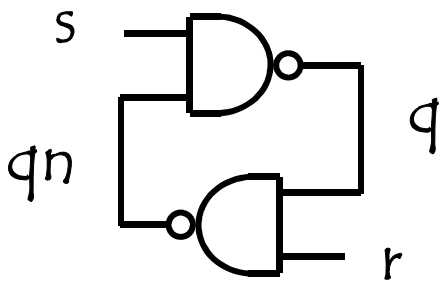


s	r	q	qn
0	1	1	0
1	0	0	1
1	1	$\overline{qn}$	$\overline{q}$
0	0	1	1

RS flip flop

CMOS Circuits

Memory :



$$q = \overline{s.qn} \qquad qn = \overline{r.q}$$

$$f = q = \overline{s \,.\, \overline{(r \,.\, q)}}$$

$$f = \overline{s} + (r \,.\, q)$$

$$f = q \,.\, (r+\overline{s}) + \overline{q} \,.\, \overline{s}$$

$$\frac{\partial f^{+}}{\partial q} = s \,.\, (\overline{s} + r) = s.r$$

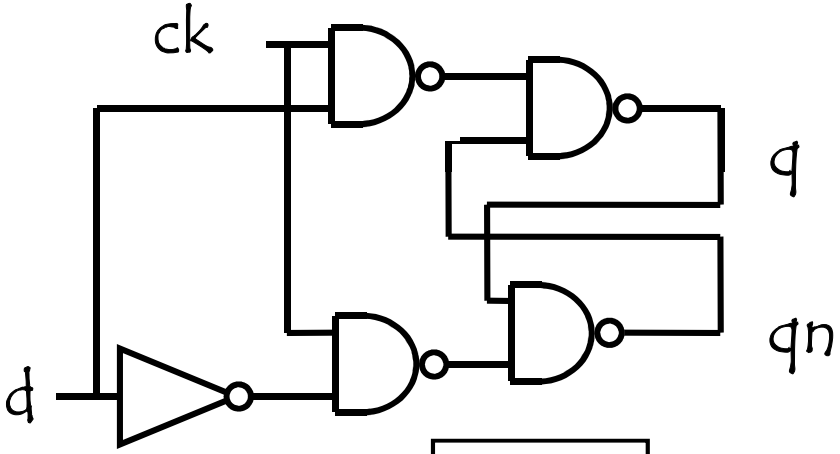
memory

$$\frac{\partial f^{-}}{\partial q} = \overline{s} \,.\, \overline{(\overline{s} + r)} = 0$$

CMOS Circuits

Synchronous Memory :

Write a data d when the clock ck = 1



d latch

s	r	q	qn
0	1	1	0
1	0	0	1
1	1	$\overline{qn}$	$\overline{q}$
0	0	1	1

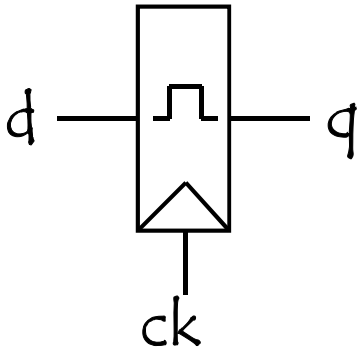
if ck.d = 1 s = 0

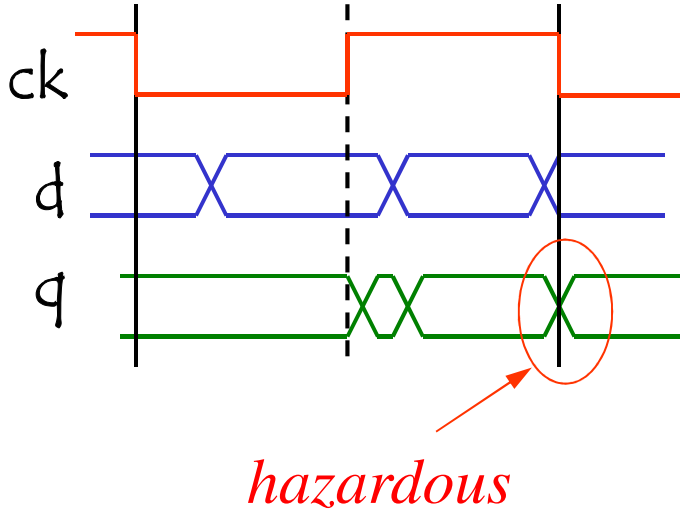
if ck.$\overline{d}$ = 1 r = 0

CMOS Circuits

Synchronous Memory :

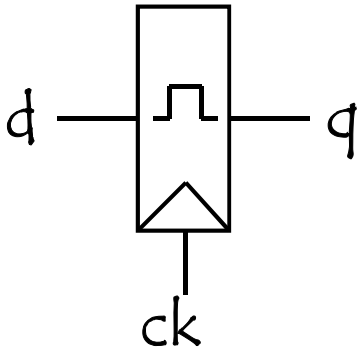
Write a data d when the clock ck = 1

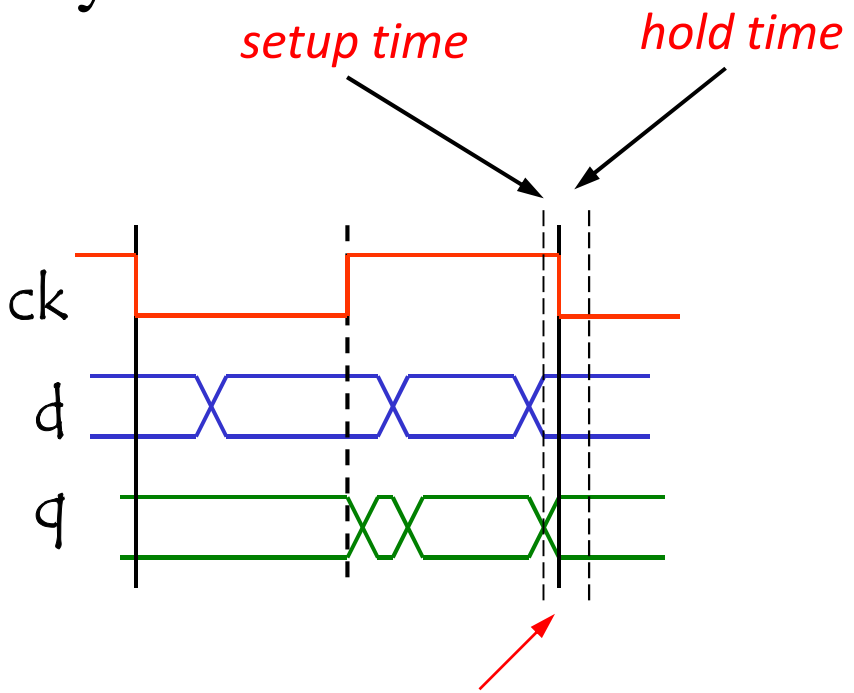




CMOS Circuits

Synchronous Memory :

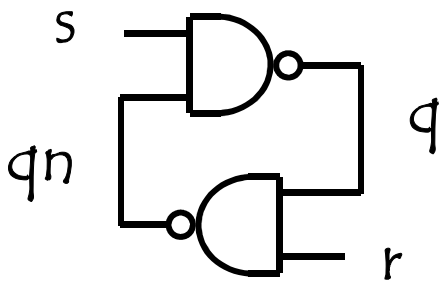


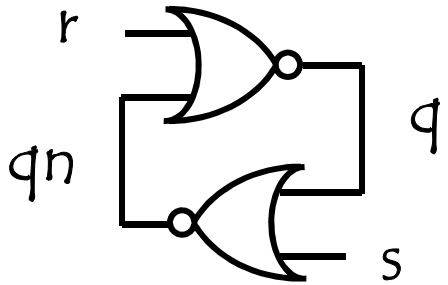


data should not be changed during this period

CMOS Circuits

Memory :





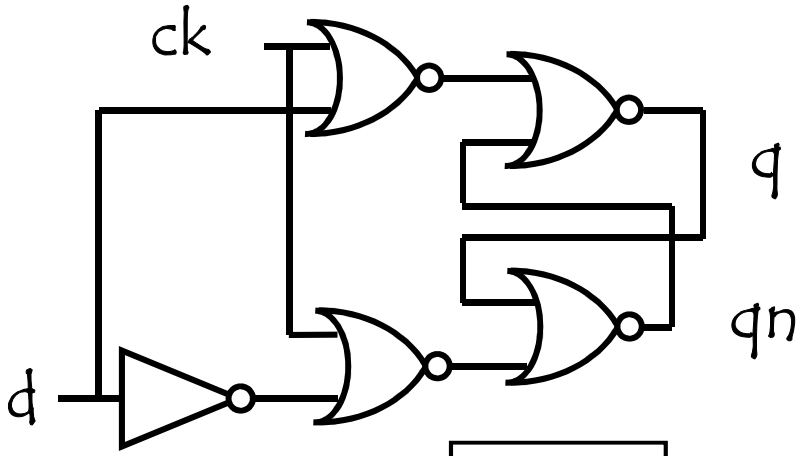
s	r	q	qn
0	1	0	1
1	0	1	0
1	1	0	0
0	0	$\overline{qn}$	$\overline{q}$

RS flip flop

CMOS Circuits

Synchronous Memory :

Write a data d when the clock ck = 0



d latch

s	r	q	qn
0	1	0	1
1	0	1	0
1	1	0	0
0	0	$\overline{qn}$	$\overline{q}$

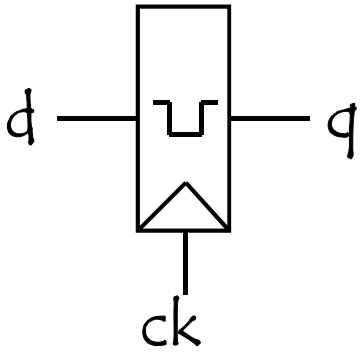
if $\overline{ck}.d = 1$ s = 1

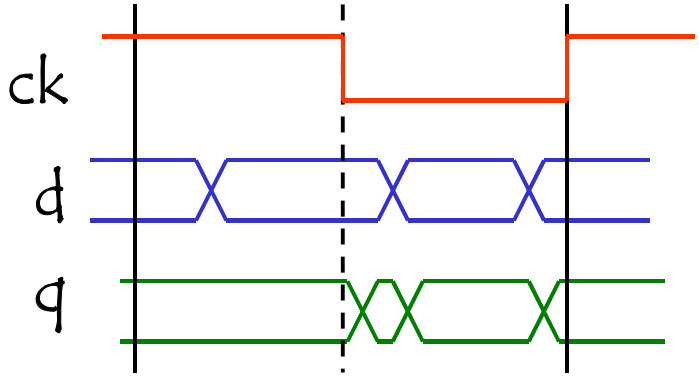
if $\overline{ck}.\overline{d} = 1$ r = 1

CMOS Circuits

Synchronous Memory :

Write a data d when the clock ck = 0

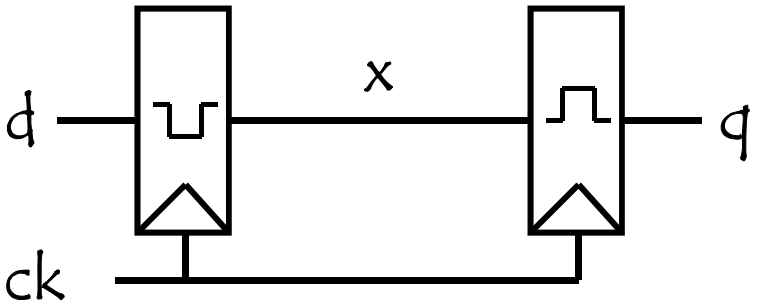


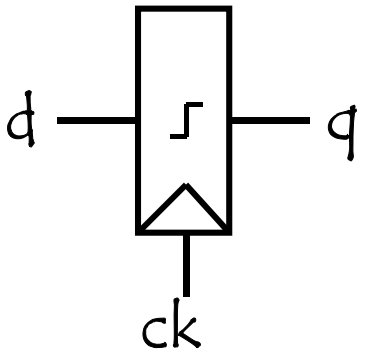


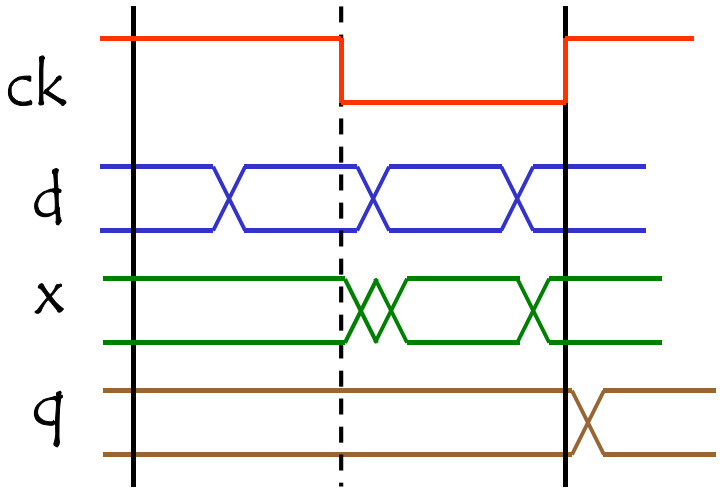
CMOS Circuits

Synchronous Memory :

Write a data d on the rising edge of the clock ck



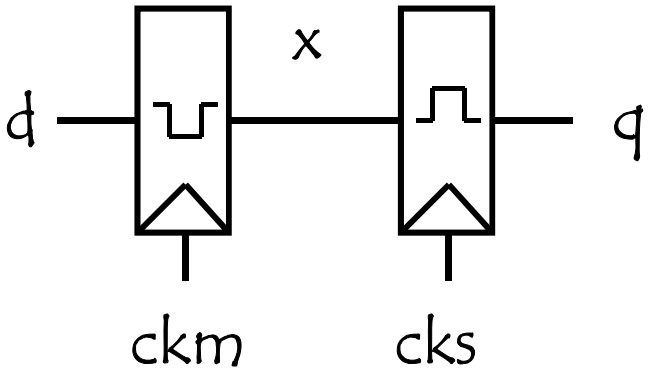


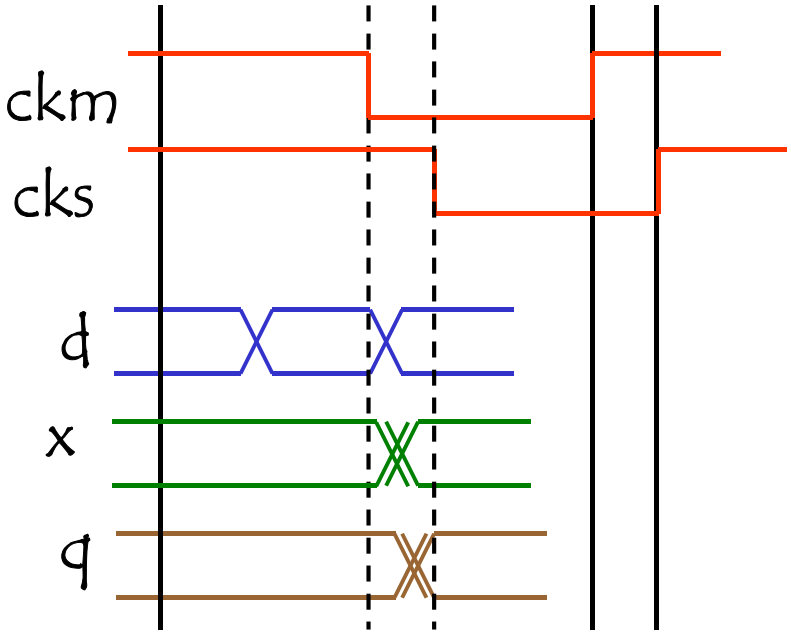


CMOS Circuits

Synchronous Memory :

Write a data d on the rising edge of the clock ck

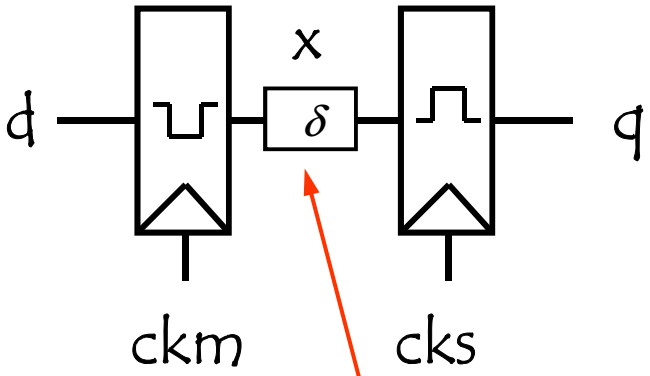


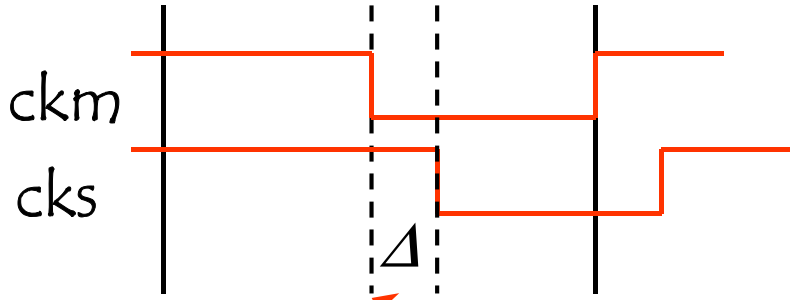


CMOS Circuits

Synchronous Memory :

Write a data d on the rising edge of the clock ck



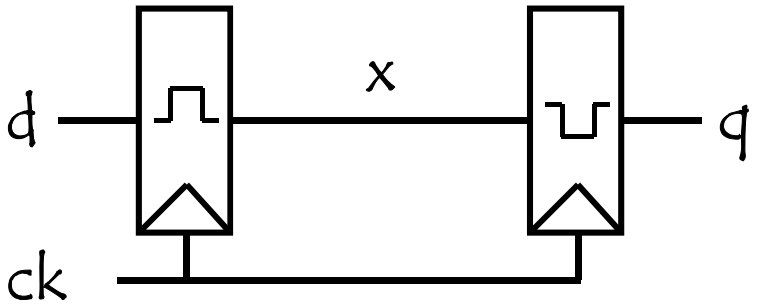


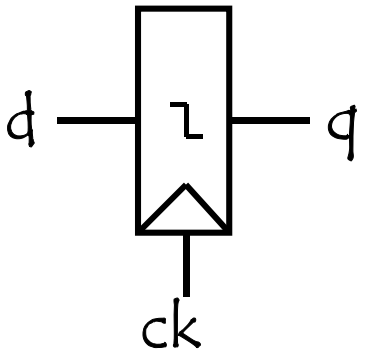
δ should be > Δ

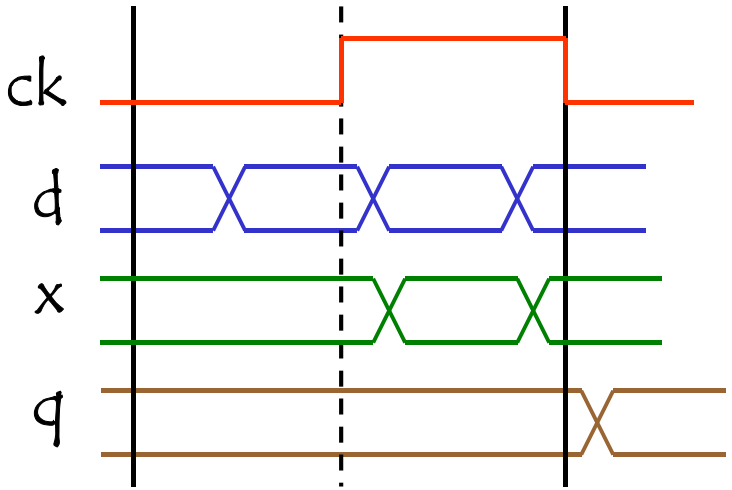
CMOS Circuits

Synchronous Memory :

Write a data d on the falling edge of the clock ck



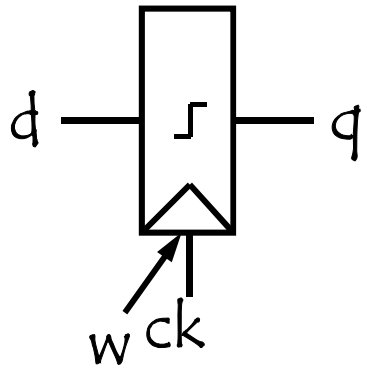


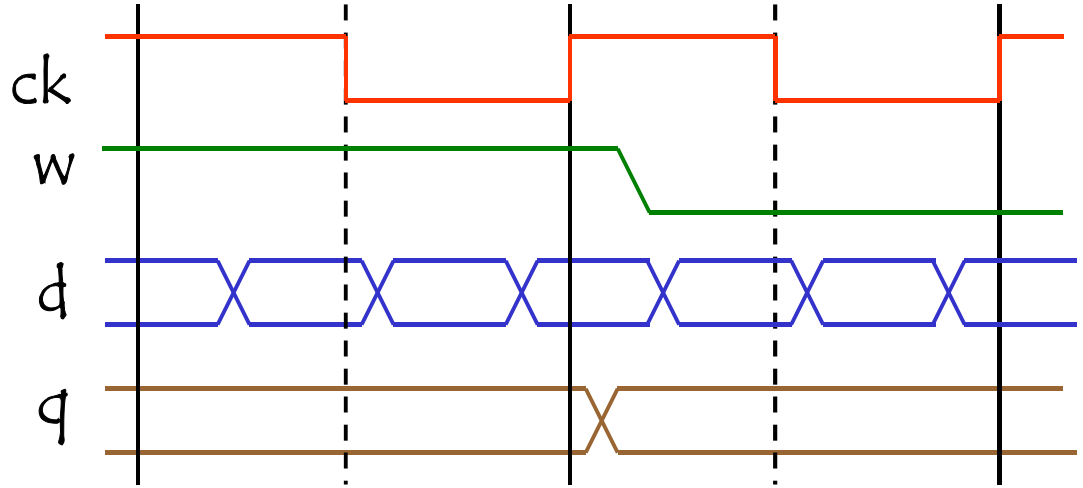


CMOS Circuits

Synchronous Memory :

Write a data d on the rising edge of the clock ck
when some condition is true (write enable)





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