

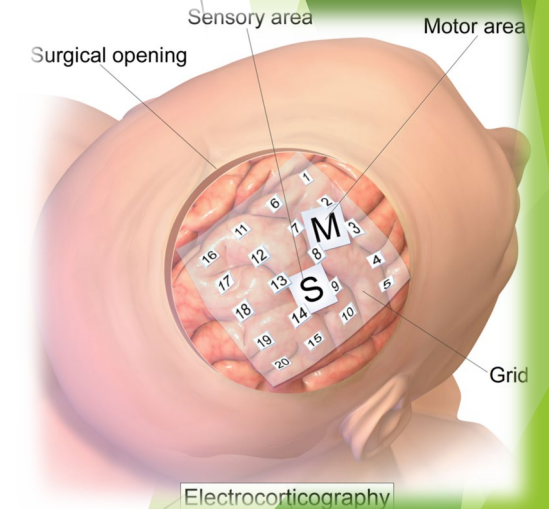
High-Channel Count Electrophysiology (HiCCE)

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Electrophysiology

- ▶ The study of electrical signals originating in the activity of the nervous system called the electrophysiology.
- ▶ Neurons produce temporally localized electric discharges.
- ▶ These discharges can be captured, using non-invasive methods

<https://en.wikipedia.org/wiki/Electrocorticography>



using invasive methods

http://www.psychologie.uzh.ch/fachrichtungen/plasti/Labor_en.html

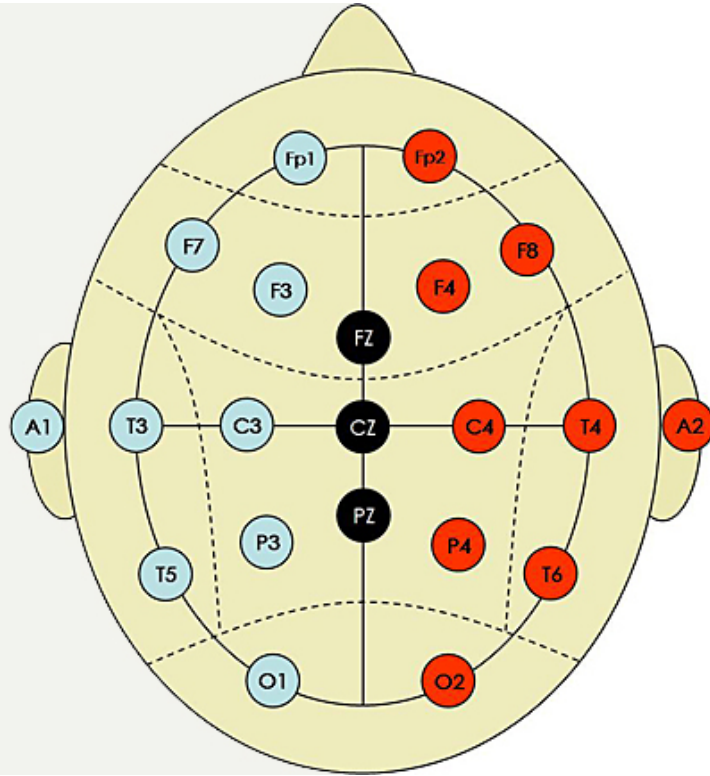
Electrophysiology

➤ Electroencephalography (EEG)

KEY:

- RIGHT Hemisphere
- LEFT Hemisphere
- Mid Line

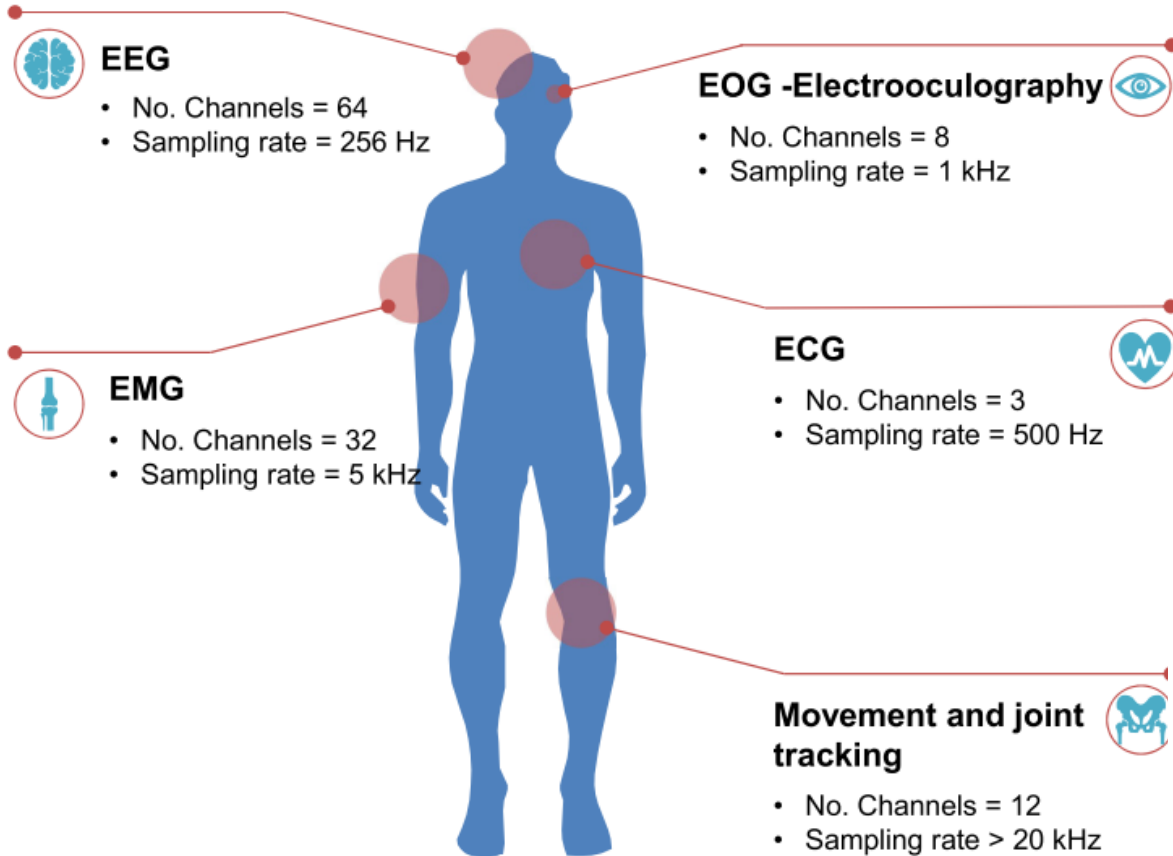
F : Frontal Lobe
T : Temporal Lobe
C : Central Lobe
P : Parietal Lobe
O : Occipital Lobe
Z : Mid Line



- ▶ EEG has been traditionally measured using the standard international 10-20 electrode system.
- ▶ The spatial resolution of the traditional 10-20 electrode system is not sufficient.

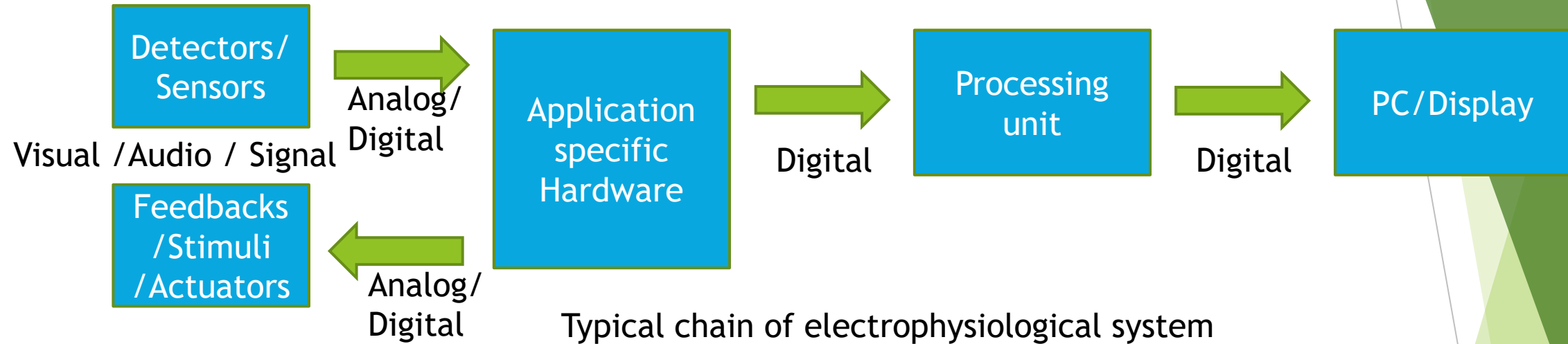
- This can be improved by recording from hundreds of sites using state-of-the-art probes.

Electrophysiology



Biopotential	Frequency range (Hz)	Amplitude range (mV)	No. of channels
Electrocardiogram (ECG)	0.05 – 150 (diagnostic)	0.1 – 5	12 (in hospital)
	0.5 – 40 (monitoring)		3 (in field)
Electroencephalogram (EEG)	0.1 – 100	0.025 – 0.1	21 (10 – 20 system)
			345 (10 – 5 system)
Electrocorticography (ECoG)	0.1 – 500	0.1 – 0.5	>500
Electromyography (EMG)	25 – 5000	0.1 – 100	<15

Electrophysiology



- ▶ **Detectors/Sensors**
In electrophysiology, these are just electrodes.
- ▶ **Feedbacks/Stimuli or actuators**
Visual/audio or digital responses

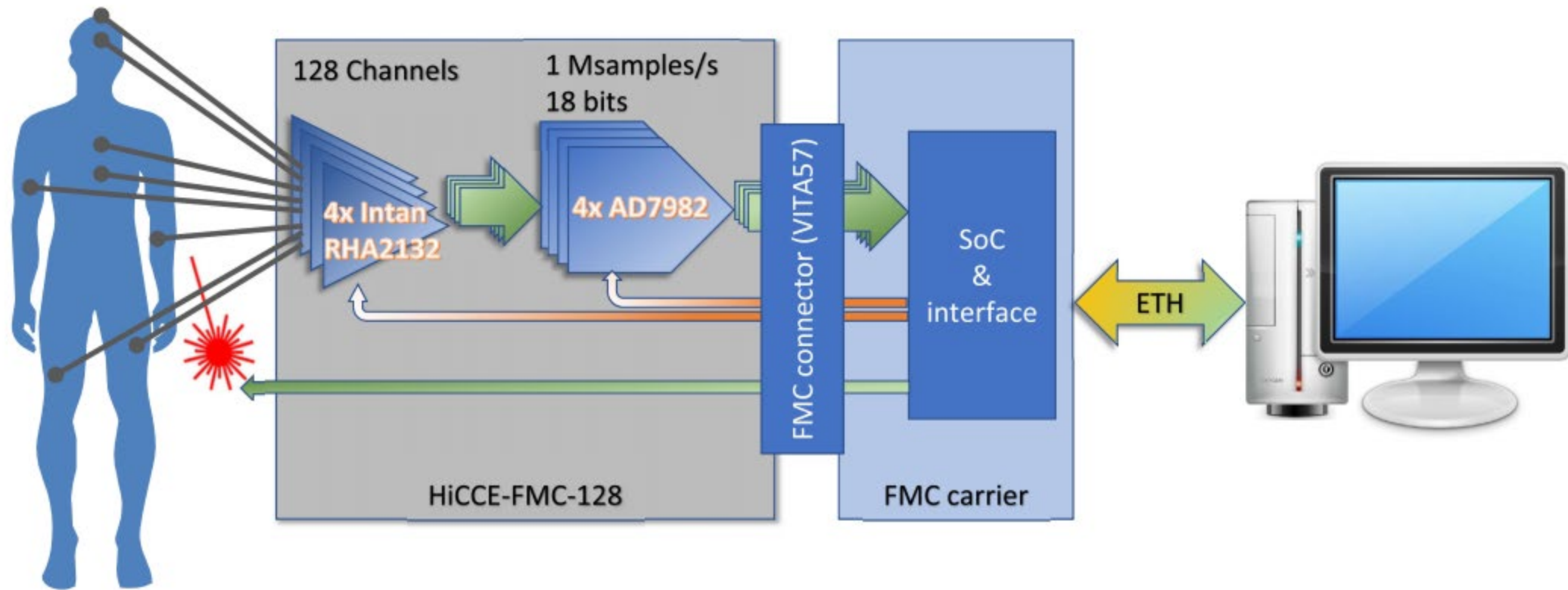
Commercial data acquisition systems

System	Max. Sampling Rate (SPS)	No. of Channels	Digital Output Resolution	Input Range (mV)	Noise Level (RMS)	Processor	Connectivity	CMRR	Price (€)
g.tec Nautilus [9]	500	64	24-bits	±187.5	<0.6 μV @ 1-30 Hz	TI DSP	Wireless 2.4 GHz/ USB 2.0	>90 dB	>4.5 k
g.tec HIamp [10]	38.4 k	256	24-bits	±340	<0.5 μV @ 1-30 Hz	TI DSP	USB 2.0	>90 dB	>31 k
TMSi Mobita [11]	2000	32	24-bits	±200	<0.4 μV @ 0.1-10 Hz	N/A	Wi-Fi IEEE 802.11 b/g	>100 dB	N/A
TMSi Refa [12]	2048	136	24-bits	±150	<1 μV @ 128 Hz	N/A	USB 2.0	>90 dB	N/A
Emotiv [13] EPOC Flex	128	32	14-bits	±4.12	N/A	N/A	Wireless proprietary 2.4 GHz	N/A	>2 k
BioSemi [14] ActiveTwo AD-box	16 k	256	24-bits	±262	<2 μV @ 16 kHz	N/A	USB 2.0	>90 dB	>40 k
ANT Neuro [15] eego mylab	16 k	256	24-bits	±50	<1 μV @ Lowest Freq.	N/A	USB 2.0	>100 dB	>25 k
Brain Products [16] actiCHamp	25 k	168	24-bits	±400	<2 μV @ 0-35 Hz	N/A	USB 2.0	>100dB	>25 k

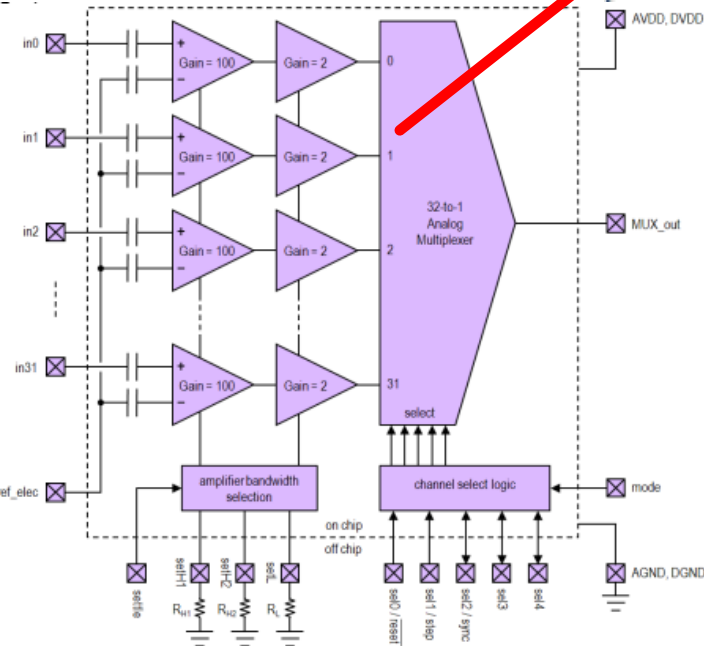
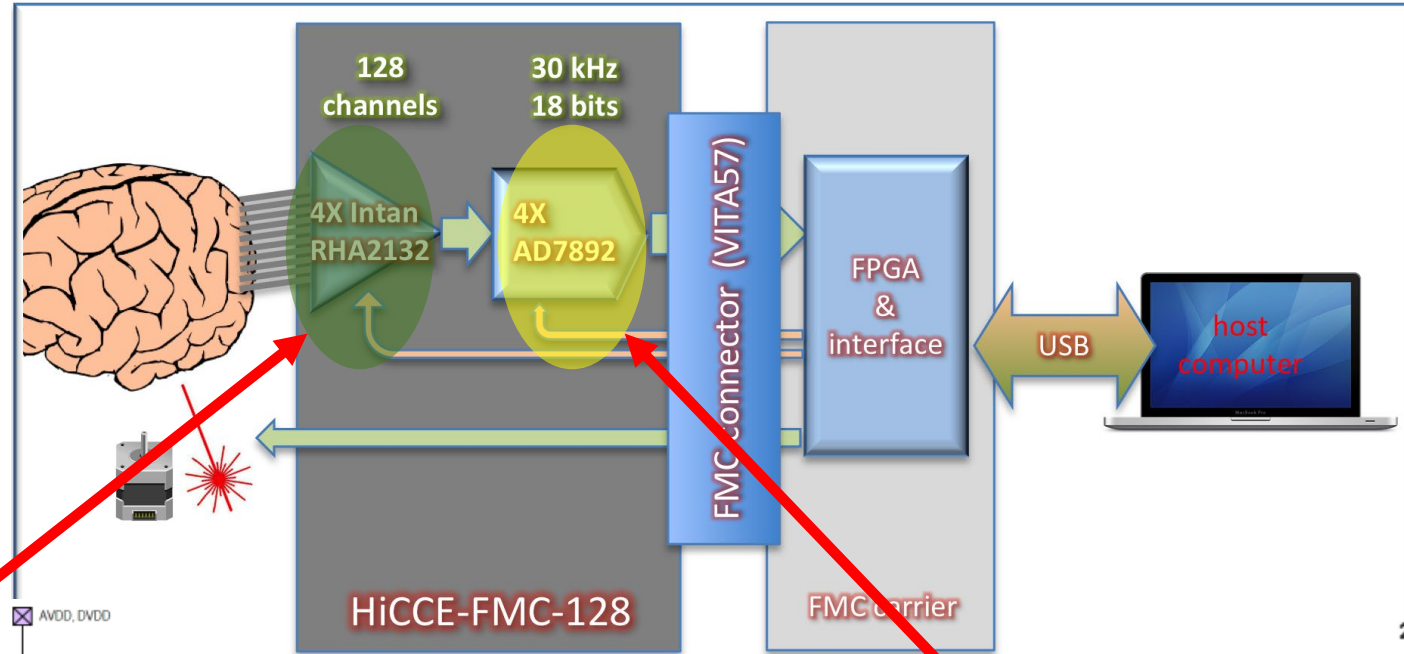
Non-commercial solutions

Property	Proposed system	Pinho et al. [21]	Feng et al. [22]	Vo et al. [23]	Wild et al. [24]	Nathan et al. [25]	Shyu et al. [26], [28]	Khurana et al. [27]	Annese et al. [7]
Modular	Yes	No	No	Yes	No	No	No	No	No
Channels	128	32	16	8	4	16	2	N/A	16
Sampling frequency, Hz	31.25k	1000	1024	250	250	N/A	8k	250	500
ADC number of bits	18	24	24	24	24	24	12	N/A	16/24
Connectivity	Ethernet	Wi-Fi 802.11 b/g/n	Wi-Fi 802.11 b/g/n	Bluetooth	Bluetooth	Bluetooth	413 MHz RF	Ethernet	N/A
Processing device	Xilinx Zynq 7020	Texas Instruments DM3730	BeagleBone Black	ST Microelectronics STM32F4	Microchip ATmega328p	Texas Instruments MSP430	Altera Cyclone II FPGA	Xilinx Spartan 3E FPGA	Altera Cyclone V FPGA
CMRR, dB	-81	-115	N/A	-110	-110	-110	130	N/A	N/A
Local processing ^a	Yes	Yes	No	No	No	No	Yes	Yes	Yes

HiCCE cont...

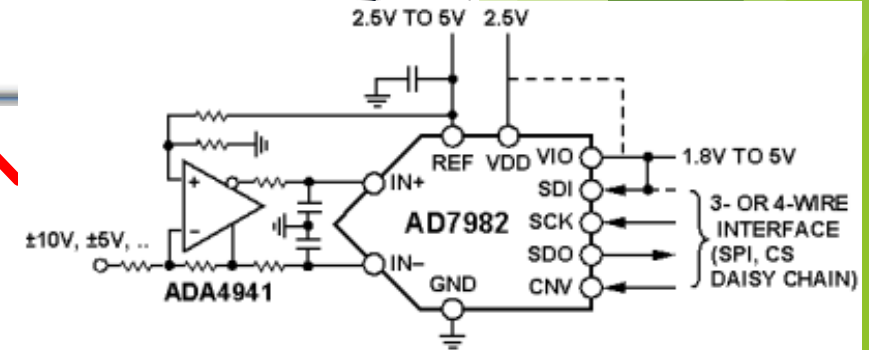


HiCCE Hardware



Intan RHA2132

- 32-channel multiplexing amplifier
- Has programmable band pass filter
- Can be individually addressed the channels



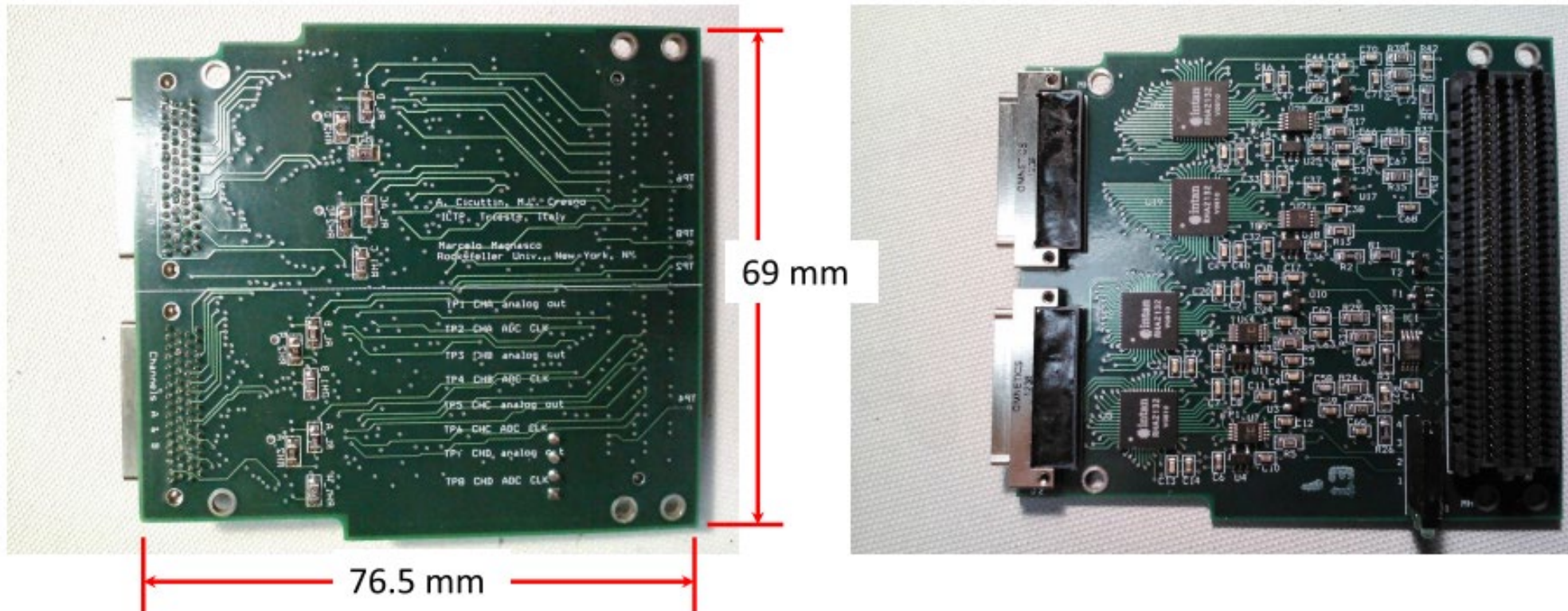
Analog Devices AD7982

- 18 - bits Successive approximation
- 1 MS/s throughput
- Low power - 7 mW at 1 MS/s

HiCCE Hardware

First prototype of the HiCCE

- 128 channels
- 31.25 kSamples per second on each channel



HiCCE Hardware

INPUT REFERRED NOISE

- The measured IRN is less than 5 μV for all channels and the average value is about 3 μV .

COMMON MODE REJECTION RATIO

- The measured CMRR is about 82 dB.

ELECTRICAL CHARACTERISTICS

- Each channel has different baselines around 1.2376 V
- Spread in the range of approximately 20 mV, which is 100 μV referred to the analog input voltages

HiCCE-128 Repository

<https://ohwr.org/project/hicce-fmc-128>

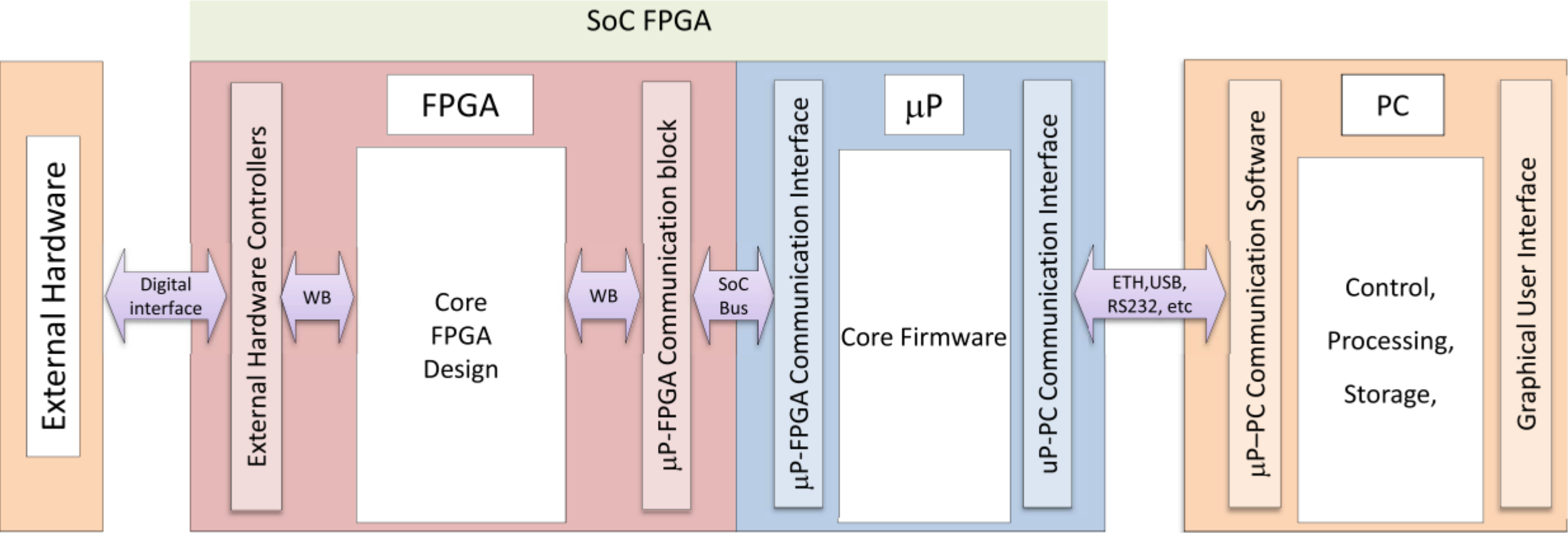
The screenshot shows the Open Hardware Repository website for the HiCCE-FMC-128 project. The browser address bar shows the URL <https://ohwr.org/project/hicce-fmc-128>. The page header includes the Open Hardware Repository logo and navigation links for Projects, Groups, Snippets, and Help. A search bar and a 'Sign in' button are also present.

The main content area displays the repository details for 'HICCE-FMC-128'. The current branch is 'master'. A recent commit is shown: 'GUIs for host PC added' by Kasun Sameera Mannatunga, authored 2 years ago, with commit hash c2b5d374.

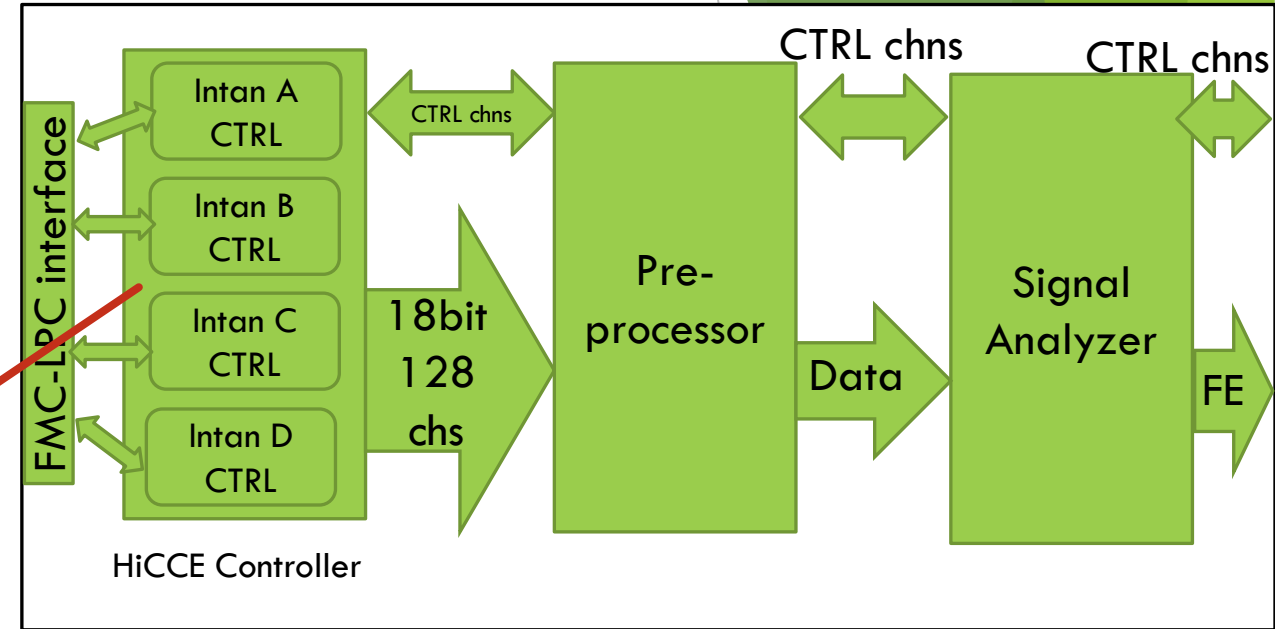
Name	Last commit	Last update
HiCCE-128-FMC version 1	1st prototype of the HiCCE	2 years ago
HiCCE-128-FMC version 2	2nd prototype of the HiCCE	2 years ago
Images	Images of HiCCE hardwares	2 years ago
PC software	GUIs for host PC added	2 years ago
SoC firmware	SoC design files added	2 years ago
README.md	Initial commit	2 years ago

The README.md file is displayed below the table, titled 'HiCCE - High-Channel Count Electrophysiology'. The text begins with: 'We have designed an FPGA Mezzanine card (standard FMC/Vita 57) for high-channel-count electrophysiology, with 128 channels (potentially up

Processing Unit



Application Specific IPs

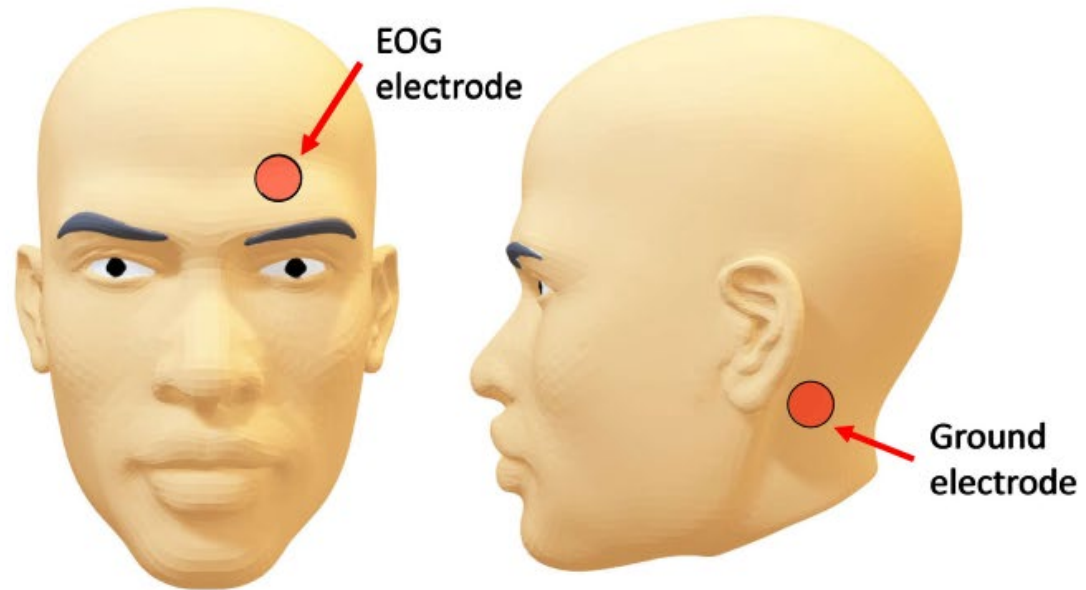
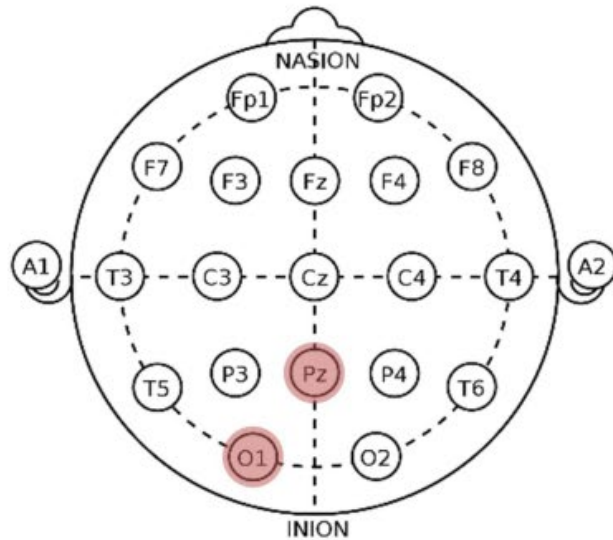


▶ HiCCE Controller

- ▶ Controls individual intan chips and ADCs
 - Channel selection
 - Control sampling rate
- ▶ Decimation
 - Change the data rate

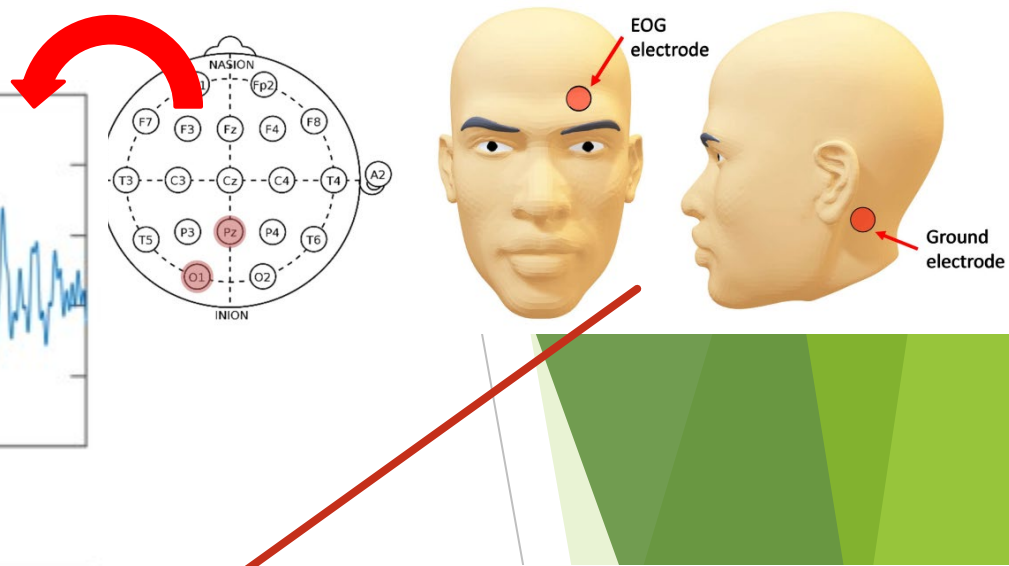
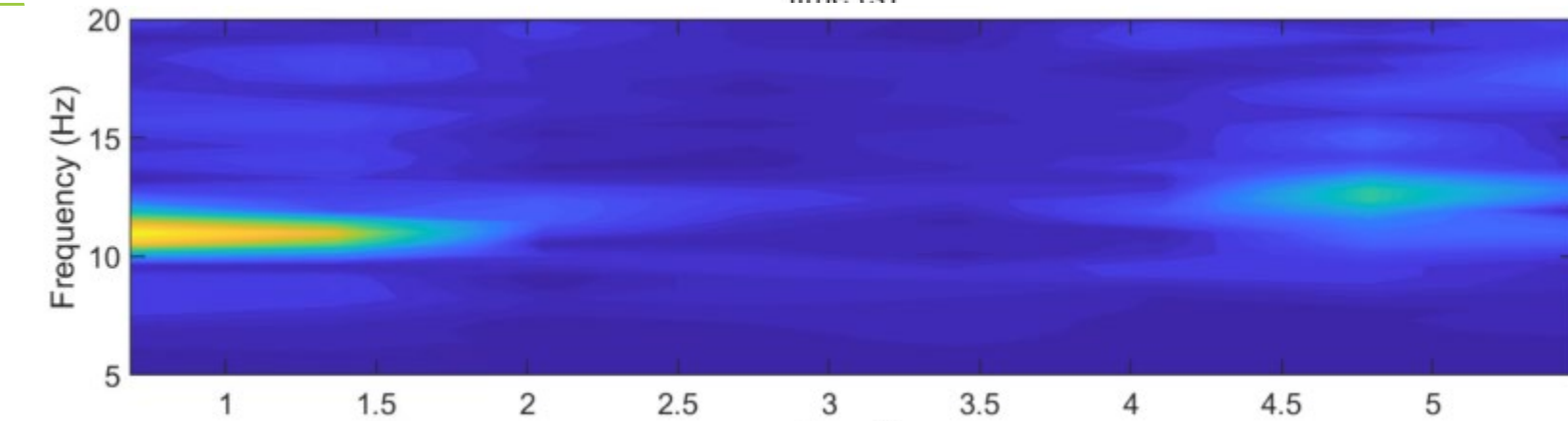
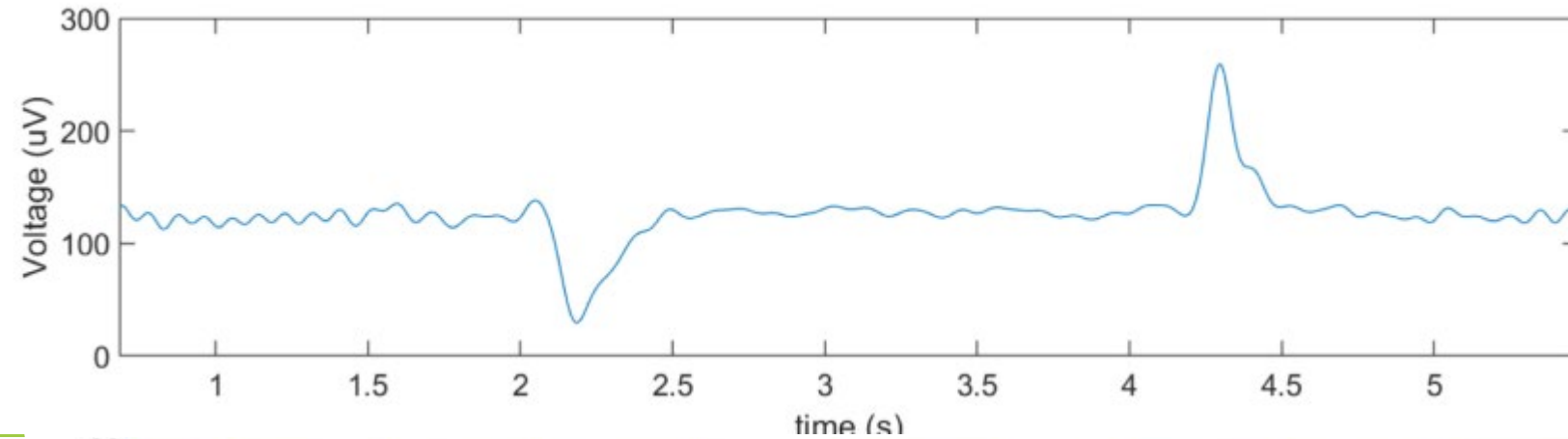
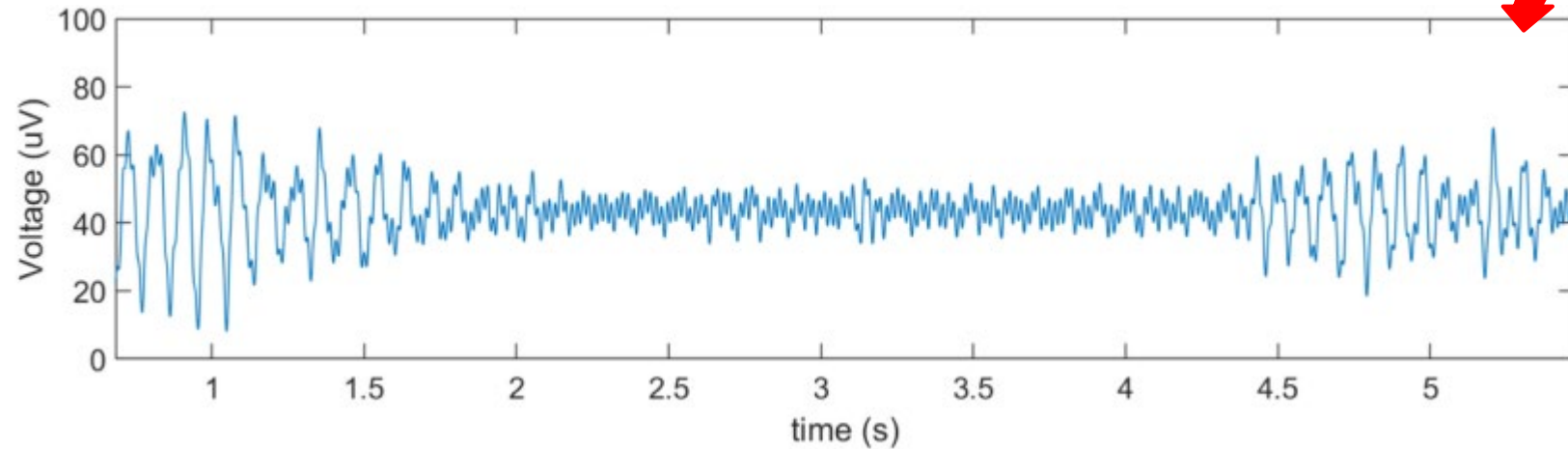
HiCCE experimental tests

1. ALPHA WAVES AND EYE BLINKS



- EEG recording - O1 occipital region
- Reference - the Pz location
- Ground - left earlobe

1. ALPHA WAVES AND EYE BLINKS

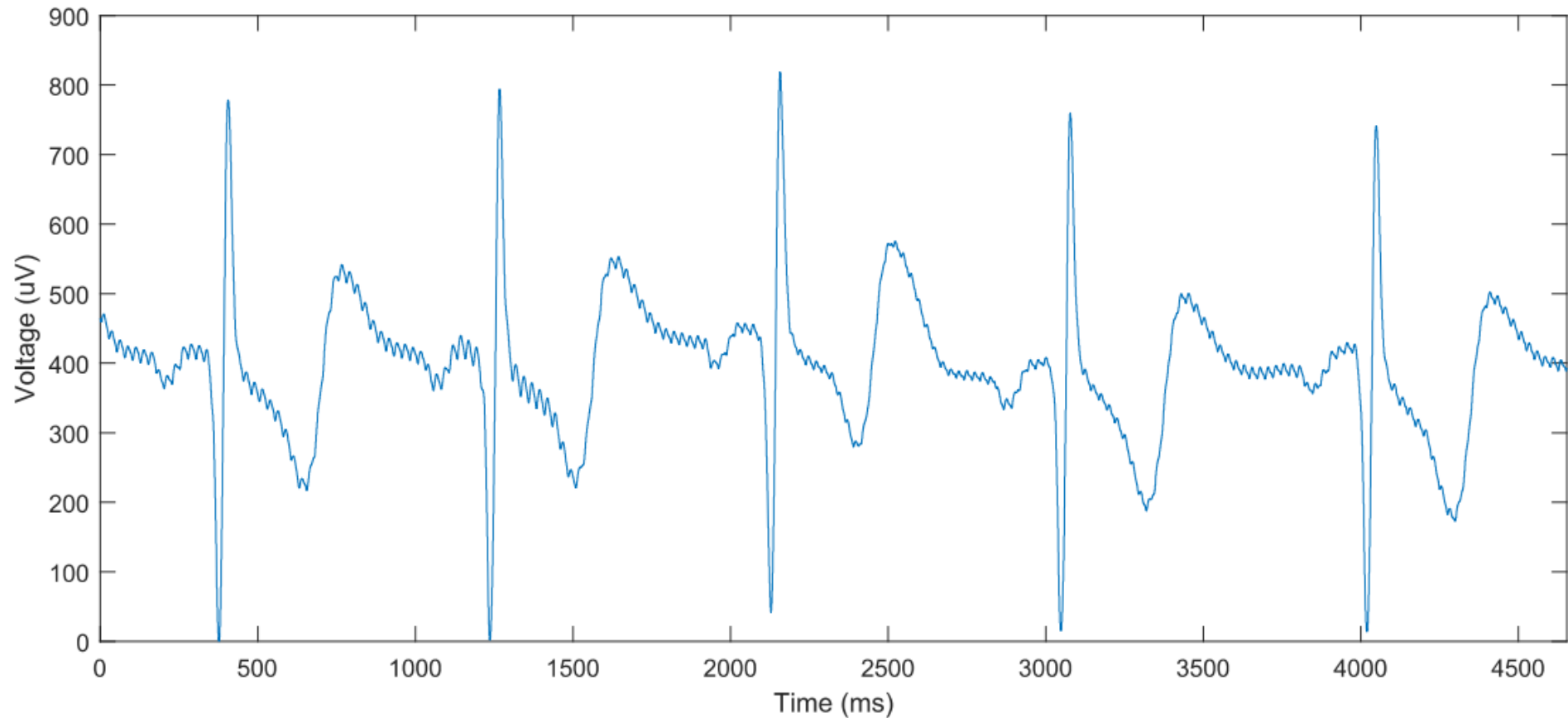
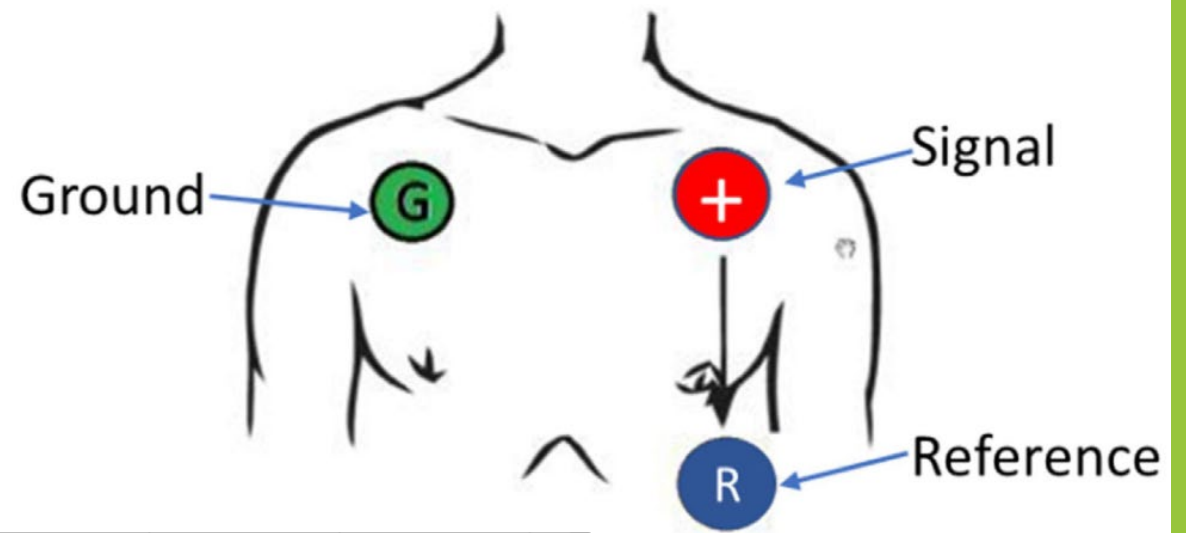


HiCCE
experimental
tests



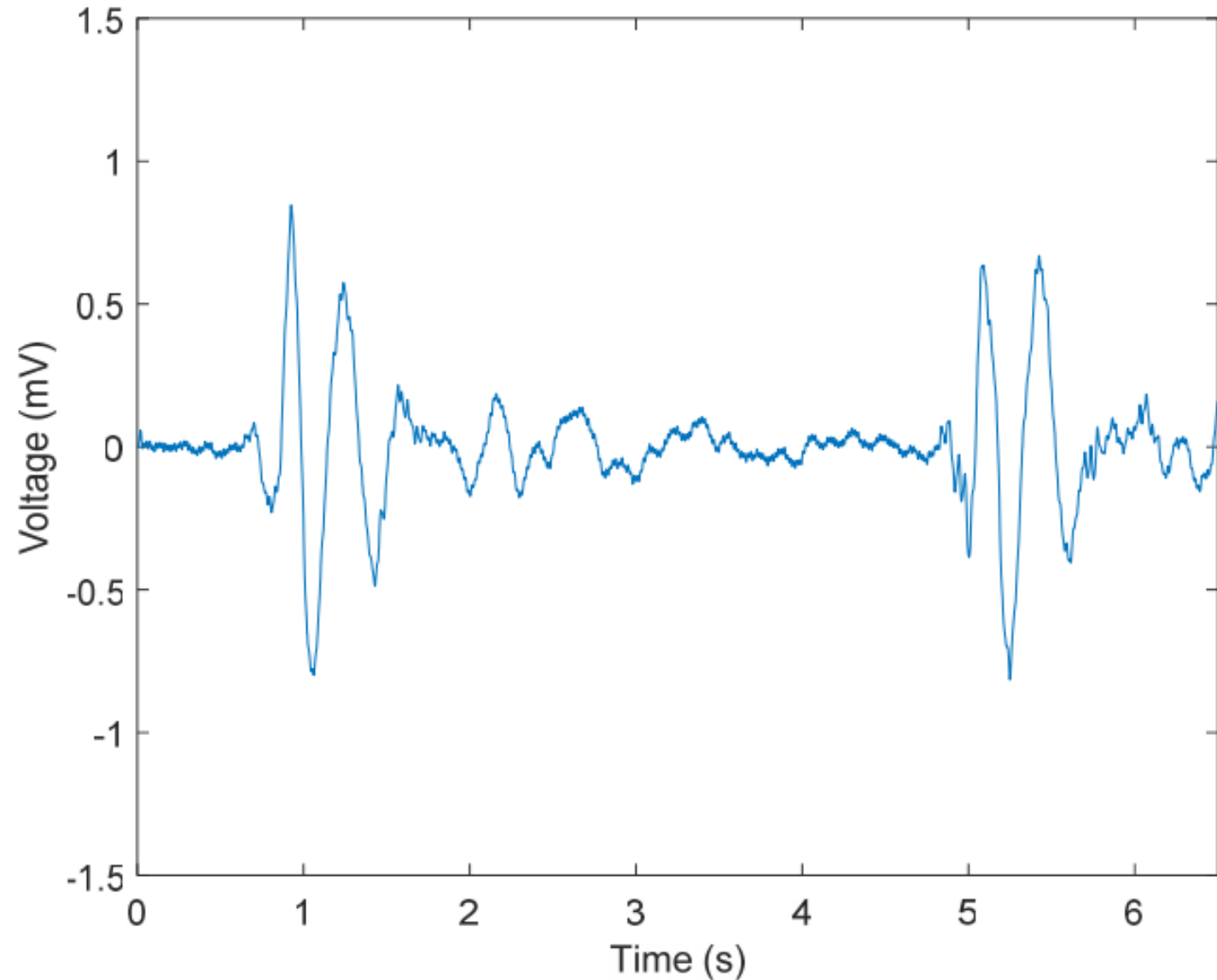
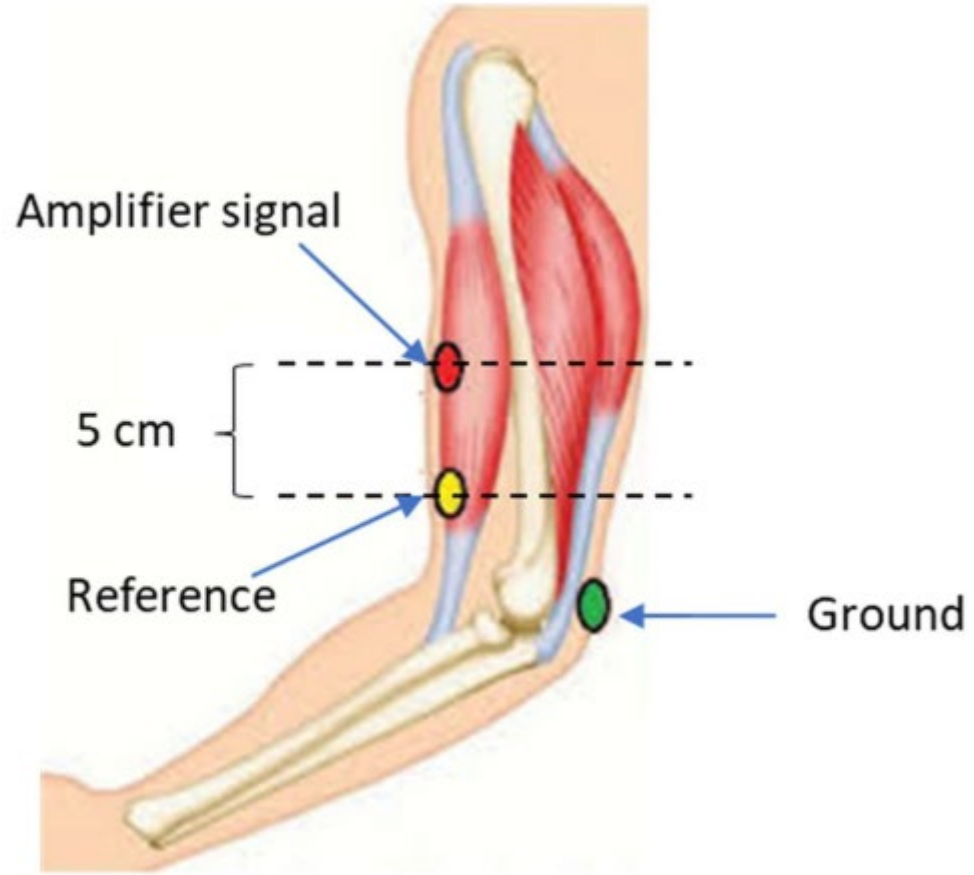
HiCCE experimental tests

2. ECG SIGNAL ACQUISITION



HiCCE experimental tests

3. EMG TEST



POWER USAGE

Resource		Power		
		(W)	(W)	(%)
FPGA Dynamic	CLOCK	0.013	0.036	2
	LOGIC	0.004		
	BRAM	0.014		
	DSP	0.000		
	PLL	0.000		
	MMCM	0.000		
	Other	0.000		
	IO	0.004		
FPGA Static		0.041	0.041	3
Processor Dynamic	LOGIC	0.348	1.390	91
	DDR	1.004		
	IO	0.038		
Processor Static		0.055	0.055	4
Total On-Chip Power			1.521	100

Condition	Voltage (mV)	Current (A)	Power (W)
Device static power	1.7	0.17	2.04
Total Power	2.4	0.24	2.85

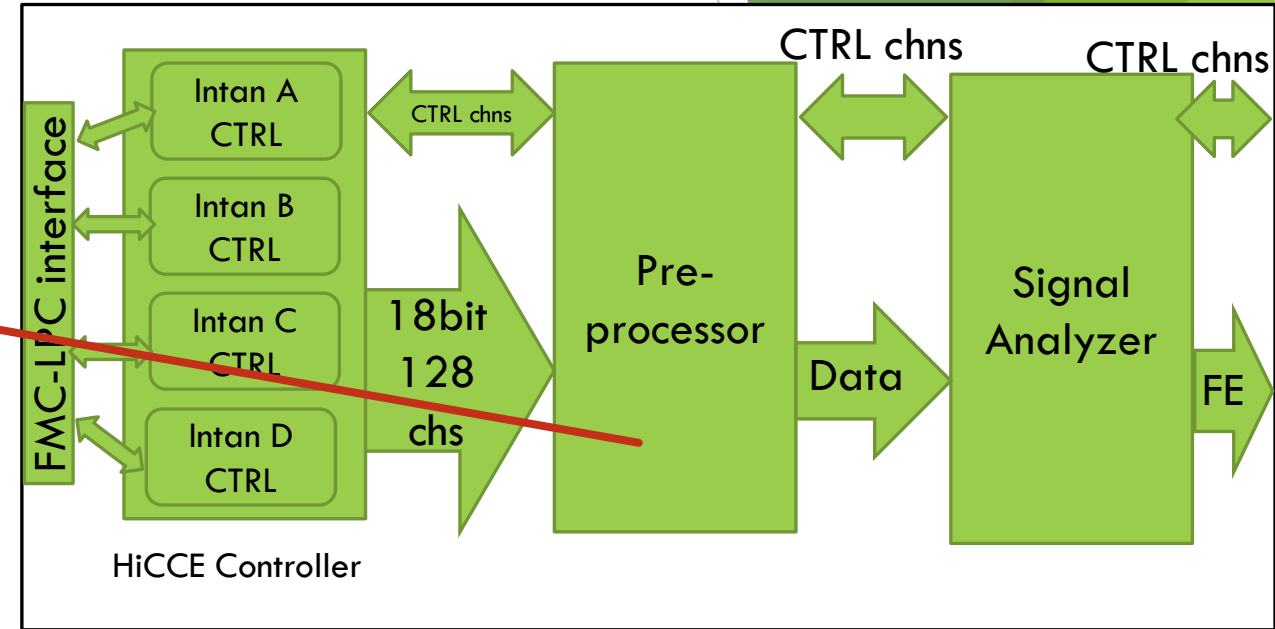
Application Specific IPs

► Pre-processor

- Remove Offset
- Normalize all channels
- Remove artifacts

► filtering

- Low Cutoff frequency = 0.5 Hz
- High Cutoff frequency = 40 Hz
- (suppression of Offset + power line interference)



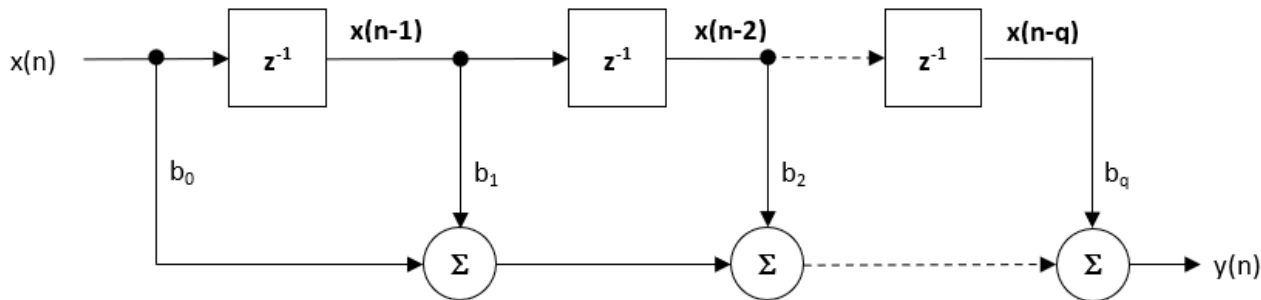
Pre-processing

Digital filtering



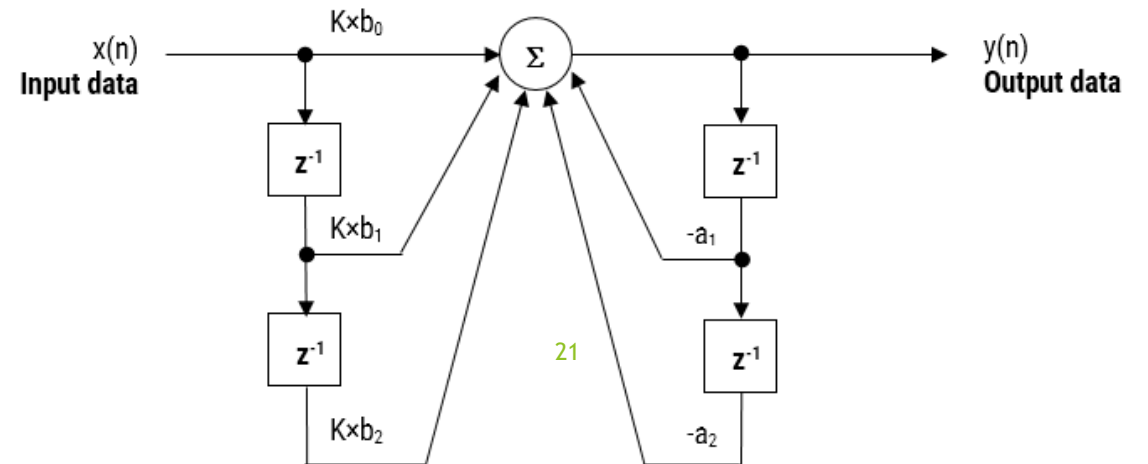
► FIR - Finite impulse response

- Stability
- Linear phase
- Arbitrary frequency response
- High implementation cost
- Higher latency

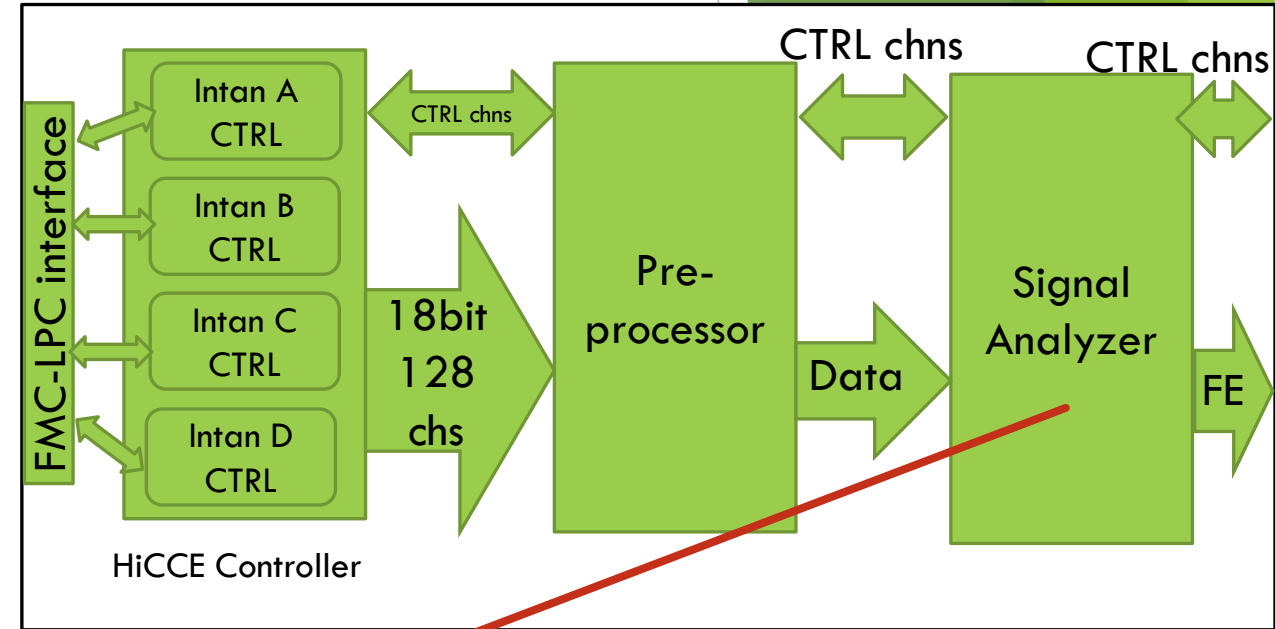


► IIR - Infinite impulse response

- Simple structure
- Low implementation cost
- Low latency
- Analog equivalent
- Less numerical stability
- Non-linear phase characteristics



Application Specific IPs



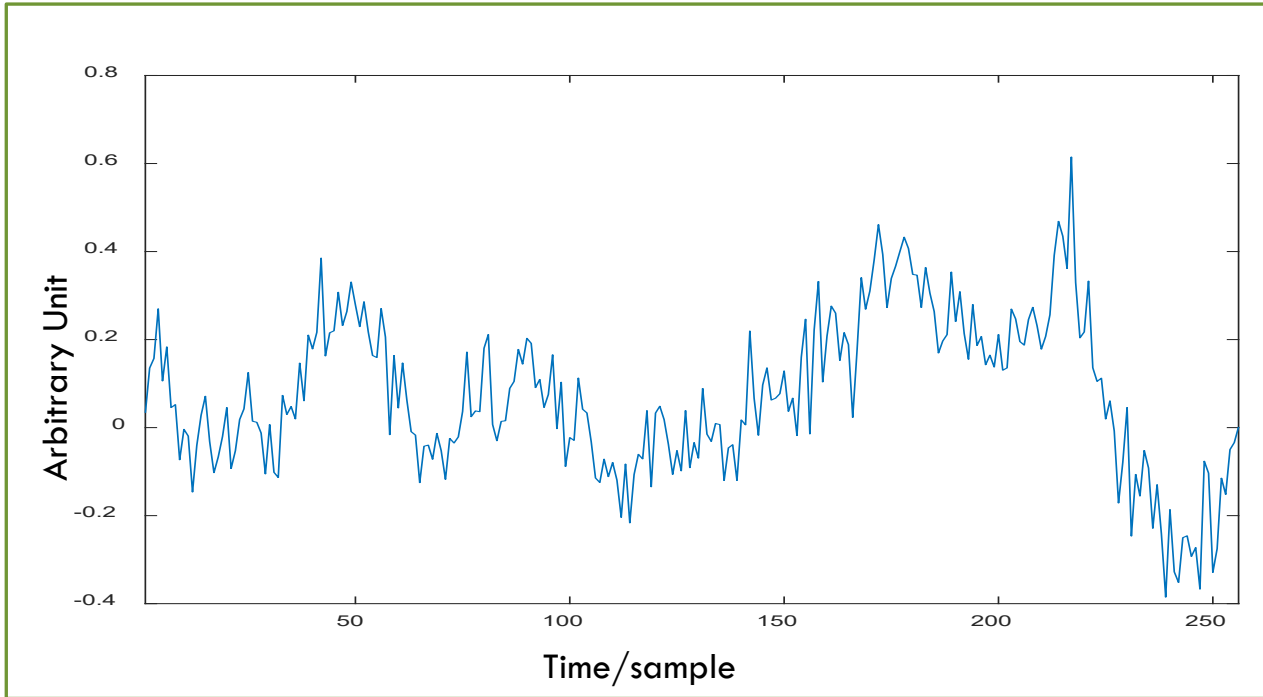
► Signal Analyzer

❖ Time-Frequency Analyzer

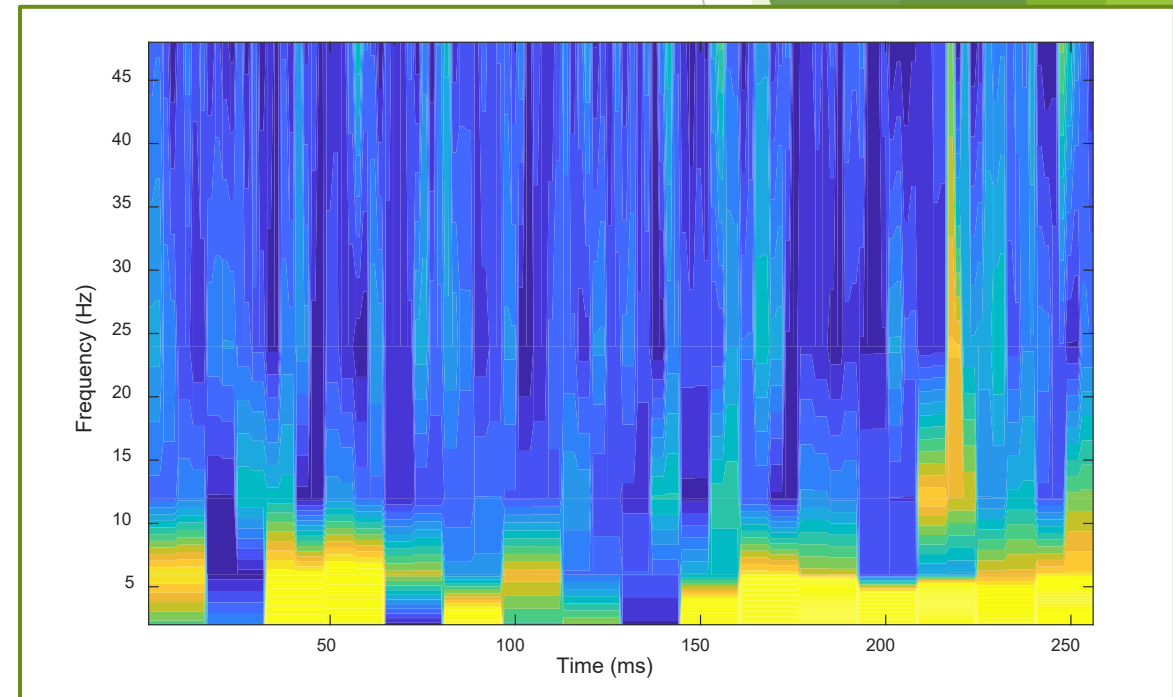
- *Discrete Wavelet Transform (DWT)*
- *Continuous Wavelet Transform (CWT)*
- *Short-Time Fast Fourier Transform (STFFT)*
- *Filter-Hilbert Transform (FHT)*

Signal Analyzer IP

➤ Discrete Wavelet Transform (DWT)



EEG Signal

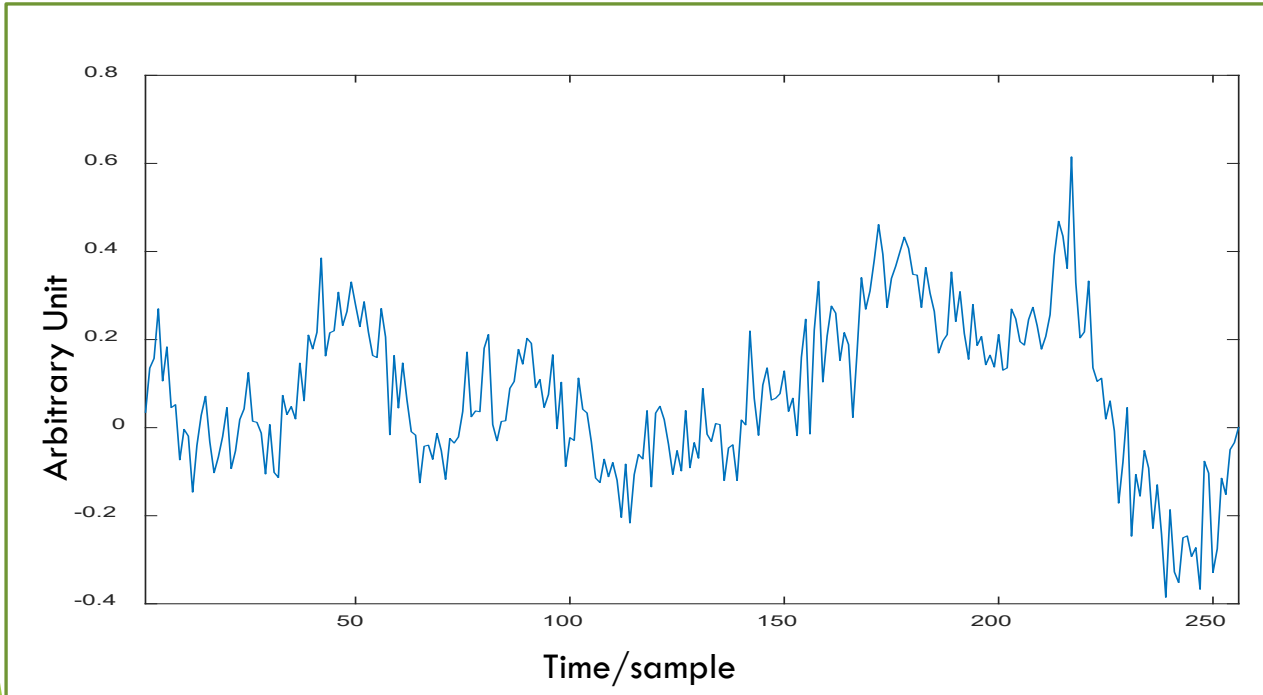


Time – Frequency Graph

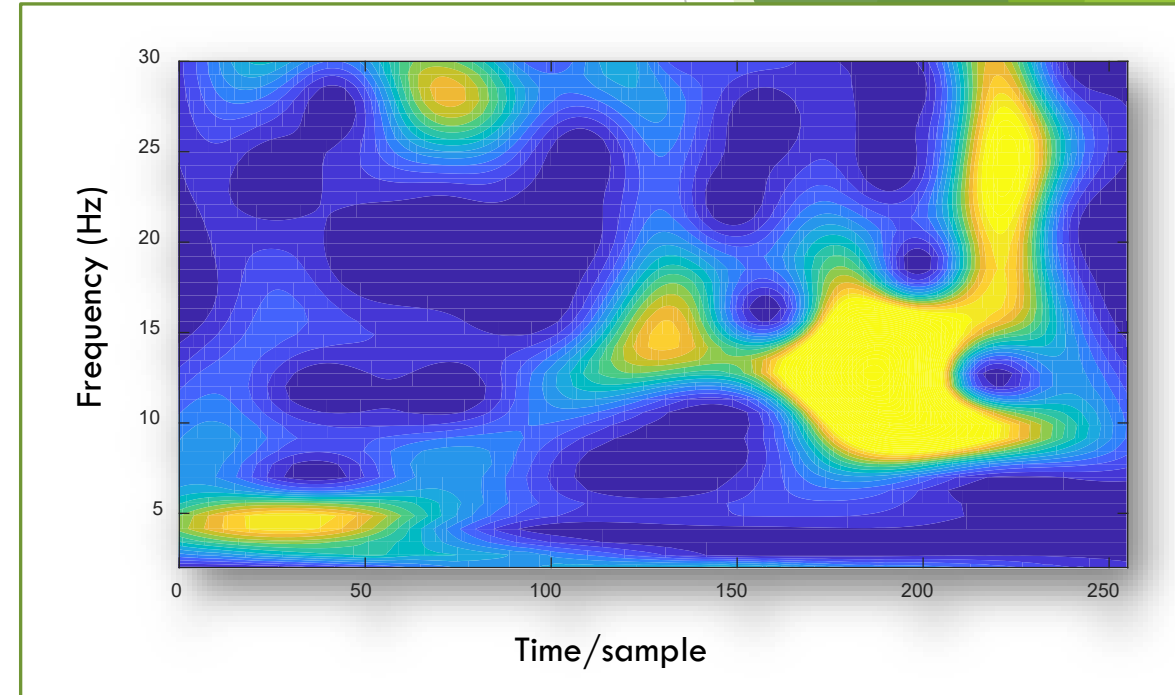
Number of clock cycles = 1028

Signal Analyzer IP

➤ Continuous Wavelet Transform (CWT)



EEG Signal

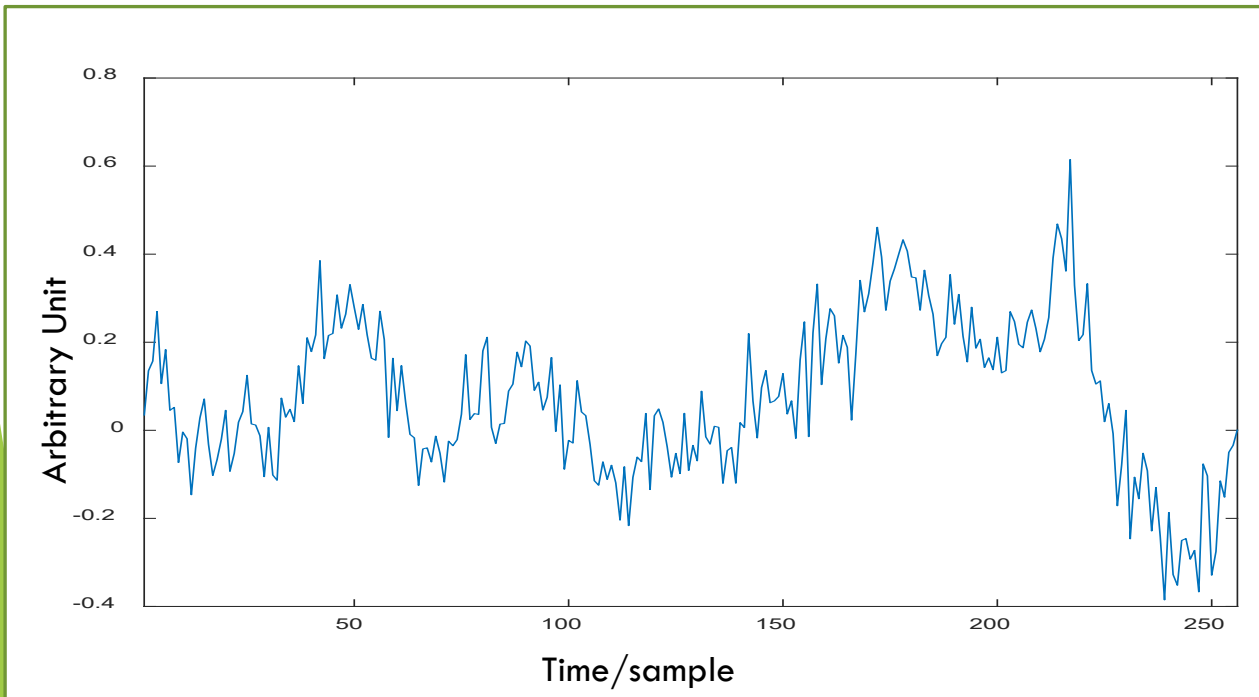


Time – Frequency Graph

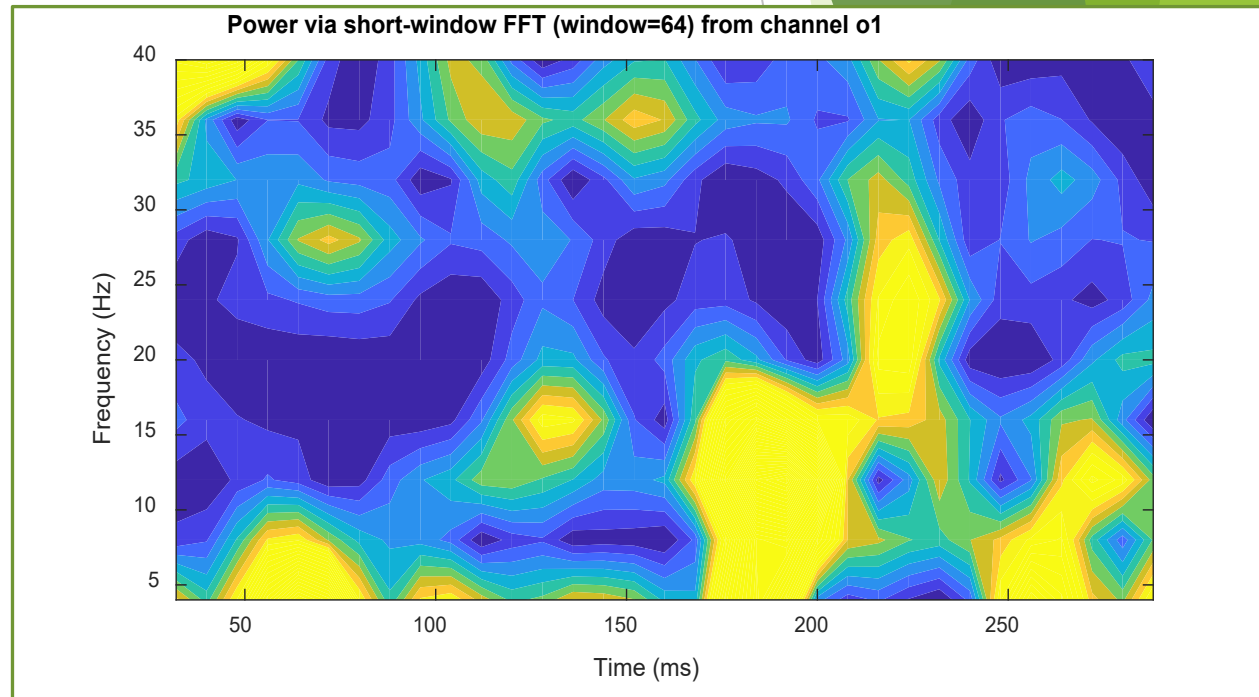
Number of clock cycles = 22809

Signal Analyzer IP

➤ Short-Time Fast Fourier Transform (STFFT)



EEG Signal

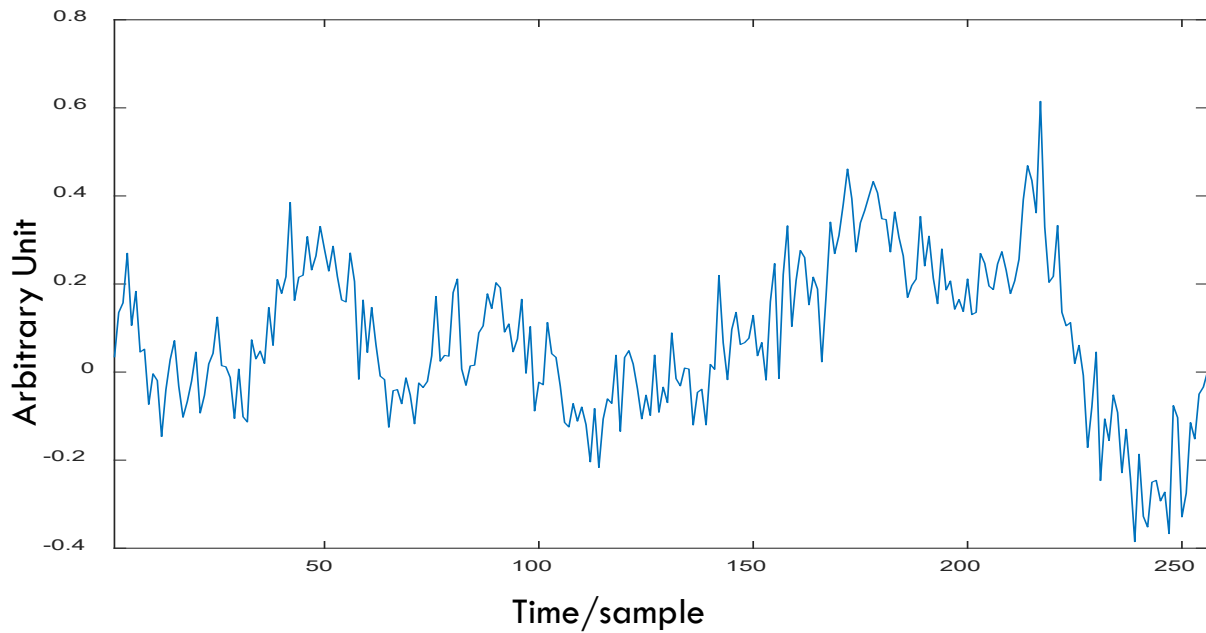


Time – Frequency Graph

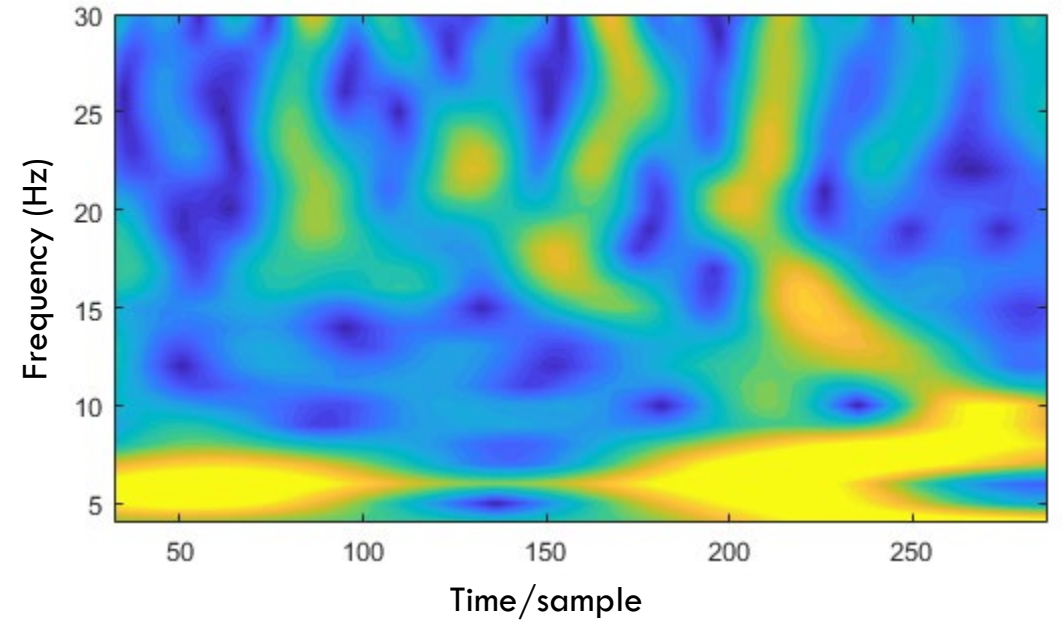
Number of clock cycles = 2346

Signal Analyzer IP

➤ Filter-Hilbert Transform (FHT)



EEG Signal



Time – Frequency Graph

Number of clock cycles = 21273

Signal Analyzer IP

➤ Resource utilization

Resources Method	Registers (106400)	LUTs (53200)	DSPs (220)	BRAMs (140)
Haar	377 (0.35 %)	1181 (2.22 %)	0	0
CWT	12147 (11.42 %)	8920 (16.77 %)	144 (65.45 %)	9.5 (6.78 %)
STFFT	4140 (3.89 %)	3125 (5.87 %)	48 (21.82 %)	2.5 (1.78 %)
Filter - Hilbert	8199 (7.71 %)	6001 (11.28 %)	100 (45.45 %)	8.5 (6.07 %)

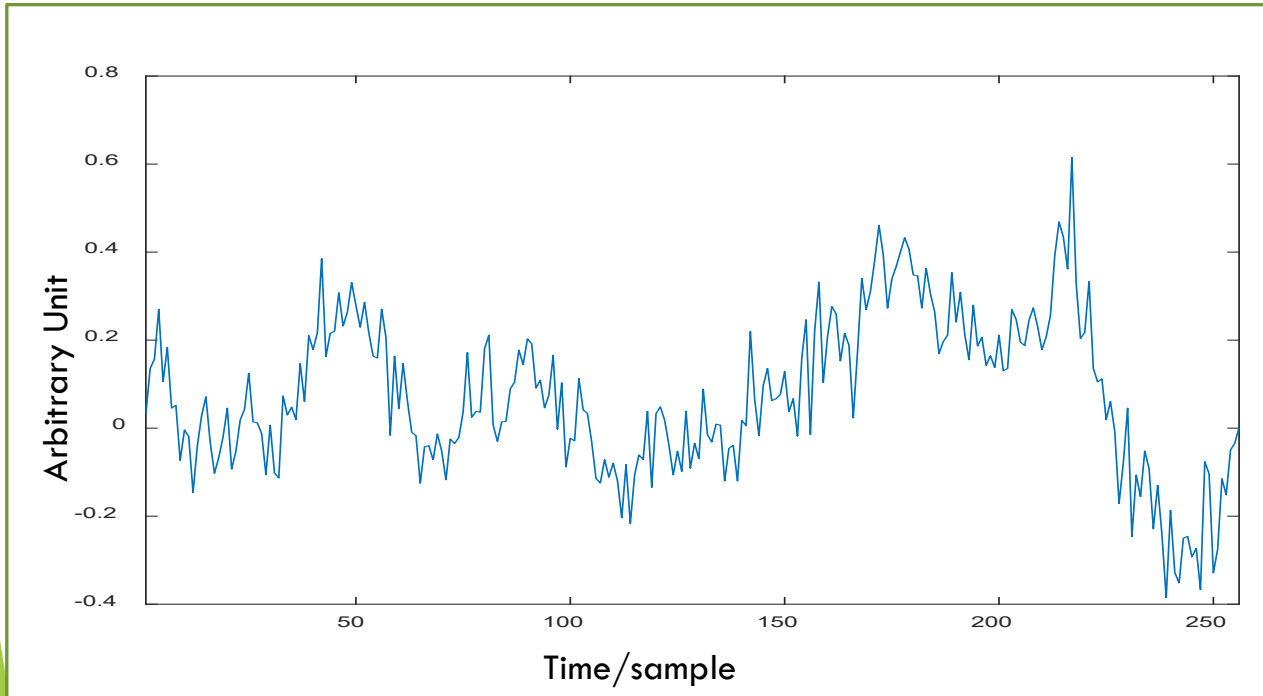
Signal Analyzer IP

- Number of clocks per TF output

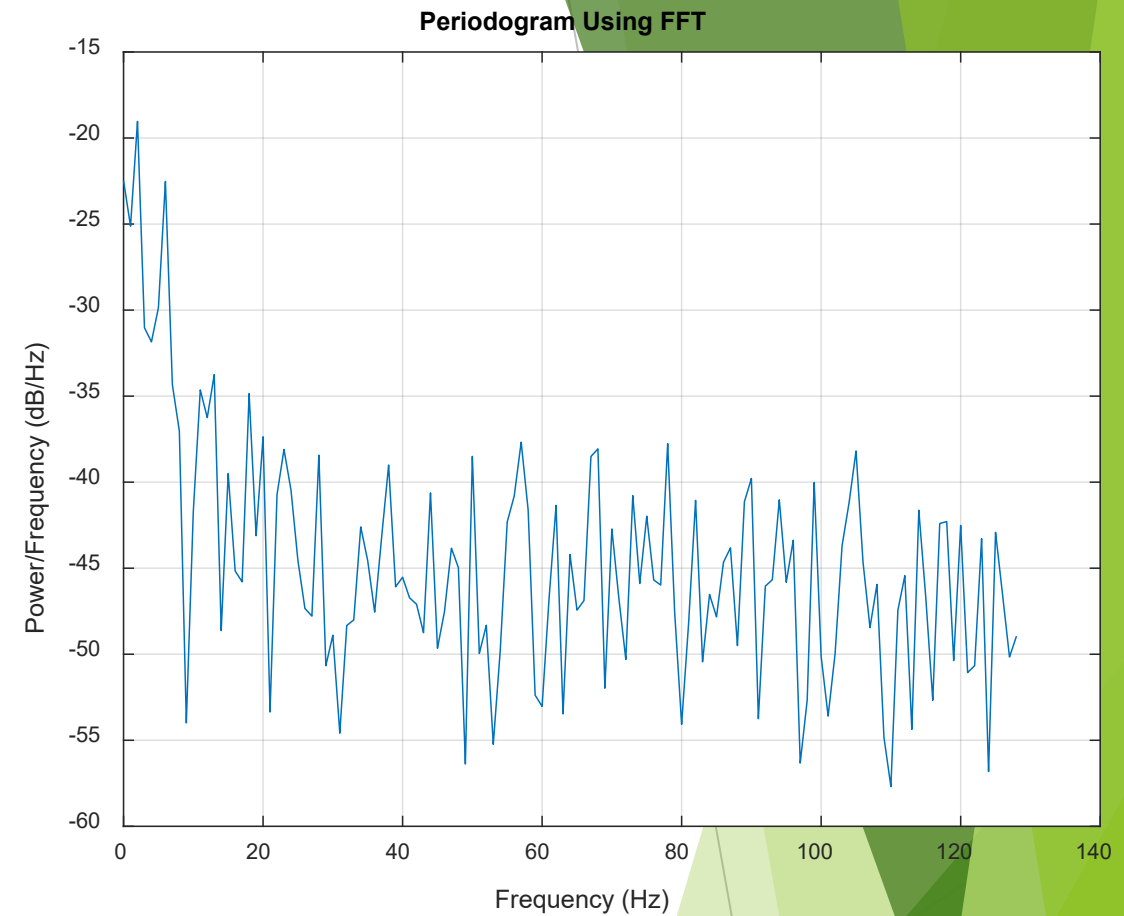
Resources Method	No. clk cycles	Time with 50 MHz clk
Haar	1028	20.56 us
CWT	22809	459.18 us
STFFT	2346	46.92 us
Filter - Hilbert	21273	425.46 us

Feature extractor IP

➤ Power Spectral Density (PSD)



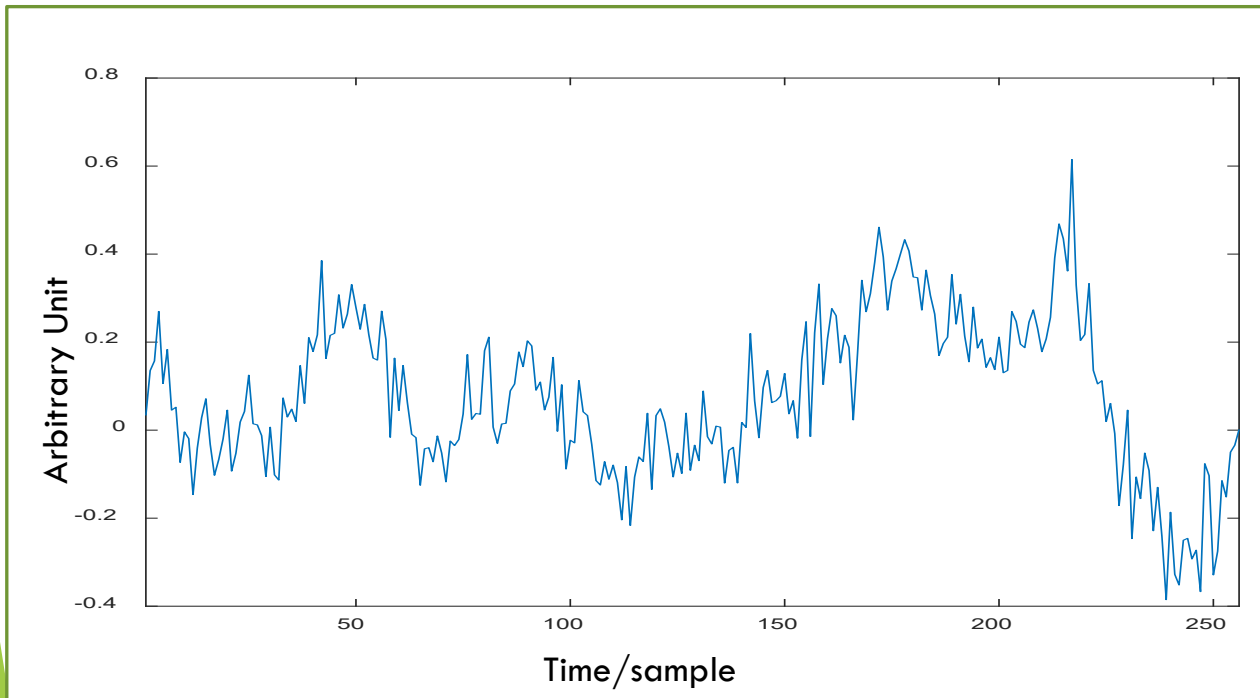
EEG Signal



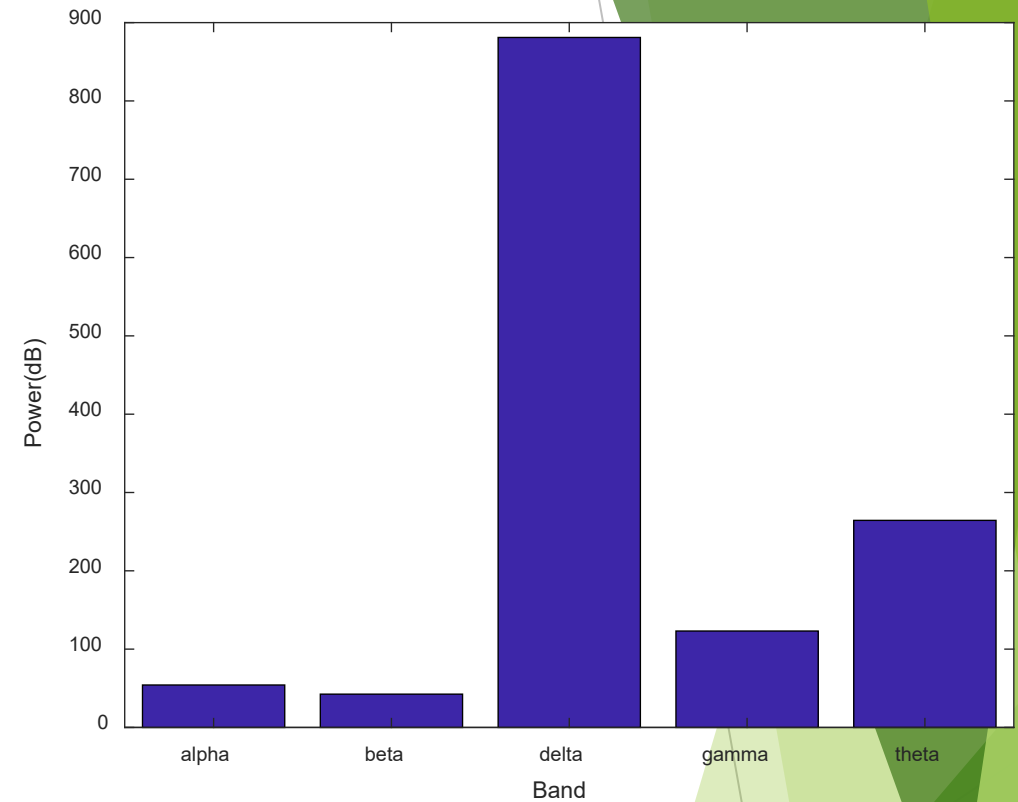
Resources	
Registers	4656
LUTs	3843
BRAMs	5
DSPs	28

Feature extractor IP

➤ Band Energies (BE)



EEG Signal



Resources	
Registers	9180
LUTs	13505
BRAMs	1
DSPs	18

Upper limb rehabilitation

End-effector

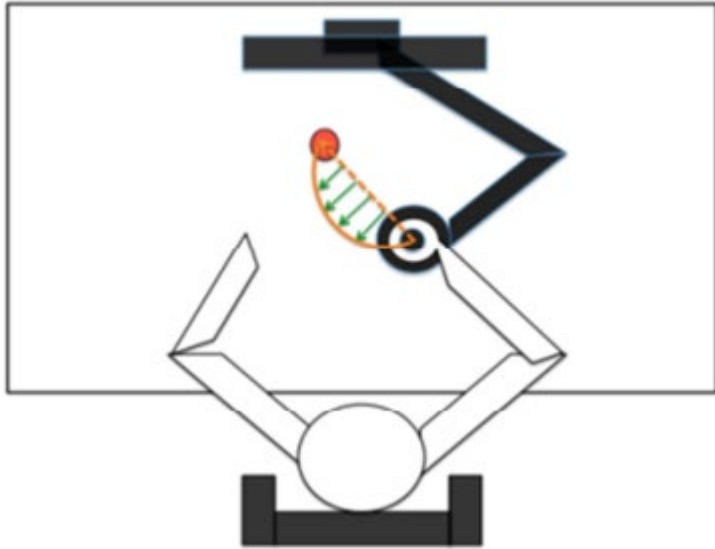
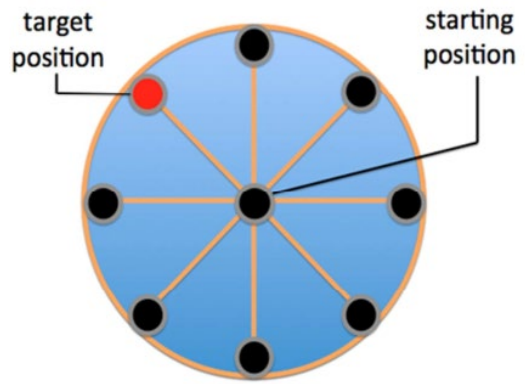
- > simpler structure
- > complex movements
- > complicated control algorithms



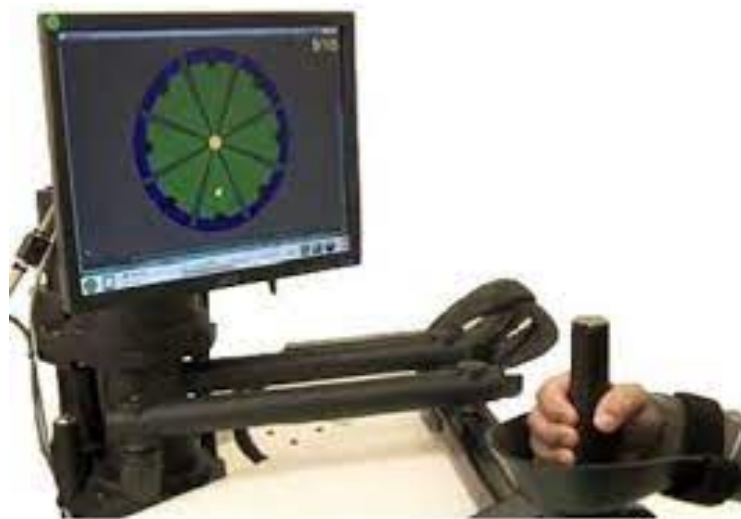
Exoskeleton

- > Long setting-up
- > Safety and comfort concerns
- > complicated control algorithms





- ▶ Movements tracking
- ▶ EEG
- ▶ EMG
- ▶ Force field feedbacks
- ▶ Visual feedbacks





Thank you!