

Outline

- Introduction – *“Is there a limit?”*
- Transistors – *“CMOS building blocks”*
- Parasitics I – *“The [un]desirables”*
- Parasitics II – *“Building a full MOS model”*
- The CMOS inverter – *“A masterpiece”*
- Technology scaling – *“Smaller, Faster and Cooler”*
- Technology – *“Building an inverter”*
- Gates I – *“Just like LEGO”*
- The pass gate – *“An useful complement”*
- Gates II – *“A portfolio”*
- Sequential circuits – *“Time also counts!”*
- DLLs and PLLs – *“A brief introduction”*
- Storage elements – *“A bit in memory”*

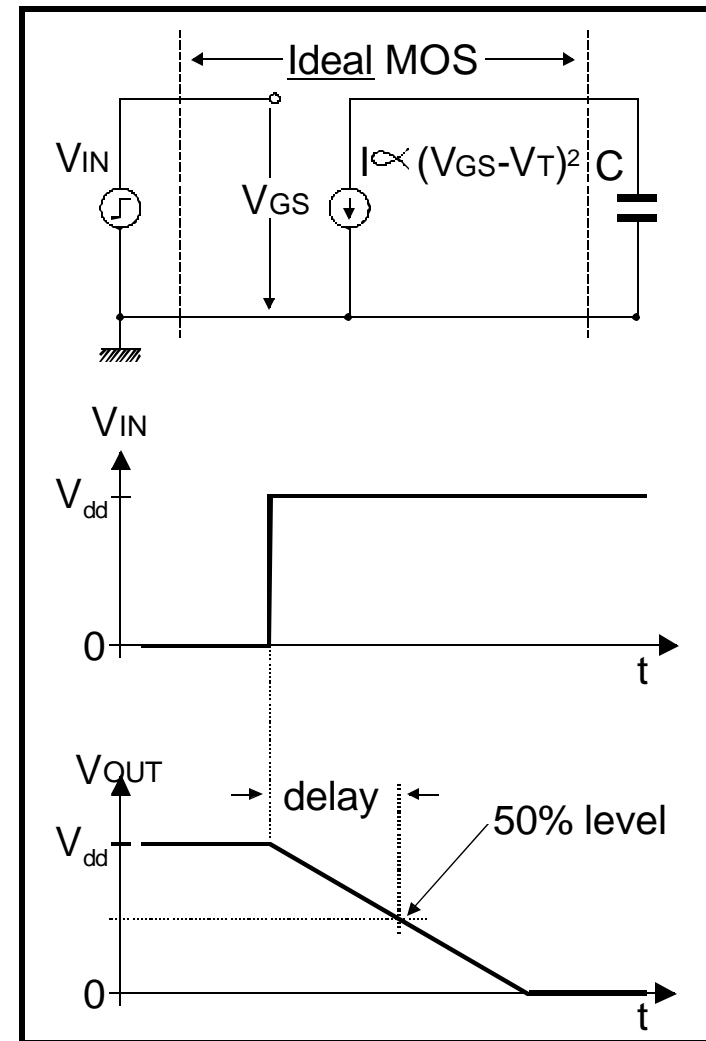
“The [un]desirables”

- Delay in CMOS circuits
- MOSFET capacitances:
 - Physical structure
 - Channel
 - p-n junctions

What causes delay?

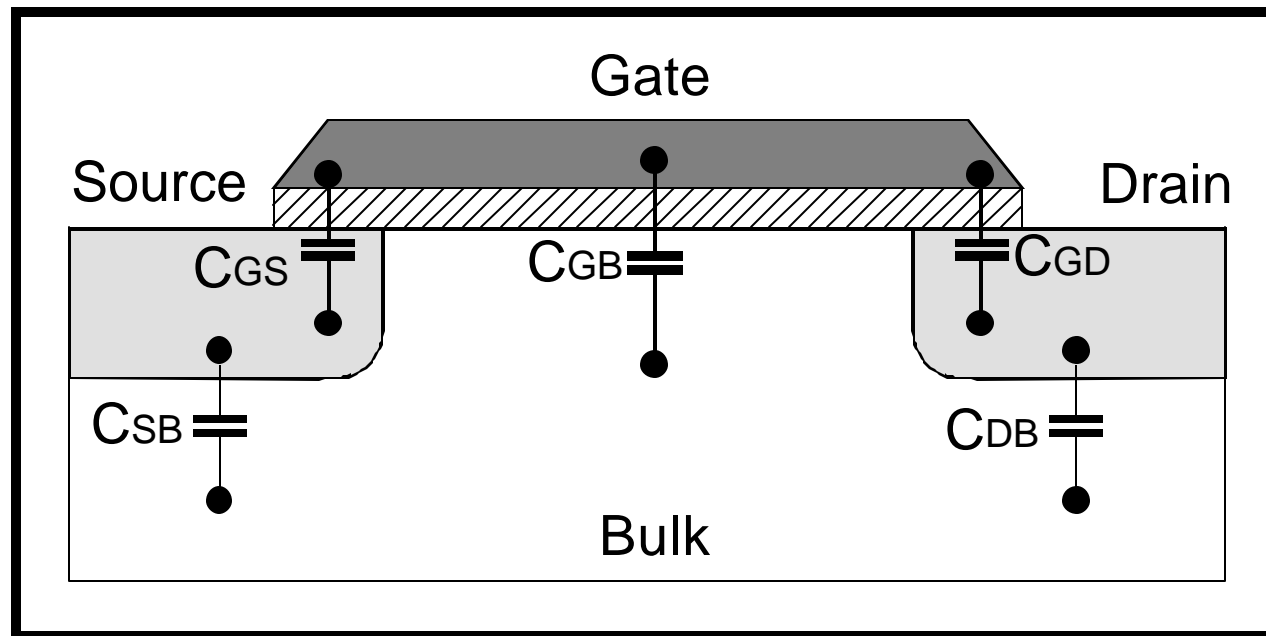
- In MOS circuits capacitive loading is the main cause
- Due to:
 - Device capacitance
 - Interconnect capacitance

$$\Delta t = C \cdot \frac{\Delta V}{I} \approx \frac{C}{2 \cdot \mu \cdot C_{ox} \cdot V_{dd}} \cdot \frac{L}{W}$$



MOSFET capacitances

- MOS capacitances have three origins:
 - The basic MOS structure
 - The channel charge
 - The pn-junctions depletion regions



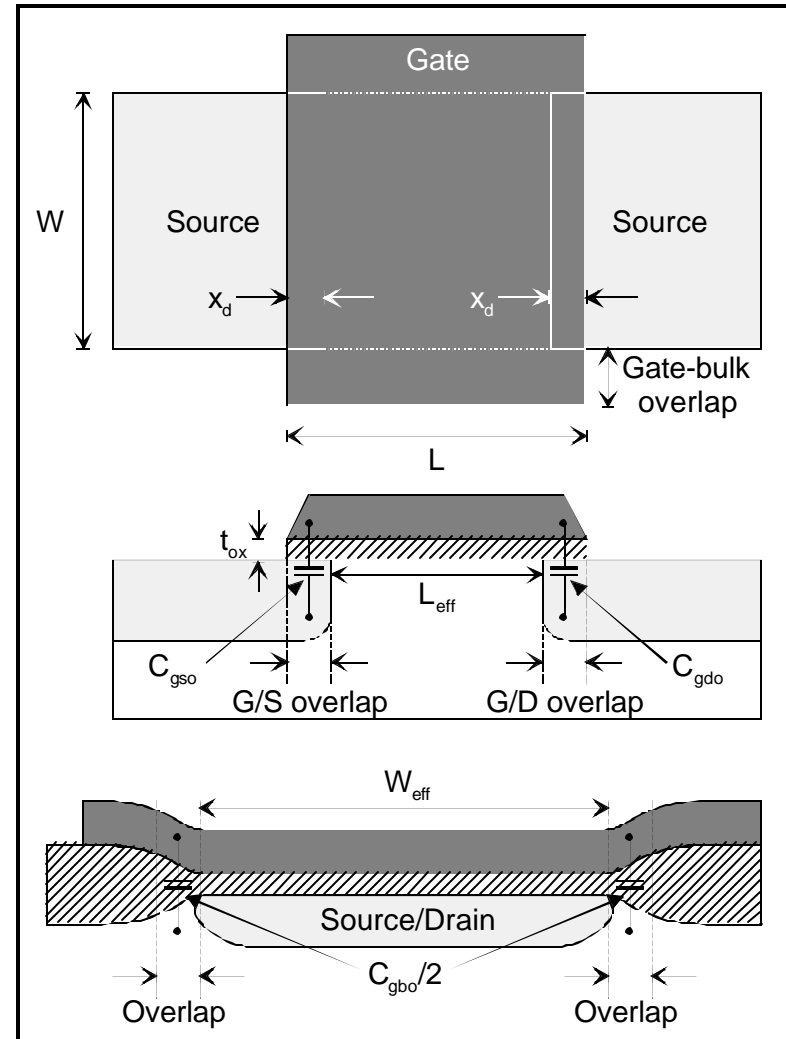
MOS structure capacitances

- Source/drain diffusion extend below the gate oxide by:
 x_d - the lateral diffusion
- This gives origin to the source/drain overlap capacitances:

$$C_{gso} = C_{gdo} = C_o \times W$$

$$C_o \text{ (F / m)}$$
- Gate-bulk overlap capacitance:

$$C_{gbo} = C'_o \times L, \quad C'_o \text{ (F / m)}$$



MOS structure capacitances

0.24 μm process

NMOS

$L(\text{drawn}) = 0.24 \mu\text{m}$

$L(\text{effective}) = 0.18 \mu\text{m}$

$W(\text{drawn}) = 2 \mu\text{m}$

$C_o (s, d, b) = 0.36 \text{ fF}/\mu\text{m}$

$C_{ox} = 5.6 \text{ fF}/\mu\text{m}^2$

$C_{gso} = C_{gdo} = 0.72 \text{ fF}$

$C_{gbo} = 0.086 \text{ fF}$

$C_g = 2.02 \text{ fF}$

Channel capacitance

- The channel capacitance is nonlinear
- Its value depends on the operation region
- Its formed of three components:
 - C_{gb} - gate-to-bulk capacitance
 - C_{gs} - gate-to-source capacitance
 - C_{gd} - gate-to-drain capacitance

<i>Operation region</i>	C_{gb}	C_{gs}	C_{gd}
Cutoff	$C_{ox} W L$	0	0
Linear	0	$(1/2) C_{ox} W L$	$(1/2) C_{ox} W L$
Saturation	0	$(2/3) C_{ox} W L$	0

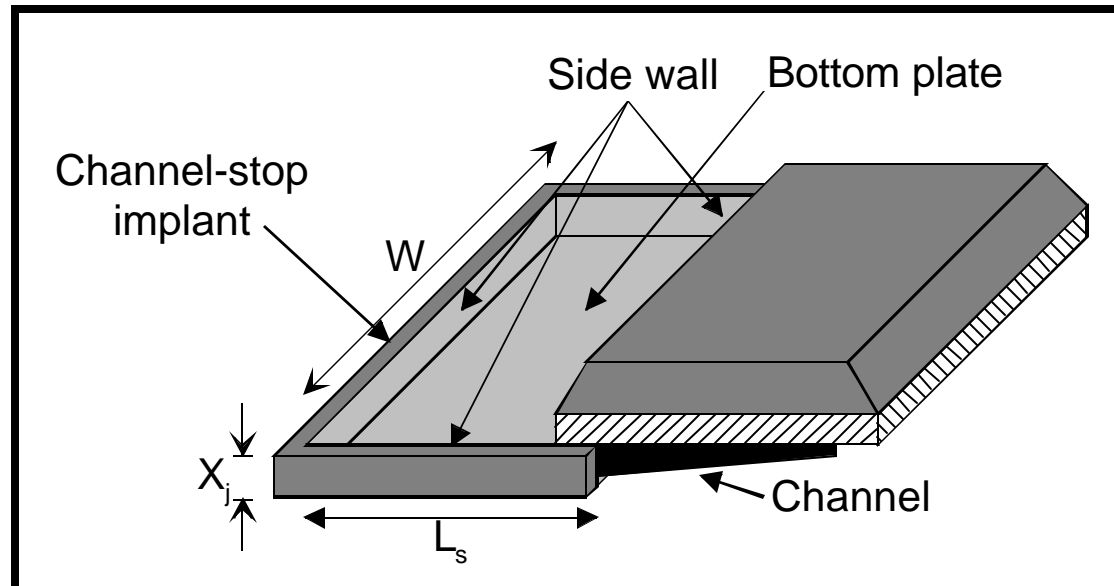
Junction capacitances

- C_{sb} and C_{db} are diffusion capacitances composed of:
 - Bottom-plate capacitance:

$$C_{bottom} = C_j \cdot W \cdot L_s$$

- Side-wall capacitance:

$$C_{sw} = C_{jsw} \cdot (2 L_s + W)$$



Junction capacitances

0.24 μm process

NMOS

$L(\text{drawn}) = 0.24 \mu\text{m}$

$L(\text{effective}) = 0.18 \mu\text{m}$

$W(\text{drawn}) = 2 \mu\text{m}$

$L_s = 0.8 \mu\text{m}$

$C_j(s, d) = 1.05 \text{ fF}/\mu\text{m}^2$

$C_{j\text{sw}} = 0.09 \text{ fF}/\mu\text{m}$

$C_{\text{bottom}} = 1.68 \text{ fF}$

$C_{\text{sw}} = 0.32 \text{ fF}$

$C_g = 2.02 \text{ fF}$