Outline

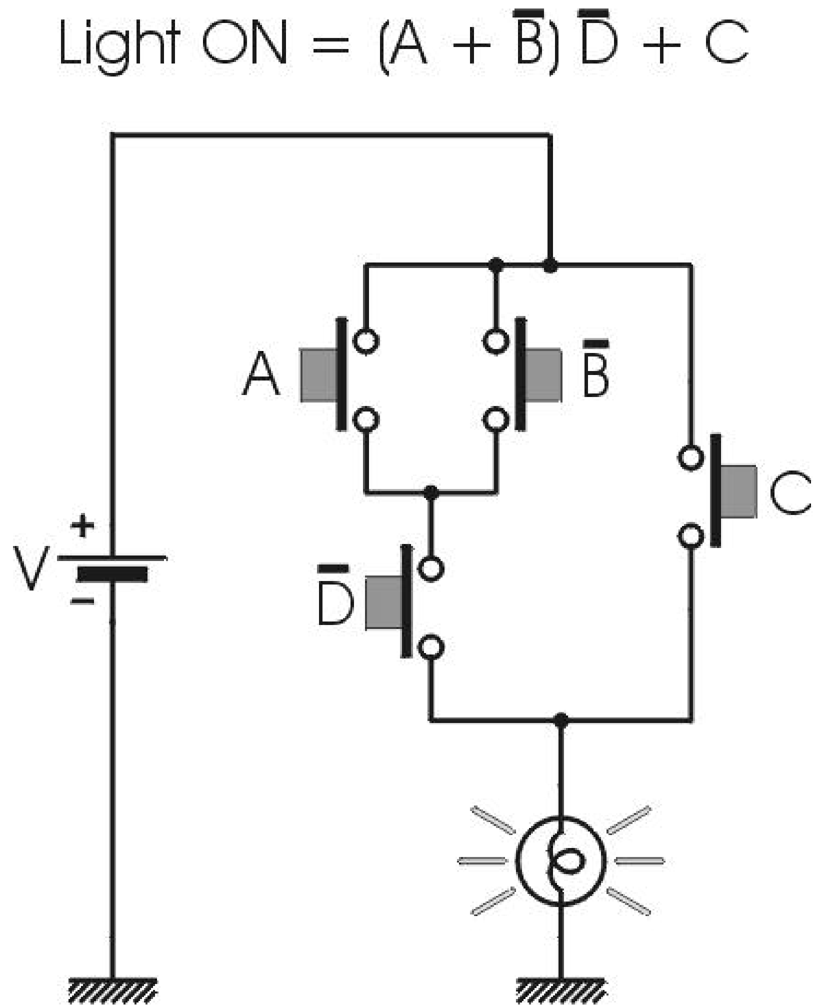
- Introduction – *“Is there a limit?”*
- Transistors – *“CMOS building blocks”*
- Parasitics I – *“The [un]desirables”*
- Parasitics II – *“Building a full MOS model”*
- The CMOS inverter – *“A masterpiece”*
- Technology scaling – *“Smaller, Faster and Cooler”*
- Technology – *“Building an inverter”*
- Gates I – *“Just like LEGO”*
- The pass gate – *“An useful complement”*
- Gates II – “A portfolio”
- Sequential circuits – *“Time also counts!”*
- DLLs and PLLs – “ A brief introduction”
- Storage elements – *“A bit in memory”*

“CMOS building blocks”

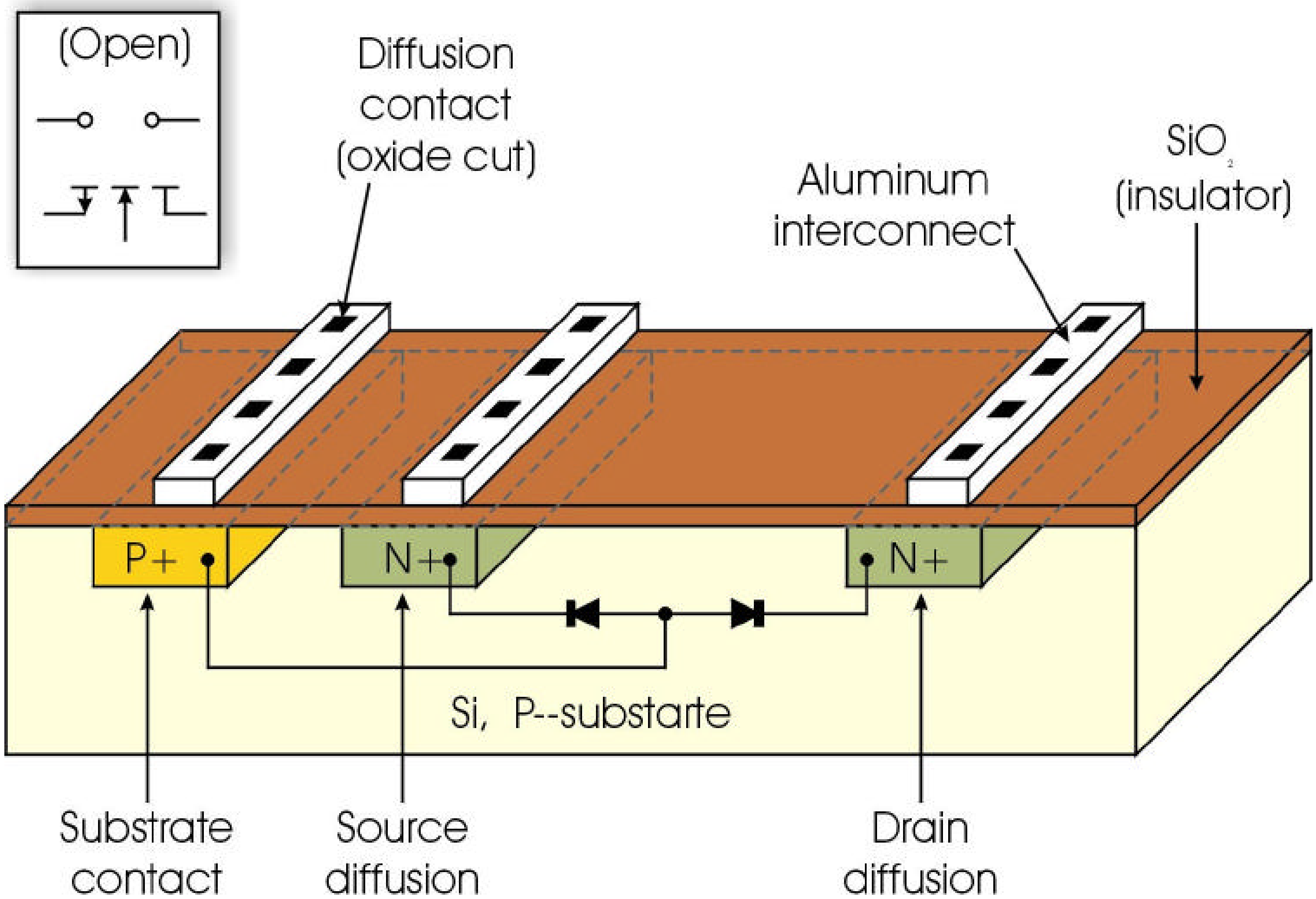
- “Making Logic”
- Silicon switches:
  – The NMOS
  – Its mirror image, the PMOS
- Electrical behavior:
  – Strong inversion
    - Model
    - How good is the approximation?
  – Weak inversion
  – Gain and inversion

“Making Logic”

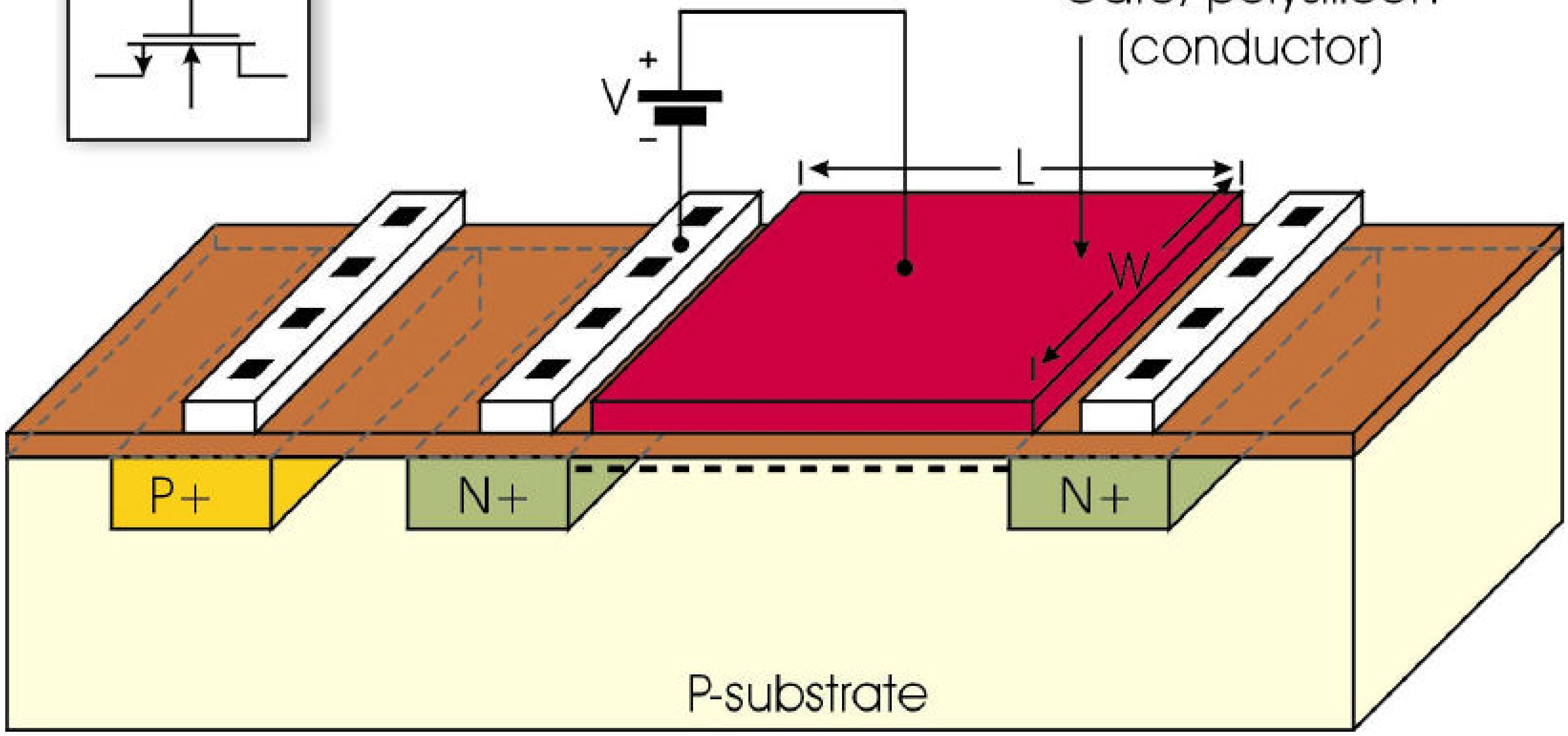
- Logic circuit “ingredients”:
  - Power source
  - Switches
  - Power gain
  - Inversion
- Power always comes from some form of external EMF generator.
- NMOS and PMOS transistors:
  - Can perform the last three functions
  - They are the building blocks of CMOS technologies!



Silicon switches: the NMOS

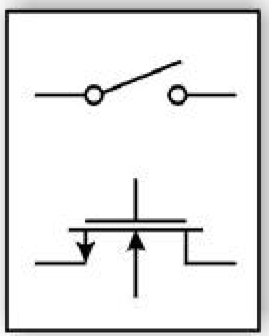


Silicon switches: the NMOS

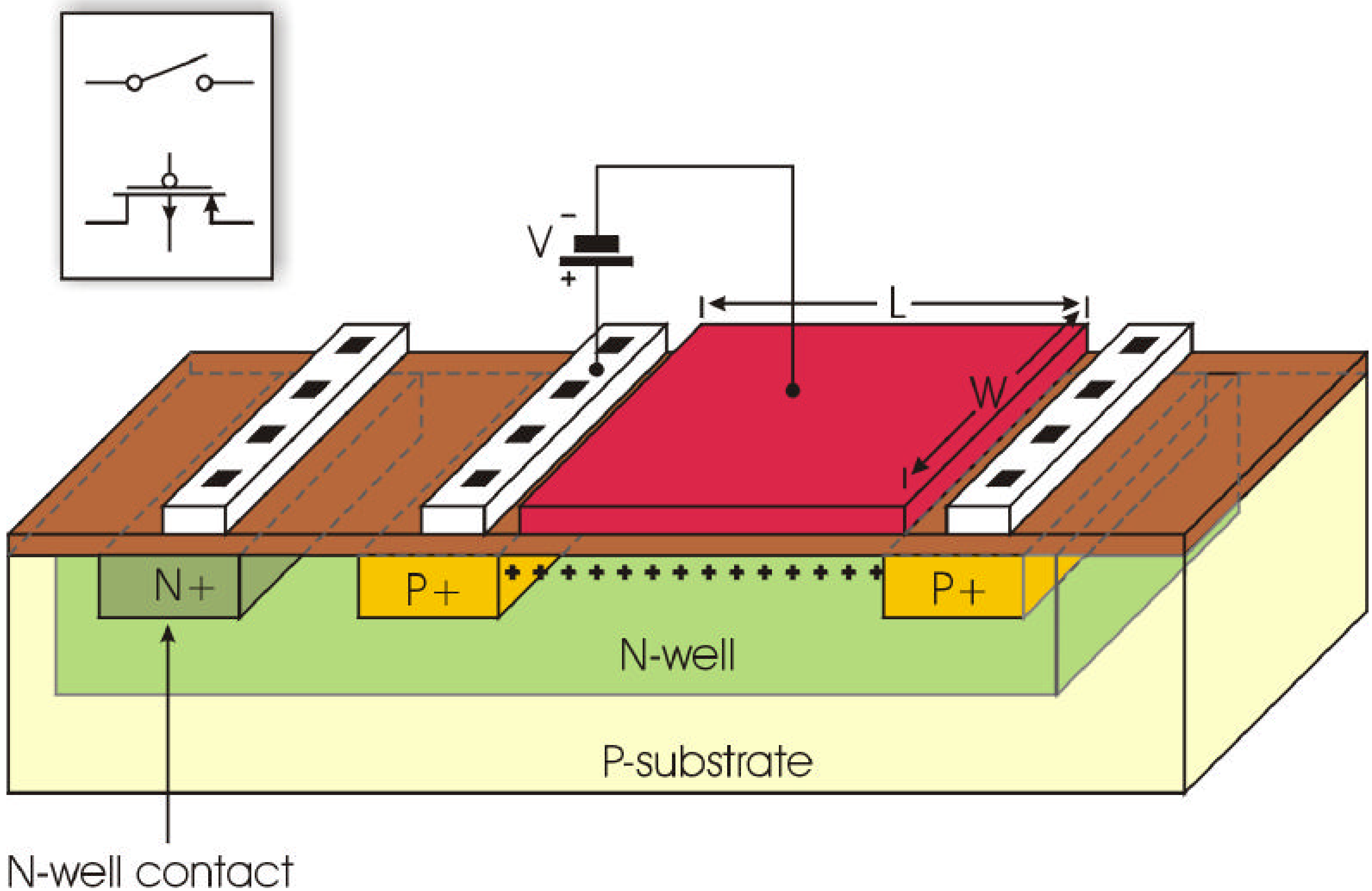


Above silicon:

- Thin oxide (SiO_2) under the gate areas;
- Thick oxide everywhere else;



Silicon switches: the PMOS



MOSFET equations

- Cut-off region

$$I_{ds} = 0 \quad \text{for} \quad V_{gs} - V_T < 0$$

- Linear region

$$I_{ds} = m \cdot C_{ox} \cdot \frac{W}{L} \cdot \left[\left(V_{gs} - V_T \right) \cdot V_{ds} - \frac{V_{ds}^2}{2} \right] \cdot \left(1 + l \cdot V_{ds} \right) \text{ for } 0 < V_{ds} < V_{gs} - V_T$$

- Saturation

$$I_{ds} = \frac{m \cdot C_{ox}}{2} \cdot \frac{W}{L} \cdot \left(V_{gs} - V_T \right)^2 \cdot \left(1 + l \cdot V_{ds} \right) \text{ for } V_{ds} > V_{gs} - V_T$$

- Oxide capacitance

$$C_{ox} = \frac{e_{ox}}{t_{ox}} \quad \left(\mathrm{F} / \mathrm{m}^2 \right)$$

- Process “transconductance”

$$m \cdot C_{ox} = \frac{m \cdot e_{ox}}{t_{ox}} \quad \left(\mathrm{A} / \mathrm{V}^2 \right)$$

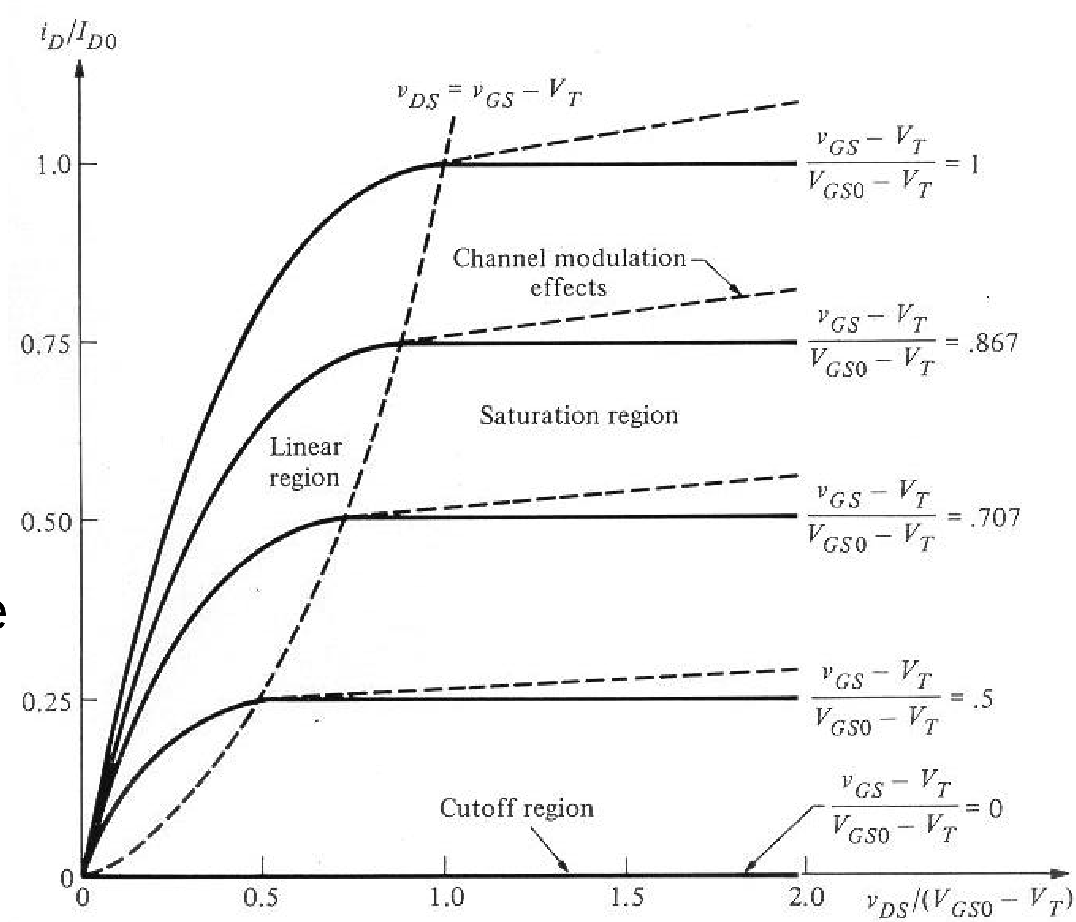
<u>0.24µm process</u>

t_{ox} = 5nm (~10 atomic layers)

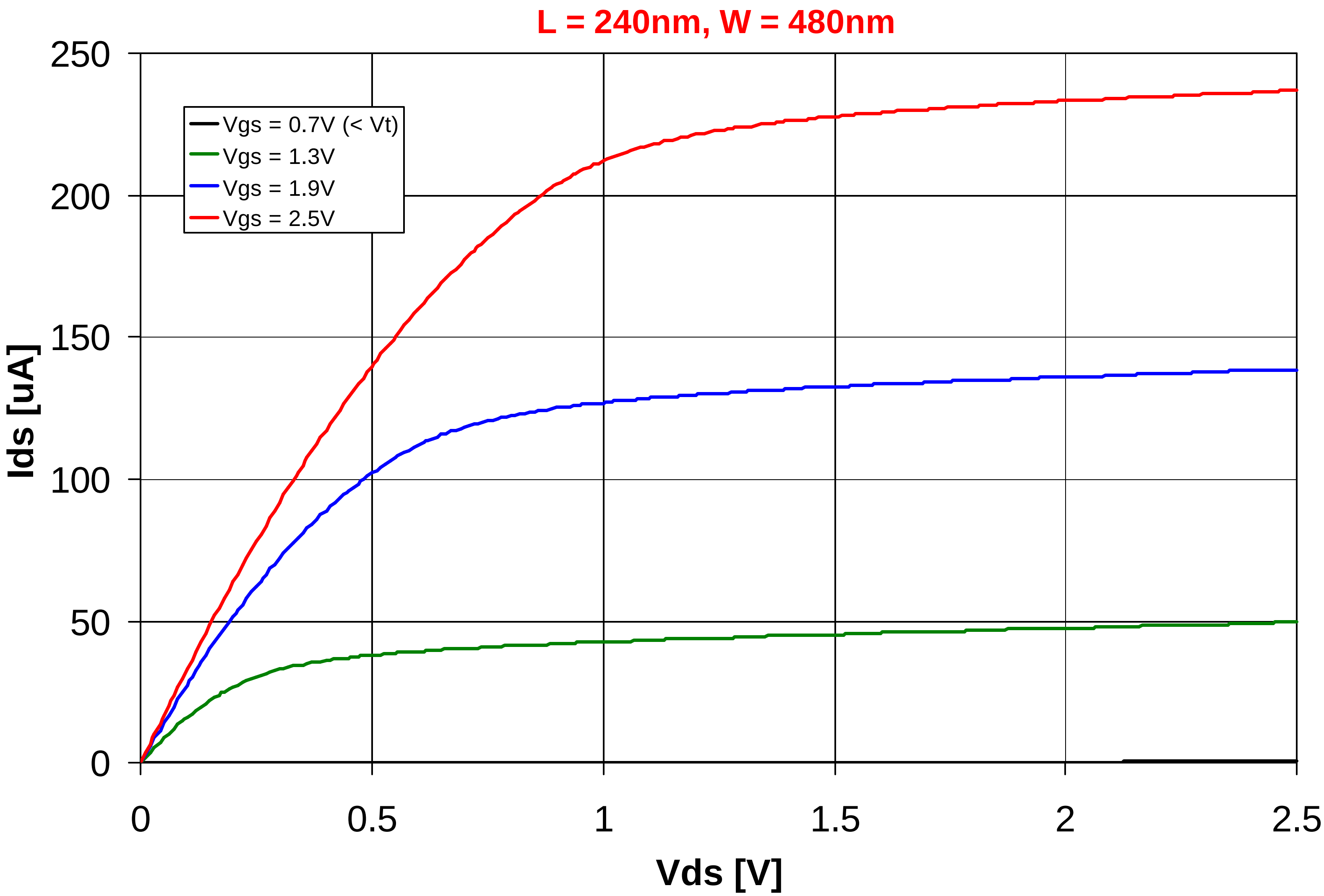
C_{ox} = 5.6fF/µm^2

MOS output characteristics

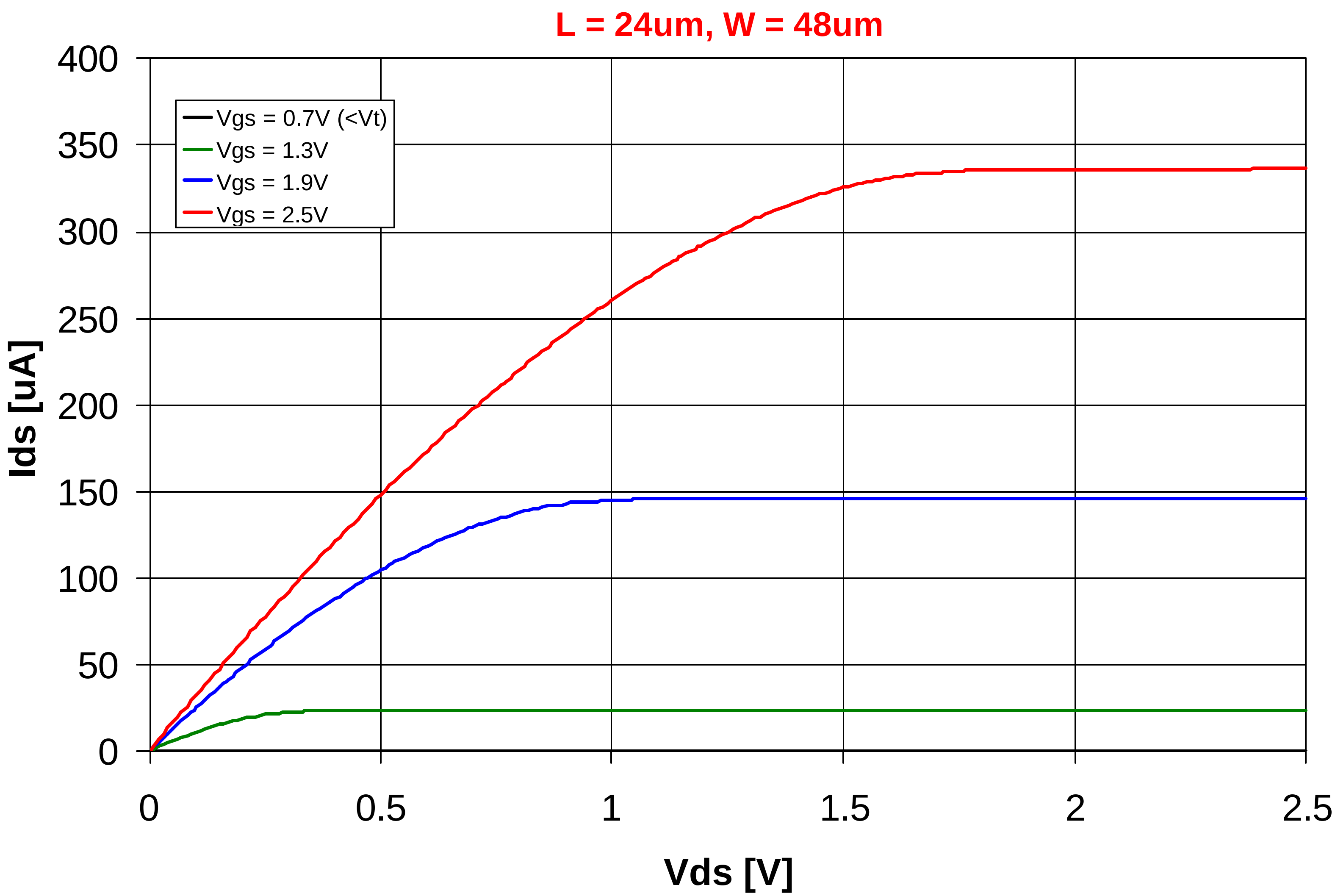
- **Linear region**:
  $V_{ds}<V_{gs}-V_T$
  - Voltage controlled resistor
- **Saturation region**:
  $V_{ds}>V_{gs}-V_T$
  - Voltage controlled current source
- Curves deviate from the ideal current source behavior due to:
  - Channel modulation effects



MOS output characteristics

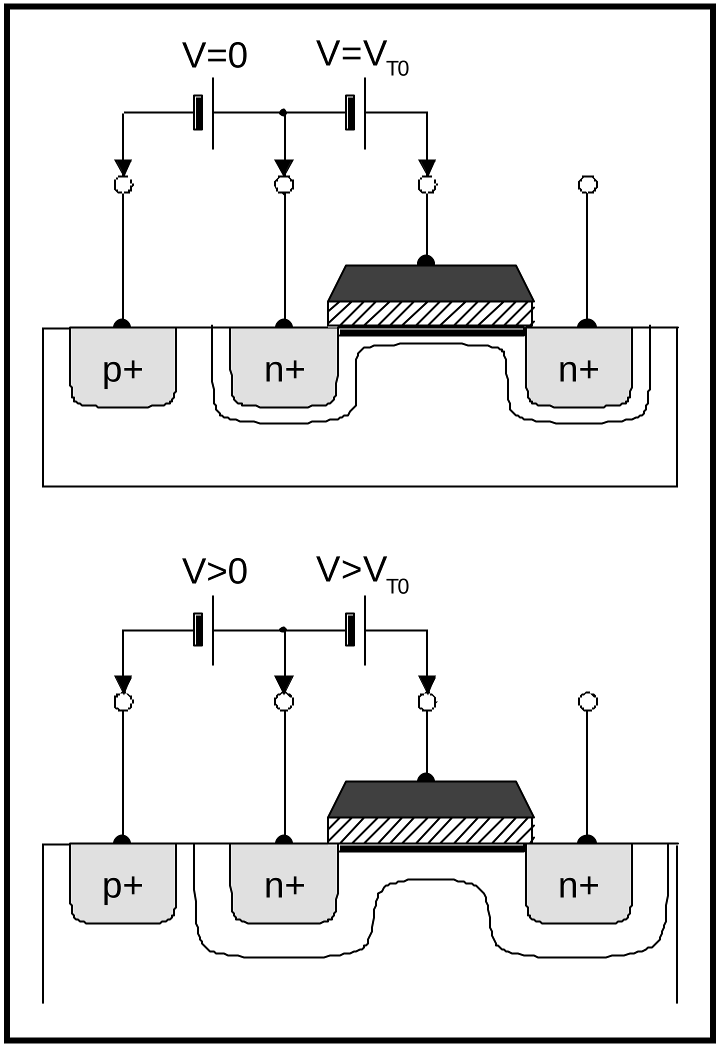


MOS output characteristics

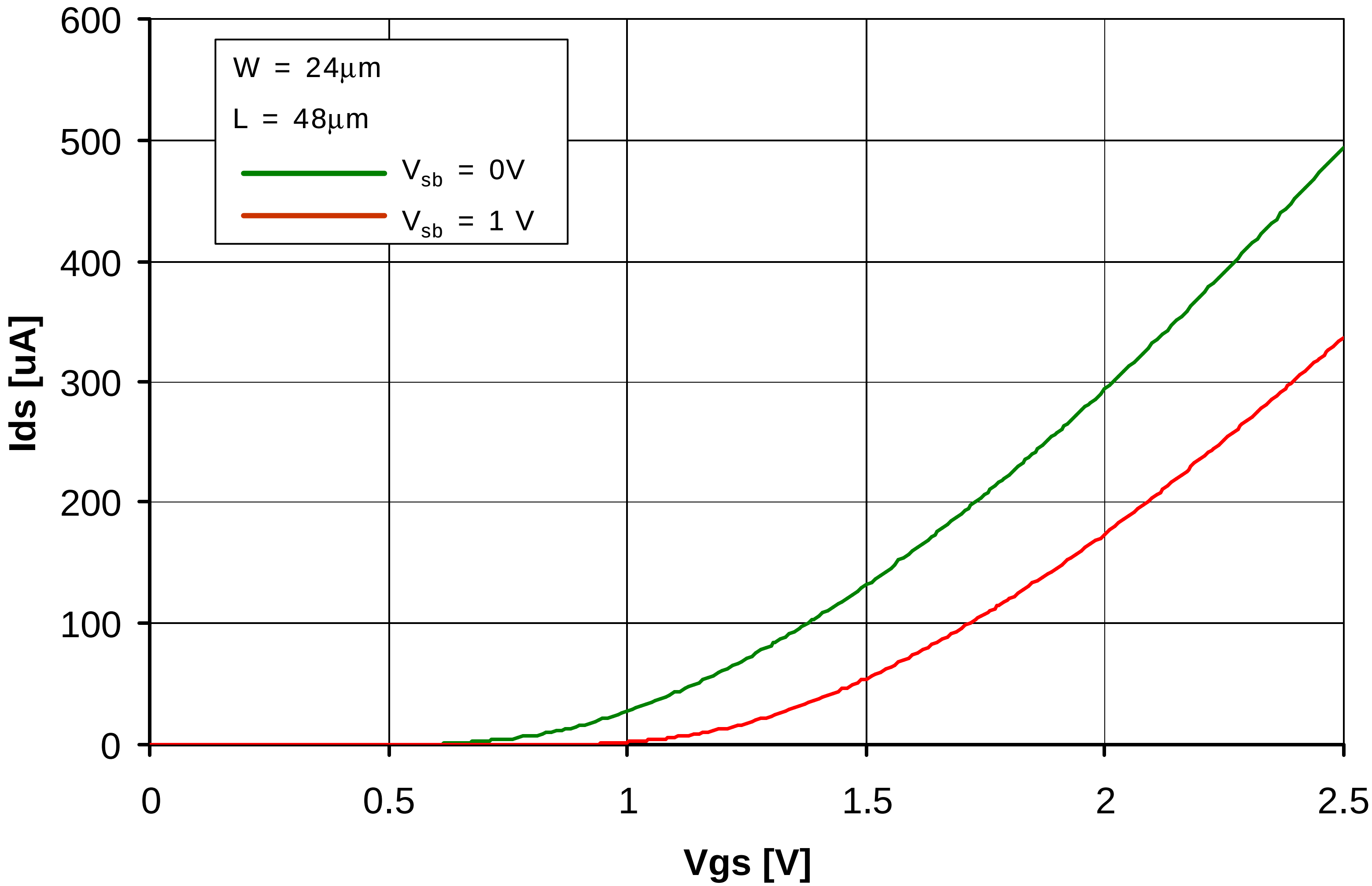


Bulk effect

- The threshold depends on:
  - Gate oxide thickness
  - Doping levels
  - Source-to-bulk voltage
- When the semiconductor surface inverts to n-type the channel is in "strong inversion"
- $V_{sb} = 0 \Rightarrow$ strong inversion for:
  - surface potential > $-2\phi_F$
- $V_{sb} > 0 \Rightarrow$ strong inversion for:
  - surface potential > $-2\phi_F + V_{sb}$

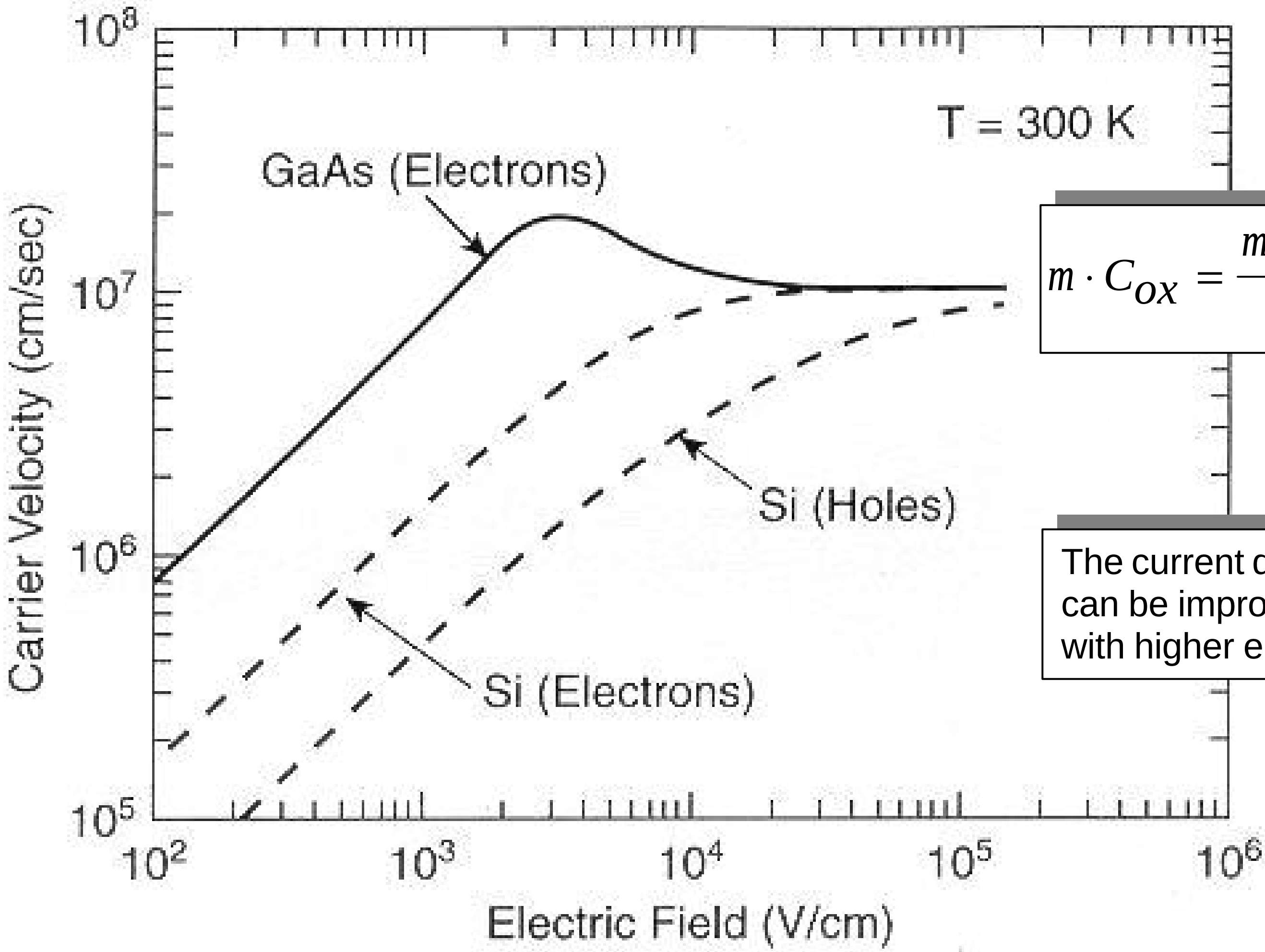


Bulk effect



W = 24µm
L = 48µm
V_sb = 0V
V_sb = 1 V
600
500
400
300
200
100
0
Ids [uA]
0
0.5
1
1.5
2
2.5
Vgs [V]

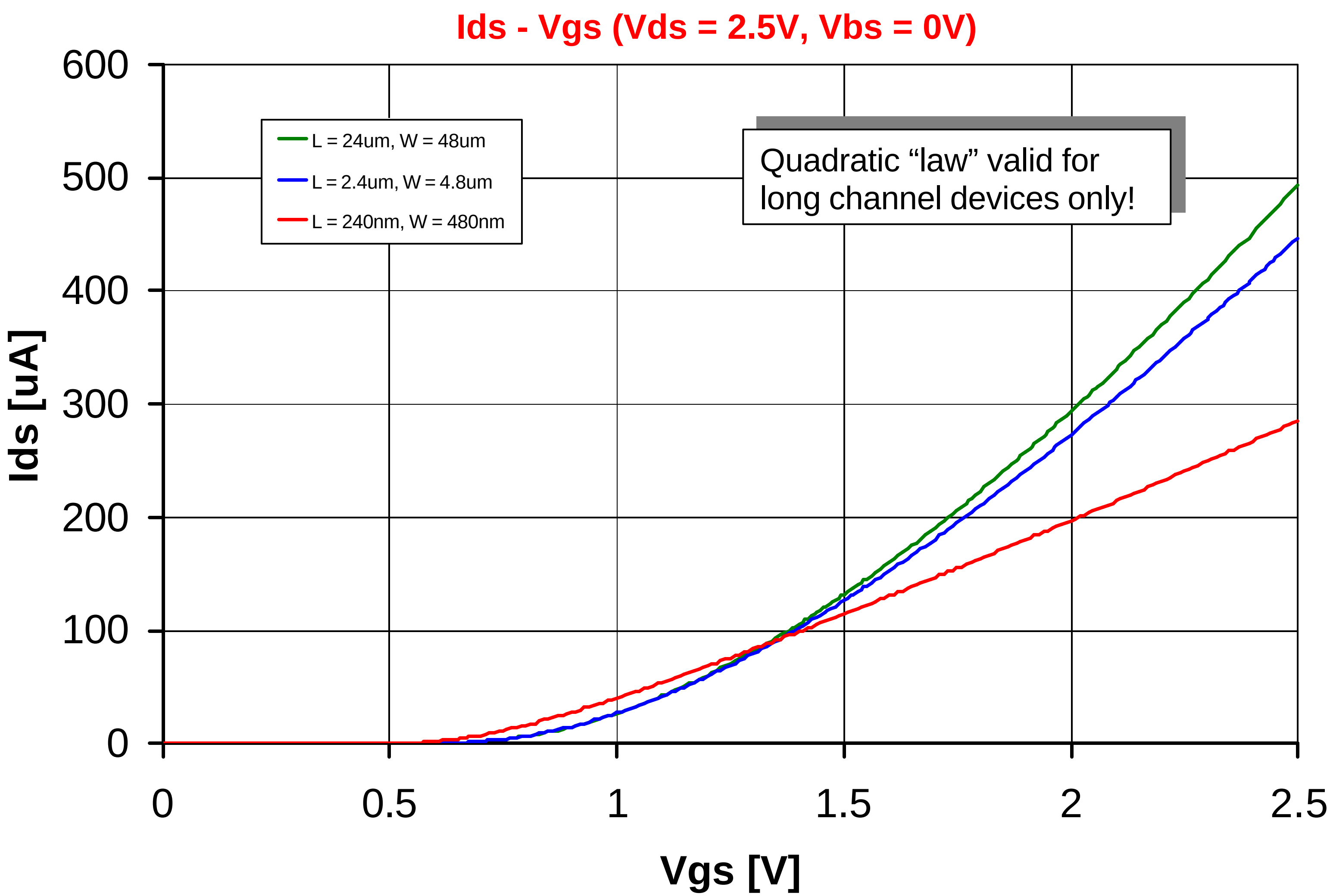
Mobility



$$m \cdot C_{ox} = \frac{m \cdot e_{ox}}{t_{ox}} \quad \left(A / V^2\right)$$

The current driving capability can be improved by using materials with higher electron mobility

Is the quadratic law valid?



Weak inversion

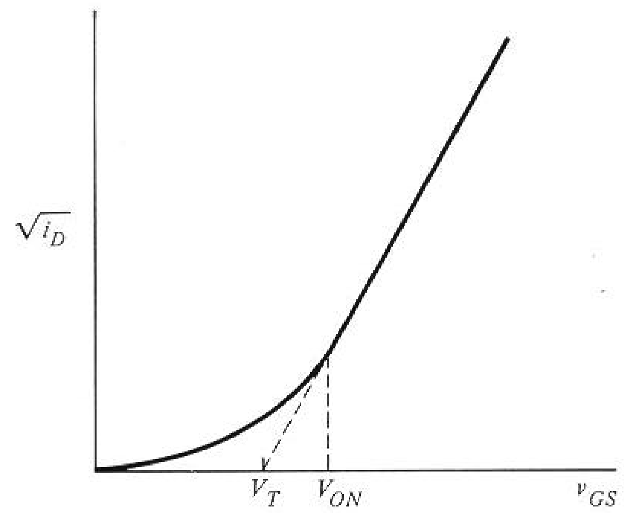
- Is $I_d=0$ when $V_{gs}<V_T$?
- For $V_{gs}<V_T$ the drain current depends exponentially on V_{gs}
- In weak inversion and saturation (V_{ds} > ~150mV):

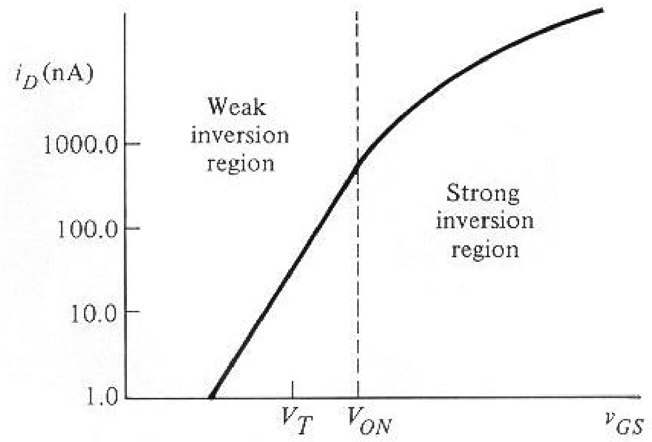
$$I_d \cong \frac{W}{L} \cdot I_{do} \cdot e^{\frac{q \cdot V_{gs}}{n \cdot k \cdot T}}$$

where

$$I_{do} = e^{-\frac{q \cdot V_T}{n \cdot k \cdot T}}$$

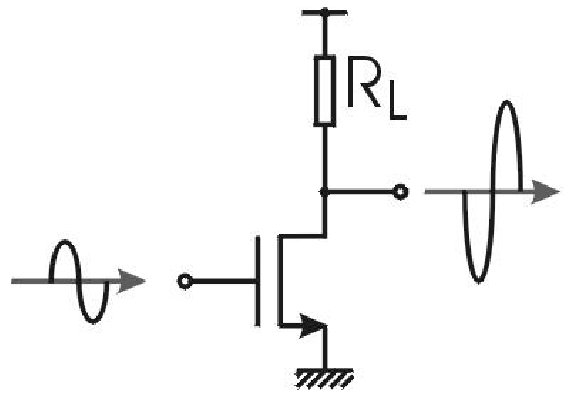
- Used in very low power designs
- Slow operation





Gain & Inversion

- Gain:
  - Signal regeneration at every logic operation
  - "Static" flip-flops
  - "Static" RW memory cells
- Inversion:
  - Intrinsic to the common-source configuration
- The gain cell load can be:
  - Resistor
  - Current source
  - Another gain device (PMOS)



$$V_{out} = -g_m \times (R_{ds} \| R_L) \times V_{in}$$