SIMPLE EPROM PROGRAMMER

CERN

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April 22, 1983

GENERAL

A common problem for microprocessor users is that one cannot take full advantage of the systems flexibility if no PROM PROGRAMMER is available. Commercial PROM PROGRAMMERS cost more than the average 8 bit microsystems. Frequently the users do not need all the options provided by expensive PROM BURNERS, if it is only required to burn or read the popular 2716 and 2732 EPROMS.

The small 8 chip box described here takes advantage of all the possibilities given to a small microsystem:

- A parallel I/O port (6821 or equivalent) parallel interface:
- +5 VOLT (450 mA):
- A programming language, Assembler or BASIC with POKE and PEEK:

For users of different interface chips than the 6821 the procedure how to drive the prom-burner is described. For 6809 or 68000-KDM users complete programs are available.

The development of a program is reqired if other interface chips than the MC 6821, or other microprocessors are used. For those users the application of an "LED - EPROM " is recommended during the program development. This is a 24 pin socket with red and green LEDs for address and data pins in place of the EPROM, allowing to visually see the activity of the program.

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(18 April - 13 May 1983)

SIMPLE EPROM PROGRAMMER

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THE PROGRAMMING CIRCUITRY (FIG 1)

Since 12 address lines, 8 data lines and several control lines are required to program a 32 K EPROM this is more than provided by one 6821 PIA -port. Therefore the addresses for the EPROM are generated by a 12 bit upcounter. The CA2 output is used to increment the counter. The clear input of the counter is used to initialize the address to zero (PB6 output).

A two-fold switch allows selection of 2716/2732 EPROMS. Both types differ in the program/verify procedure which is taken care of by the logic in the box. Eproms with several supply voltages cannot be used.

Each EPROM address is programmed by application of a stable +25 VOLT level together with a pulse on the CHIP-select input of 50 ms duration. The +25 VOLT level is generated by DC/DC conversion of the +5 VOLT supply using a cheap integrated circuit (TL497, Texas instruments). The 50 ms pulse is geneated by an NE555 timer triggered by the CB2 output.

The program voltage is switched on (13 ms rise time !) when the PIA output PB7 is programmed low (indicated by the PROGRM LED) The EPROM is programmed at the specified address (up-counter) with the data-byte on the PA -outputs as soon as the 50 ms timer is triggered (CB2 low - high).

The READ or VERIFY of an EPROM is possible by programming PB7 high. This disables the 25 volts and the timer. The Chip select of the EPROM is then always enabled and the EPROM data can be read on the PA inputs.

The pulse to increment the counter has to go low-high on the CA2 output. The same applies to the CLEAR (PB6) and the Trigger input (CB2). The noise suppression on these pulse sensitive inputs works such that the termination capacitors have to be discharged by the PIA output transistors across the cable in order to fall below the Schmitt trigger threshold .When the transistor is switched off again the capacitor is recharged with ~100 ns rise time.

After 50 ms the next address can be programmed. In order to recognize the end of the programming pulse the CA1 input of the PIA has to be watched. The rising end of the pulse sets a flag in the PIA control register. This could also be used to generate an interrupt.

Since the PIA outputs can only drive savely 2 Standard TTL loads, Low -power Shottky circuits are made use of. The peak current during programming is 450 mA.

DETAILED PIA CONTROL PROCEDURE

This applies only to an MC 6821 PIA. It is recommended to use the LED EPROM in order to check every single step. The procedure to read the content of an EPROM differs only in several steps which is indicated in brackets.

* HARDWARE RESET FOR PIA
* Clear bit 3 in CRA
* Set all bits in PA (clear all bits)
* Set bit 3 in CRA
  PA lines are now outputs
* Clear bit 3 in CRB
* Set bits 6 and 7 in DRB
* Set bit 3 in CRB
  PB6 and PB7 are now outputs
* Set all bits in DRA (security)
* Set bits 6 and 7 in DRA
  PB6 and PB7 =1
* Set bits 1,4,5 in CRA
  enables CRA-7 flag on rising edge of CA1
  and makes CA2 output
* Set bits 4 and 5 in CRB (not required)
  makes CB2 output
* Time loop > 50 ms in case the (not required)
  timer has triggered during initialisation
* Clear bit 6 in DRB
* Set bit 6 in DRB
  Counter was cleared on PB6
* Read DRA to clear CRA-7 Flag (" ")
* Clear bit 7 DRB (set bit 7 DRB)
  enables program and 25 VOLT
* TIME loop (not required)

> 15 ms to wait for satble 25 VOLTS

```
* Data byte to DRA                          (read byte from DRA)  <-
    Eprom is prepared now                                          |
* Clear bit 3 CRB                             (not required )      |
* Set bit 3 CRB                                 "       "          |
    Timer is triggered, Eprom being programmed                     |
* Loop till bit 7 =1 in CRA  (CRA-7 -Flag)      "       "          |
* Read DRA  to clear the CRA-7 Flag             "       "          |
    ready                                                          |
* Clear bit 3 CRA                                                  |
* Set bit 3 CRA                                                    |
    increment the counter, next address                            |
* More data ?   if yes ----------------------------------------------
    if no   Set Bit 7 DRB to disable 25 volts
```

CRITICAL POINTS

There are some point requiring special care .

a.) trying to program more locations then available in the EPROM will overwrite the first locations

b.) The 100 % rise time of the 25 Volt level is 12 ms after the PB7 bit was set low. Programming must not start before this delay.

c.) The +5 Volt connection must be able to deliver at least 450 mA. A bad power/ground connection is indicated if the 5 Volt indicator LED starts to flicker during programming.

d.) The 25 Volts must be adjusted to + 25,0 Volts (PB7 grounded).

e.) The timer must be adjusted to generate pulses of duration no longer than 55 ms.

ATTENTION:

NEVER INSERT OR REMOVE AN EPROM WHILE 25 VOLTS ARE ENABLED
NEVER INSERT THE EPROM IN THE WRONG SENSE there is a high probability that the Eproms are destroyed this way

64 K EPROMS:

Provisions are made on the board to mount a 28 pin Eprom socket for 2764 EPROMS. However, additional patch wiring is necessary to provide one more address.

PROGRAM EXTENSIONS

All extensions to make programming more comfortable increase the effort for the program writer. It is recommended to write the basic algorithm and add each single extension in modular form.

Useful options are:

* ZERO check, to test if the EPROM is still empty. NOTE that an unprogrammed location reads as $FF.
* VERIFY, to compare after programming the EPROM content with the source in the memory.
* OFFSET, allows to start programming at an offset from address zero in the Eprom.
* DUMP, lists the content of the EPROM in compact form on the terminal.
* 16BIT, allows to program subsequently two parallel EPROMS on alternating addresses for 16 bit microprocessors

Appendix A

HARDWARE COMPONENTS

1	LS245	1	TRIMPOT 100K
3	LS193	1	TRIMPOT 10K
1	LS132	2	RESISTOR ARRAYS 1K
1	LS 02	26	-PIN MALE FLAT CABLE CONNECTOR
1	NE 555	1	ZERO INSERTION FORCE
1	TL 497 (TEXAS INSTR.)		-24 PIN CONNECTOR
1	2N3054		-TEXTOOL 224-3344
1	SWITCH (3 INVERTERS)	1	DIODE 1N4118
1	REED RELAIS 5V		
	CELDUC D31 C2240		LED-EPROM :
SEVERAL RESISTORS, CAPACITORS		1	24 PIN IC SOCKET
1	MICROFUSE 500 MA	8	RED LEDS (DATA)
1	FERRITE TORE 23 mm	11	GREEN LEDS (ADDRESS)
	Philipps NR 97150	1	YELLOW LED (CHIP SEL)
	15 TURNS		
1	NOISE SUPPESSION FERRITE COIL		
2	RED LEDs		

BOARD : CERN ref DD-5255 (FIG.2,3)
12 x 15 cm double sided, plated through
two side mounting of all components including
switch and prom socket

Connector:

26 pin two-row connector

1	+5	2	+5
3	CB2	4	-
5	PB7	6	PB6
7	-	8	-
9	-	10	-
11	-	12	-
13	PA7	14	PA6
15	PA5	16	PA4
17	PA3	18	PA2
19	PA1	20	PA0
21	CA1	22	CA2
23	GND	24	GND
25	-	26	-

Appendix B

6809 AND 68000 PROGRAMS

The 6809 package, written by P. Payre[1] for this Prom burner, is a completely position independent and self contained EPROM program (PIA, ACIA or MONITOR-10 addresses have to be specified) In a self explaining menu the user is asked what he wants to do. The program fits into one 16 k EPROM.
An Example:

```
PROM TYPE= 2716 OR 2732 ?  2732 <CR>
START POINT IN EPROM ?  0010
MEMORY RANGE IN RAM -> 1000 1200 <CR>
ENTER=>
1: ENTER ADDRESS
2: RAM =>EPROM
3: EPROM=>RAM
4: VERIFY EPROM
5: CHECK EPROM BLANK
6: RETURN TO MONITOR

5 <CR>
    -> OK
ENTER=>
"  "   "   "   "
```

The 68000 program is written for the MOTOROLA MACBUG monitor. It allows to program parallel or single EPROMS from the source in the memory, to read an EPROM content into a specified memory section or to dump the content on the terminal. Offsets in the EPROM are possible. There is no selection menu, but the program asks all input parameters.

For Program listings contact P. Payre or author

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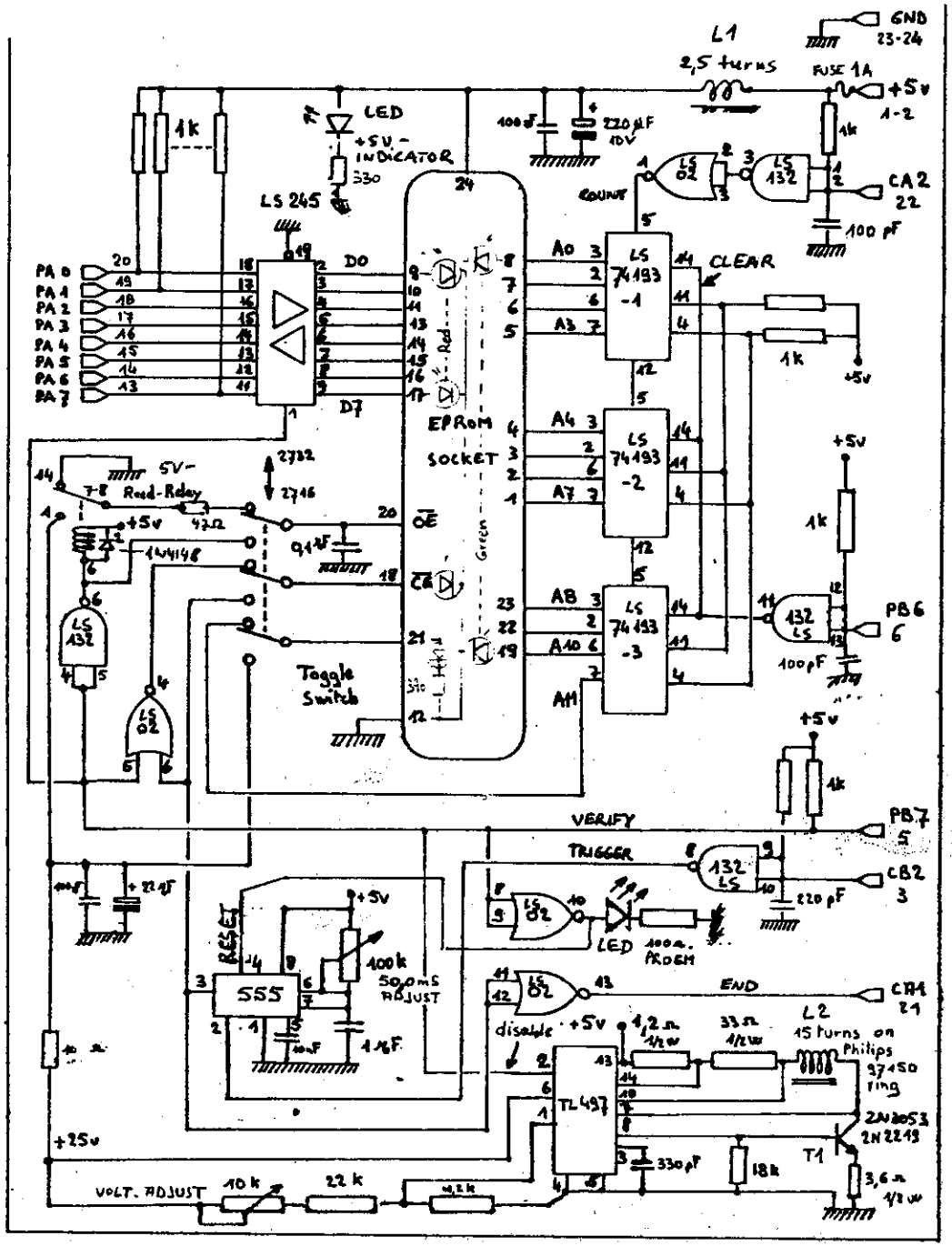
[1] Universite Marseilles

EPROM PROGRAMMER FIG 1



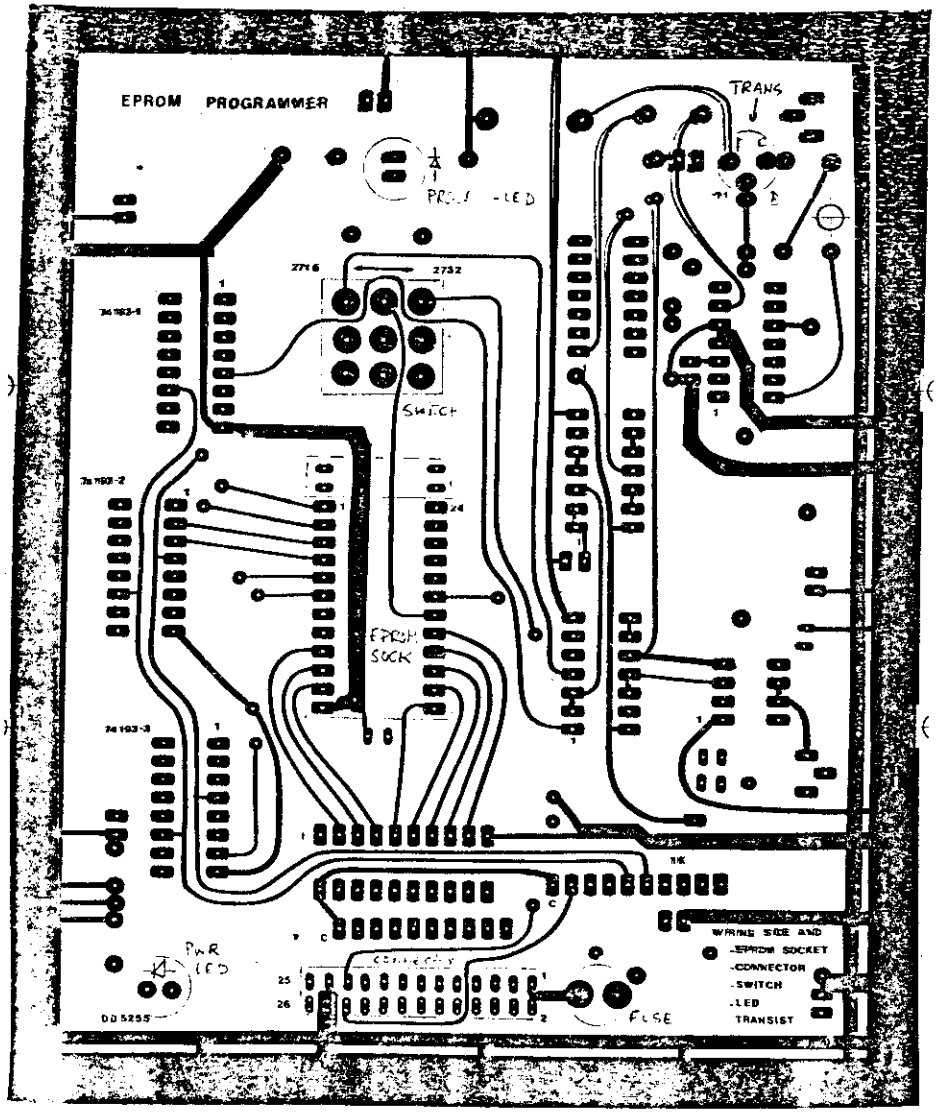


FIG 2 TOP VIEW

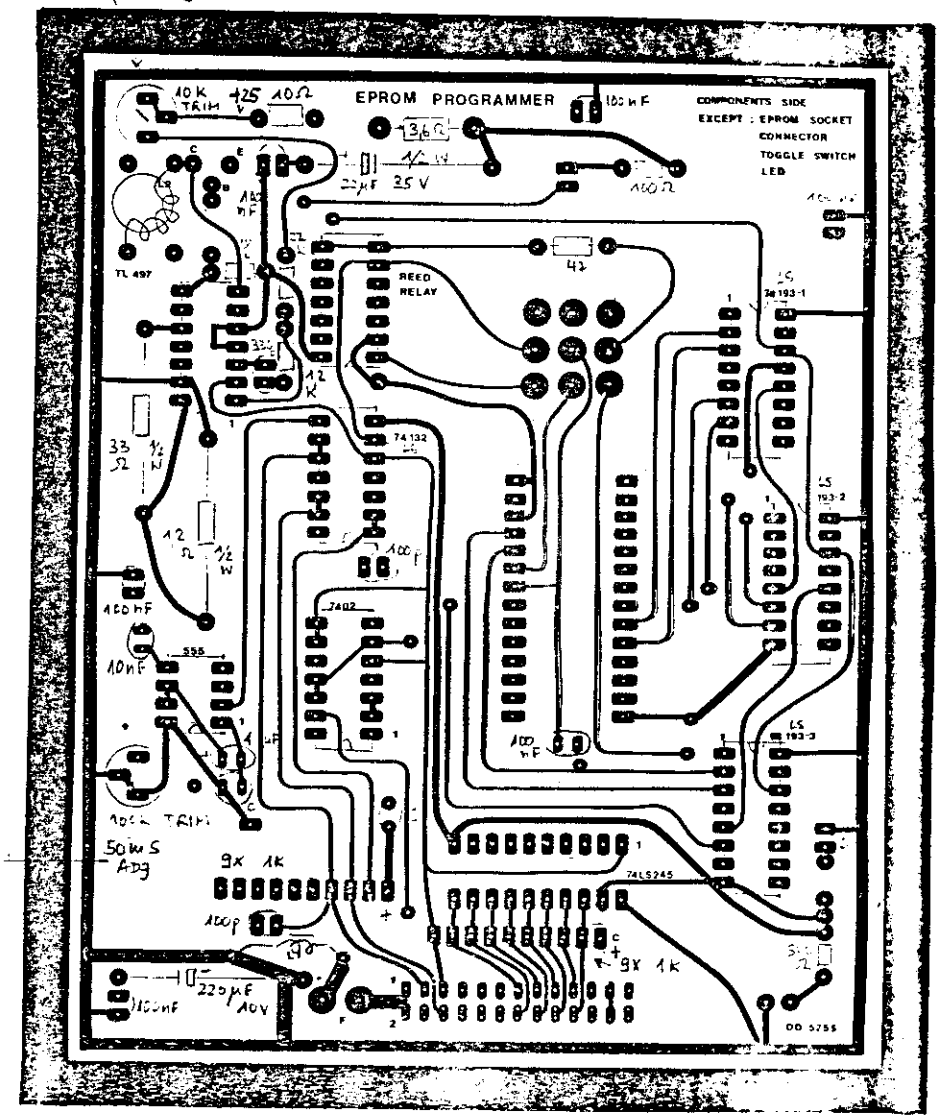


FIG 3 BOTTOM (Components)

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2716
16K (2K x 8) UV ERASABLE PROM

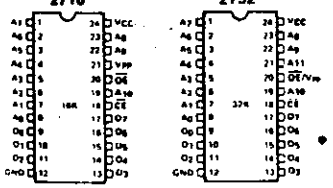
- **Fast Access Time**
  - — 350 ns Max. 2716-1
  - — 390 ns Max. 2716-2
  - — 450 ns Max. 2716
  - — 490 ns Max. 2716-5
  - — 650 ns Max. 2716-6
- **Single +5V Power Supply**
- **Low Power Dissipation**
  - — 525 mW Max. Active Power
  - — 132 mW Max. Standby Power
- **Pin Compatible to Intel® 2732 EPROM**
- **Simple Programming Requirements**
  - — Single Location Programming
  - — Programs with One 50 ms Pulse
- **Inputs and Outputs TTL Compatible during Read and Program**
- **Completely Static**

The Intel® 2716 is a 16,384-bit ultraviolet erasable and electrically programmable read-only memory (EPROM). The 2716 operates from a single 5-volt power supply, has a static standby mode, and features fast single address location programming. It makes designing with EPROMs faster, easier and more economical.

The 2716, with its single 5-volt supply and with an access time up to 350 ns, is ideal for use with the newer high performance +5V microprocessors such as Intel's 8085 and 8086. A selected 2716-5 and 2716-6 is available for slower speed applications. The 2716 is also the first EPROM with a static standby mode which reduces the power dissipation without increasing access time. The maximum active power dissipation is 525 mW while the maximum standby power dissipation is only 132 mW, a 75% savings.

The 2716 has the simplest and fastest method yet devised for programming EPROMs – single pulse TTL level programming. No need for high voltage pulsing because all programming controls are handled by TTL signals. Program any location at any time—either individually, sequentially or at random, with the 2716's single address location programming. Total programming time for all 16,384 bits is only 100 seconds.

PIN CONFIGURATION



†Refer to 2732 data sheet for specifications

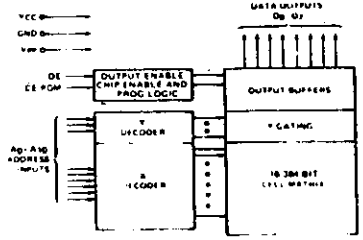
PIN NAMES

A_0–A_{10}	ADDRESSES
$\overline{CE}$/PGM	CHIP ENABLE/PROGRAM
$\overline{OE}$	OUTPUT ENABLE
O_0–O_7	OUTPUTS

MODE SELECTION

MODE \ PINS	$\overline{CE}$/PGM (18)	$\overline{OE}$ (20)	V_{PP} (21)	V_{CC} (24)	OUTPUTS (9-11, 13-17)
Read	V_{IL}	V_{IL}	+5	+5	D_{OUT}
Standby	V_{IH}	Don't Care	+5	+5	High Z
Program	Pulsed V_{IL} to V_{IH}	V_{IH}	+25	+5	D_{IN}
Program Verify	V_{IL}	V_{IL}	+25	+5	D_{OUT}
Program Inhibit	V_{IL}	V_{IH}	+25	+5	High Z

BLOCK DIAGRAM



ERASURE CHARACTERISTICS

The erasure characteristics of the 2716 are such that erasure begins to occur when exposed to light with wavelengths shorter than approximately 4000 Angstroms (Å). It should be noted that sunlight and certain types of fluorescent lamps have wavelengths in the 3000–4000Å range. Data show that constant exposure to room level fluorescent lighting could erase the typical 2716 in approximately 3 years, while it would take approximatley 1 week to cause erasure when exposed to direct sunlight. If the 2716 is to be exposed to these types of lighting conditions for extended periods of time, opaque labels are available from Intel which should be placed over the 2716 window to prevent unintentional erasure.

The recommended erasure procedure (see Data Catalog PROM/ROM Programming Instruction Section) for the 2716 is exposure to shortwave ultraviolet light which has a wavelength of 2537 Angstroms (Å). The integrated dose (i.e., UV intensity X exposure time) for erasure should be a minimum of 15 W-sec/cm^2. The erasure time with this dosage is approximately 15 to 20 minutes using an ultraviolet lamp with a 12000 μW/cm^2 power rating. The 2716 should be placed within 1 inch of the lamp tubes during erasure. Some lamps have a filter on their tubes which should be removed before erasure.

DEVICE OPERATION

The five modes of operation of the 2716 are listed in Table I. It should be noted that all inputs for the five modes are at TTL levels. The power supplies required are a +5V V_{CC} and a V_{PP}. The V_{PP} power supply must be at 25V during the three programming modes, and must be at 5V in the other two modes.

TABLE I. MODE SELECTION

MODE \ PINS	$\overline{CE}$/PGM (18)	$\overline{OE}$ (20)	V_{PP} (21)	V_{CC} (24)	OUTPUTS (9-11, 13-17)
Read	V_{IL}	V_{IL}	+5	+5	D_{OUT}
Standby	V_{IH}	Don't Care	+5	+5	High Z
Program	Pulsed V_{IL} to V_{IH}	V_{IH}	+25	+5	D_{IN}
Program Verify	V_{IL}	V_{IL}	+25	+5	D_{OUT}
Program Inhibit	V_{IL}	V_{IH}	+25	+5	High Z

READ MODE

The 2716 has two control functions, both of which must be logically satisfied in order to obtain data at the outputs. Chip Enable ($\overline{CE}$) is the power control and should be used for device selection. Output Enable ($\overline{OE}$) is the output control and should be used to gate data to the output pins, independent of device selection. Assuming that addresses are stable, address access time (t_{ACC}) is equal to the delay from $\overline{CE}$ to output (t_{CE}). Data is available at the outputs 120 ns (t_{OE}) after the falling edge of $\overline{OE}$, assuming that $\overline{CE}$ has been low and addresses have been stable for at least $t_{ACC} - t_{OE}$.

STANDBY MODE

The 2716 has a standby mode which reduces the active power dissipation by 75%, from 525 mW to 132 mW. The 2716 is placed in the standby mode by applying a TTL high signal to the $\overline{CE}$ input. When in standby mode, the outputs are in a high impedence state, independent of the $\overline{OE}$ input.

OUTPUT OR-TIEING

Because 2716's are usually used in larger memory arrays, Intel has provided a 2 line control function that accomodates this use of multiple memory connections. The two line control function allows for:

a) the lowest possible memory power dissipation, and
b) complete assurance that output bus contention will not occur.

To most efficiently use these two control lines, it is recommended that $\overline{CE}$ (pin 18) be decoded and used as the primary device selecting function, while $\overline{OE}$ (pin 20) be made a common connection to all devices in the array and connected to the READ line from the system control bus. This assures that all deselected memory devices are in their low power standby mode and that the output pins are only active when data is desired from a particular memory device.

PROGRAMMING

Initially, and after each erasure, all bits of the 2716 are in the "1" state. Data is introduced by selectively programming "0's" into the desired bit locations. Although only "0's" will be programmed, both "1's" and "0's" can be presented in the data word. The only way to change a "0" to a "1" is by ultraviolet light erasure.

The 2716 is in the programming mode when the V_{PP} power supply is at 25V and $\overline{OE}$ is at V_{IH}. The data to be programmed is applied 8 bits in parallel to the data output pins. The levels required for the address and data inputs are TTL.

When the address and data are stable, a 50 msec, active high, TTL program pulse is applied to the $\overline{CE}$/PGM input. A program pulse must be applied at each address location to be programmed. You can program any location at any time — either individually, sequentially, or at random. The program pulse has a maximum width of 55 msec. The 2716 must not be programmed with a DC signal applied to the $\overline{CE}$/PGM input.

Programming of multiple 2716s in parallel with the same data can be easily accomplished due to the simplicity of the programming requirements. Like inputs of the paralleled 2716s may be connected together when they are programmed with the same data. A high level TTL pulse applied to the $\overline{CE}$/PGM input programs the paralleled 2716s.

PROGRAM INHIBIT

Programming of multiple 2716s in parallel with different data is also easily accomplished. Except for $\overline{CE}$/PGM, all like inputs (including $\overline{OE}$) of the parallel 2716s may be common. A TTL level program pulse applied to a 2716's $\overline{CE}$/PGM input with V_{PP} at 25V will program that 2716. A low level $\overline{CE}$/PGM input inhibits the other 2716 from being programmed.

PROGRAM VERIFY

A verify should be performed on the programmed bits to determine that they were correctly programmed. The verify may be performed with V_{PP} at 25V. Except during programming and program verify, V_{PP} must be at 5V.

intel

PRELIMINARY

2732
32K (4K x 8) UV ERASABLE PROM

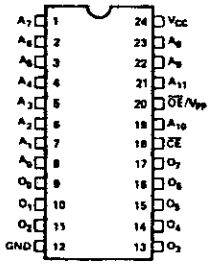
- **Fast Access Time:**
  - **— 450 ns Max. 2732**
  - **— 550 ns Max. 2732-6**
- **Single +5V ± 5% Power Supply**
- **Output Enable for MCS-85™ and MCS-86™ Compatibility**
- **Low Power Dissipation:**
  150mA Max. Active Current
  30mA Max. Standby Current
- **Pin Compatible to Intel® 2716 EPROM**
- **Completely Static**
- **Simple Programming Requirements**
  - **— Single Location Programming**
  - **— Programs with One 50ms Pulse**
- **Three-State Output for Direct Bus Interface**

The Intel® 2732 is a 32,768-bit ultraviolet erasable and electrically programmable read-only memory (EPROM). The 2732 operates from a single 5-volt power supply, has a standby mode, and features an output enable control. The total programming time for all bits is three and a half minutes. All these features make designing with the 2732 in microcomputer systems faster, easier, and more economical.

An important 2732 feature is the separate output control, Output Enable ($\overline{OE}$) from the Chip Enable control ($\overline{CE}$). The OE control eliminates bus contention in multiple bus microprocessor systems. Intel's Application Note AP-72 describes the microprocessor system implementation of the $\overline{OE}$ and $\overline{CE}$ controls on Intel's 2716 and 2732 EPROMs. AP-72 is available from Intel's Literature Department.

The 2732 has a standby mode which reduces the power dissipation without increasing access time. The maximum active current is 150mA, while the maximum standby current is only 30mA, an 80% savings. The standby mode is achieved by applying a TTL-high signal to the $\overline{CE}$ input.

PIN CONFIGURATION



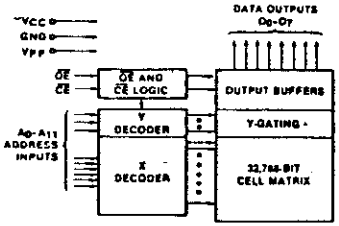
PIN NAMES

A_0-A_{11}	ADDRESSES
$\overline{CE}$	CHIP ENABLE
$\overline{OE}$	OUTPUT ENABLE
O_0-O_7	OUTPUTS

MODE SELECTION

MODE \ PINS	$\overline{CE}$ (18)	$\overline{OE}/V_{PP}$ (20)	V_{CC} (24)	OUTPUTS (9-11,13-17)
Read	V_{IL}	V_{IL}	+5	D_{OUT}
Standby	V_{IH}	Don't Care	+5	High Z
Program	V_{IL}	V_{PP}	+5	D_{IN}
Program Verify	V_{IL}	V_{IL}	+5	D_{OUT}
Program Inhibit	V_{IH}	V_{PP}	+5	High Z

BLOCK DIAGRAM



ERASURE CHARACTERISTICS

The erasure characteristics of the 2732 are such that erasure begins to occur when exposed to light with wavelengths shorter than approximately 4000 Angstroms (Å). It should be noted that sunlight and certain types of fluorescent lamps have wavelengths in the 3000-4000Å range. Data show that constant exposure to room level fluorescent lighting could erase the typical 2732 in approximately 3 years, while it would take approximately 1 week to cause erasure when exposed to direct sunlight. If the 2732 is to be exposed to these types of lighting conditions for extended periods of time, opaque labels are available from Intel which should be placed over the 2732 window to prevent unintentional erasure.

The recommended erasure procedure (see Data Catalog page 4-83) for the 2732 is exposure to shortwave ultraviolet light which has a wavelength of 2537 Angstroms (Å). The integrated dose (i.e., UV intensity X exposure time) for erasure should be a minimum of 15 W-sec/cm². The erasure time with this dosage is approximately 15 to 20 minutes using an ultraviolet lamp with a 12000 μW/cm² power rating. The 2732 should be placed within 1 inch of the lamp tubes during erasure. Some lamps have a filter on their tubes which should be removed before erasure.

DEVICE OPERATION

The five modes of operation of the 2732 are listed in Table 1. A single 5V power supply is required in the read mode. All inputs are TTL levels except for $\overline{OE}/V_{PP}$ during programming. In the program mode the $\overline{OE}/V_{PP}$ input is pulsed from a TTL level to 25V.

TABLE 1. Mode Selection

MODE \ PINS	$\overline{CE}$ (18)	$\overline{OE}/V_{PP}$ (20)	V_{CC} (24)	OUTPUTS (9-11,13-17)
Read	V_{IL}	V_{IL}	+5	D_{OUT}
Standby	V_{IH}	Don't Care	+5	High Z
Program	V_{IL}	V_{PP}	+5	D_{IN}
Program Verify	V_{IL}	V_{IL}	+5	D_{OUT}
Program Inhibit	V_{IH}	V_{PP}	+5	High Z

Read Mode

The 2732 has two control functions, both of which must be logically satisfied in order to obtain data at the outputs. Chip Enable ($\overline{CE}$) is the power control and should be used for device selection. Output Enable ($\overline{OE}$) is the output control and should be used to gate data to the output pins, independent of device selection. Assuming that addresses are stable, address access time (t_{ACC}) is equal to the delay from $\overline{CE}$ to output (t_{CE}). Data is available at the outputs 120ns (t_{OE}) after the falling edge of $\overline{OE}$, assuming that $\overline{CE}$ has been low and addresses have been stable for at least $t_{ACC} - t_{OE}$.

Standby Mode

The 2732 has a standby mode which reduces the active power current by 80%, from 150mA to 30mA. The 2732 is placed in the standby mode by applying a TTL high signal to the $\overline{CE}$ input. When in standby mode, the outputs are in a high impedance state, independent of the $\overline{OE}$ input.

Output OR-Tieing

Because EPROMs are usually used in larger memory arrays, Intel has provided a 2 line control function that accommodates this use of multiple memory connections. The two line control function allows for:

a) the lowest possible memory power dissipation, and
b) complete assurance that output bus contention will not occur.

To most efficiently use these two control lines, it is recommended that $\overline{CE}$ (pin 18) be decoded and used as the primary device selecting function, while $\overline{OE}$ (pin 20) be made a common connection to all devices in the array and connected to the READ line from the system control bus. This assures that all deselected memory devices are in their low power standby mode and that the output pins are only active when data is desired from a particular memory device.

Programming

Initially, and after each erasure, all bits of the 2732 are in the "1" state. Data is introduced by selectively programming "0's" into the desired bit locations. Although only "0's" will be programmed, both "1's" and "0's" can be presented in the data word. The only way to change a "0" to a "1" is by ultraviolet light erasure.

The 2732 is in the programming mode when the $\overline{OE}/V_{PP}$ input is at 25V. It is required that a 0.1μF capacitor be placed across $\overline{OE}/V_{PP}$ and ground to suppress spurious voltage transients which may damage the device. The data to be programmed is applied 8 bits in parallel to the data output pins. The levels required for the address and data inputs are TTL.

When the address and data are stable, a 50msec. active low, TTL program pulse is applied to the $\overline{CE}$ input. A program pulse must be applied at each address location to be programmed. You can program any location at any time — either individually, sequentially, or at random. The program pulse has a maximum width of 55msec. The 2732 must not be programmed with a DC signal applied to the $\overline{CE}$ input.

Programming of multiple 2732s in parallel with the same data can be easily accomplished due to the simplicity of the programming requirements. Like inputs of the paralleled 2732s may be connected together when they are programmed with the same data. A low level TTL pulse applied to the $\overline{CE}$ input programs the paralleled 2732s.

Program Inhibit

Programming of multiple 2732s in parallel with different data is also easily accomplished. Except for $\overline{CE}$, all like inputs (including $\overline{OE}$) of the parallel 2732s may be common. A TTL level program pulse applied to a 2732's $\overline{CE}$ input with $\overline{OE}/V_{PP}$ at 25V will program that 2732. A high level $\overline{CE}$ input inhibits the other 2732s from being programmed.

Program Verify

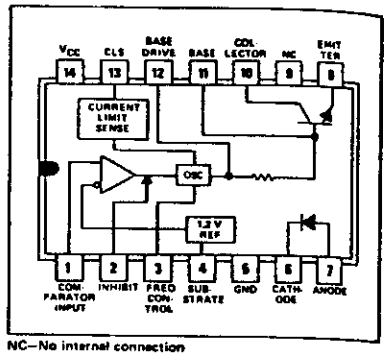
A verify should be performed on the programmed bits to determine that they were correctly programmed. The verify is accomplished with $\overline{OE}/V_{PP}$ and $\overline{CE}$ at V_{IL}. Data should be verified t_{DV} after the falling edge of $\overline{CE}$.

TYPES TL497M, TL497I, TL497C SWITCHING VOLTAGE REGULATORS

BULLETIN NO. DL-S 7612422, JUNE 1976

- All Monolithic
- High Efficiency . . . 60% or Greater
- Output Current . . . 500 mA
- Input Current Limit Protection
- TTL Compatible Inhibit
- Adjustable Output Voltage
- Input Regulation . . . 0.2% Typ
- Output Regulation . . . 0.4% Typ
- Soft Start-up Capability

J OR N
DUAL-IN-LINE PACKAGE (TOP VIEW)



NC—No internal connection

description

The TL497 incorporates on a single monolithic chip all the active functions required in the construction of a switching voltage regulator. It can also be used as the control element to drive external components for high-power-output applications. The TL497 was designed for ease of use in step-up, step-down, or voltage inversion applications requiring high efficiency.

A block diagram of the TL497 is shown in the pinout. A 1.2-volt precision reference is internally connected between the inverting input of the high-gain comparator and the substrate. The output voltage is established using a resistive voltage-divider network whose node voltage is sensed by the noninverting input of the comparator. When the voltage at the noninverting input is more negative than the 1.2 volt reference, the oscillator is gated on. When the voltage at the noninverting input is more positive than the 1.2-volt reference, the oscillator is gated off. The maximum frequency of the oscillator is established by the external timing capacitor connected between the frequency control pin and ground.

TIMING CAPACITOR (pF)	5	10	20	50	100	200	500	1000
MAX FREQUENCY (kHz)	385	313	238	135	80.6	47.6	19.6	10

The transistor switch is normally connected to external inductive components and a diode to generate the output voltage. The TL497 switching transistor and diode may be used directly for switching currents up to 500 milliamperes, or used to drive an external transistor and diode for higher output-power applications.

The TL497 also provides current limiting for protection of the switching transistor and the load. With proper current limiting, saturation of the power inductor may be prevented and soft start-up achieved. Current limiting is accomplished with the current-limit control provided. The voltage developed across the series current-limit resistor, R_{CL}, is sensed. When the voltage at the current-sense terminal is approximately 0.7 volt (one V_{BE} drop) less than the input voltage, the power switch transistor is turned off.

External gating is provided by the inhibit control. When the inhibit control is high, the output is turned off.

The TL497M is characterized for operation over the full military temperature range of −55°C to 125°C, the TL497I is characterized for operation from −25°C to 85°C, and the TL497C from 0°C to 70°C.

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Input voltage (see Note 1)	15 V
Output voltage	35 V
Comparator input voltage	5 V
Inhibit input voltage	5 V
Diode reverse voltage	35 V
Power switch current	750 mA
Diode continuous forward current	750 mA
Continuous total dissipation at (or below) 25°C free-air temperature (see Note 2)	1000 mW
Operating free-air temperature range: TL497M	−55°C to 125°C
TL497I	−25°C to 85°C
TL497C	0°C to 70°C
Storage temperature range	−65°C to 150°C
Lead temperature 1/16 inch from case for 60 seconds: J package	300°C
Lead temperature 1/16 inch from case for 10 seconds: N package	260°C

NOTES: 1. All voltage values except diode voltages are with respect to network ground terminal.
2. For operation above 25°C free-air temperature, refer to Dissipation Derating Curves, Section 2.

recommended operating conditions

	MIN	MAX	UNIT
Input voltage, V_I	4.5	12	V
Output voltage: step-up configuration (see Figure 2)	$V_I + 2$	30	V
step-down configuration (see Figure 3)	V_{ref}	$V_I - 1$	V
negative regulator (see Figure 4)	$-V_{ref}$	−25	V
Output current		500	mA

electrical characteristics at specified free-air temperature, V_I = 6 V (unless otherwise noted)

PARAMETER	TEST CONDITIONS†			TL497M, TL497I			TL497C			UNIT
				MIN	TYP‡	MAX	MIN	TYP‡	MAX	
High-level inhibit input voltage			Full range	2			2			V
Low-level inhibit input voltage			Full range			0.6			0.8	V
High-level inhibit input current	$V_{I(I)}$ = 5 V		Full range		0.8	1.5		0.8	1.5	mA
Low-level inhibit input current	$V_{I(I)}$ = 0 V		Full range		5	20		5	10	μA
Comparator reference voltage	V_I = 4.5 V to 6 V		Full range	1.14	1.20	1.26	1.08	1.20	1.32	V
Comparator input bias current	V_I = 6 V		Full range		40	100		40	100	μA
Regulator output voltage	See Figure 1 R1 = 11.3 kΩ, R2 = 1 kΩ		25°C	14.25	15	15.75	13.5	15	16.5	V
Switch on-state voltage	V_I = 4.5 V	I_O = 100 mA	25°C		0.13	0.2		0.13	0.2	V
		I_O = 500 mA	Full range			1			0.85	
Switch off-state current	V_I = 4.5 V		25°C		10	50		10	50	μA
			Full range			500			200	
Current-limit sense voltage	V_{CC} = 6 V		25°C	0.45		1	0.45		1	V
Diode forward voltage	I_O = 10 mA		Full range		0.75	0.95		0.75	0.85	V
	I_O = 100 mA		Full range		0.9	1.1		0.9	1	
	I_O = 500 mA		Full range		1.33	1.7		1.33	1.55	
Diode reverse voltage	I_O = 500 μA		Full range	30						V
	I_O = 200 μA		Full range				30			
On-state supply current			25°C		11	14		11	14	mA
			Full range			16			15	
Off-state supply current			25°C		6	9		6	9	mA
			Full range			11			10	

†Full range for TL497M is −55°C to 125°C, for TL497I is −25°C to 85°C, and for TL497C is 0°C to 70°C.
‡All typical values are at T_A = 25°C.

TYPES TL497M, TL497I, TL497C
SWITCHING VOLTAGE REGULATORS

PARAMETER MEASUREMENT INFORMATION

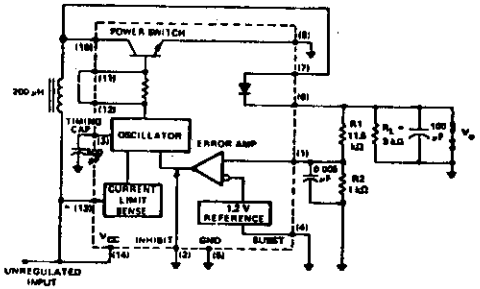


FIGURE 1–TEST CIRCUIT

TYPICAL APPLICATION DATA

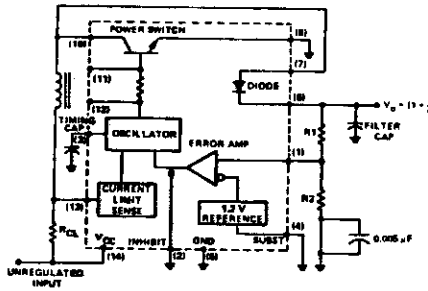


FIGURE 2–POSITIVE REGULATOR, STEP-UP CONFIGURATION

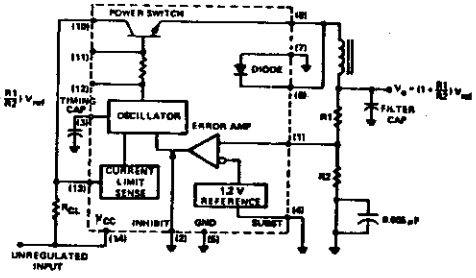


FIGURE 3–POSITIVE REGULATOR, STEP-DOWN CONFIGURATION

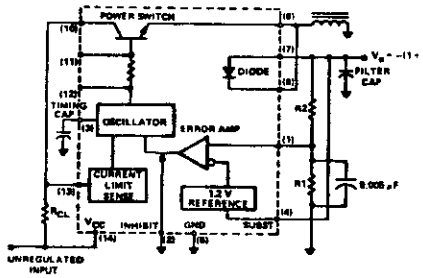


FIGURE 4–NEGATIVE REGULATOR
(e.g., +5 VOLTS INPUT TO −5 VOLTS OUTPUT)
OR
(i.e., POSITIVE INPUT, NEGATIVE OUTPUT)

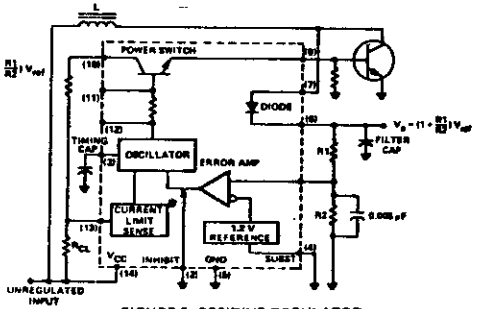


FIGURE 5–POSITIVE REGULATOR WITH BUFFERED OUTPUT