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UNITED NATIONS EDUCATIONAL, SCIENTIFIC AND CULTURAL ORGANIZATION

INTERNATIONAL CENTRE FOR THEORETICAL PHYSICS
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SMR/101 - 13

SECOND COLLEGE ON MICROPROCESSORS: TECHNOLOGY AND APPLICATIONS IN PHYSICS

(18 April - 13 May 1983)

MICROPROCESSOR DEVELOPMENT SYSTEMS

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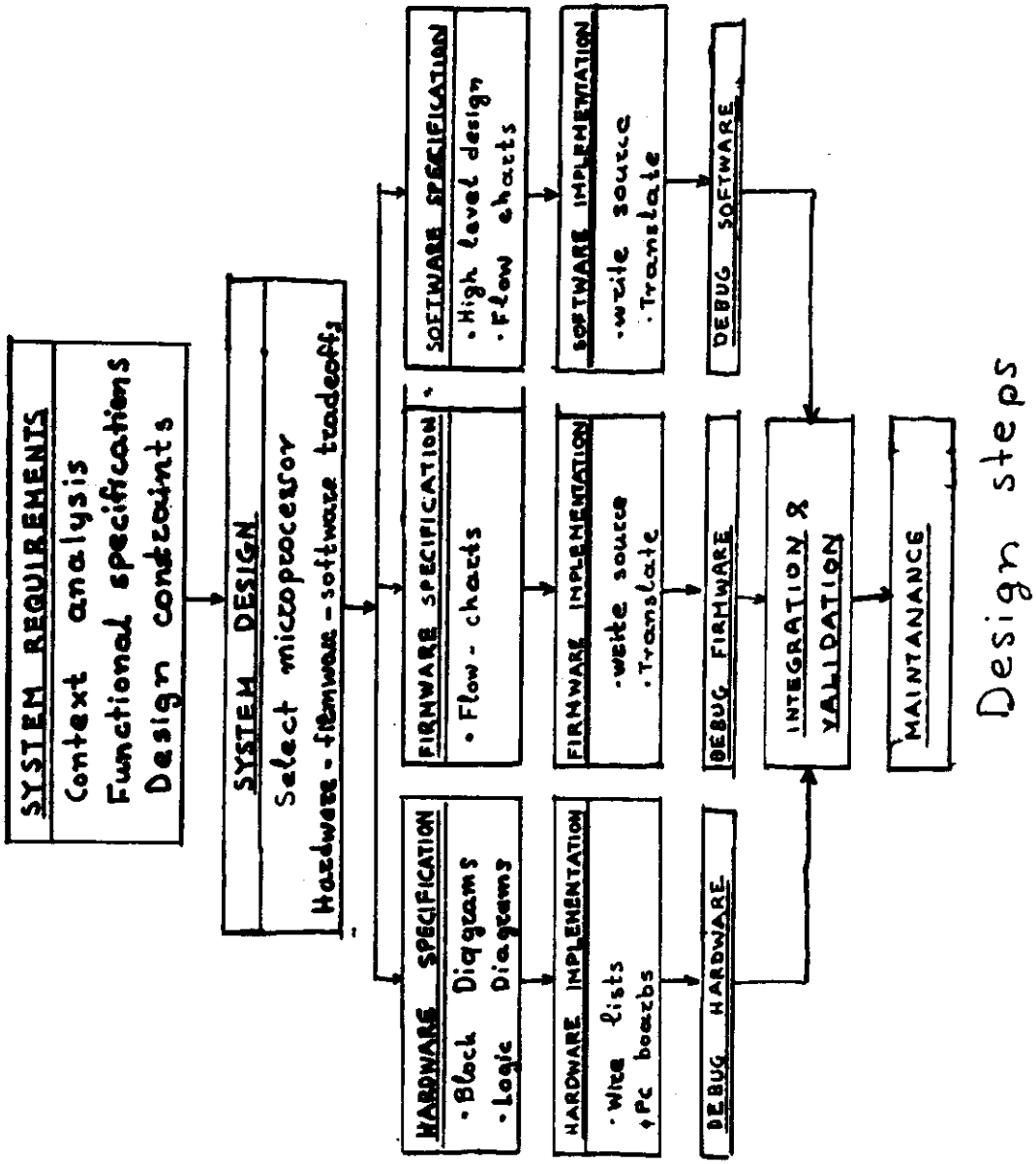


Design steps

MICROPROCESSOR SELECTION CRITERIA

TECHNICAL CRITERIA

- COMPUTING PERFORMANCE
- DEMANDS OF SUPPORT CIRCUITS
- CO-PROCESSORS
- ADDRESSING RANGE
- INTERRUPTS
- TECHNOLOGY
- POWER
- MPU CHIP FAMILY
- SUPPORT CHIP FAMILY
- APPLICATION SUPPORT

OTHER CRITERIA

- AVAILABILITY
- MULTIPLE SOURCES
- COMMITMENT
- POPULARITY
- PRICES
- TECHNICAL TRAINING

- MINI & LARGE COMPUTERS
- INTEGRATED μP DEVELOPMENT SYSTEMS
- IN-CIRCUIT EMULATORS
- MICRO-BASED DEVELOPMENT SYSTEMS
- PROTOTYPING KITS
- PROGRAMMER PANELS
- PROM PROGRAMMERS
- μP ANALYSERS
- LOGIC ANALYSERS
- OSCILLOSCOPES

Spectrum of μP Development tools

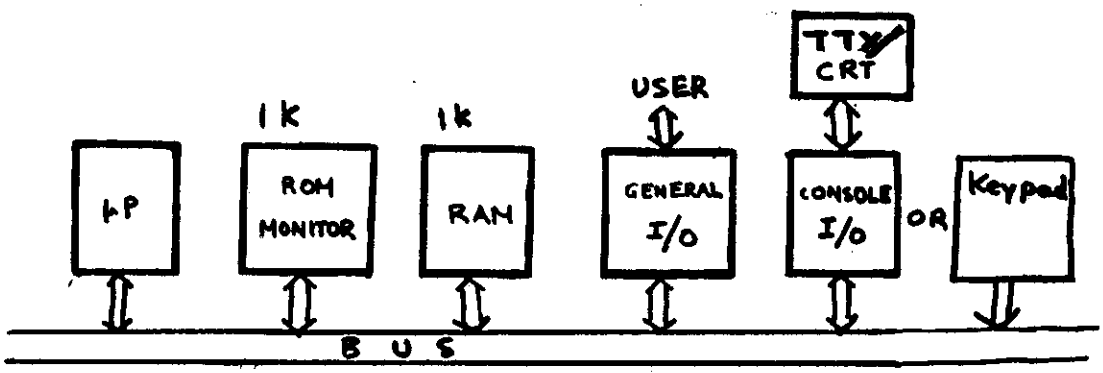
MICRO PROCESSOR
DEVELOPMENT
SYSTEMS

USED MAINLY FOR

- SOFTWARE DEVELOPMENT
- DEBUGGING
- INTEGRATION

- PRIMITIVE MONITOR : **L**oad **P**unch **M**emory **R**egisters **G**o

- HANDCODING
  - NO ASSEMBLER
  - NO EDITOR
- NO DEBUGGING FACILITIES EXCEPT SWI



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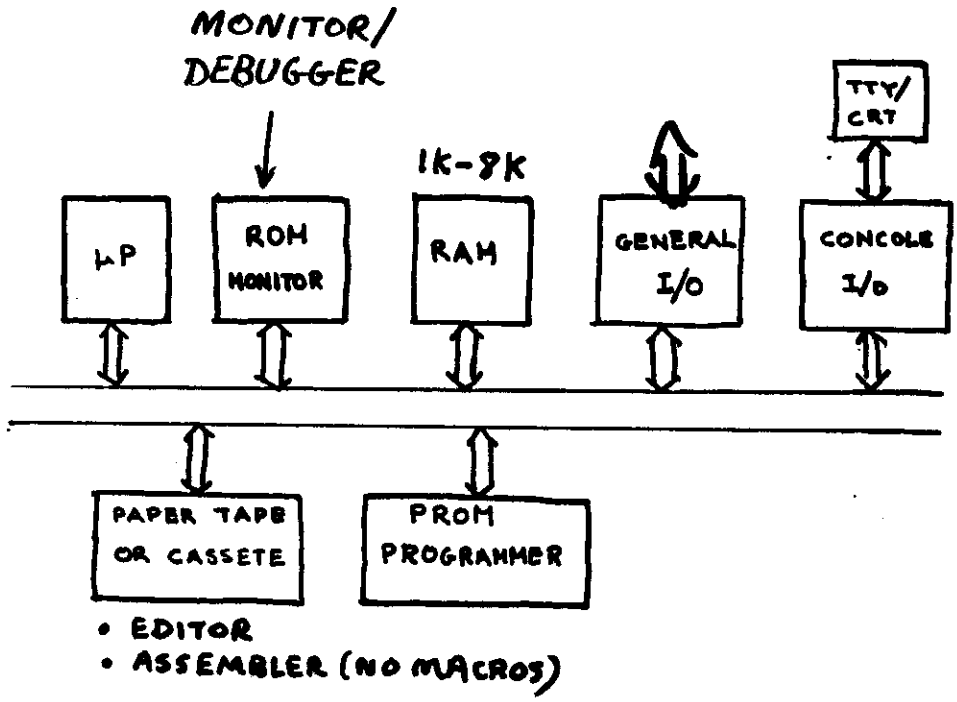
1ST generation MDS : no mass storage



- EDITOR
- ASSEMBLER (NO MACROS)

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2nd generation : Tape based MDS

Display / Set Registers

Display / Set Memory

Set / Remove Breakpoints

Set Trace Mode

Single Instruction Step

Start Execution of a program

Load program

Dump program

Prom program

ROSY (Resident Operating SYstem) COMMANDS

ASSEMBLER

BREAKPOINT - SET/CLEAR

COPY (Block start) (Block End) (To)
DATA-CONVERT (Value)
DECODE (From) (To)
EDITOR
GO [ADDRESS]
HELP [STRING]

MEMORY - COMPARE/DUMP/FILL/LIST/LOAD
MODIFY/VERIFY/

MON-EXEC (Number) Monitor Call

REGISTER - DISPLAY/MODIFY

RESTART

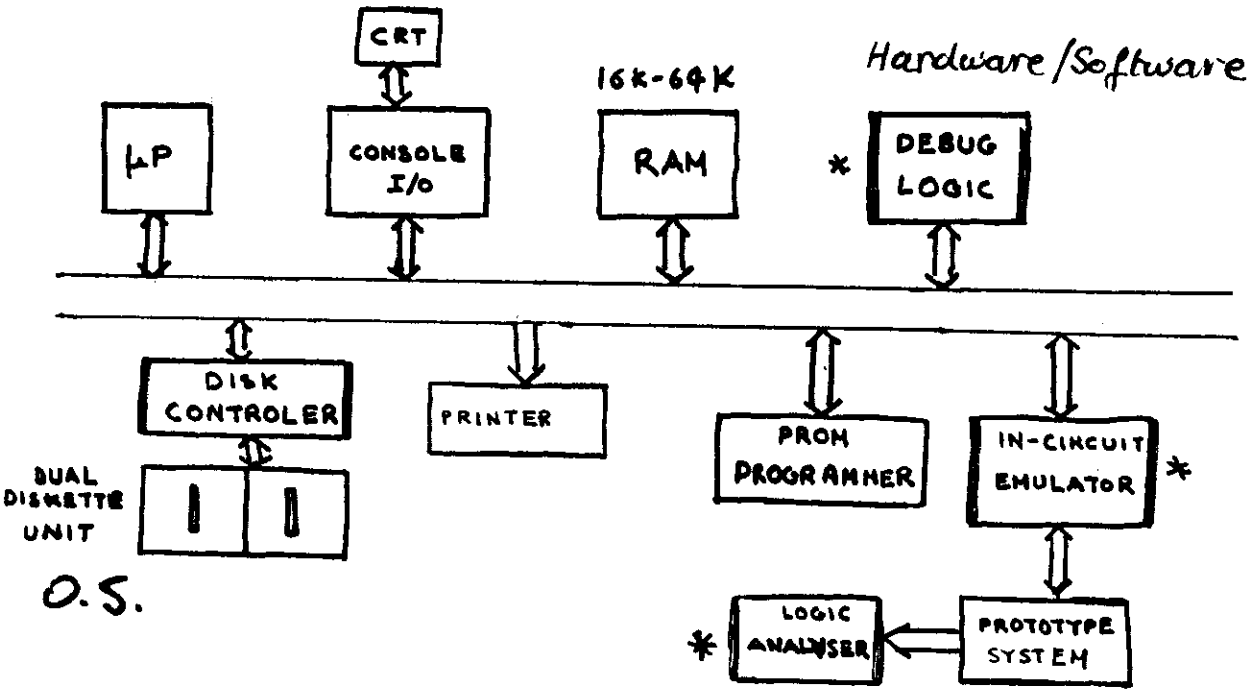
SEARCH (From) (To) (Byte or String)
SET-NUMBER-BASE
SLAVE [LUN]
TMODE [LUN] [BREAK] Transparent mode
TRACE [COUNT]

SINGLE-BOARD SYSTEMS : 1ST CLASS
(RECOMMENDATION OF THE CERN μP WG1)

- INCLUDE
  - EVALUATION KITS
  - EDUCATIONAL BOARDS
  - MONOBOARD MICROCOMPUTERS
- MOST COST/EFFECTIVE FOR
  - INITIAL FAMILIARIZATION
  - TECHNICAL TRAINING
  - REALIZATION OF SMALL PROJECTS
- LOW COST : SF 0.6 - 6 K
- SUPPORT
  - DEBUGGER/MONITOR
  - PROM PROGRAMMER
  - RESIDENT EDITOR - ASSEMBLER
  - CROSS-ASSEMBLER
  - DOWNLOADING
- PITFALL TO AVOID : WORK STARTED ON SUCH A SYSTEM EXPANDS TO A PROJECT WHICH NEEDS MORE APPROPRIATE SUPPORT.
- RECOMMENDATION : USE A MONOBOARD AND A MONITOR COMPATIBLE TO THE 2ND CLASS

Single-board μC's

- Over 70 manufacturers (E.D. March 1981)
- 8-bit & 16-bit μP's
- RAM 128 bytes - 64 kbytes
- ROM 1 kb - 32 kbytes
- DMA capability
- Buses : Multibus, Flexibus, EXORciser, Cyberbus, Exorbus, P, S-100, STD
- Parallel I/O lines : 8 - 48
- Serial I/O ports : 1 - 8
  Baud rate 110 baud - 500 kbaud
- Interrupt provisions
- Multi-processor capability
- Counter-times : 1 - 16
- Monitor/debugger up to O.S.
- Assembler up to HLL's (resident)
- Interfaces for : Audio-cassette, Printer, Video etc
- Special features



3rd generation : Disk-based MDS

- Card Cage
- Motherboard/BUS
- Power Supply

- SINGLE USER - [SINGLE TASK / MULTI TASK]
- MULTI USER - MULTI TASK
  MANY TERMINALS - HARDDISK

FILE MANAGEMENT SYSTEM on an MDS

- Allows creation and deletion of files
- Allows access to files for read/write
- Performs automatic management of secondary memory space. The user is not concerned about the whereabouts of his files
- Allows reference to files by symbolic names.
- Protects files against system failure
- Allows the sharing of files between co-operating users but protects files against unauthorized users.

Example:

MDOS COMMANDS

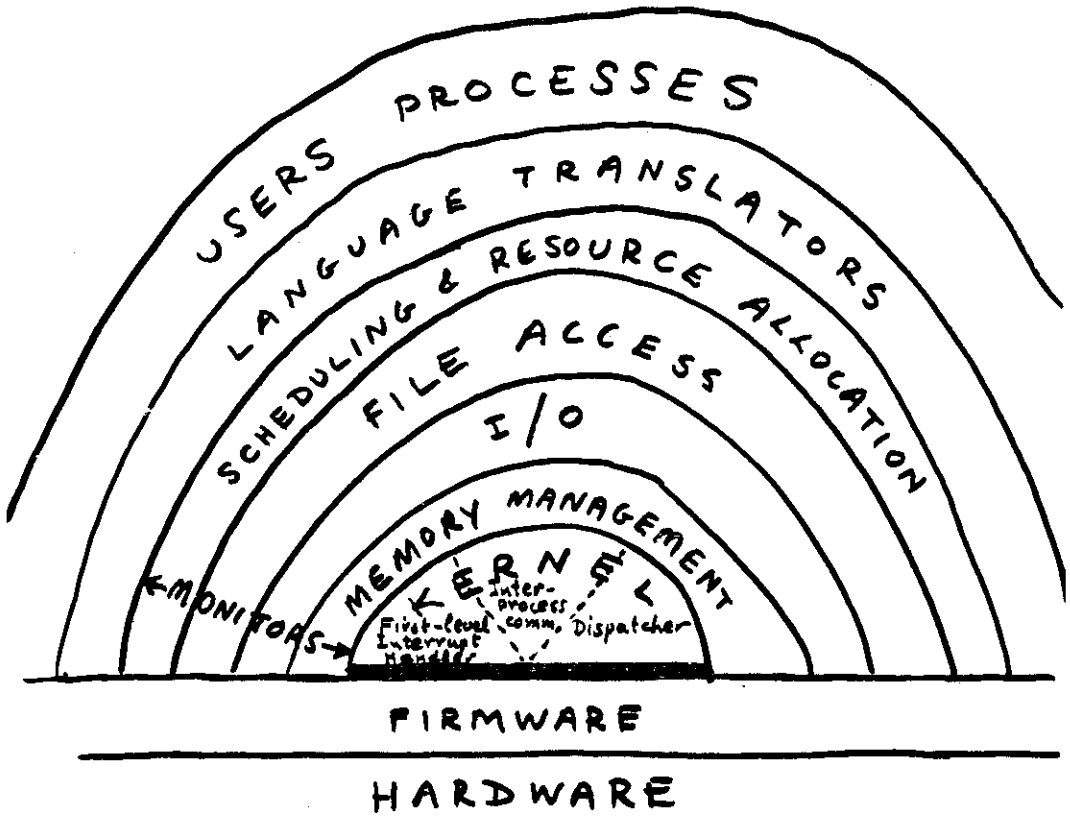
DIR	Display the file directory information
COPY	Copy file — Disk → Disk; Disk → Device; Device → Disk
DEL	Delete file from directory and free space
LIST	Display a disk file
LOAD	Load object disk file into memory
MERGE	Concatenate files to form a new file
NAME	Change file name and/or file attributes
PATCH	Patch Object disk file
CHAIN	Chain Console input to a disk file
BLOKEDIT	Copy selected lines from text files to a new file
BINEX	Convert Binary Object file to EXORciser Object
BACKUP	Create copy of disk; Optional file reorganization
DOSGEN	Create DOS tables & files
DUMP	Display disk sectors
EMCOPY	Convert EDOS files to MDOS files
FORMAT	format Disk
FREE	Display Free Space on disk
REPAIR	Examine and allow repair of System disk tables
ROLLOUT	Write memory block to disk

Example:

MDOS SYSTEM CALLS SCALLS

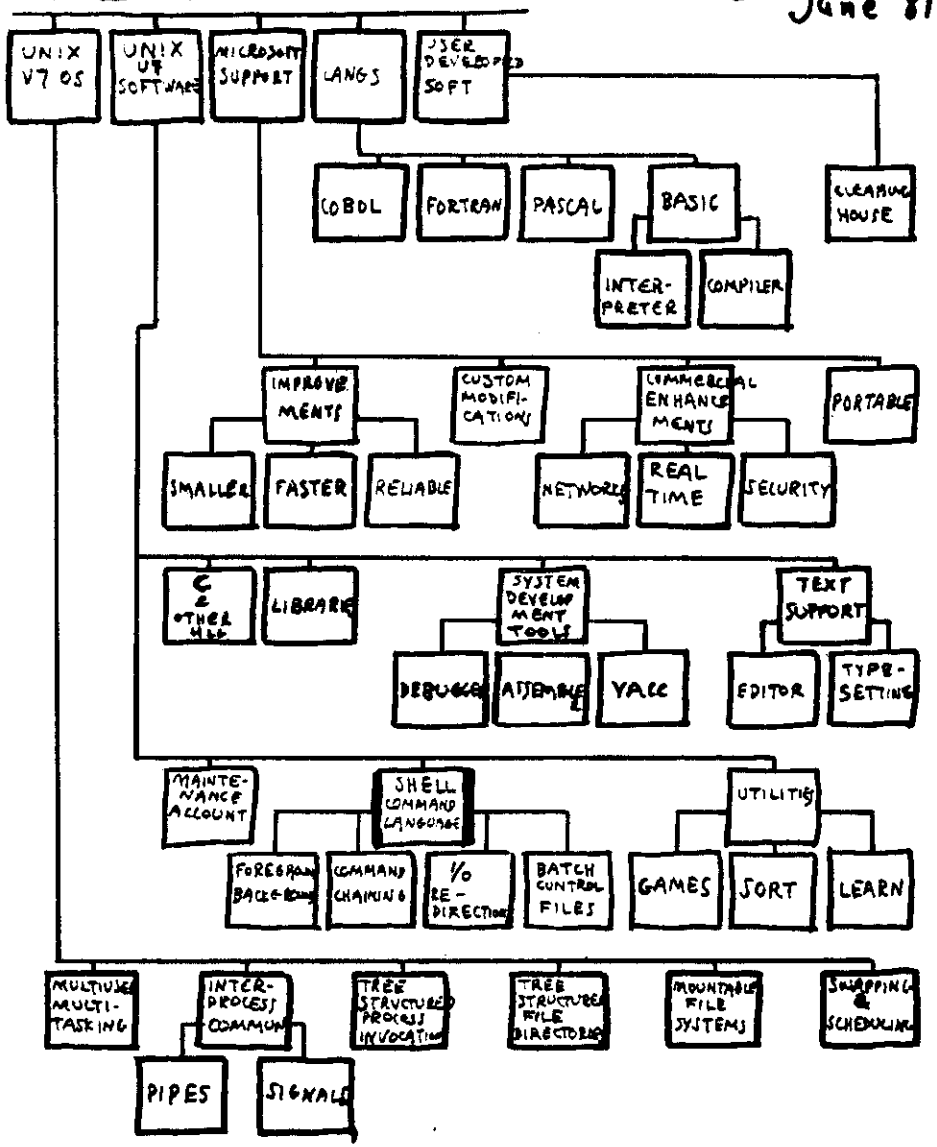
via SWI XX — system calls; user defined calls

1) Physical disk I/O functions
2) System console/printer I/O functions
3) file/memory functions
4) Register functions - Extend Instruction Repertoire
5) Arithmetic functions - Word Arithmetic
6) Unified I/O functions
7) String functions



ONION-SKIN VIEW OF COMPUTER SYSTEM

XENIX OPERATING SYSTEM [see BYTE June 81]



MULTI-BOARD SYSTEM : 2ND CLASS
(RECOMMENDATION OF THE CERN MP WG-1)

- A MULTI-BOARD MICROCOMPUTER
  - OF VARIABLE CONFIGURATION
  - FULL LOCAL OR HOST-BASED SOFTWARE
  - ENHANCED DEBUGGING FEATURES
  - AUTONOMOUS LOGIC STATE/TIMING ANALYSER (OPTIONAL)
  - FLOPPY OR HARD DISK ENVISAGED
- BASED ON A SELECTED RECOMMENDED BUS - STANDARD
- CARDS COMMERCIALLY AVAILABLE (ALSO HOME MADE)
- MEDIUM COST SF 10 - 50 K
- MOST COST/EFFECTIVE FOR
  - PROJECTS IN WHICH THE TARGET SYSTEM HAS THE SAME PHYSICAL FORM AS THE DEVELOPMENT SYSTEM (SAME BOARDS AND BUS)
  - PROJECTS FOR WHICH THE ADDITIONAL EXPENCE OF A REAL-TIME EMULATOR IS EITHER NOT JUSTIFIED (FEW REAL TIME CONSTAINTS) OR NOT POSSIBLE ANYWAY
- NEEDED SOFTWARE :
  - ENHANCED DEBUG MONITOR (SYMBOLIC DEBUGGING)
  - GOOD EDITOR (SCREEN EDITOR)
  - ASSEMBLER - HLL COMPILERS
  - OPERATIN SYSTEM WITH FRIENDLY USER INTERFACE AND MULTI-TASKING KERNEL WHICH TO BE USED IN TARGET SYSTEM ALSO WHEN NEEDED.

RECOMMENDED DEBUG MONITOR FEATURES

HELP FACILITY. COMMANDS ACCEPTED IN FULL OR ABBREVIATED FORM

TRANSPARENT MODE OF COMMUNICATION BETWEEN USER TERMINAL AND HOST. SELECTABLE EXIT CHARACTER

DOWNLINE LOADING OF OBJECT CODE (WITH OPTIONAL ADDRESS OFFSET) FROM THE HOST IN A STANDARD FORMAT. POSSIBLY UPLINE DUMPING

REGISTER DISPLAY (WITH SELECTION OPTION) & MODIFY

STACK DISPLAY

MEMORY DISPLAY & MODIFY. COMMANDS TO MODIFY, FILL OR DUMP BLOCKS OF MEMORY AS WELL AS INDIVIDUAL LOCATIONS

RELOCATION CONSTANT DEFINITION

SYMBOLIC DEBUGGING, IMPLEMENTED EITHER IN THE DEVELOPMENT SYSTEM OR VIA THE HOST

RUN CONTROL. GO FROM A SPECIFIED ADDRESS, LABEL, OR LINE NUMBER. GO FROM ....TILL.... CONTINUE

TRACING THROUGH SELECTED NUMBER OF INSTRUCTIONS OR LINES

BREAKPOINT HANDLING

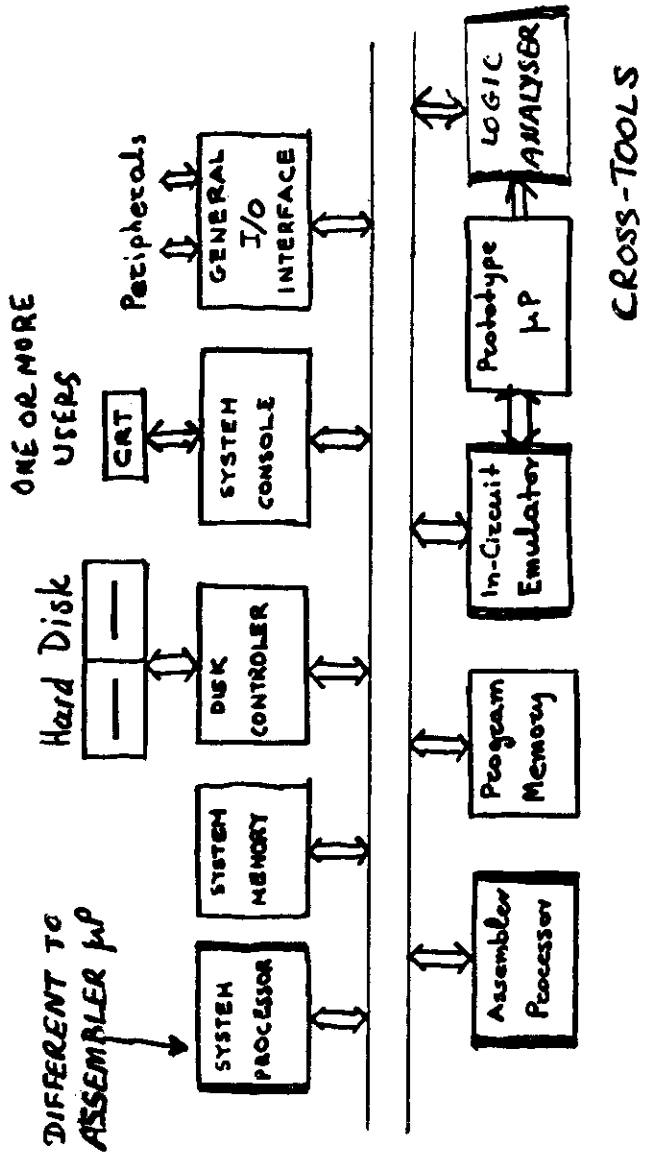
ABORT FUNCTION BY TERMINAL INTERRUPT

USER CALLABLE UTILITIES AND I/O ROUTINES

DISASSEMBLER.

ADDITIONAL OPTIONAL FEATURES FOR 2ND CLASS SYSTEMS

- LINE BY LINE ASSEMBLER
- SUBROUTINE CALLS FROM MONITOR
- NUMBER CONVERSIONS
- BLOCK MOVE FACILITY
- STRING AND PATTERN SEARCH FACILITIES
- TEST ROUTINES FOR MEMORY AND I/O



4th Generation: Universal MDS (UDS)

REMARKS ON UD SYSTEMS

UDS MANUFACTURERS HAVE A STRONG INTEREST IN PROVIDING SUPPORT WHERE POSSIBLE

HOWEVER,

FULL EMULATION OF SOME PRESENT μP's INCORPORATING INSTRUCTION PRE-FETCHING IS A FORMIDABLE TASK

THE INTRODUCTION OF CACHE MEMORY WILL MAKE FULL EMULATION IMPOSSIBLE - EXTRA STATUS LINES ARE NEEDED

THE SPEED OF SOME μP's WILL SOON EXCEED THE POSSIBILITIES OF THE EMULATOR LOGIC

THERE IS AN INEVITABLE TIME LAG BETWEEN THE INTRODUCTION OF A NEW μP AND THE AVAILABILITY OF FULL SUPPORT ON A UDS

UNIVERSAL DEVELOPMENT SYSTEM : 3RD CLASS
(RECOMMENDATION OF THE CERN MP WG1)

- UNIVERSAL MDS ADAPTED TO A RANGE OF μP's
- INCLUDE FULL FACILITIES FOR SOFTWARE DEVELOPMENT
- INCLUDE HARDWARE/SOFTWARE INTEGRATION BY IN-CIRCUIT EMULATION
- PROM PROGRAMMING
- LOGIC STATE & TIMING ANALYSIS OPTIONAL
- MOST COST/EFFECTIVE FOR
  - PROJECTS IN WHICH THE TARGET SYSTEM IS MADE FROM INDIVIDUAL LSI CHIPS AND IT DOES NOT INCORPORATE DEBUG FACILITIES AND IT IS NOT COMPATIBLE WITH THE STANDARD BUS
  - PROJECTS WHERE REAL-TIME EMULATION IS PARTICULAR VALUABLE TO DIAGNOSE BUGS
- HIGH COST SF 30 K - 100 K per USER STATION

Most Known MDS's

Motorola : EXORciser (680x) EXORmacs (68000)

Intel : Intelec MDS (808x)

* H/P : 64000 (6800, 8080, Z80, 68000...)

* Tektronix : 8002A (8080, 6800, Z80, 9900)

Texas : 990 (9900, TMS-1000)

Zilog : PDS-8000 (Z80-Z8000)

Advanced micro-Computers : AmSYS 8/8 (Z9000, 8080, Z80)

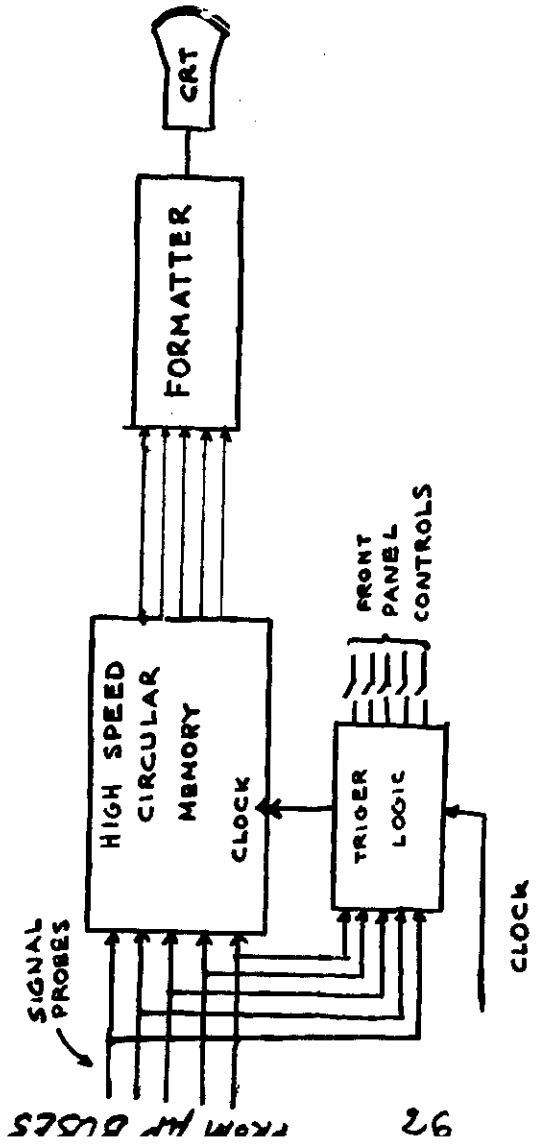
* GenRad/Futuredata : GR2300 (8010, 6800, Z80, 6502)

* International Data Services : MUDS 11 (Z8000, 8080, Z80, 69000, 6502)

Rockwell : System 65 (6502)

* Philips 4420 (68000, 6809, Z80 ...)

* Tektronix 8560 (6800, 6909, Z80 ...)



Block diagram of a typical logic analyser

LOGIC ANALYSERS - MODES OF OPERATION

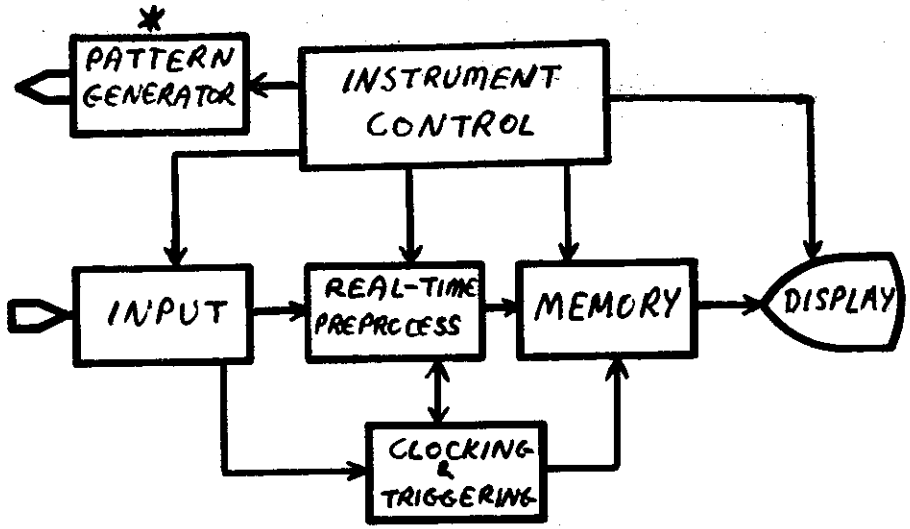
SYNCHRONOUS MODE

- PERFORMS LOGIC STATE (SOFTWARE) ANALYSIS
- USES THE CLOCK OF THE μP UNDER EXAMINATION
- SAMPLES THE μP buses AT THE EDGE OF THE CLOCK
- OUTPUT IN BINARY, HEX, OR DISSASSEMBLY
- PERSONALITY MODULES FOR VARIOUS μP's

ASYNCHRONOUS MODE

- PERFORMS LOGIC TIMING (HARDWARE) ANALYSIS
  YOU CAN OBSERVE TIMING RELATIONSHIPS BETWEEN LOGIC LEVEL TRANSITIONS ON SELECTED μP LINES
- USES ITS OWN CLOCK
- SAMPLES μP LINES AT MUCH HIGHER RATE THAN THE μP's CLOCK
- HENCE MORE EXPENSIVE
- OUTPUT IN WAVEFORM TIME DIAGRAMS

ARCHITECTURE OF LOGIC ANALYSERS



- INPUT : 8 to ≥100 INPUT LINES
- REAL-TIME PREPROCESS :
  - CLOCK QUALIFICATION : SORTING THE DATA ACCORDING TO TIME RELATIONSHIPS TO OTHER BUS SIGNALS
  - DATA QUALIFICATION : SORTING THE DATA BASED ON THEIR CONTENT

  INCREASES THE EFFECTIVE SIZE OF MEMORY
- MEMORY : ACQUISITION MEMORY DATA IS STORED INTO THIS MEMORY CONTINUOUSLY, OVERWRITING PREVIOUS DATA UNTIL A TRIGGER EVENT ENDS ACQUISITION

  REFERENCE MEMORY STORES A PATTERN FOR COMPARISON WITH CONTENT OF ACQUISITION MEMORY. DIFFERENCES ARE HIGHLIGHTED

- CLOCKING & TRIGGERING :
  - CLOCKING : SYNCHRONOUS
    ASYNCHRONOUS
  - TRIGGERING : BASED ON
    a) WORD RECOGNIZERS
       SIMPLE (A, B
       SEQUENTIAL (A→B→C)
       NESTED (MONITOR COND. BRANC
       NON-SEQUENTIAL (SOFT ALGORITH *
    b) EVENT COUNTERS
    c) DELAY TIMERS
  - TRIGGER ARMING ALLOWS THE ANALYZER TO ACQUIRE DATA BASED ON TWO DIFFERENT CLOCKS (SLOW - FAST)
  - GLITCH TRIGGERING

DISPLAY : TIMING DIAGRAM
STATE TABLE
MNEMONIC DISSASSEMBLY

INSTRUMENT CONTROL : CONVENTIONAL KNOBS
MENU DRIVEN
SOFT KEYS
PROGRAMMING
USER DEFINED MNEMONICS
SYMBOLIC SIGNAL IDENTIFICATION

PATTERN GENERATION : STIMULATES THE SYSTEM UNDER TEST
ALSO PROGRAMMED

LOGIC ANALYZERS COME AS :

- STAND-ALONE
- MDS ADD-ON

ONLY SYNCHRONOUS - STATE ANACYSIS
ONLY ASYNCHRONOUS - TIMING ANALYSIS
BOTH STATE & TIMING ANALYSIS

MANUFACTURERS : DOLCH, KONTRON
GOULD-BIOMATION, HP, NICOLET PARATRONICS,
PHILIPS, TEKTRONIX

DESIRABLE FEATURES FOR LOGIC ANALYSERS

LOGIC STATE (SOFTWARE) ANALYSIS

- TO OPERATE SYNCHRONOUSLY AT THE MAX μP CLOCK FREQUENCY (25 MHz for 16-bit μP's)
- TO HAVE ADEQUATE CLOCK QUALIFICATION LOGIC
- CHANNEL WIDTH AT LEAST EQUAL TO THE μP BUS LINES PLUS SOME ADDITIONAL STATUS LINES (48 channels for 16-bit μP's)
- ADEQUATE MEMORY DEPTH (256 STATES)
- ADEQUATE TRIGGER SEQUENCE DEPTH (8-16)
- USER-DEFINED MNEMONICS AND LABELS
- NON-VOLITILE RAM FOR SETTING-UP PARAMETERS
- PORTABILITY

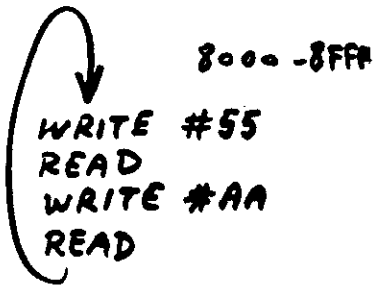
LOGIC TIMING (HARDWARE) ANALYSIS

- HIGH FREQUENCY OF ASYNCHRONOUS CLOCK (200 MHz ADEQUATE FOR 2 MHz μP's)
- SUFFICIENT NUMBER OF CHANNELS (min 4-8) TRIGGERED BY STATE ANALYSIS FUNCTION PLUS ADDITIONAL QUALIFICATION

EXAMPLE: RAM TEST USING 7D02 of Tektronix

```
1 IF                                          LOOP WHILE <
  NOT
  WORD RECOGNIZER #1                          no RAM read
  DATA = XX
  ADDRESS = 8XXX
  IO/M = X  INRQ = X  FETCH = X  R/W = 1
  INACK = X  HOLD = X  EXT TRIG IN = X
  TIMING WR = X
  OR                                          OR
  WORD RECOGNIZER  #2                         READ 55
  DATA = 55
  ADDRESS = XXXX
  IO/M = X  INRQ = X  FETCH = X  R/W = X
  OR                                          OR
  WORD RECOGNIZER  # 3                        READ AA >
  DATA = AA
  ADDRESS = XXXX
  IO/M = X  INRQ = X  FETCH = X  R/W = X
THEN DO
  GO TO 1                                     LOOP-END
ELSE DO
TRIGGER Ø - MAIN                              TRIGGER
    2 - AFTER DATA
    0 - SYSTEM UNDER TEST CONT
    0 - STANDARD CLOCK QUAL
TRIGGER 1 - TIMING
    - CENTERED
    THRESHOLD  V = Ø - PLUS 1.4Ø
    SAMPLE PERIOD 1 x 1 - 100NS
    WORD RECOGNIZER = XXXX XXXX
END TEST 1
  QUALIFY
Q STORE ON
Q WORD RECOGNIZER # 1                         8000 - 8FFF
Q DATA = XX
Q ADDRESS = 8XXX
      R/W = X
  END QUALIFY
```

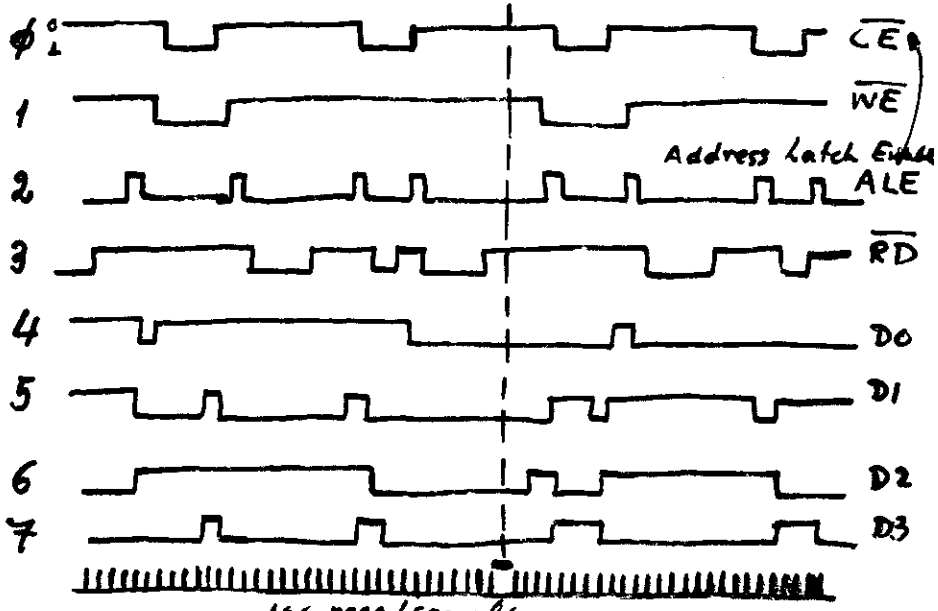
ONLY DATA READS ARE STORED & DISPLAYED



OUTPUT OF TEST

LOC	ADDR	OPERATION	
231	80F9	55 READ	
232	80F9	AA READ	
233	80FA	55 READ	
234	80FA	AA READ	LOGIC STATE ANALYSIS OUTPUT
235T	80FB	5F READ	
236	80FB	AA READ	
237	80FC	55 READ	
238	80FC	AA READ	
239	80FD	55 READ	
240	80FD	AA READ	

TIMING ANALYSIS OUTPUT



DEBUGGING AIDS ON AN MDS

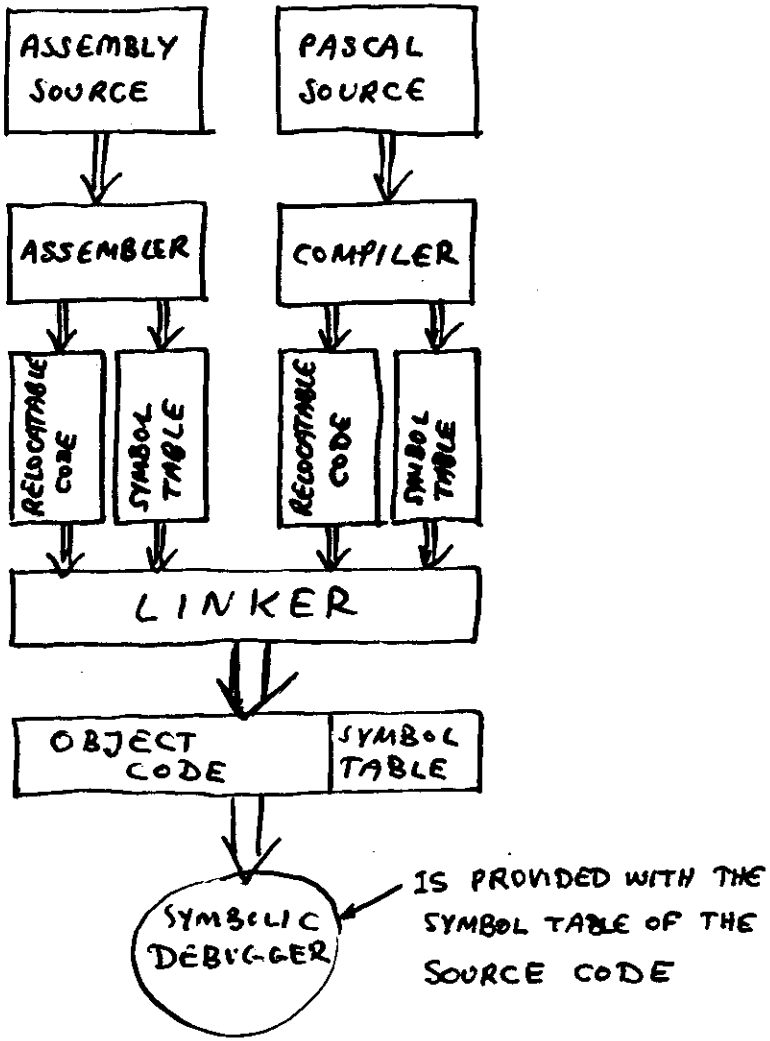
* MIXTURE OF HARDWARE & SOFTWARE

- SINGLE INSTRUCTION STEPPING
- PROGRAM TRACING
- BREAKPOINTS — HARDWARE / SOFTWARE (SWI)
- SYMBOLIC DEBUGGING
- MULTIPLE BREAKPOINTS

  AND, OR

  OF BREAKPOINT CONDITIONS
- IN-CIRCUIT EMULATORS

  They extend the debugging facilities of an MDS <u>into</u> the user's prototype system!



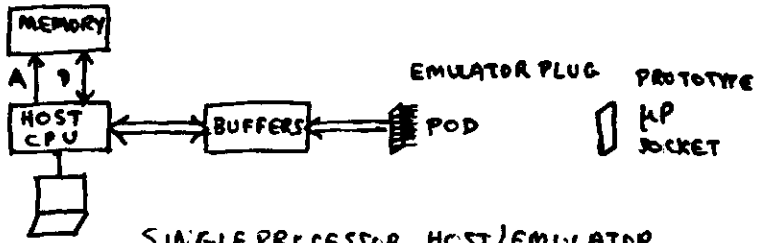
IN-CIRCUIT EMULATOR

DEBUGGER + LOGIC ANALYSER

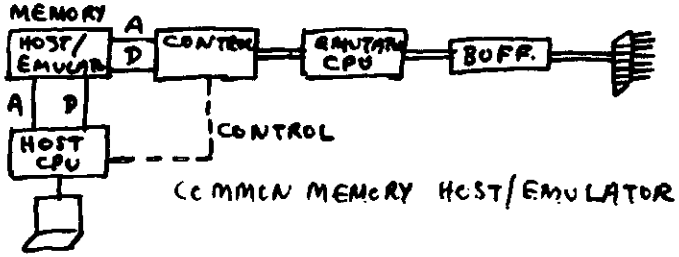
- CPU EMULATOR (Debugging)
- LOGIC ANALYSER
- ROM/RAM SIMULATOR
- I/O SIMULATOR

IT HELPS THE DESIGNER TO MONITOR, CONTROL, AND MODIFY IN AN INTERACTIVE / DYNAMIC WAY THE INTERPLAY BETWEEN THE HARDWARE - SOFTWARE OF THE PROTOTYPE SYSTEM

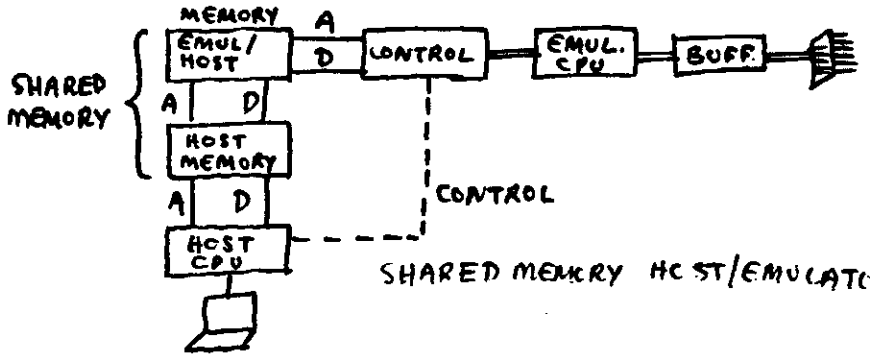
IN-CIRCUIT EMULATOR ARCHITECTURES



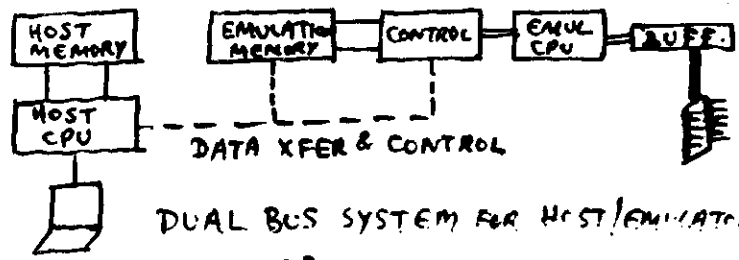
SINGLE PROCESSOR HOST/EMULATOR



COMMON MEMORY HOST/EMULATOR

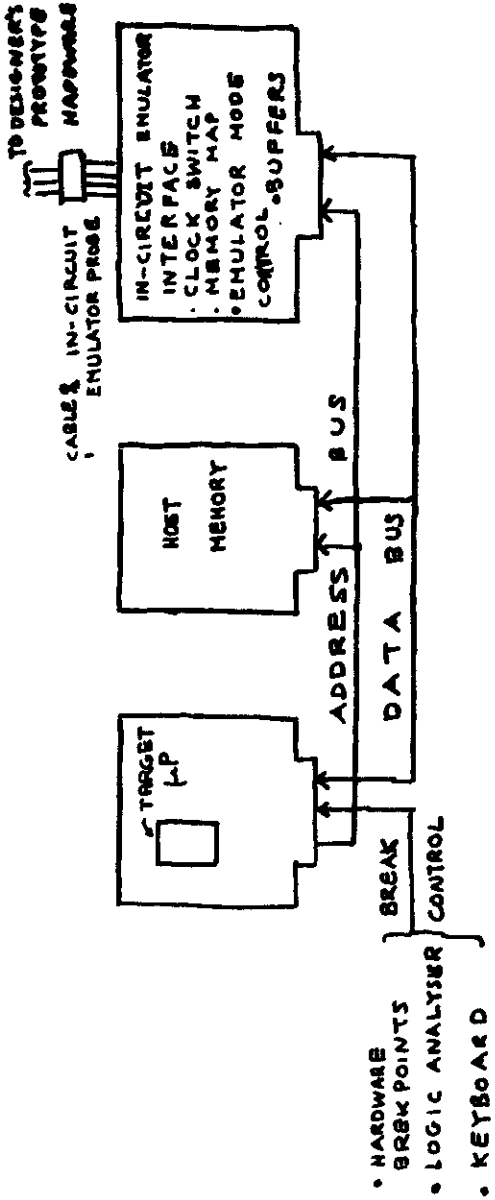


SHARED MEMORY HOST/EMULATOR



DUAL BUS SYSTEM FOR HOST/EMULATOR

Single-processor ICE architecture



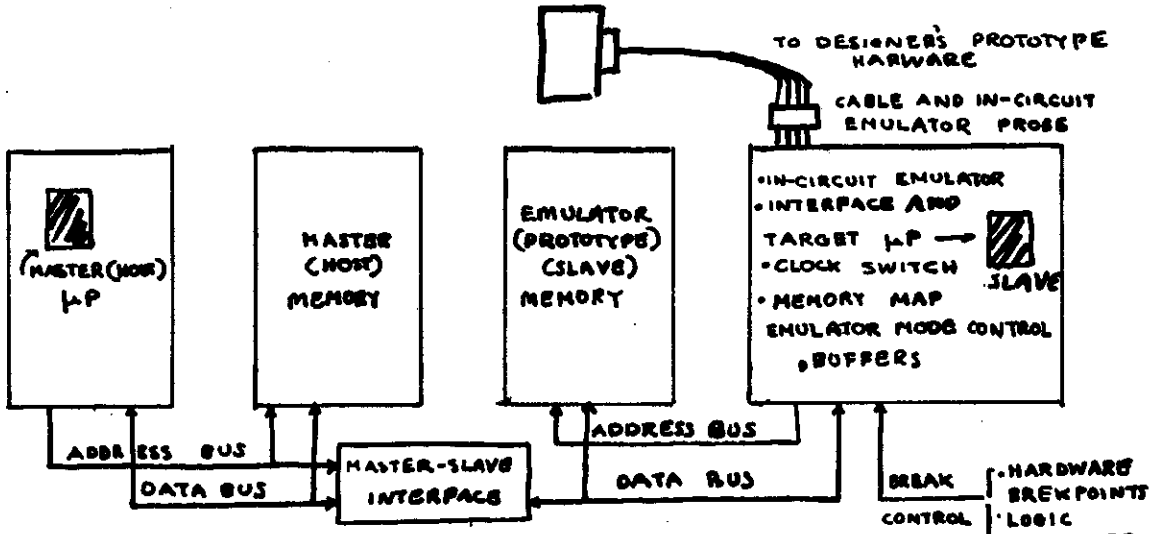
ADVANTAGES

- low cost
- one large memory

DISADVANTAGES

- need to rewrite software for new μP
- emulation is not completely separate

MASTER-SLAVE ICE architecture



MASTER μP performs
·system development functions

TARGET μP performs :
- prototype program execution
- prototype I/O
- in-prototype testing

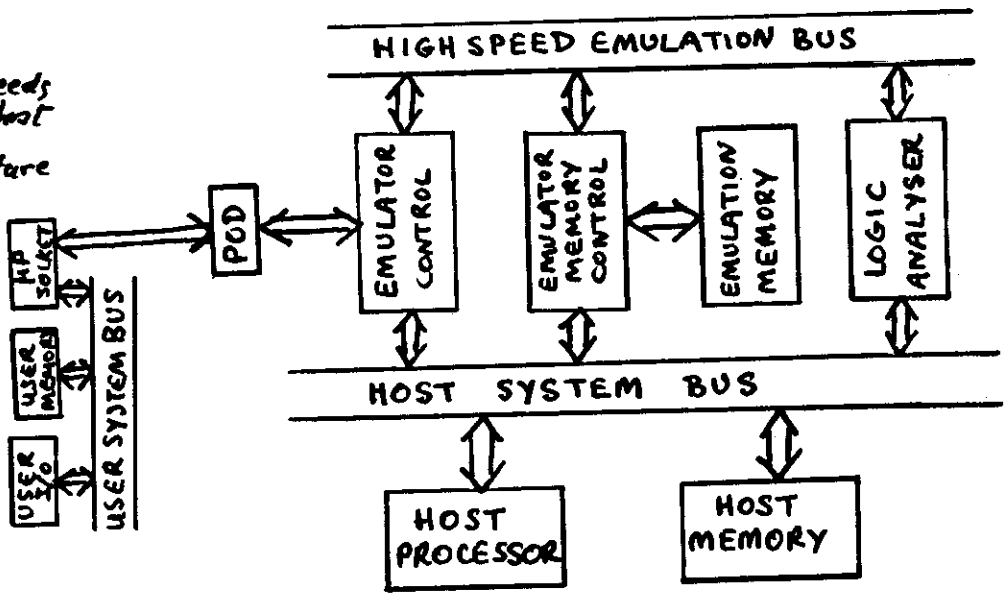
ADVANTAGES
- minimum software cost for implementing a new μP
- Host requires less of the system resources

DISADVANTAGES
- memory is split into two
- higher cost when adding memory and μP's
- Difficulty to handle a.s. modification for an unfamiliar host μP

UDS BLOCK DIAGRAM : TWO-BUS SYSTEM FOR ICE

Disadvantages
Same as previous scheme

Advantages
Emulation process proceeds independently of the host (sporadic events)
More flexible To future expansions



The ICE-80 in-circuit emulator of Intel

- Emulation / Single Step Commands

GO	Set up emulation conditions & start
STEP BY n	Step emulation
RANGE	of memory for tracing in real-time
CALL	emulates interrupt handling routines
CONTINUE	emulation

- Interrogation Commands

BASE	mode of display (decimal, Hex, Oct)
DISPLAY	display data of memory / register
CHANGE	data in memory / register
XFORM	define memory & I/O mapping
SEARCH	search user memory

- Utility Commands

LOAD	load the symbol table
SAVE	save a piece of code
EQUATE	Enter new name to Symbol table
FILL	fill memory with specific value
MOVE	move block of data in memory

IN-CIRCUIT EMULATER'S FEATURES

- PROCESSOR SWITCHING (HOST - EMULATOR)
- SHARING OF CIRCUITRY (FOR VARIOUS μP's)
- DEBUGGING CAPABILITIES
  - TRIGGERS & BREAKPOINTS
    - CONDITIONAL TRIGGERS
      - INSTRUCTION FETCH
      - MEMORY R/W
      - I/O R/W
      - COMBINATIONS
    - BREAKPOINTS (SOFT, HARD)
  - LOGIC STATE ANALYSIS
    - CONDITIONAL ANALYSIS & "WINDOWING"
    - DATA QUALIFICATION
  - MEMORY ACCESS
  - INSTRUCTION TRACING
- MEMORY MAPPING
- EMULATION WITHOUT PROTOTYPE

COMPARISON OF THREE UDS's (by the CERN µP WG1)

HP64000/TEKTRONIX 8560/PHYLIPS 4420

		HP 64000	TEKTR 8560	PHILIPS 4420
PORTABLE STATION FOR FIELD USE AVAILABLE?		64111c	N/c	N/c
STAND-ALONE STATION WITH LINK	- TO VENDOR'S HOST?	N/A	8540	N/A
	- TO OTHER HOST?	V24	8540	V24
STAND-ALONE STATION WITH	- HARD DISK?	YES	No	YES
	- FLOPPY DISK?	YES	8550	YES
	- CASSETTES?	Y/N	No	No
MULTIPLE STATIONS SHARING HARD DISK?		YES	8560	YES
FAMILY OF PERIPHERALS	HARD DISKS?	YES	YES	YES
	FLOPPIES	YES	YES	YES
	CASSETTES	YES	No	No
	TAPES	YES	No	YES
	PRINTERS	YES	YES	YES
RANGE OF EMULATORS	68000?	YES	YES	YES
	99000?	No	No	No
	6809?	YES	YES	YES
	Z80?	YES	YES	YES
	others?	MANY	YES	MANY
BIT-SLICE SUPPORT		SOME	No	No
PROM PROGRAMMING	2716	YES	YES	STAND ALONE PROM PROGR
	2732	YES	YES	
	2764	YES	YES	
	others	MANY	SOME	
CPU		HP	LSI 11/23	P851 + 68000
MAXIMUM MEMORY		96+32K	192 Ky	1 Mb
OPERATING SYSTEM		HP	TNIX	UNIX
LINKS BETWEEN UNITS - SPEED		4 Mbit/s	153 kb	9600 B
LOCAL AREA NETWORK CONNECTION		No ETHER	No ETHER	No ETHER
FUTURE TRENDS		?	?	

IN-CIRCUIT EMULATOR'S FEATURES

		HP	TEKTR	PHILIPS
BUS STRUCTURE - DUAL BUS?		YES	YES	YES
REAL-TIME EMULATION WITHOUT WAIT STATES (68000)		8 MHz	8 MHz	16 MHz
MAXIMUM EMULATOR MEMORY		128 Kb	256 Kb	256 Kb
MEMORY CONFIG. emulator → target	- MINIMUM block size	256 b - 1 Mb	4 Kb	256 b
	- ROM/RAM Illegal	YES	YES	YES
	- TOTAL ADDRESS SPACE	Target	Target	Target
DMA INTO EMULATOR MEMORY?		YES	?	YES
I/O SIMULATION (TRAPS etc)?		YES	YES	YES
MULTIPROCESSOR EMULATION?		YES	with multi 8540	4 µP / 2 µP
USER DEFINABLE EMULATOR		YES	No	NO

UP TO 24 ADDRESS LINES
UP TO 16 DATA LINES
UP TO 8 STATUS LINES
MEMORY CYCLE UP TO 4 MHz

UDS's LOGIC TIMING (HARDWARE) ANALYSIS

* TEKTRONIX & PHILIPS SUGGEST THE USE OF A STAND-ALONE ANALYSER

	HP	TEKTR. *	PHILIPS *
MEMORY DEPTH	4000		
MAX NUMBER OF CHANNELS	16		
MAX FREQUENCY			
4 CHANNELS	400 MHz		
8 CHANNELS	400 MHz		
16 CHANNELS	200 MHz		
DUAL THRESHOLD	YES		
TRIGGERING COMPLEXITY			
PATTERN ?	YES		
GLITCH ?	3 nsec		
SYMBOLIC ?	YES		

UDS's STATE (SOFTWARE) ANALYSIS

	HP	TEKTR	PHILIPS
MAXIMUN NUMBER OF CHANNELS	120	62	62
SYMBOLIC TRACING ?	YES	YES	YES
MNEMONIC DISASSEMBLY	YES	YES	YES
MEMORY-DEPTH	256	256	256
MAXIMUM CLOCK RATE	25 MHz	8 MHz	11 MHz
TRIGGER SEQUENCER	16 LVLS	4 LVLS	2 LVLS
OVERVIEW ? HISTOGRAMS	YES	^<	^<

UDS's USER INTERFACE

	HP	TEKTR	PHILIPS
DIRECTED SYNTAX (SOFT-KEYS)?	YES	*	*
MENU DRIVEN ?	NO	YES	YES
UNIX-LIKE ?	NO	YES	YES

* PROGRAMMABLE FUNCTION KEYS ARE AVAILABLE

DIRECTED-SYNTAX (SOFT-KEYS)

1ST LEVEL SOFT-KEYS

(EDIT) (COMPILE) (ASSEMBLE) (LINK) (EMULATE) (PROM.PRG) (RUN) (-ETC-)

THEY CHANGE WITH EACH KEYSTROKE TO REFLECT THE NEXT EXPECTED KEYWORD OR DATA IN A COMMAND

(DIRECTORY) PURGE RENAME COPY LIBRARY RECOVER LOG -ETC-

<FILE> (ALL-FILES) REC-FILES TAPEFILES — — LISTFILE —

<USERID> <DISK#> <TYPE> ALLUSERS (MODIFIED) ACCESSED LISTFILE -ETC-

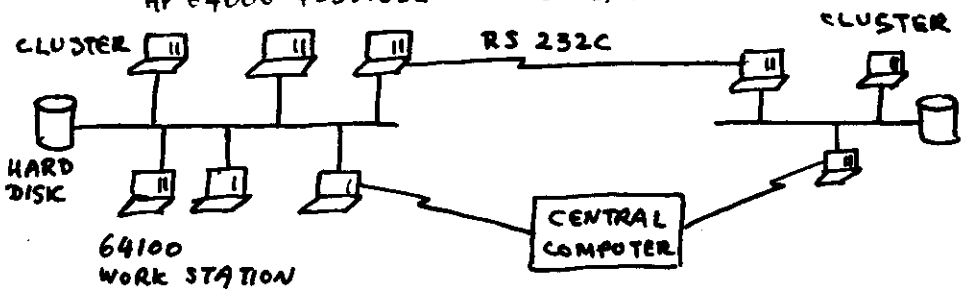
COMPLETE COMMAND

DIRECTORY ALL FILES MODIFIED AFTER [illegible] LISTFILE PRINTER -

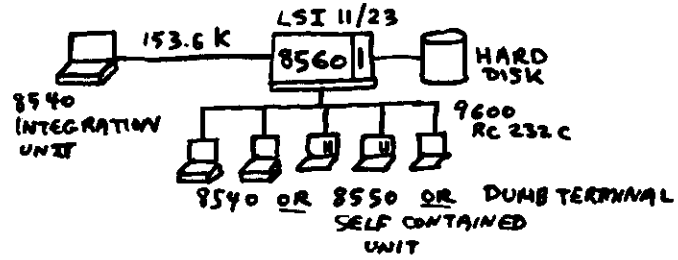
UDS's PRICES (KSF)

HP64000	TEKTRONIX	PHILIPS
BASIC SYSTEM (65) 16 K ROM/65 K RAM HARD-DISK 5Mb DUAL FLOPPY 0.5 Mb PROM PROG + 2 PERSONAL 48 CH STATE ANALYSER EMUL CONTROL + 68000 POD 8K EMUL MEMORY	8560 MULTI-USER (65) LSI 11/23 128 Kb RAM 35 Mb HARD DISK 1M FLOPPY I/o PROCESSOR 4 PORT	BASIC SYSTEM (75) P851 PROCESSOR 64 Kb RAM V.24 I/o 2 x 320 Kb FLOPPIES 68000 µP + UNIX V7 5Mb HARD DISK STATE ANALYSER SYMBOLIC DEBUG 8Kb EMUL MEMORY 68000 POD 68000 PASCAL COMPILER 68000 ASSEMBLER
LOGIC TIMING ANALYSIS 8 CH 200 MHz (22)	8540 INTEGRATION UNIT	
STATE ANALYSIS (15) 20 CH w. OVERVIEW 40 CH w/o -"-	MAX SYSTEM : (55) 32 Kb EMULATION MEM POD SYMBOLIC DEBUG STATE ANALYSIS PROM PROG	ADDITIONAL USER TERMINALS (3c EACH
SOFTWARE 68000 ASS+L+L (2.4) 68000 PASCAL (6.4)	8550 SELF-CONTAINED UNIT	
PORTABLE STATION (29) DUAL-FLOPPY	MAX SYSTEM (8c) 2Mb FLOPPY 32 Kb EMUL. MEMORY ASSEMBLER POD SYMBOLIC DEBUG STATE ANALYSIS PASCAL-COMPILER PROM PROG	
64 Mb HARD DISK (31)		

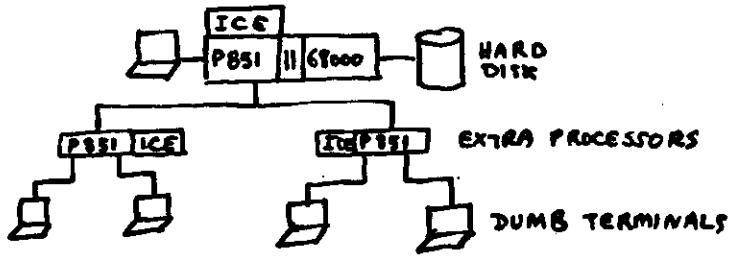
HP 64000 POSSIBLE CONFIGURATION



TEKTRONIX 8560 POSSIBLE CONFIGURATION



PHILLIPS 4420



MAIN FEATURES OF HP 64000 UDS
(IT IS THE WINNER)

DIRECTED SYNTAX (SOFT KEYS) IN ALL PHASES { SOFT. DEVELOP, EMULATION, STATE ANALYSIS, TIMING ANALYSIS }

DUAL-BUS FOR IN-CIRCUIT EMULATION

LOGIC STATE (SOFTWARE) ANALYSIS

LOGIC TIMING (HARDWARE) ANALYSIS

USER DEFINABLE EMULATOR

OVERVIW FACILITY TO SPOT SYSTEM BOTTLENECKS
HISTOGRAMS OF VARIOUS ACTIVITIES

SYMBOLIC DEBUGGING IN ALL PHASES { EMULATION, STATE ANALYSIS, TIMING ANALYSIS }

INTERACTION BETWEEN

- OVERVIEW ↔ STATE ANALYSIS
- TIMING ANALYSIS ↔ STATE ANALYSIS
- EMULATION ↔ ANALYSIS

DUAL THRESHOLD (TO IDENTIFY MARGINAL SIGNAL LEVELS)

SCREEN EDITOR
USER-DEFINABLE ASSEMBLER

References on MDSs

1) See references given in "Software Tools for Microprocessors Based Systems" by C. Halatsis, Proceedings 1980 CERN School of Computing,

2) Vincent Tseng, "Microprocessor Development and Development Systems" Granada Publishing, 1982, ISBN 0-246-11490-8

3) For a survey on MDS manufacturers see "A guide to tool Selection" by M.L Stiefel, Mini-Micro Systems, Aug 1980

4) For CERN WG1 recommendations on MDS's see Interim Report of the Steering Committee for Microprocessor Standardization, CERN, 2 Aug 1982