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Artificial Retina Chips, Vision for Automated Image Processing

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Artificial Retina Chips and Other Approaches to Direct Image Processing: Concepts and Applications

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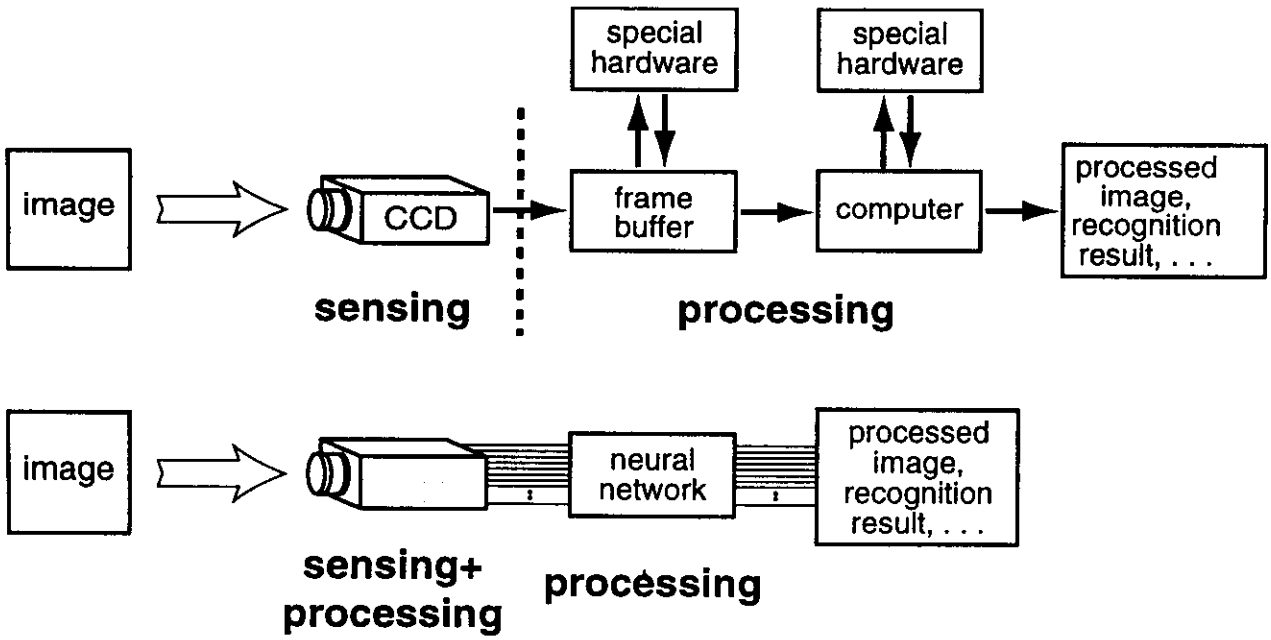
1. Benefits and limitations
2. Detector types
3. Building blocks
4. Optical neurochips
5. GaAs retina chips
6. CMOS retina chips
7. Retina chip applications

Vision Chip vs. CCD

Conventional, CCD-based image processing systems seperate sensing and processing, rely on serial data transfer, and tend to be not very compact, even if the processing task is simple. Vision chips employ on-chip sensing and processing, sometimes combined with parallel postprocessing, resulting in simple systems with a fast response time.



Vision Chips: Motivation

- Data reduction (avoiding redundant data acquisition).
- Significant amount of preprocessing.
- Understanding and modeling biological visual systems.
- Seeing the unseen (example: overcoming limitations with regard to speed and dynamic range).

Vision Chip Trade-Offs

Sensitivity, Low Noise vs. Sophisticated Processing

- Maximum feasible chip size is limited.
- Increasing space for processing functions (transistors) reduces photosensitive area.
- Can be partially overcome (for example, by microlens-array, but: increases manufacturing complexity).

Vision Chip Trade-Offs

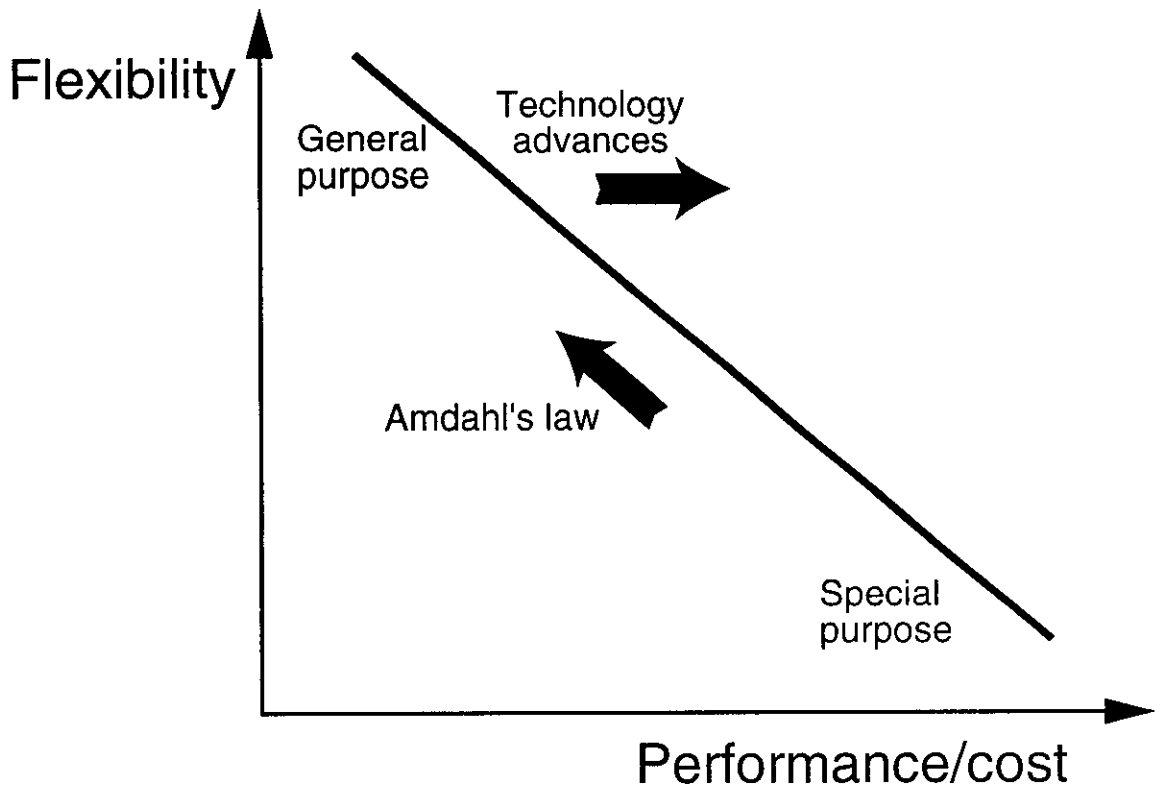
High Resolution vs. Sophisticated Pixel-Level Processing

- Increasing the resolution reduces the maximum area available for processing (even when noise and sensitivity issues are ignored).
- Therefore: most chips with significant pixel-level processing capabilities have low resolution (128×128 pixels or less).
- When compared to the central area of the human retina, such resolutions correspond to a field of view of just a few degrees.
- Concentrating sophisticated processing along the border of the sensor and using only simple pixel-level processing can help.
- Shrinking design rules help to increase transistor count, too (but: make design of effective photodetectors harder).

Vision Chip Trade-Offs

Flexible vs. General Purpose

- Applies to many kinds of special purpose processors.



Vision Chip Trade-Offs

Flexible vs. General Purpose

- AMDAHL's law tends to push in the direction of more flexible solutions (maximum speed-up achieved by parallel computing is in inverse proportion to the size of the part of the program the can not run in parallel).
- Technology advances push the curve to the right.

Vision Chip vs. CCD

Disadvantages and advantages of direct image processing using vision chips:

− Low flexibility. (Often adapted to a specific processing task, which requires special design that is not available of-the-shelf.)

− Low accuracy. (Complex pixel-level analog designs introduce errors like fixed pattern noise.)

+ High speed of operation, fast response. (Example: motion detection combined with fast random access read-out of important areas.)

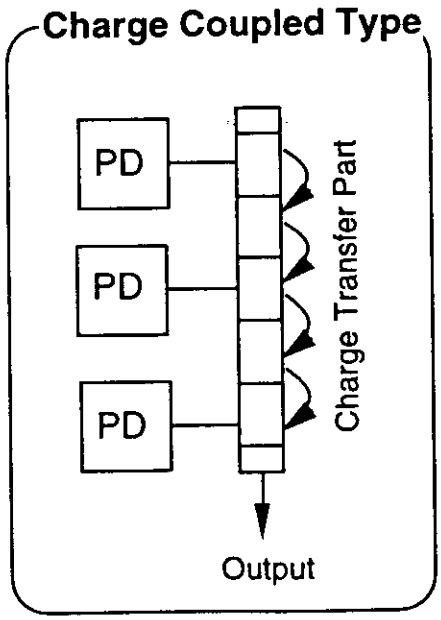
+ Large dynamic range. (Logarithmic response or local gain control can be implemented.)

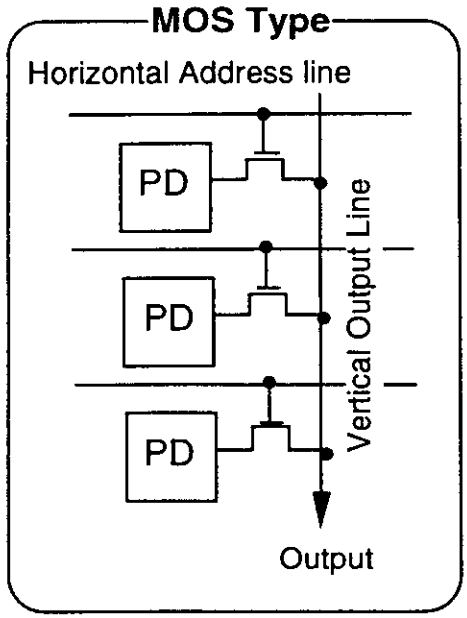
+ Low power dissipation. (Milliwatts instead of hundreds of milliwatts — no need to drive many high-capacity lines with high voltages.)

+ Low cost. (Integration of several components on one chip — no need for seperate driver and A/D converter chips).

+ Small system size.

Detector Types: CCD vs. MOS



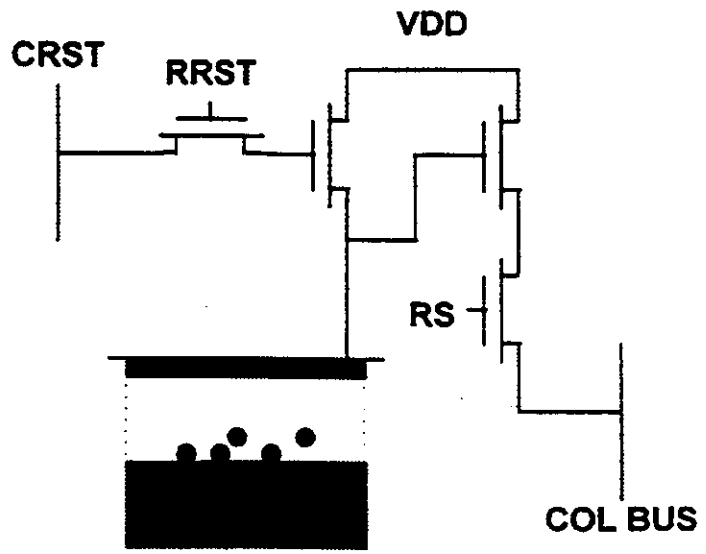


Remarkable CCD Characteristics

- Large pixel count (up to 7000×9000).
- Extensive spectral coverage (0.1 nm–1.1 μm).
- 99.9999 % pixel transfer efficiency (one electron lost when transfering 1000 electrons 1000 times).

Detector Types: Photodiode Active Pixel Sensor

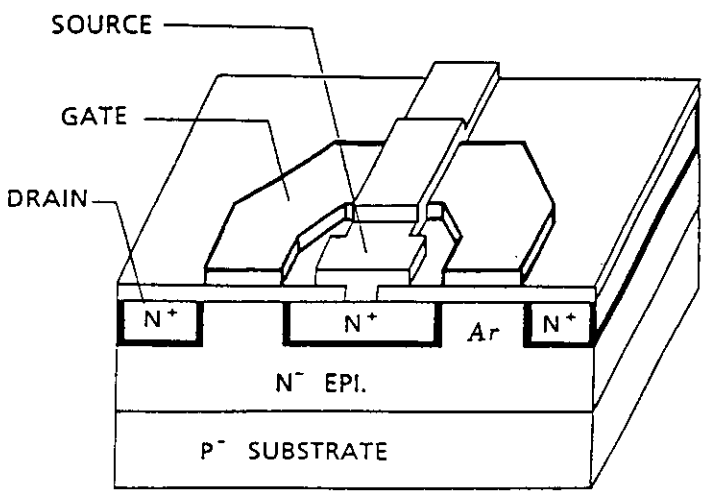
- Shown: photodiode-type active pixel sensor with individual pixel reset circuitry [Yadi 97].
- 64×64 array of these sensors is used as star tracker that can capture bright and dim stars simultaneously.
- 80 dB dynamic range.



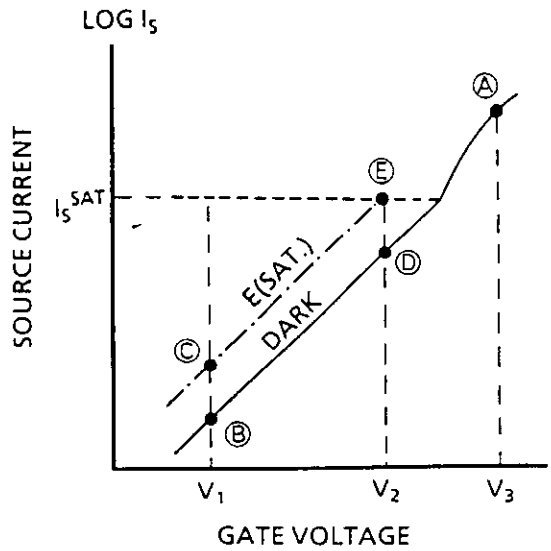
[Yadi 97]

Detector Types: CMD

- Very compact design (just one transistor) [Mats 91].
- Variable sensitivity.
- 4M pixel CMD sensor with block and skip Aacess capability has been implemented [Nomo 97].



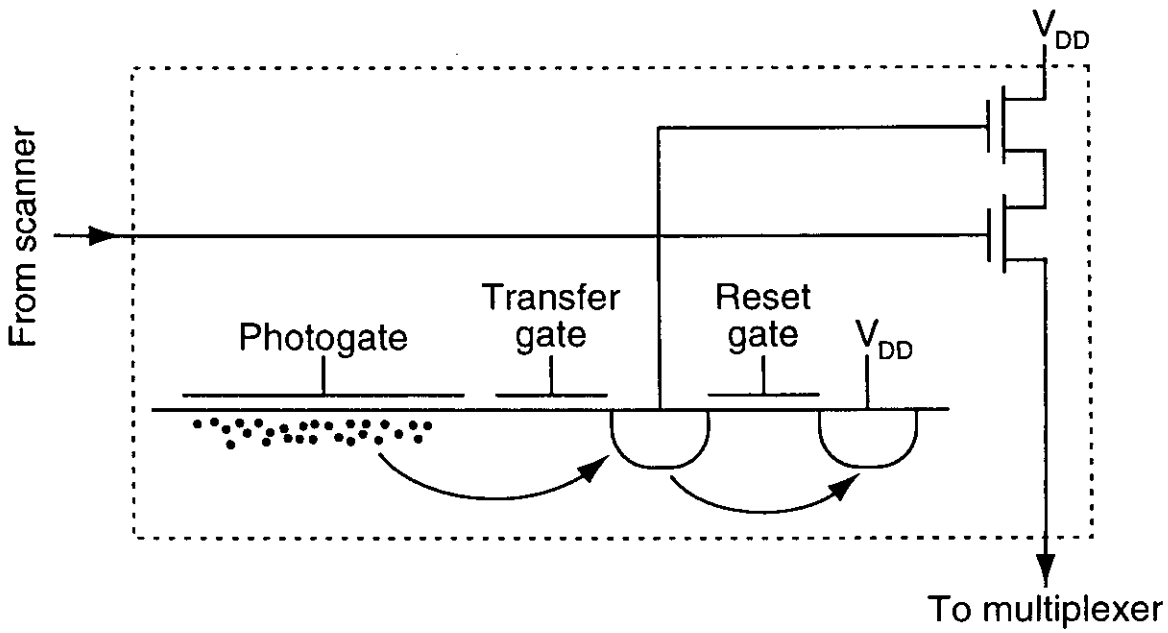
[Mats 91].



[Mats 91].

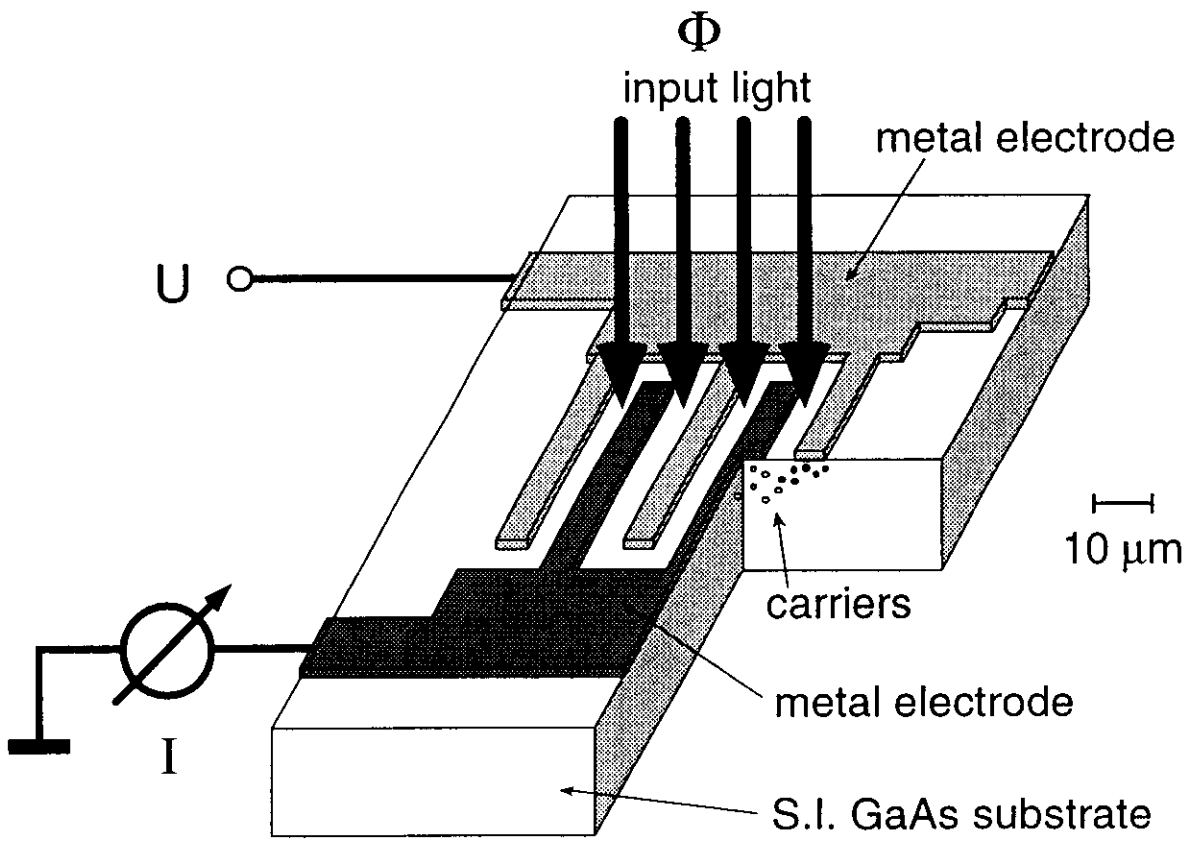
Detector Types: 1-pixel CCD

- Each pixel of Fossum's active pixel image sensor resembles a small single-stage CCD [Foss 95].
- Can store previous image, and output difference between two images (in combination with correlated double sampling).
- Example: 675×900 pixel, 37×28 mm^2 sensor for Dental X-rays [Nixo 98].



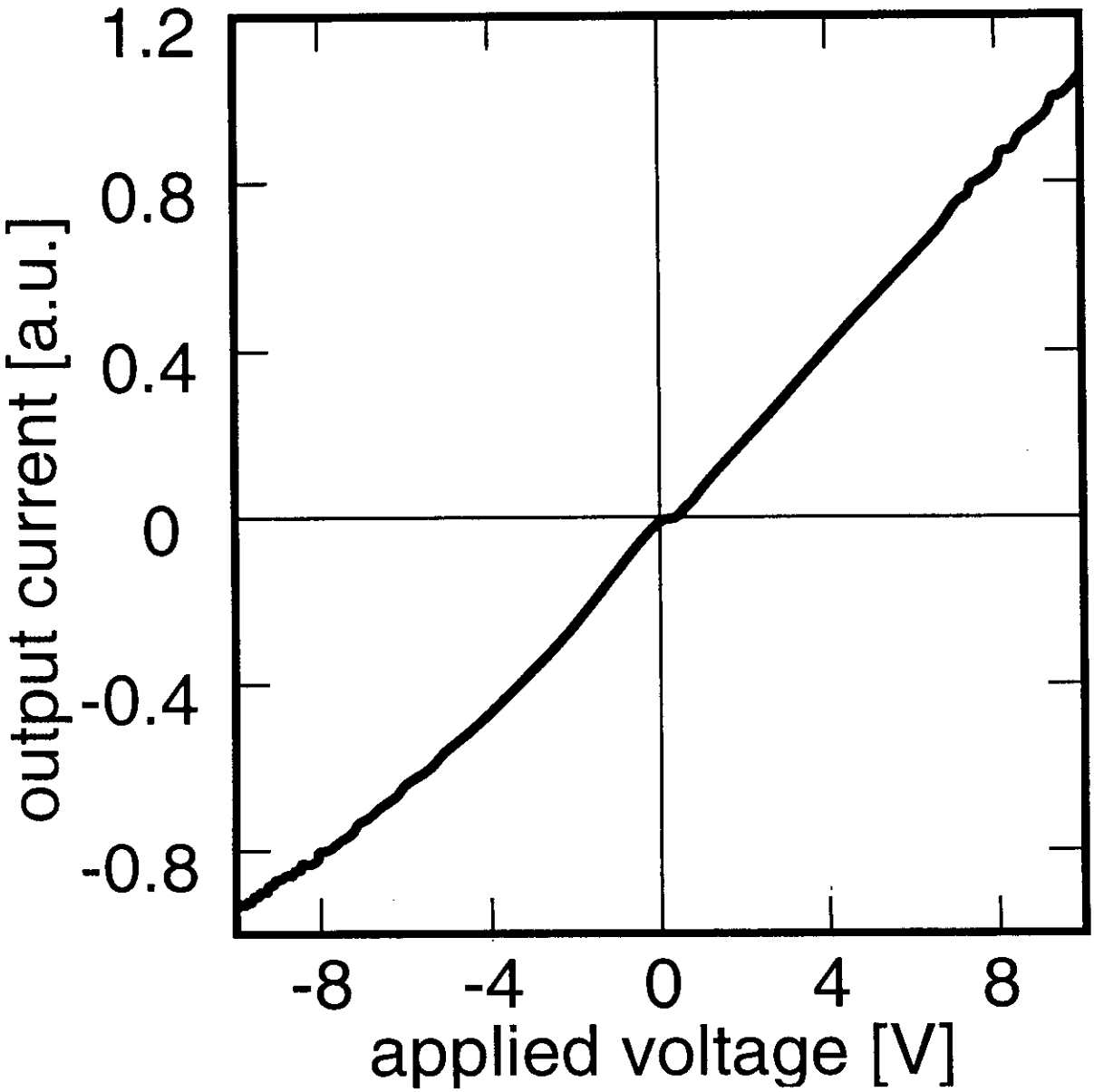
Detector Types: MSM-VSPD

Metal-semiconductor-metal variable sensitivity photodetectors have a simple, planar structur, but lacks charge integration capability [Nitt 91].



MSM-VSPD Response Curve

The applied bias voltage controls the sensitivity of MSM-VSPDs.



1-D Resistive Networks

Resistive chain, applied to centroid computation:

$$\frac{I_a}{I_b} = \frac{U/(kR)}{U/(nR)} = \frac{n}{k} ,$$

I_b rises in proportion to the position of the point of injection, k:

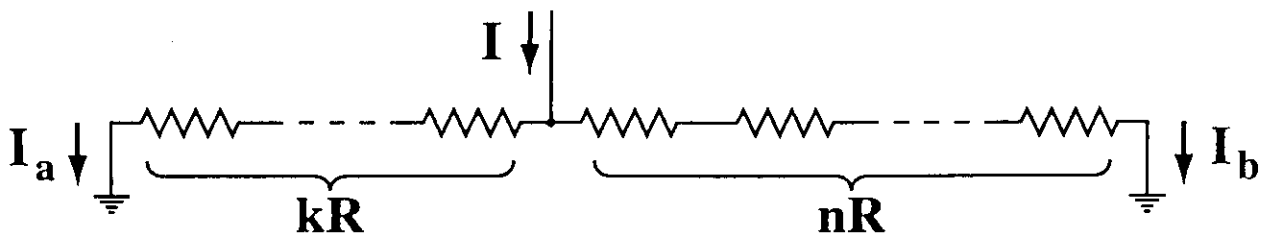
$$\frac{I_b}{I} = \frac{I_b}{I_a + I_b} = \frac{k}{N} , \quad \text{with } N = n + k .$$

Injecting (photo-) currents I_k at multiple nodes results in the superposition of the output currents,

$$I_b = 1/N \sum_{k=1}^{N-1} k\, I_k ,$$

so that the centroid $\bar{k}$ of the input currents (or of a light spot) can be easily derived:

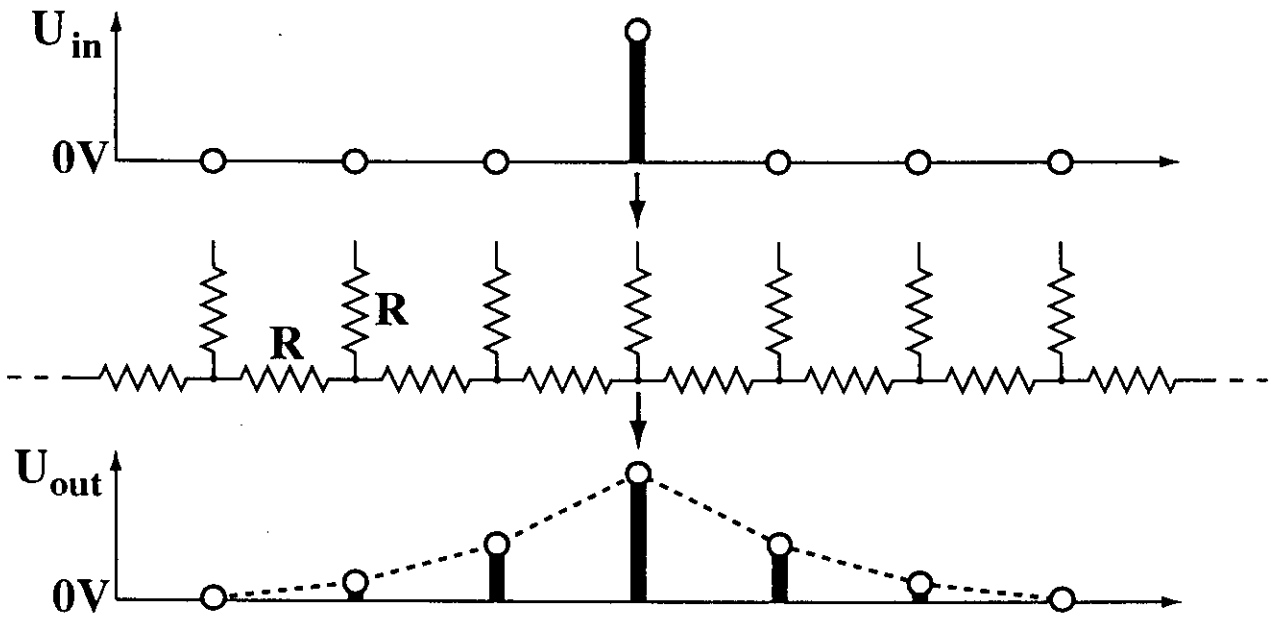
$$\bar{k} = \frac{\sum_{k=1}^{N-1} k\, I_k}{\sum_{k=1}^{N-1} I_k} = N \frac{I_b}{I_a + I_b} . \qquad (1)$$



1-D Resistive Networks

Resistive chain, applied to spatial smoothing:

- The output voltage distribution represents the result of convolving the input signal with a symmetrically decaying exponential function.
- The ratio of the resistance of the vertical resistors to the resistance of the horizontal resistors determines the amount of spatial smoothing.
- Example: edge detection chip [Bair 91].



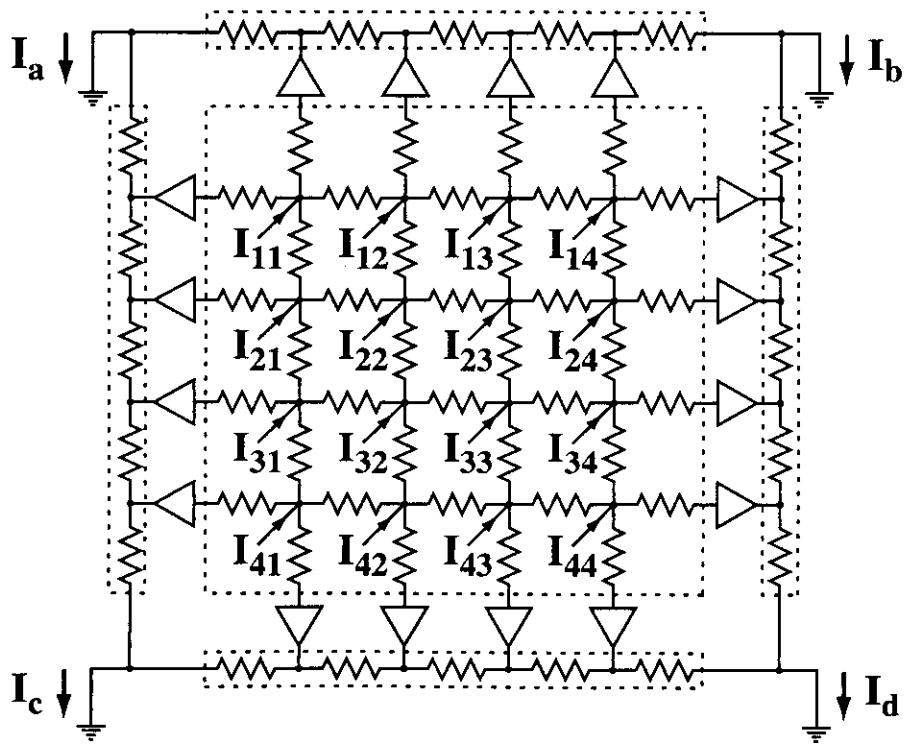
2-D Resistive Networks

2-D Resistive grid, applied to orientation and position detection: Standley's object position and orientation detection chip [Stan 91] computes five moments $M(l,m)$ of an image's brightness distribution W_{xy},

$$M(l,m) = \sum_{xy} x^l W_{xy} y^m \ ,$$

using linear and quadratic resitive chains and a resistive grid with 30×30 resistors. Estimates position and axis of least inertia of a bright object on a dark background up to 5000 times per second.

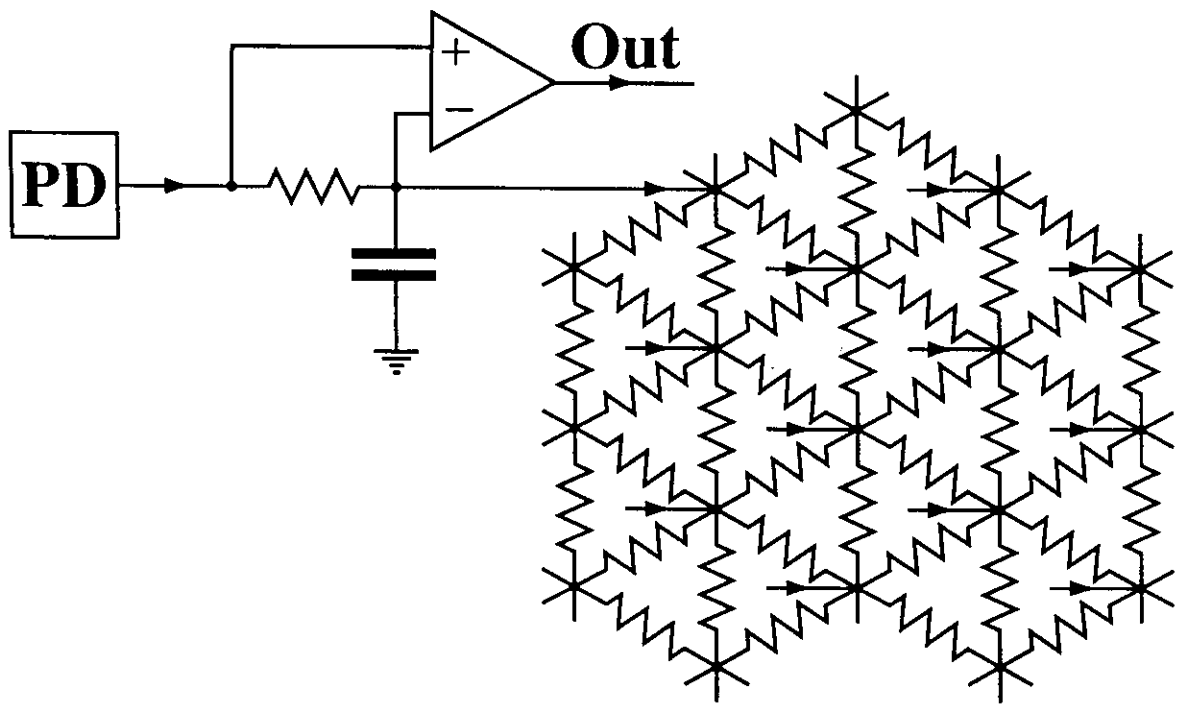
A similarily configured spherical 2-D Resistive grid has been used for sun tracking [22] (Veni 95).



2-D Resistive Networks

2-D Resistive grid, applied to spatiotemporal smoothing (Mahowald and Mead's silicon retina [Maho 89]):

- Two-dimensional, hexagonal, active resistive grid for variable spatial smoothing.
- Logarithmic photodetectors.
- Network capacitances result in additional smoothing in the temporal domain.
- Differential amplifier generates high-pass filtered output signal..



Resistive Networks Applications

- Many other computational vision algorithms can be formulated as minimization problems that can be mapped to resistive networks [Pogg 85, Koch 94].
- Nonlinear resistive elements add further processing functions.
- Resistive fuses: usual linear resistor for small voltage drops, but open circuit for large voltage drops [Harr 89, Yu 92, Luo 92].

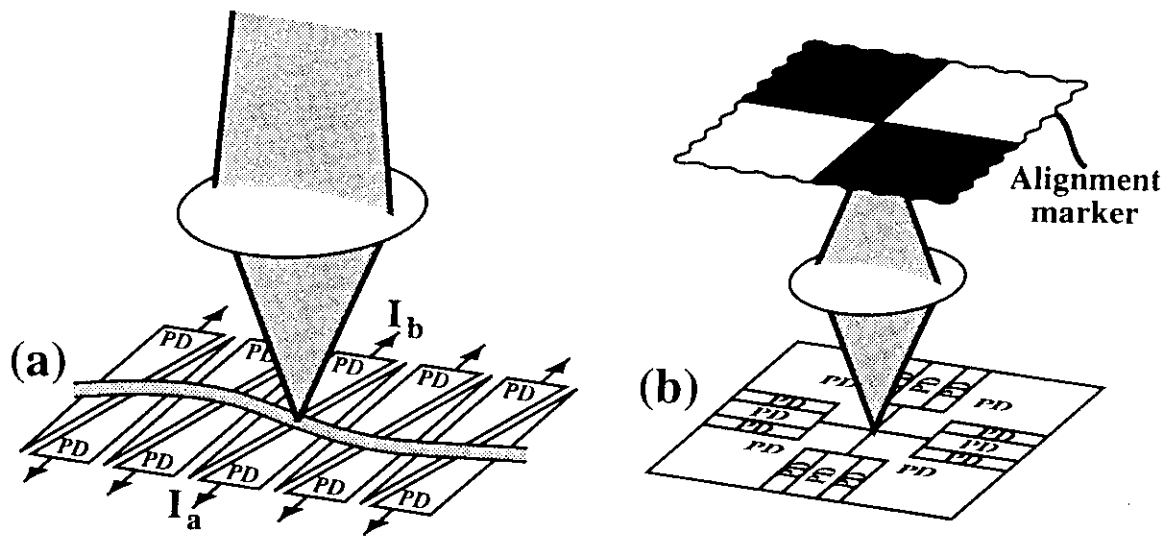
Processing using Detector Geometry

- Semiconductor manufacturing processes achieve submicrometer precision.
- 'Smart' detector shapes can be implemented reliably.
- Problem: large-scale distortions (but: good repeatability).

Processing using Detector Geometry

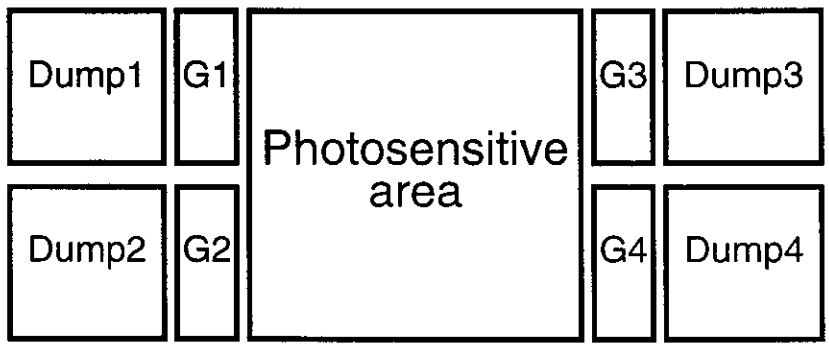
Examples:

- A line of pairs of triangular photodetectors senses the position of the centroids of a light profile (used for 3-D camera operating at video speed) [Kram 92, Seit 93].
- 16 precisely shaped photodetectors sense the position of an alignment marker (minimum repeatability: 0.3 μm) [Ummi 95].



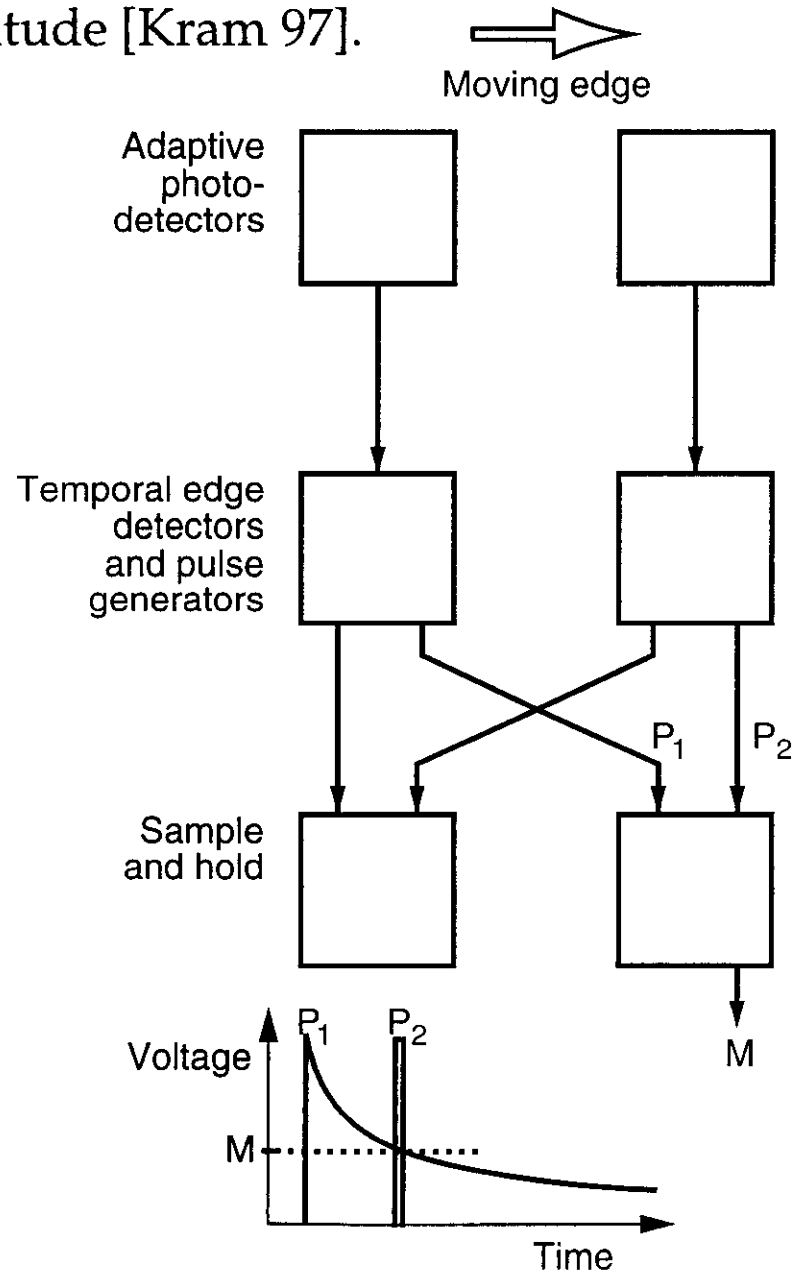
Lock-In Detection

- Lock-in detection of light in standard CCDs is limited by their low frame rates.
- A pixel layout that has four charge accumulation areas (instead of one) overcomes the problem [Spir 95].
- Application: 2-D phase measurement of rapidly oscillating light intensity.



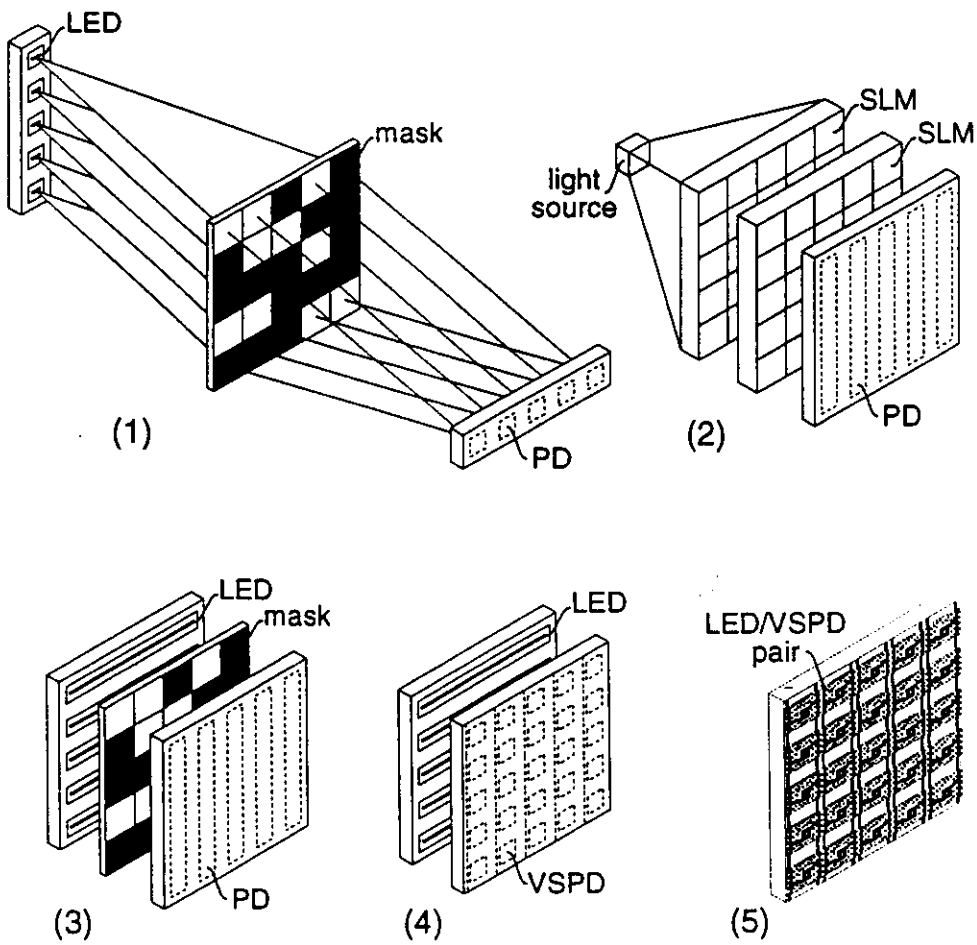
Velocity Sensors

- Achieving a wide dynamic range when measuring the velocity of moving image features is hard using conventional sensor technologies.
- An asynchroneous, pulse-based velocity detector estimates velocities of moving brightness gradients reliably over several orders of magnitude [Kram 97].

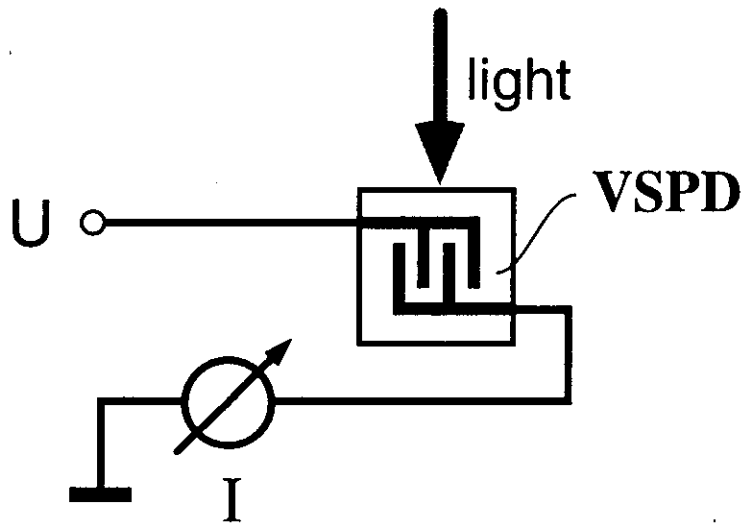


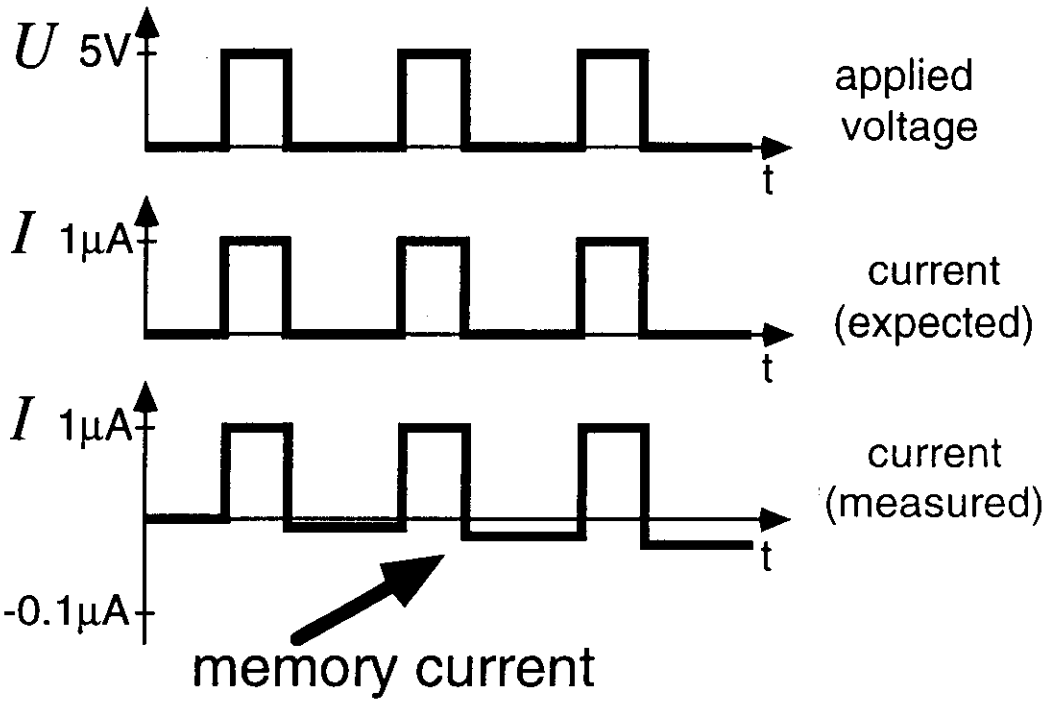
Optical Neurochip Timeline

1. Optical matrix-vector multiplier [Good 78, Farh 85].
2. Spatial light modulator based optical neurochip [Farh 87].
3. Hybrid optical neurochip (static) [Nitt 89, Ohta 89].
4. Hybrid optical neurochip (dynamic) [Ohta 91].
5. Monolithically integrated optical neurochip [Nitt 93].



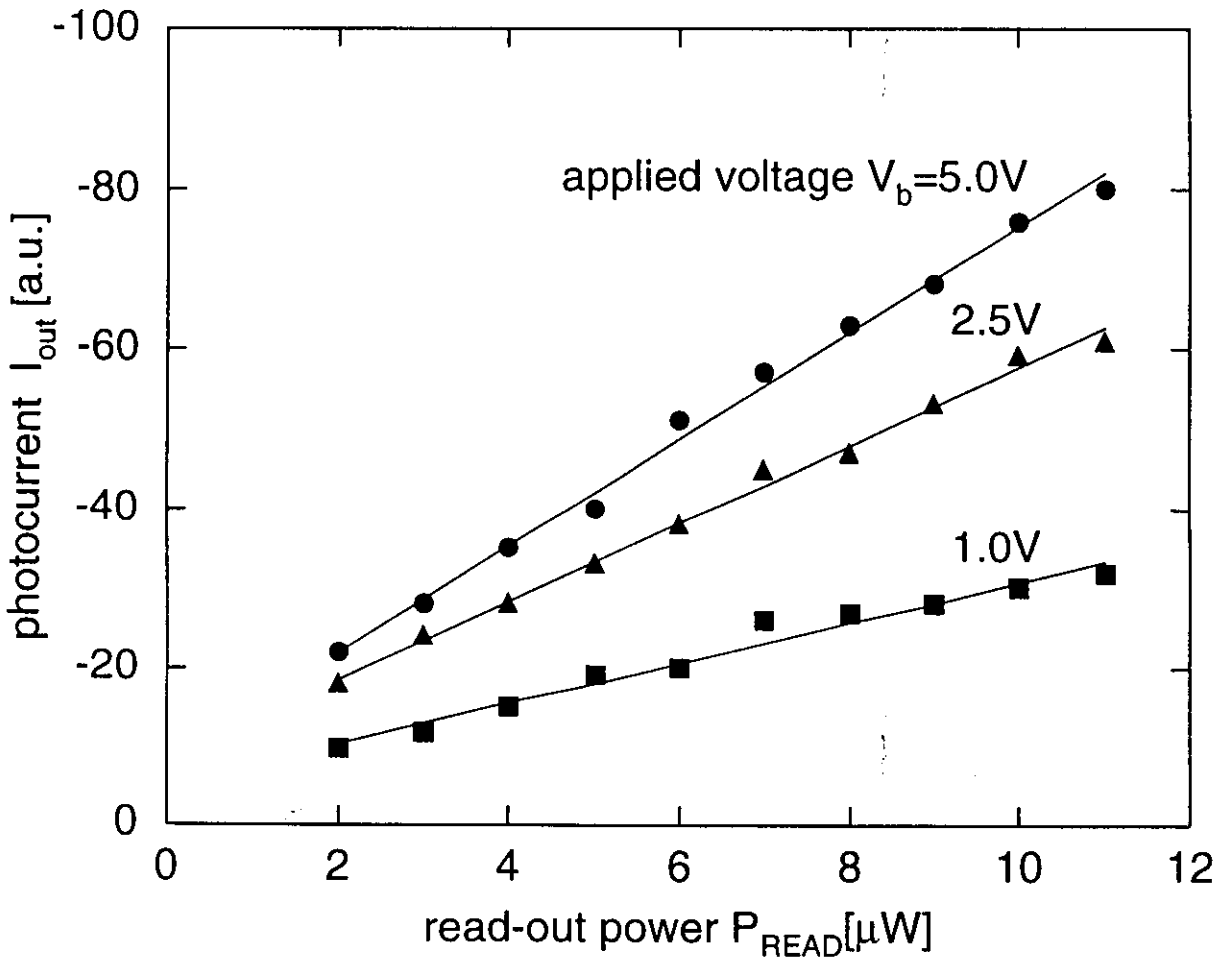
MSM-VSPD Analog Memory Function





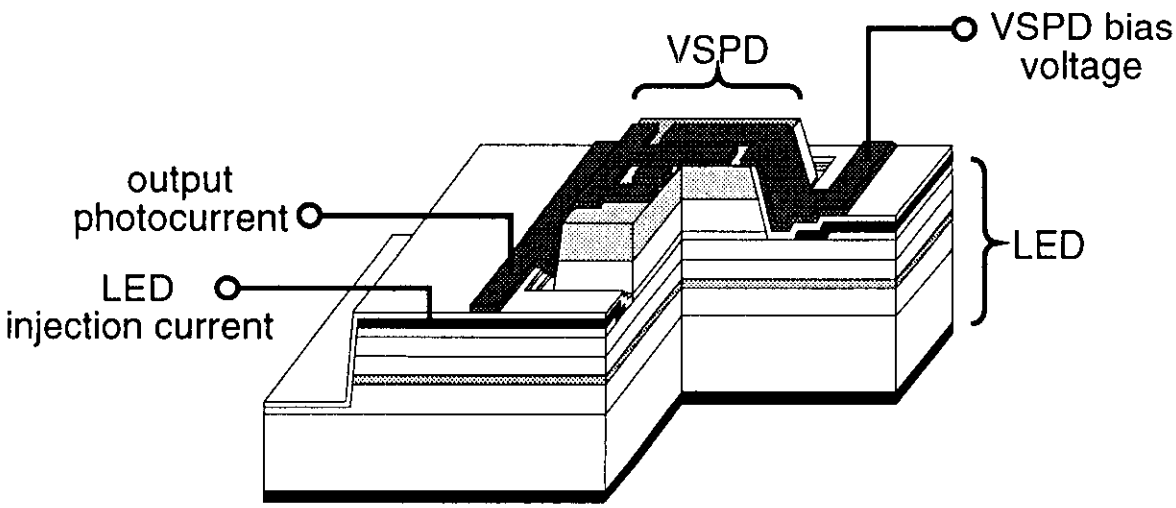
MSM-VSPD Analog Memory Function

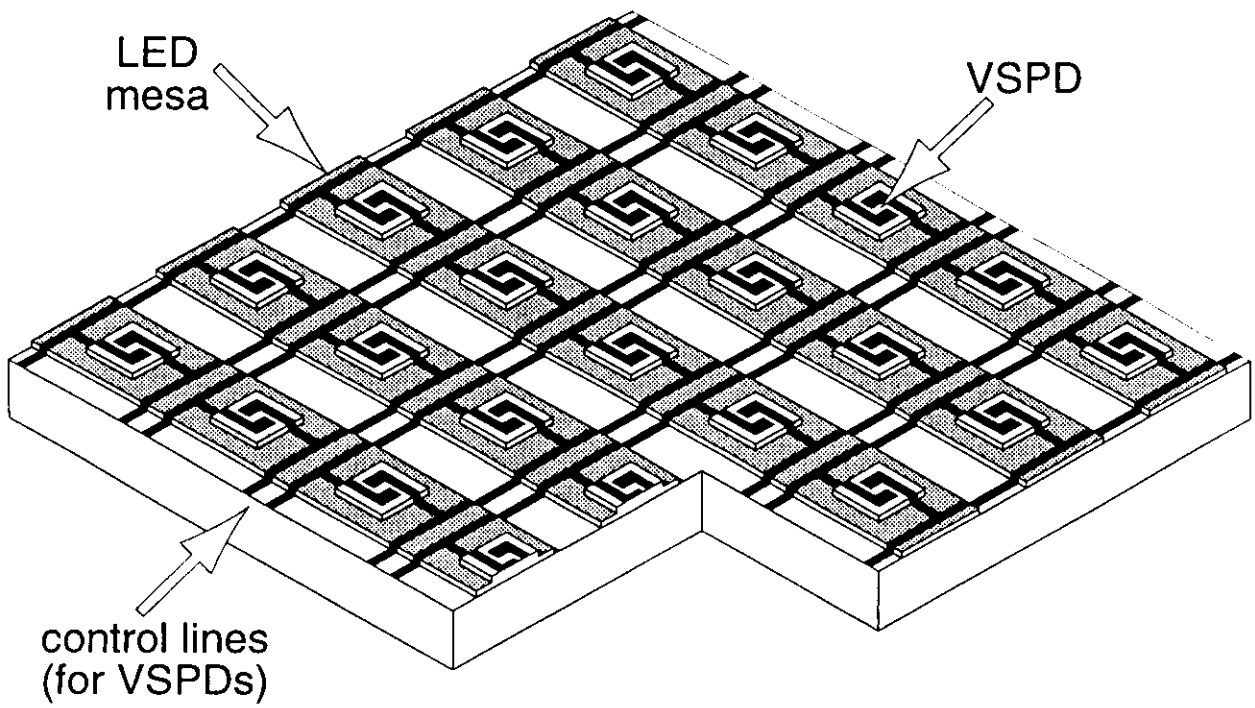
The photocurrent in the read phase rises in proportion to the incident optical power, in dependence on the voltage applied in the write phase [Nitt 93].



Optical Neurochip

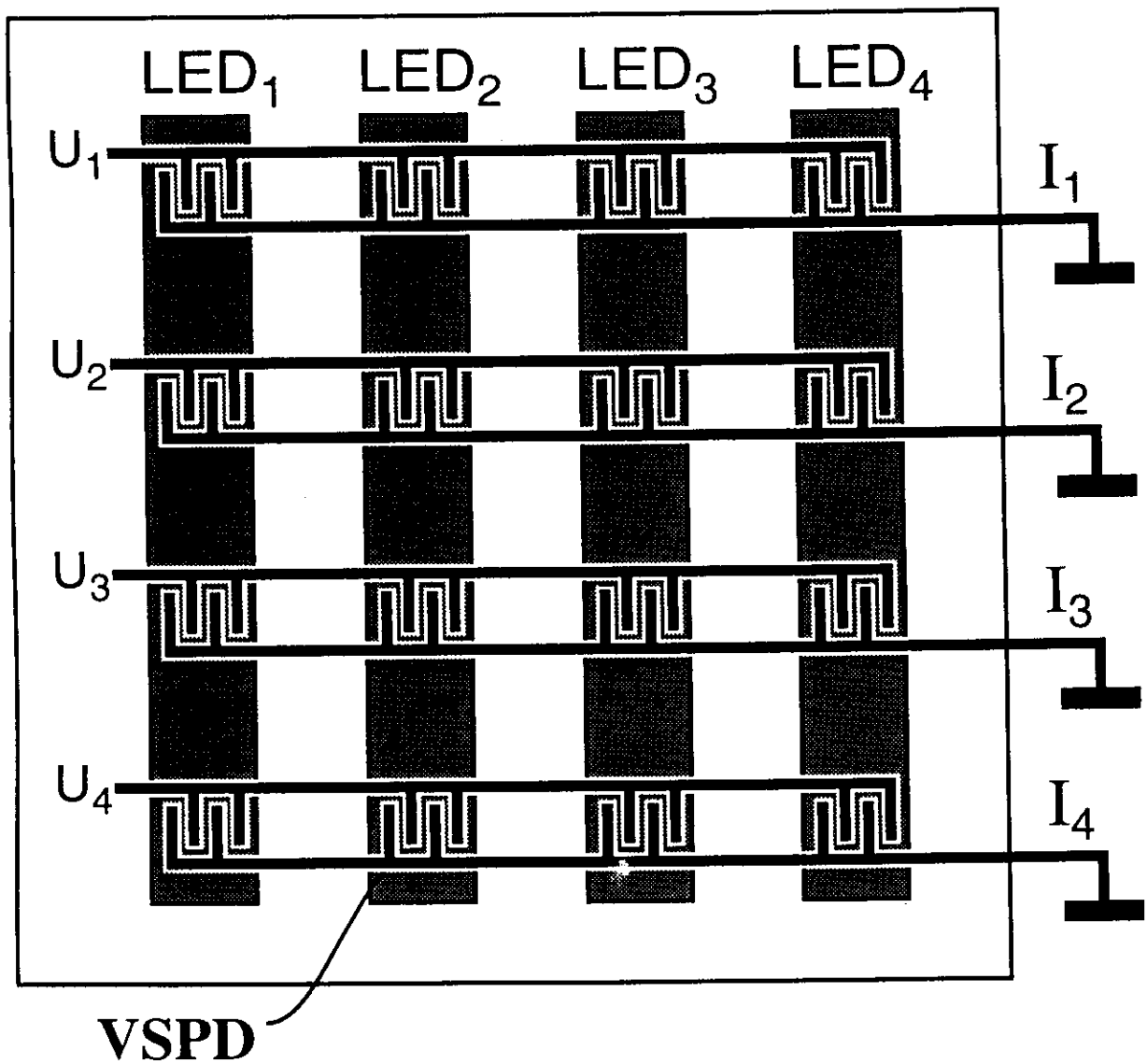
MSM-VSPDs are monolithically integrated on top of LEDs [Nitt 93].





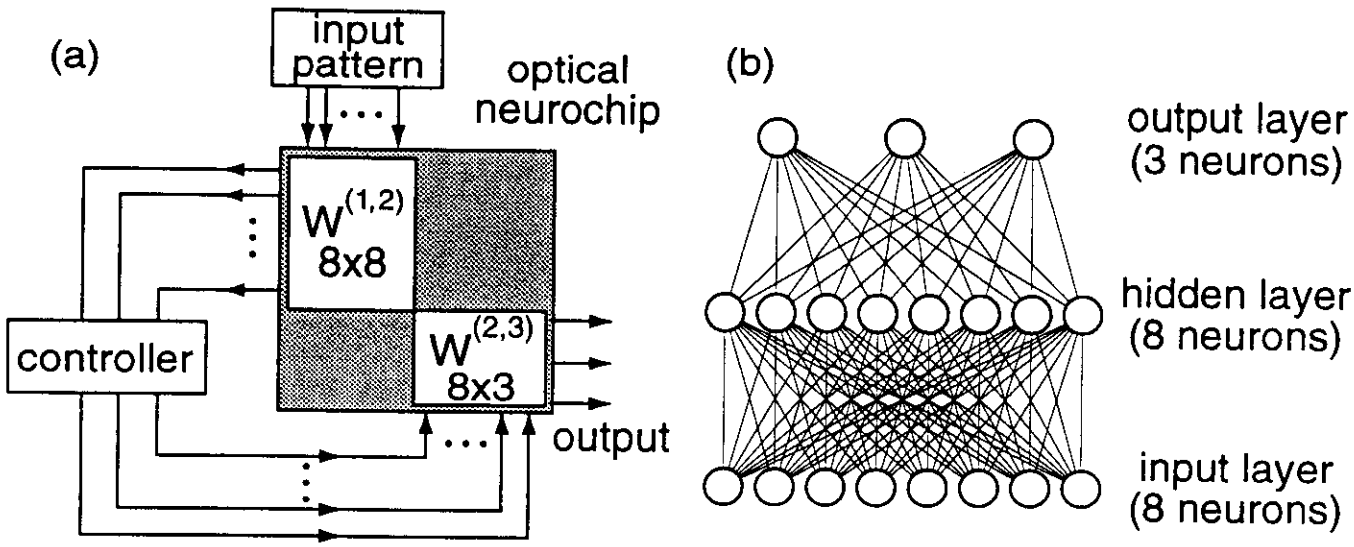
Optical Neurochip

Schematic diagram of the optical neurochip. Rows of VSPDs are interconnected.



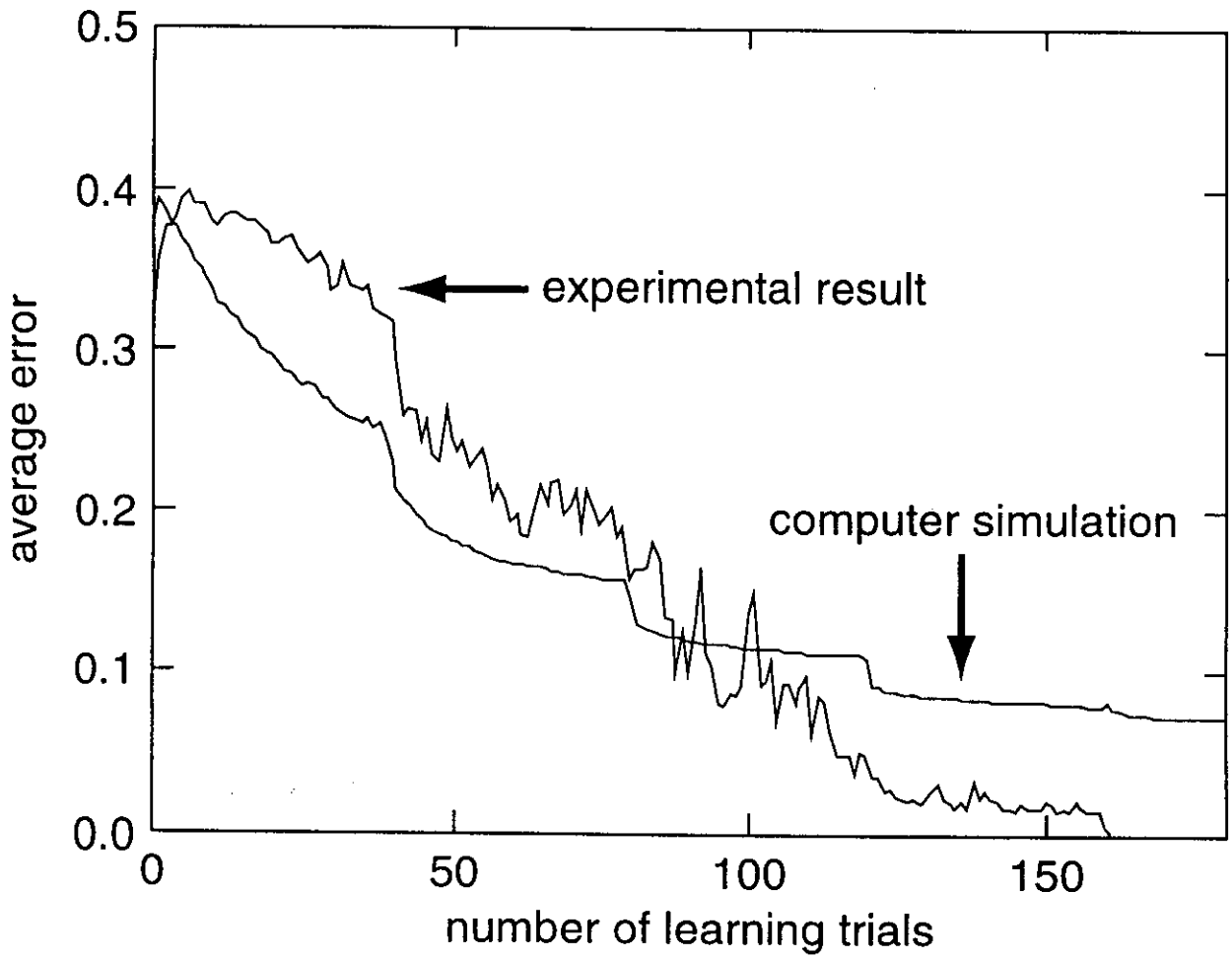
Optical Neurochip: Learning

A neural network with two processing layers: implementation on chip (a) and structure of the neural network (b).



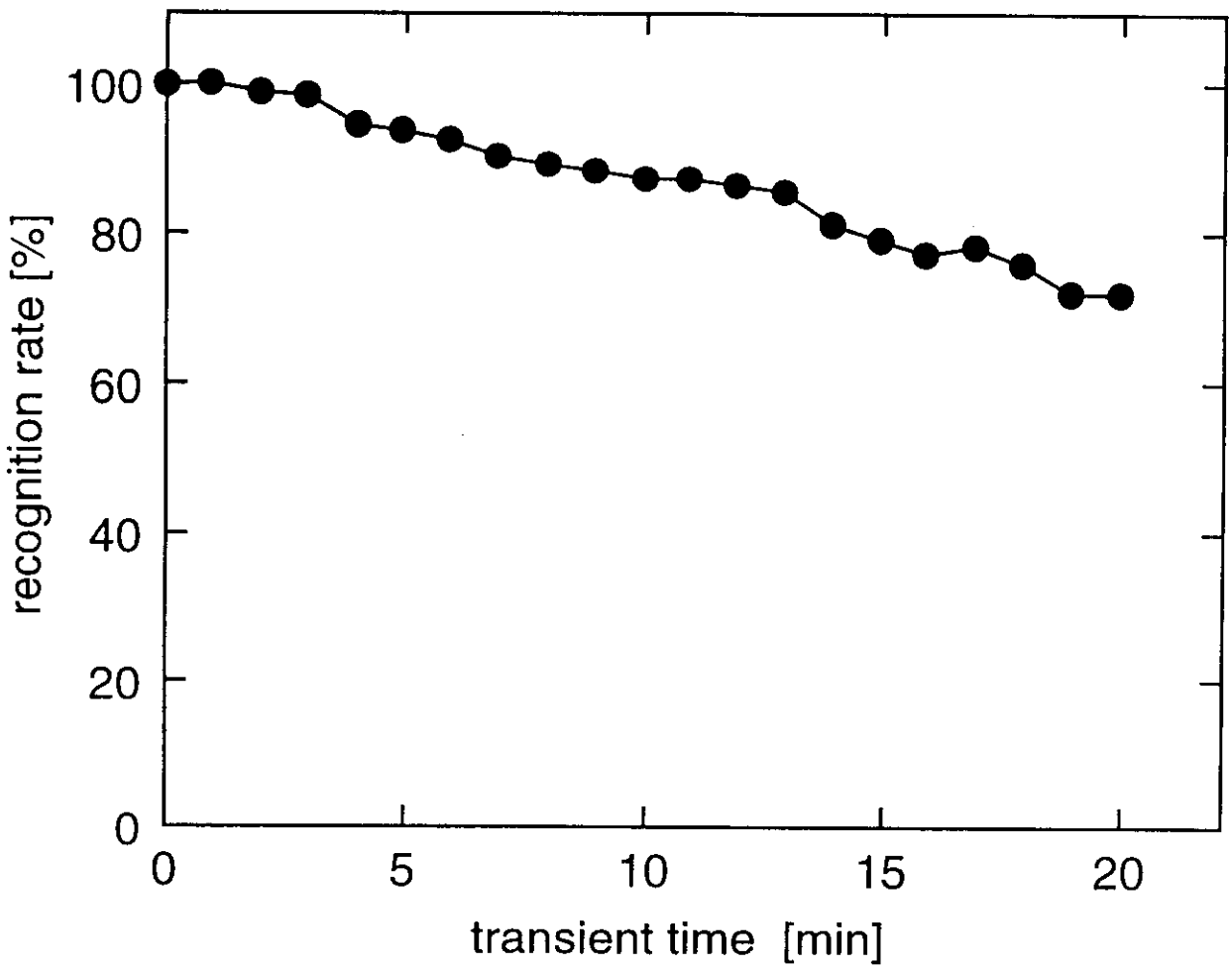
Optical Neurochip: Learning

Learning process in optical Neurochip. Compared to a computer simulation, the average error decreases faster and reaches lower levels (probably because of beneficial effects of noise on learning).



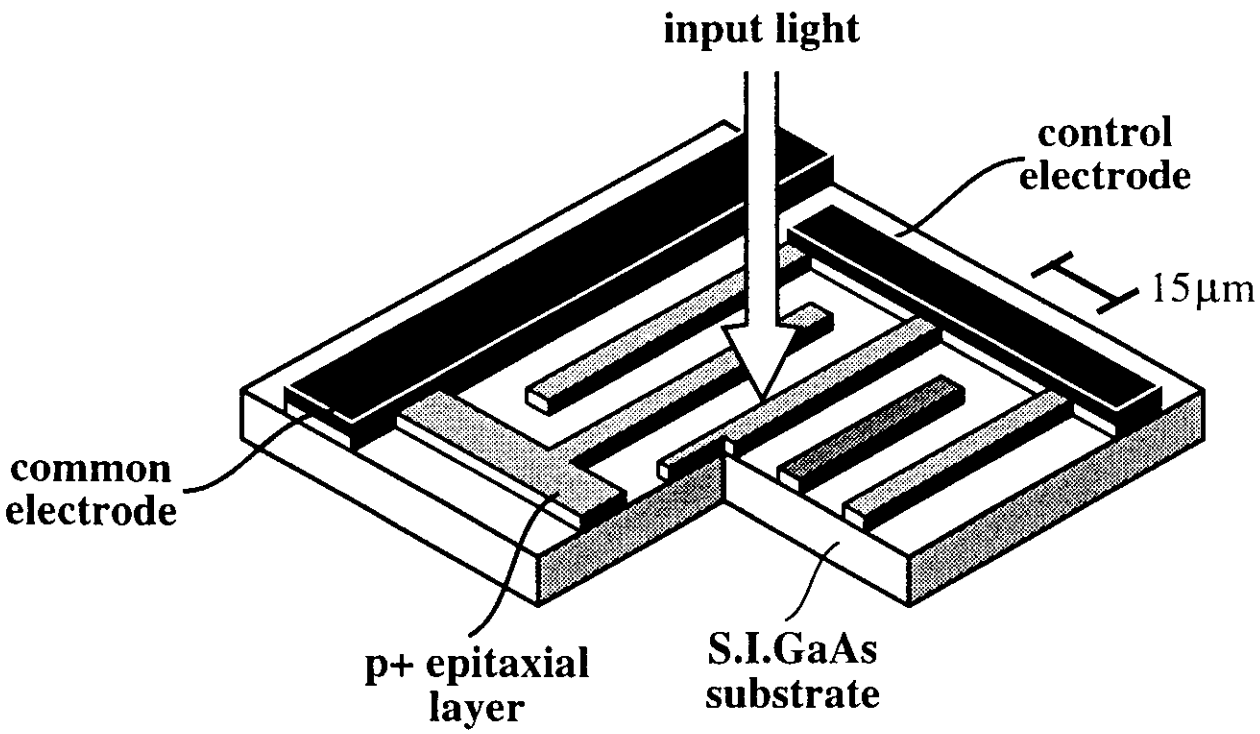
Optical Neurochip: Learning

After completion of the training process, the recognition rate decays slowly.



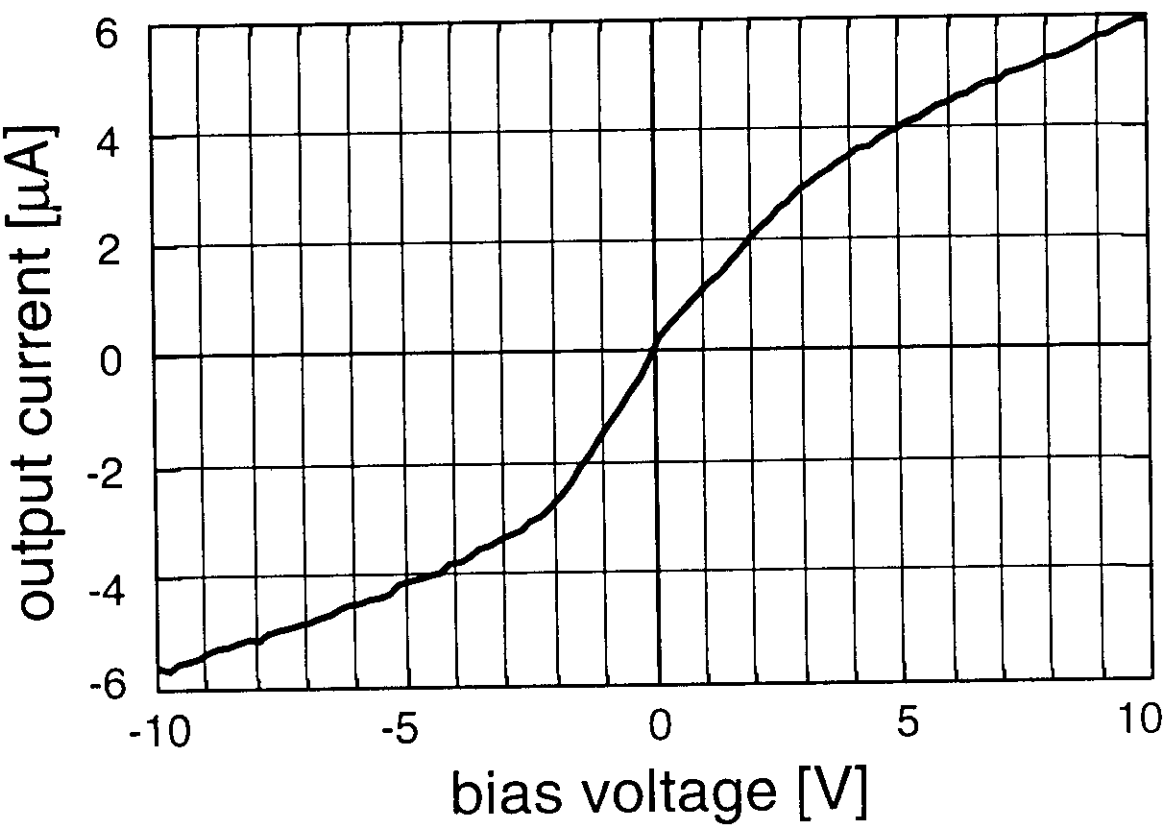
Detector Types: *pn-np* VSPD

A VSPD-type that eliminates memory currents.



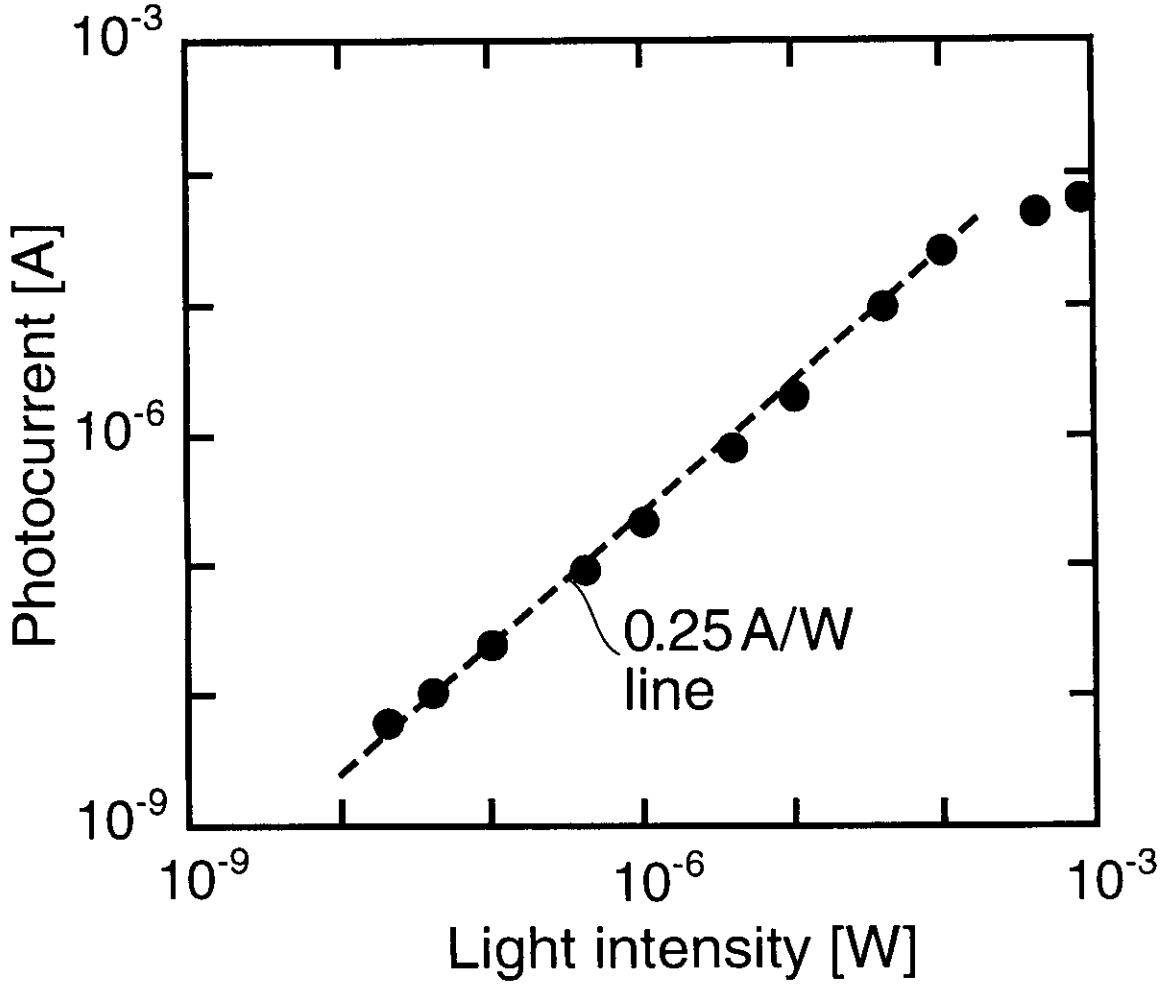
pn-np VSPD Response Curve

The maximum slope of the response curve is small; it is easy to set the sensitivity accurately [Funa 94].



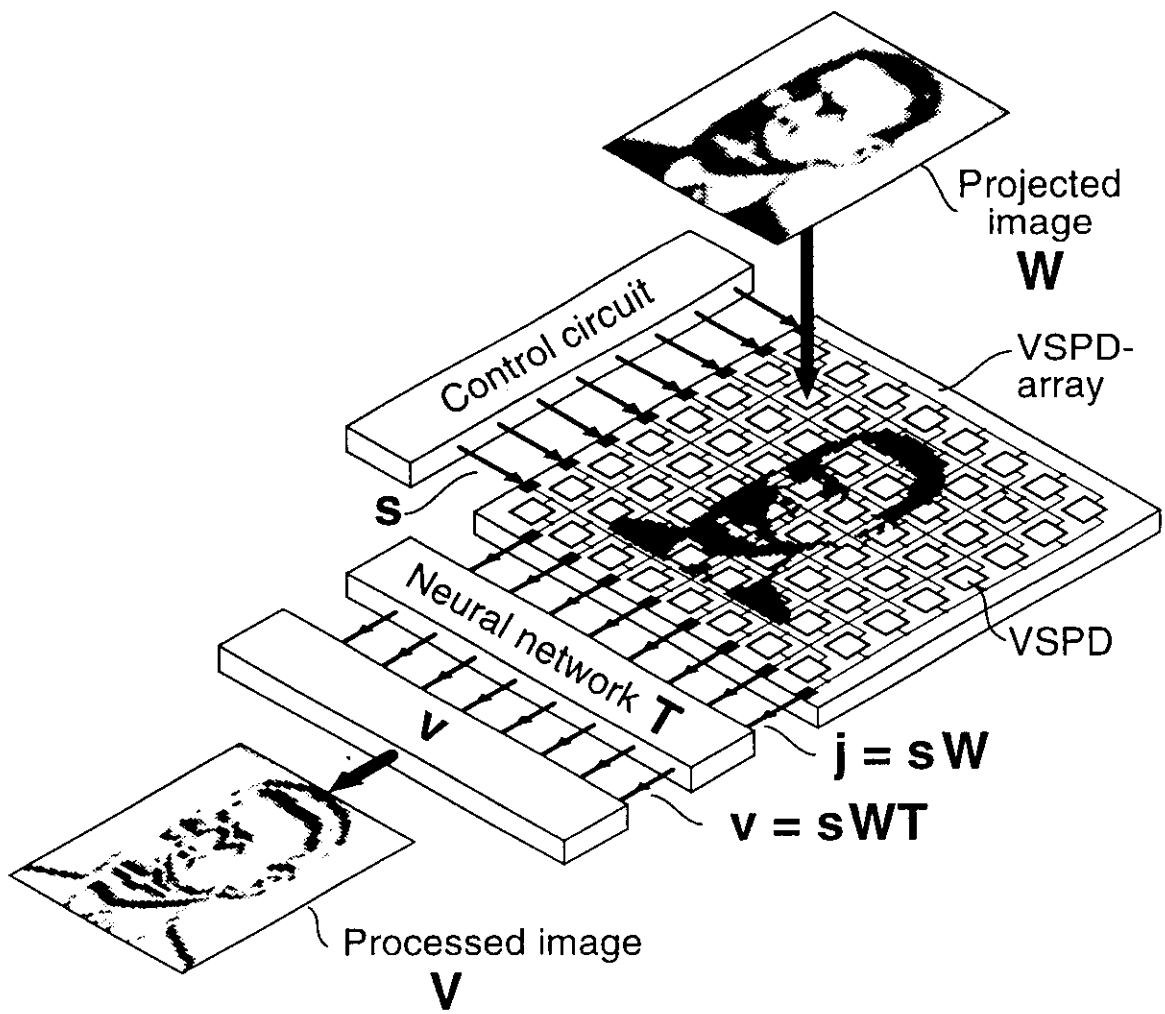
pn-np VSPD Photoresponse

pn-np VSPDs Photoresponse shows good linearity.



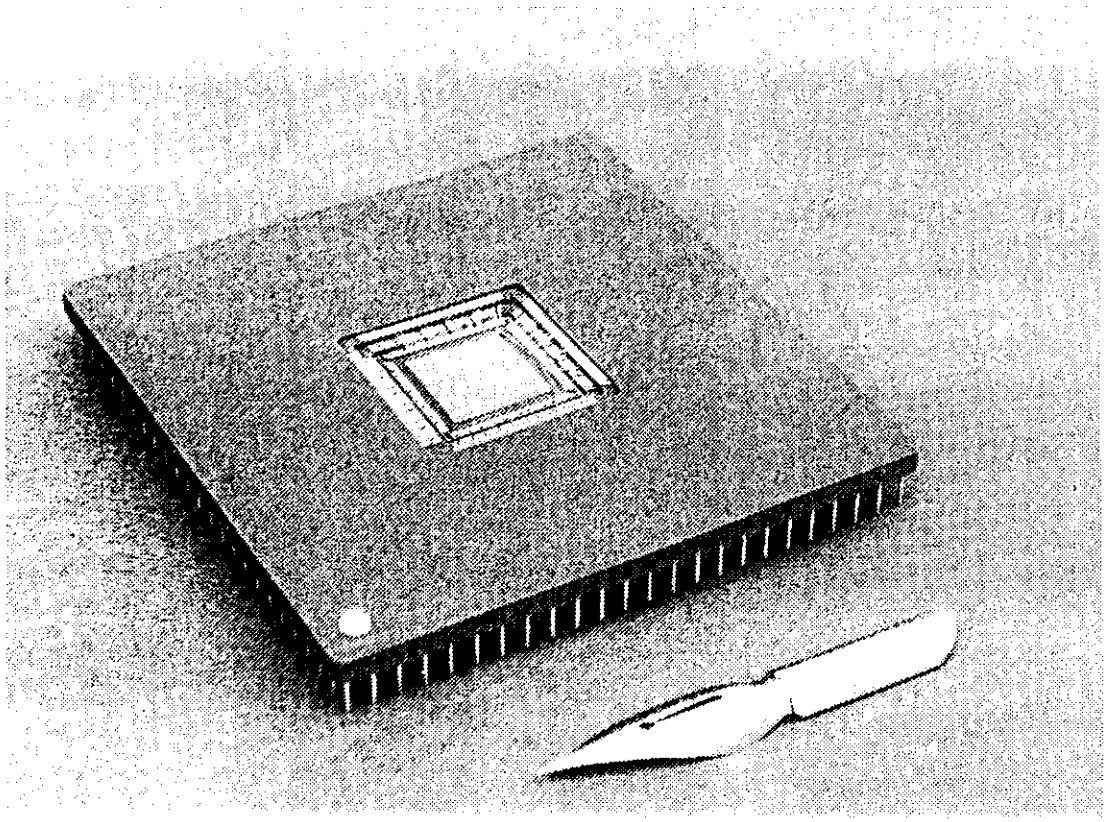
Artificial Retina Chip

In Mitsubishi Electric's Artifical Retina (AR), an array of VSPD's in conjunction with an optional neural network processes the projected image. system (c. f. [Lang 94, Kyum 94, Lang 95, Lang 96a, Lang 96b]).

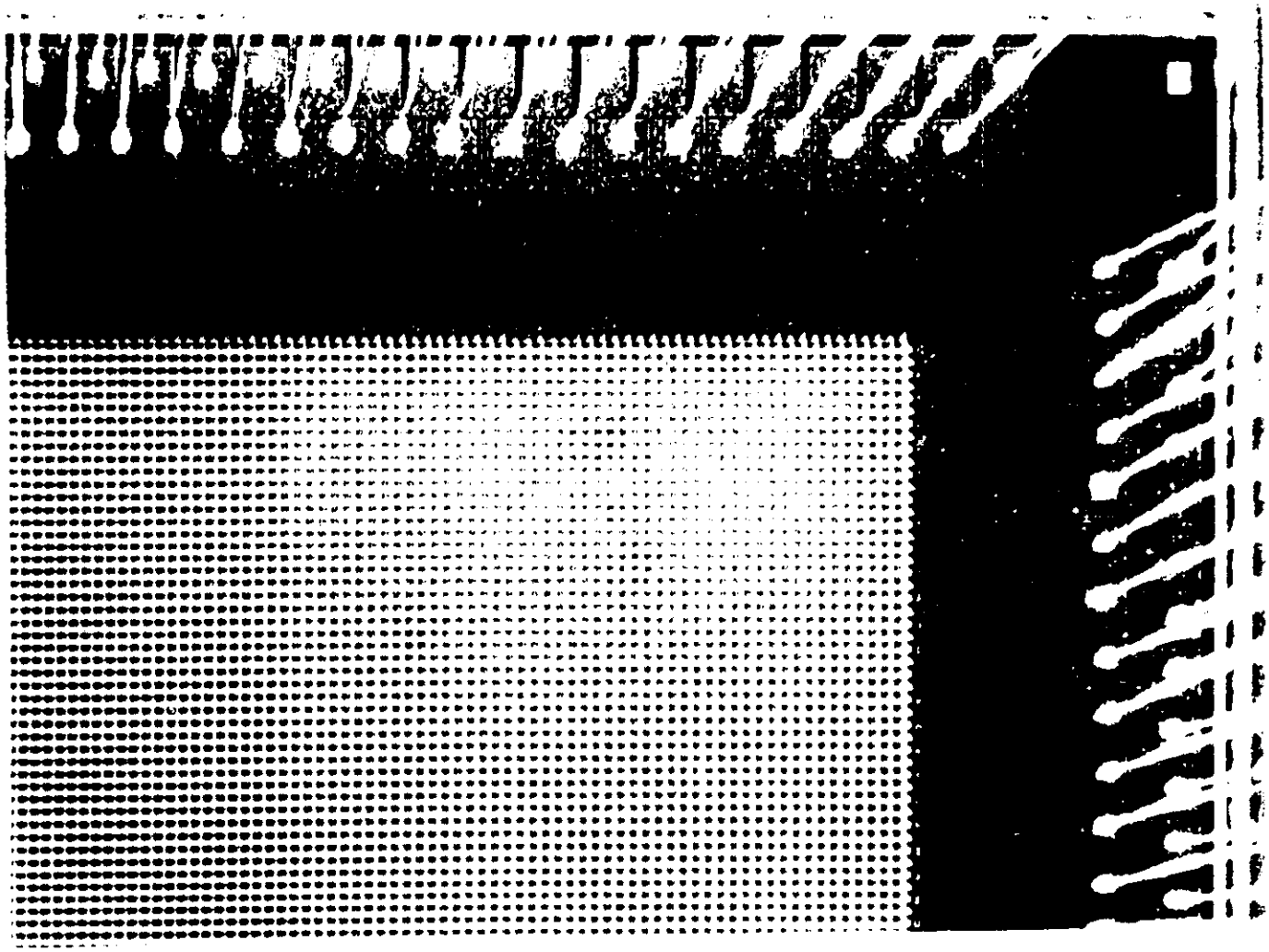


AR: 64×64 MSM-type VSPD Array

GaAs-based ARs need to be mounted in large PGA packages with up to 401 pins.

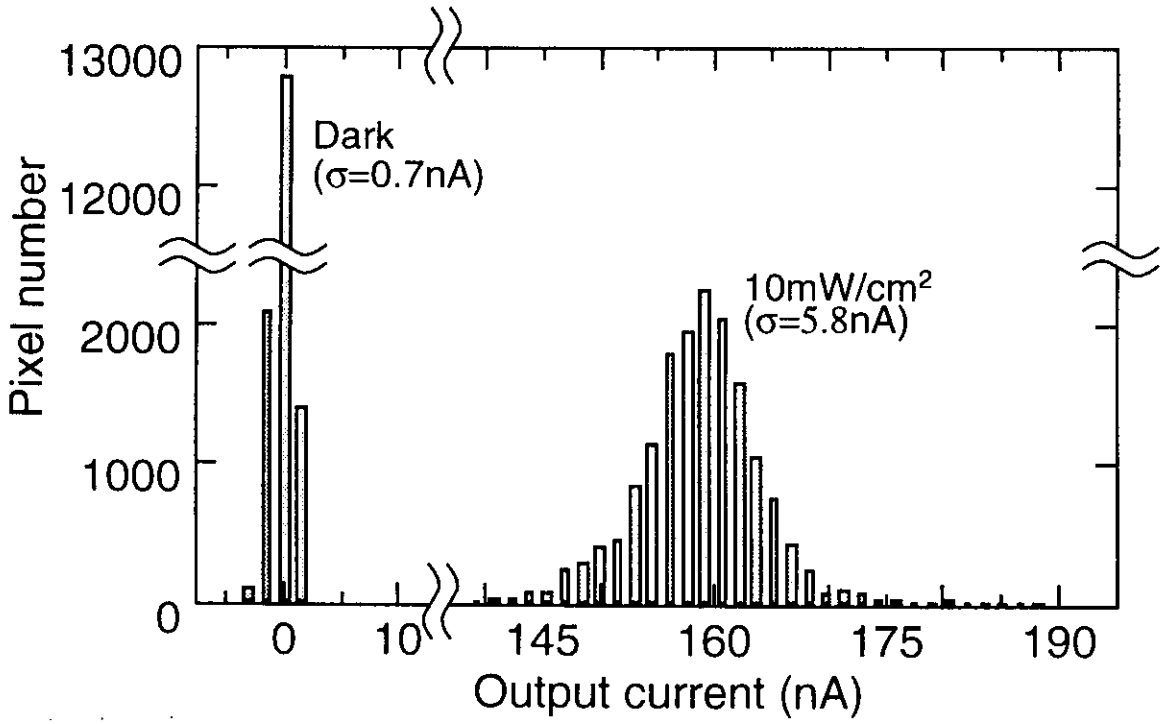


AR: 128×128 *pn-np*-type VSPD Array

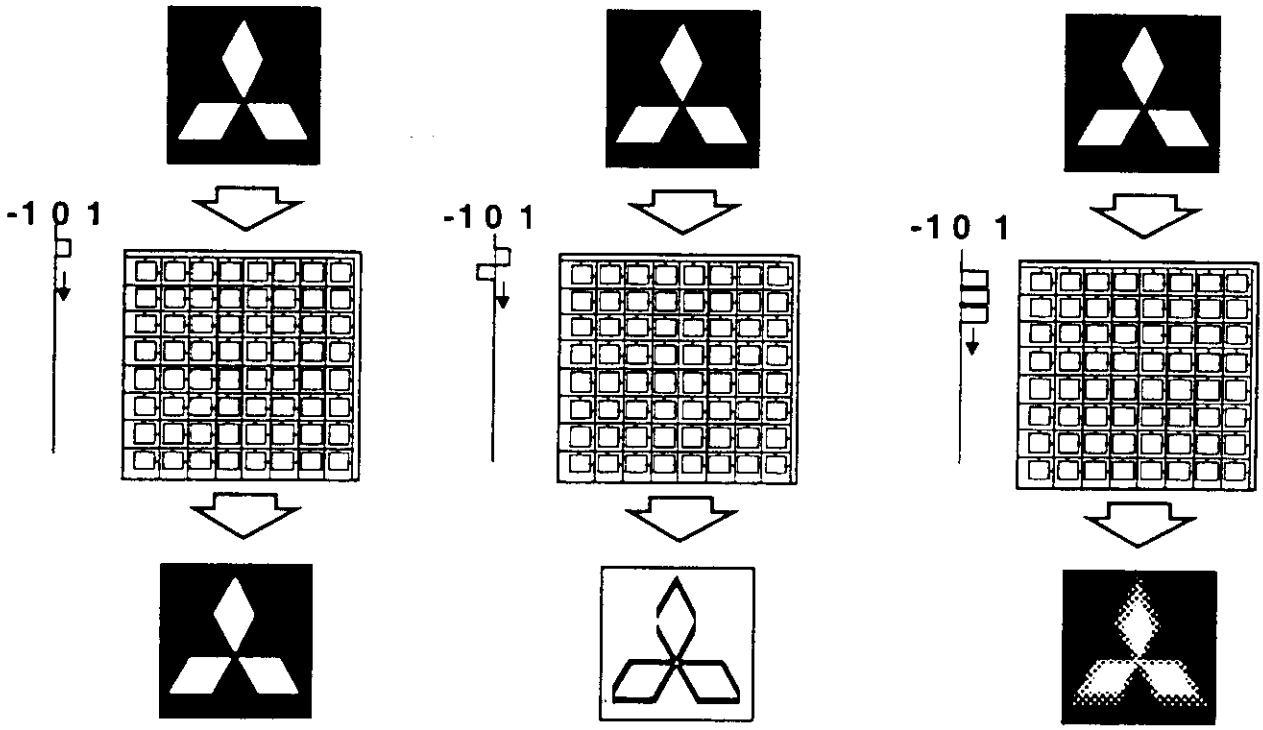


AR: Array Uniformity

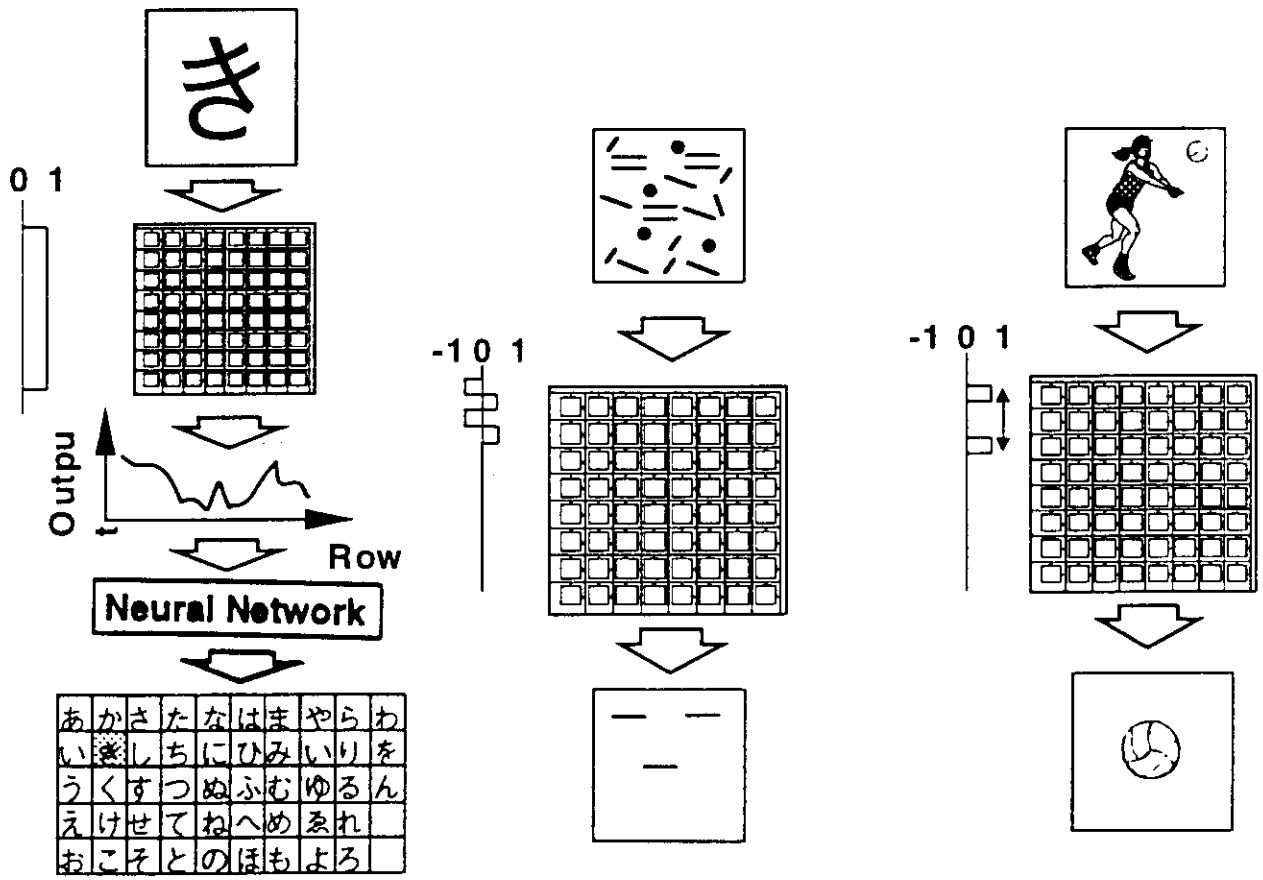
Uniformity of a *pn-np*-type VSPD Array with 128×128 pixels. Fix pattern noise of a few percent is a common problem of many detector arrays.



AR: Some Processing Functions



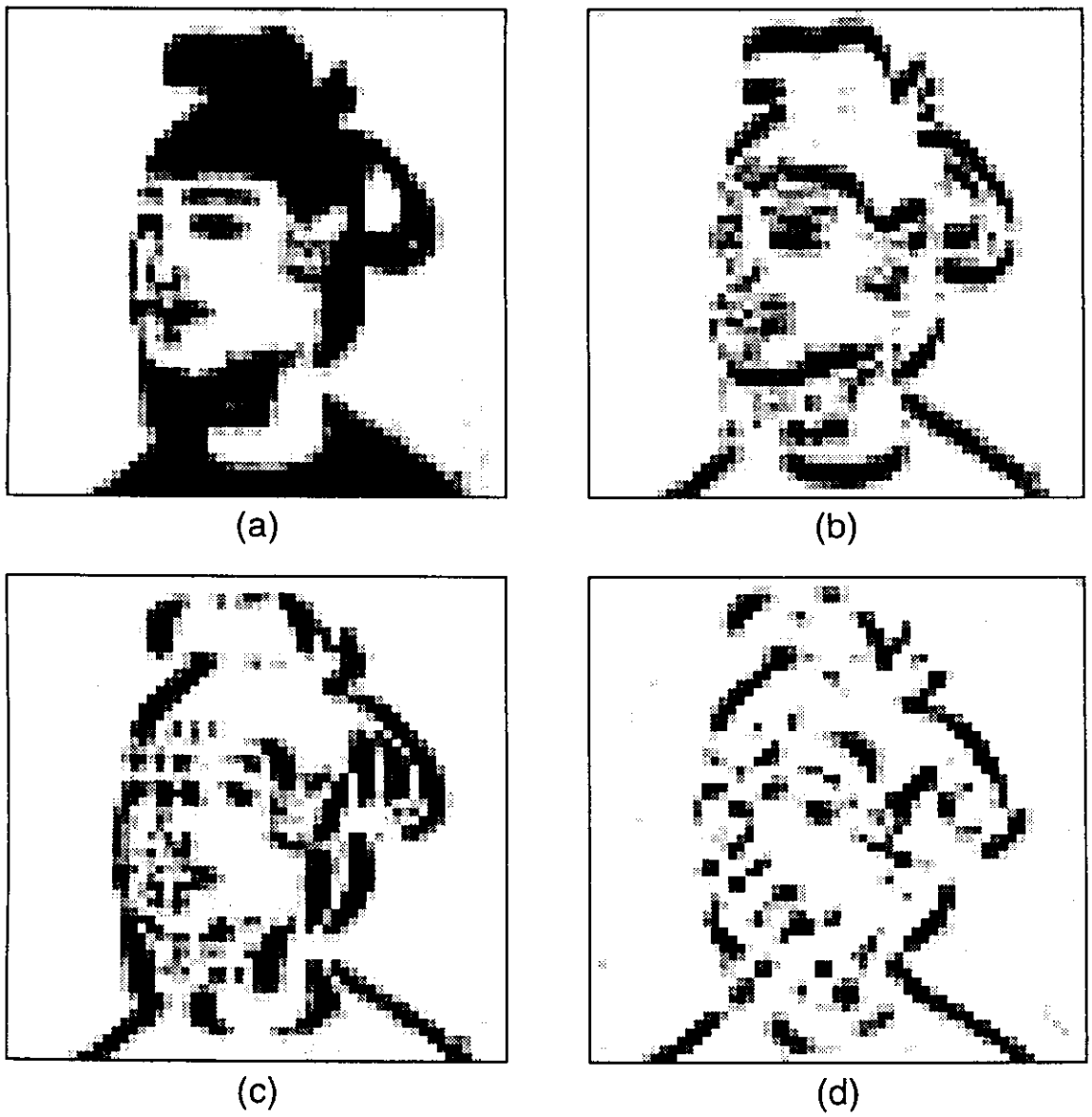
(a) Image Acquisition (b) Edge Extraction (c) Variable Resolution



(d) 2D→1D Projection (e) Pattern Matching (f) Random Access

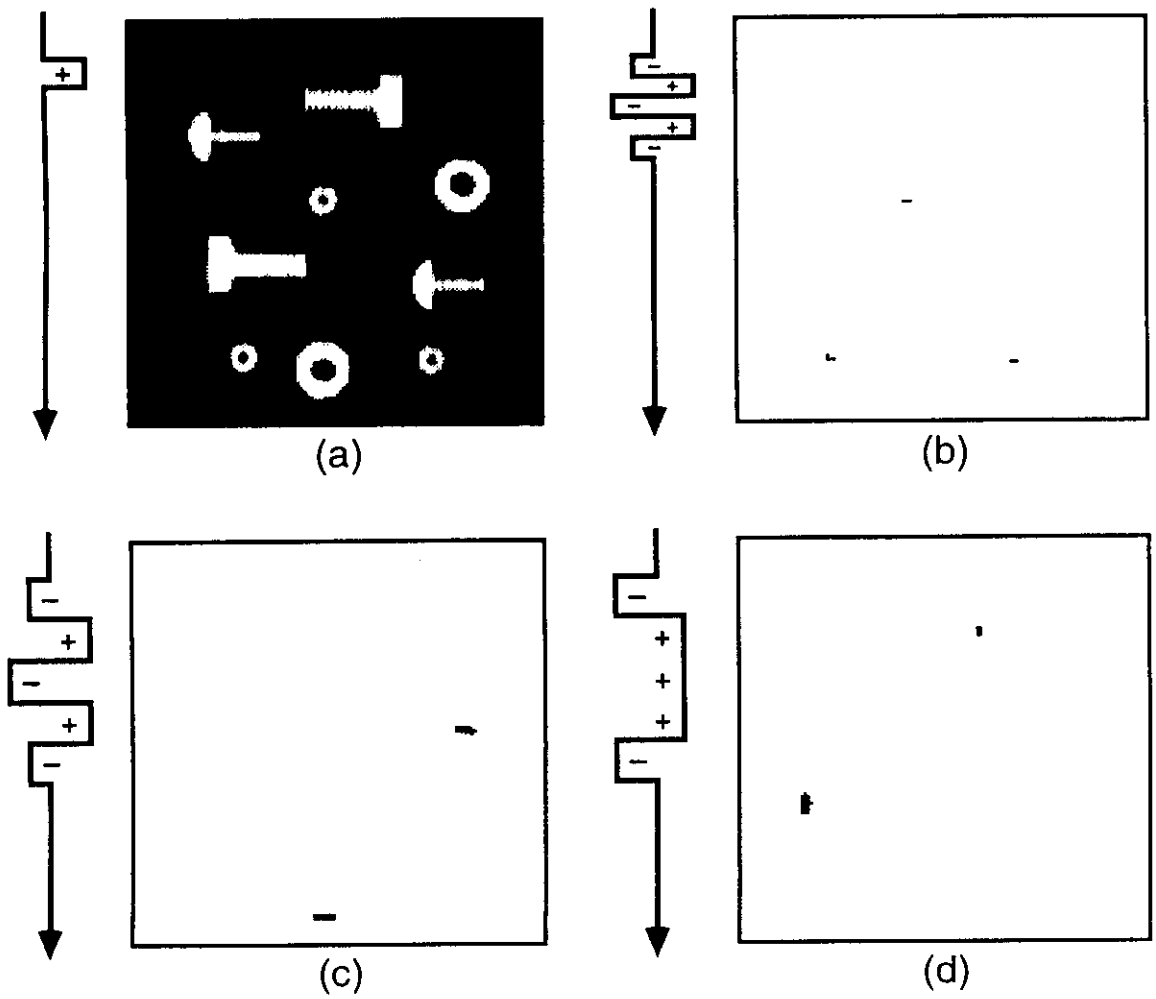
AR: Edge Enhancement

(a) Direct sensing; (b) horizontal, (c) vertical, and (d) diagonal edge enhancement; (c) and (d) wih postprocessing.



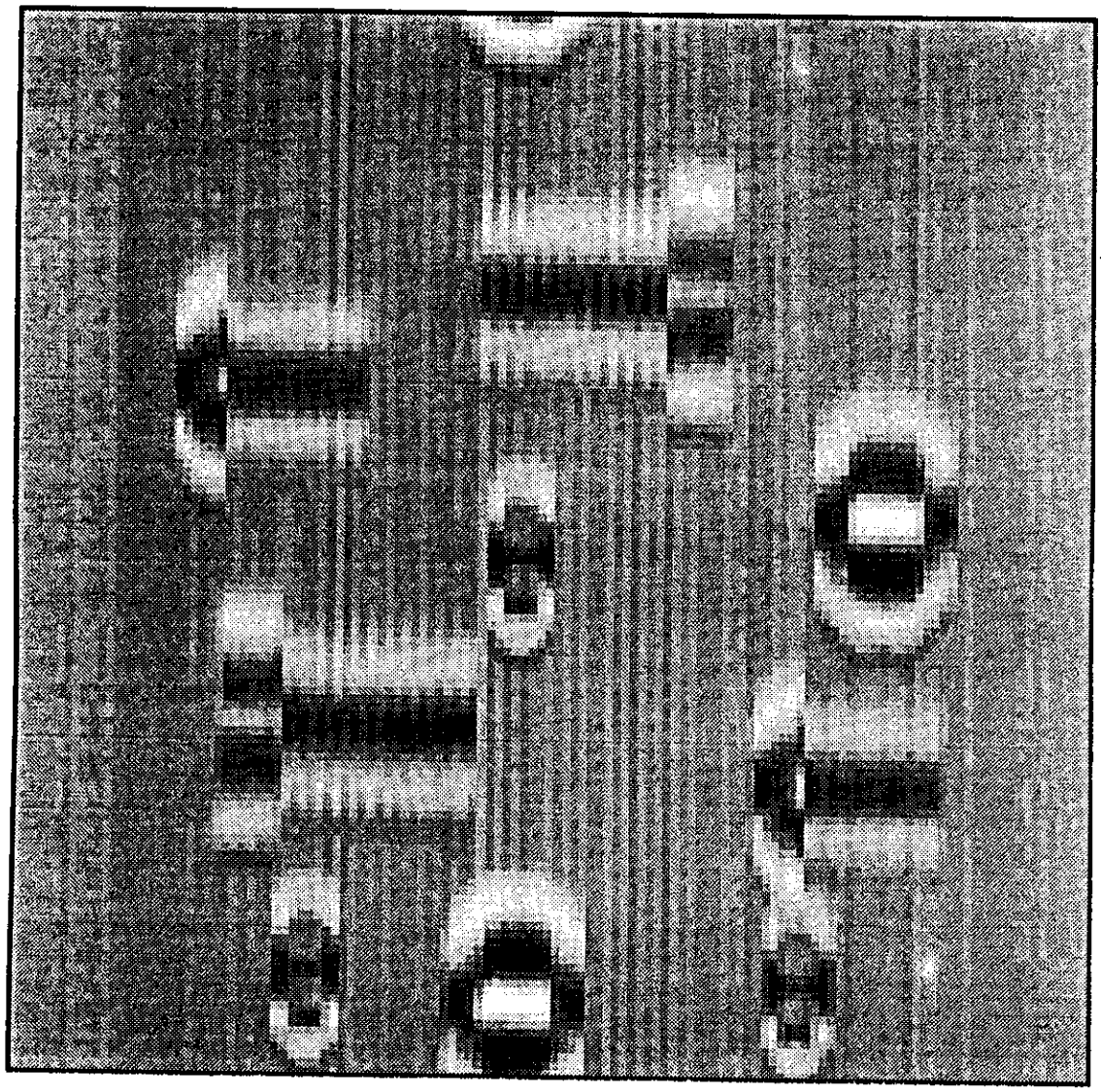
AR: Feature Extraction

(a) Direct sensing; (b-d) three different feature extraction modes.



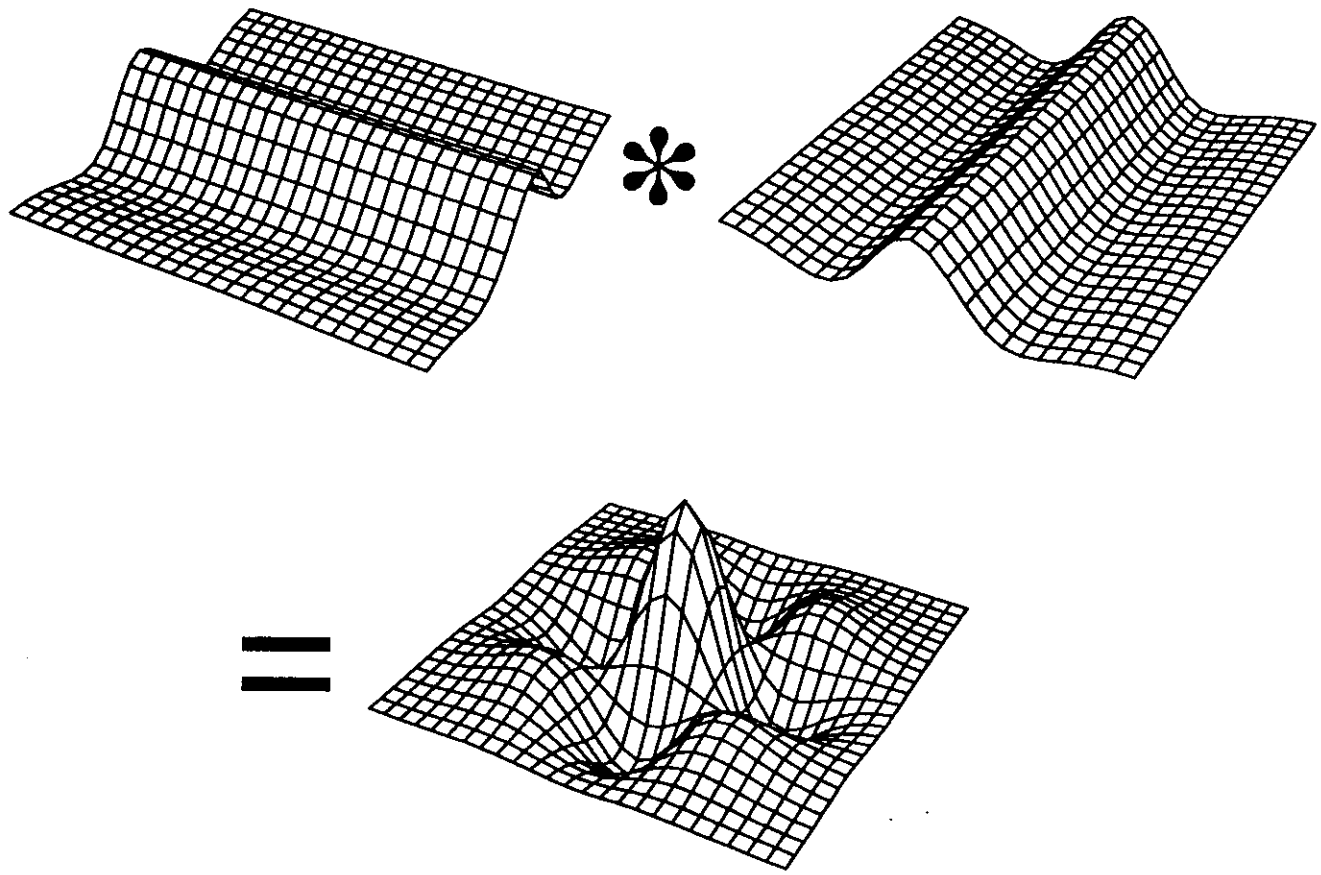
AR: Feature Extraction

Example showing full range of pixel values.



AR: Limitations of Filtering

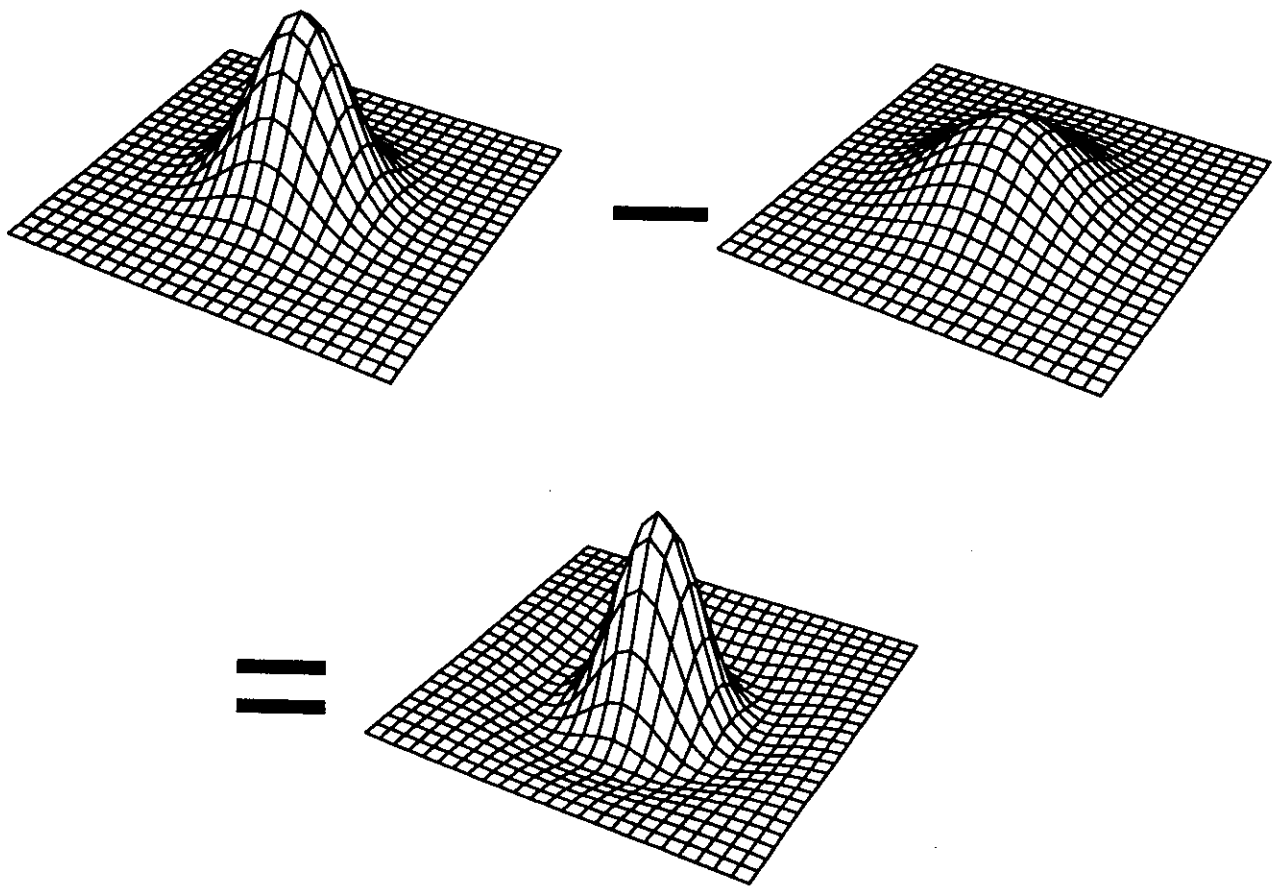
The Artificial retina processes images by pre- and postmultiplying them with matrices. This limits shift-invariant filtering to convolution with separable kernels; example:



enhancement of diagonal edges

AR: DOG Filtering

Non-separable convolution kernels require more complex postprocessing (for example, in a multilayer neural network). Example: difference-of-Gaussians (DOG) filter for general edge enhancement.

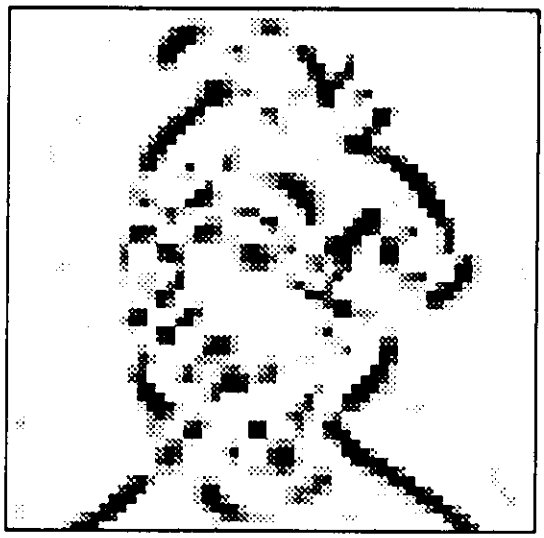


enhancement of all edges

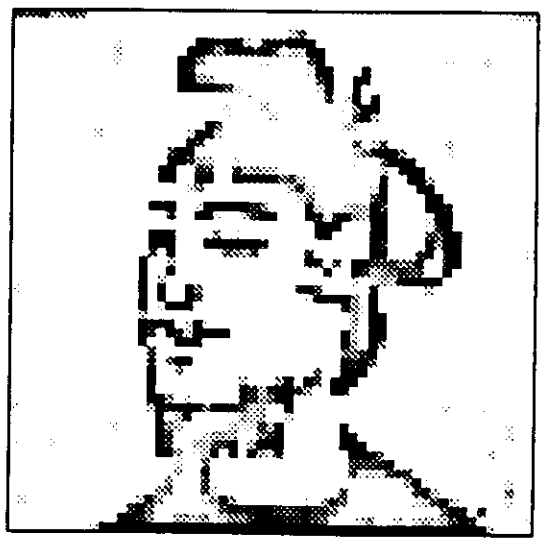
AR: DOG Filtering

Example of filtering in an AR: (a) image sensed in TV-like operation mode, and same image after convolution with (b) separable convolution kernel for enhancement of diagonal edges and (c) non-separable difference of Gaussians filter for general edge enhancement.

(a)



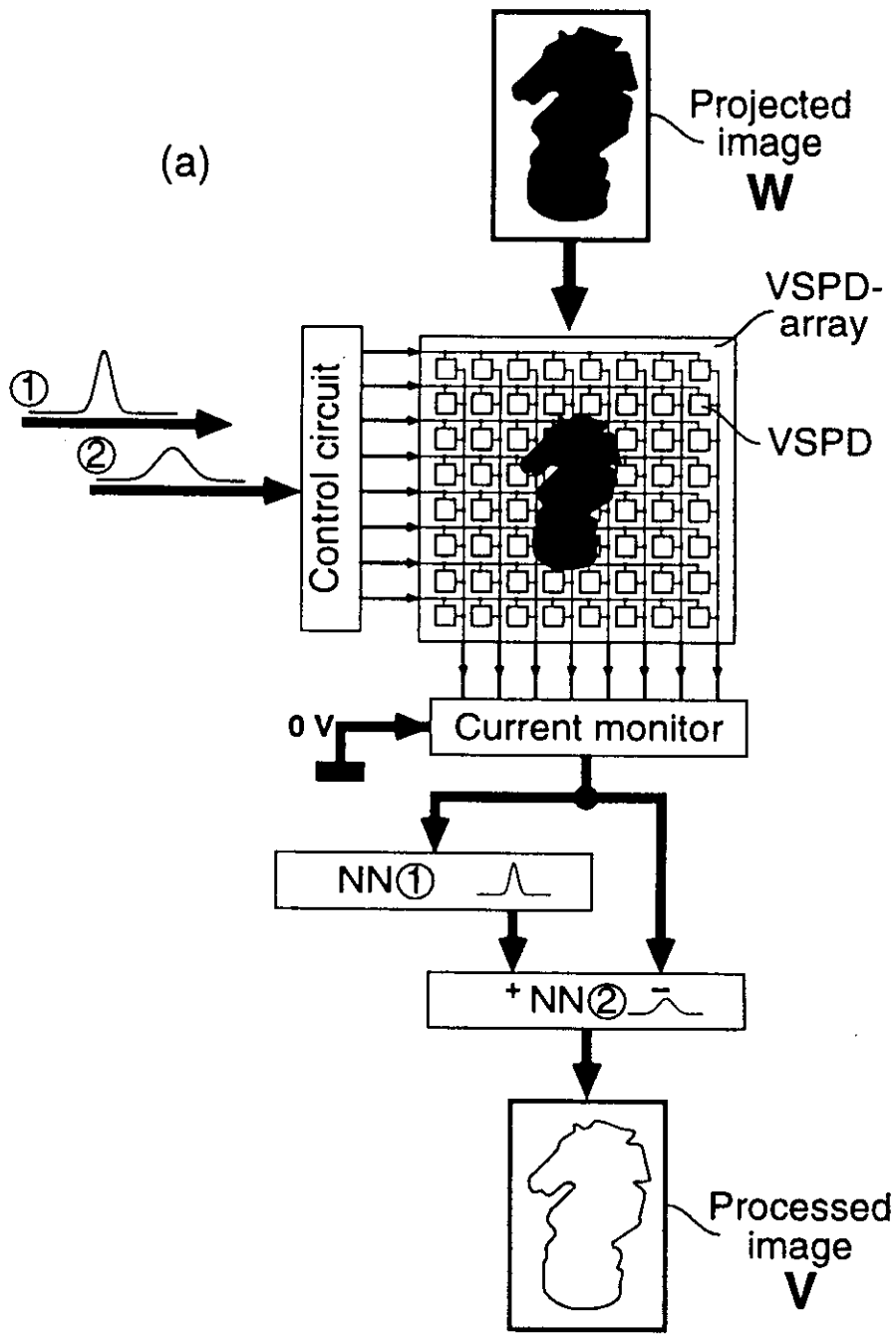
(b)



(c)

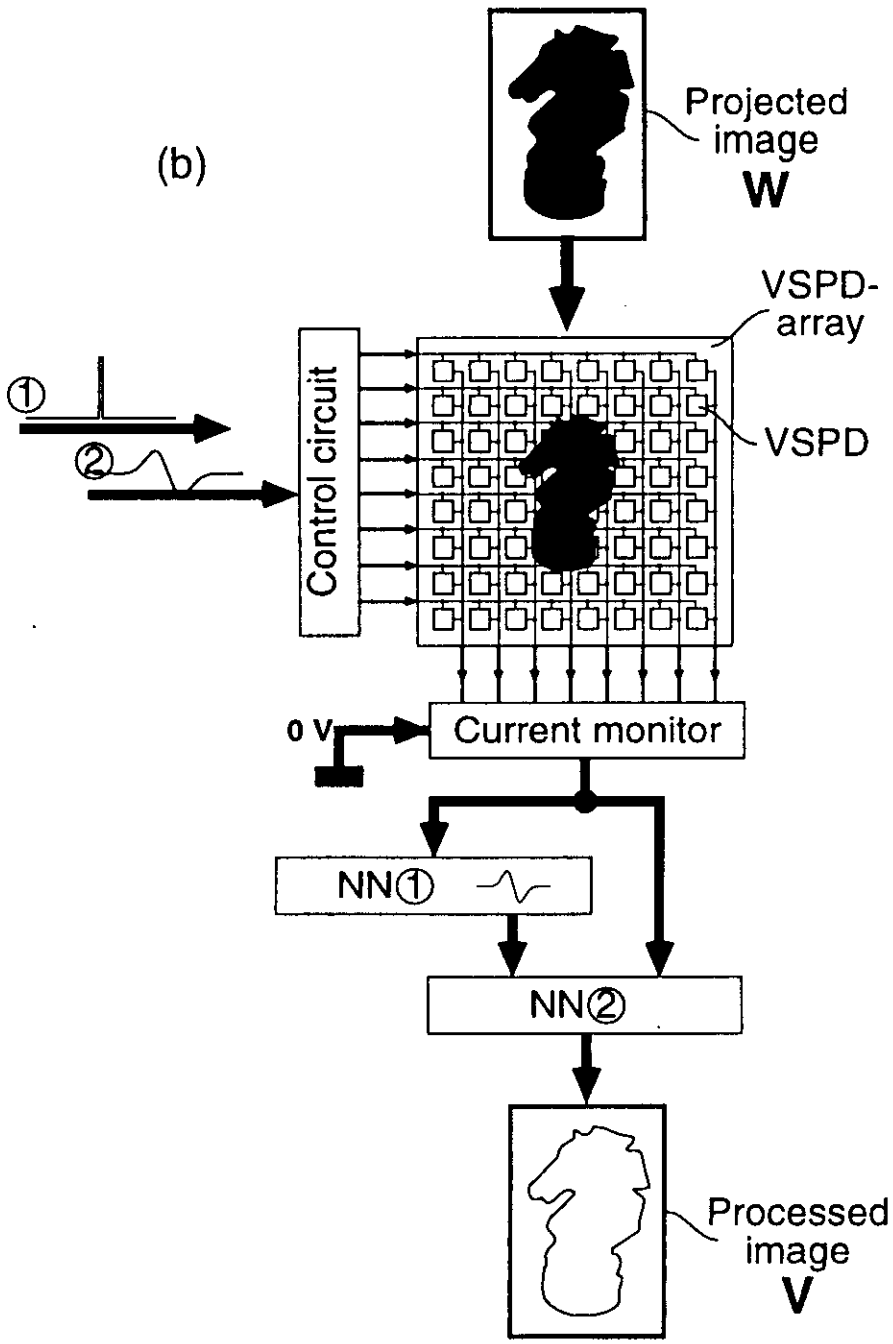
AR: DOG Filtering

Example for implementation of general edge enhancement: difference-of-Gaussians filter.



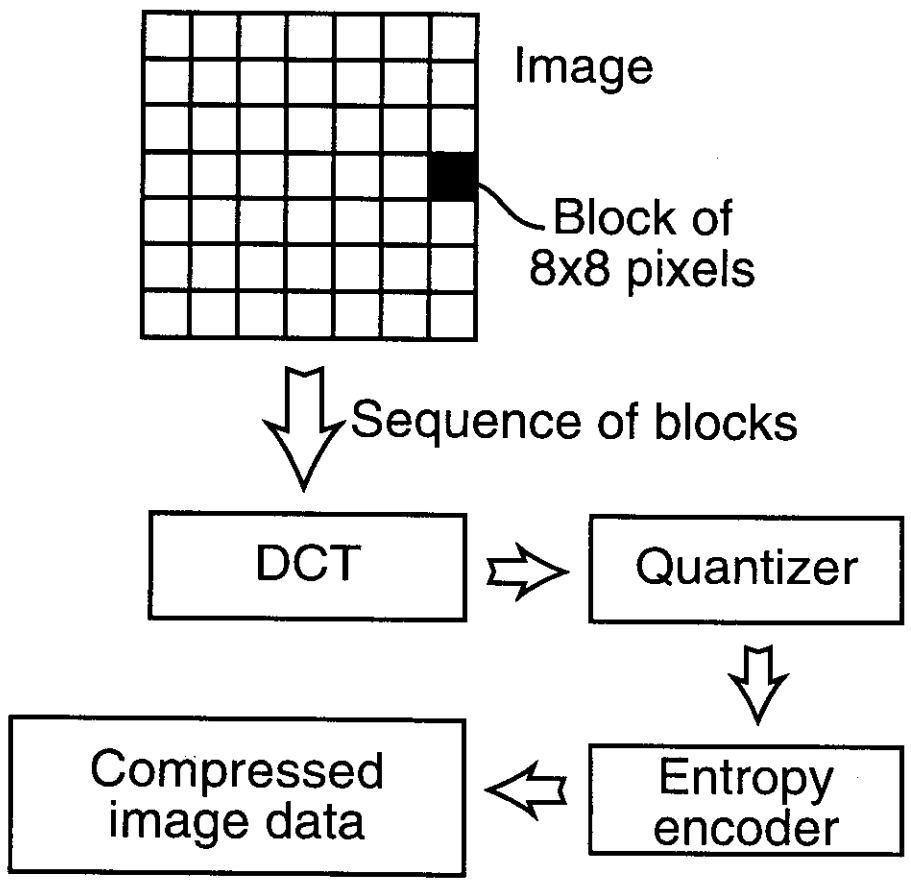
AR: DOG Filtering

Example for implementation of general edge enhancement: gradient-based filter.



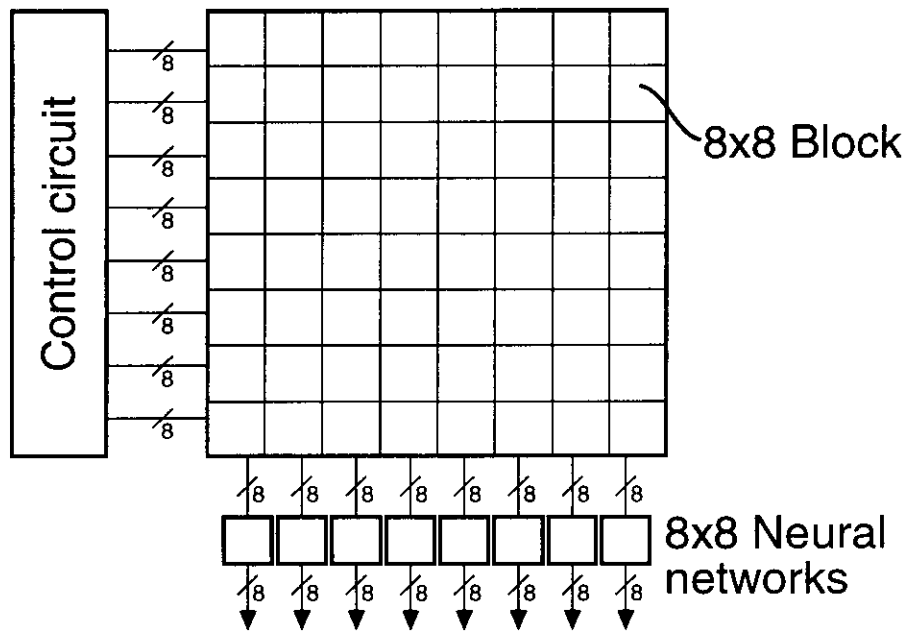
AR: Image Compression

Principle of operation of JPEG image compression (baseline algorithm). The discrete cosine transform of image blocks with 8×8 pixels represents the computationally most expensive step.



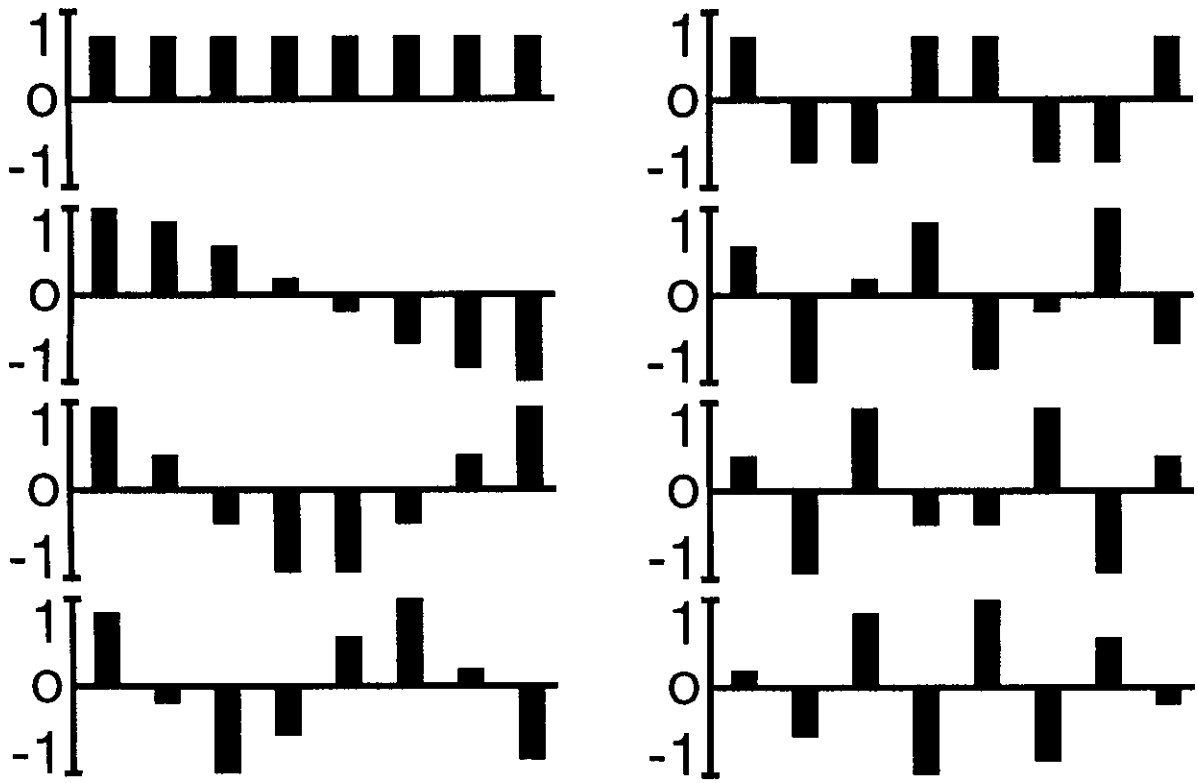
AR: Image Compression

Implementation of discrete cosine transform of image blocks using an artificial retina device. On-chip processing performs discrete cosine transforms in the vertical direction. Small neural networks with 8×8 synapses perform the horizontal transformation.



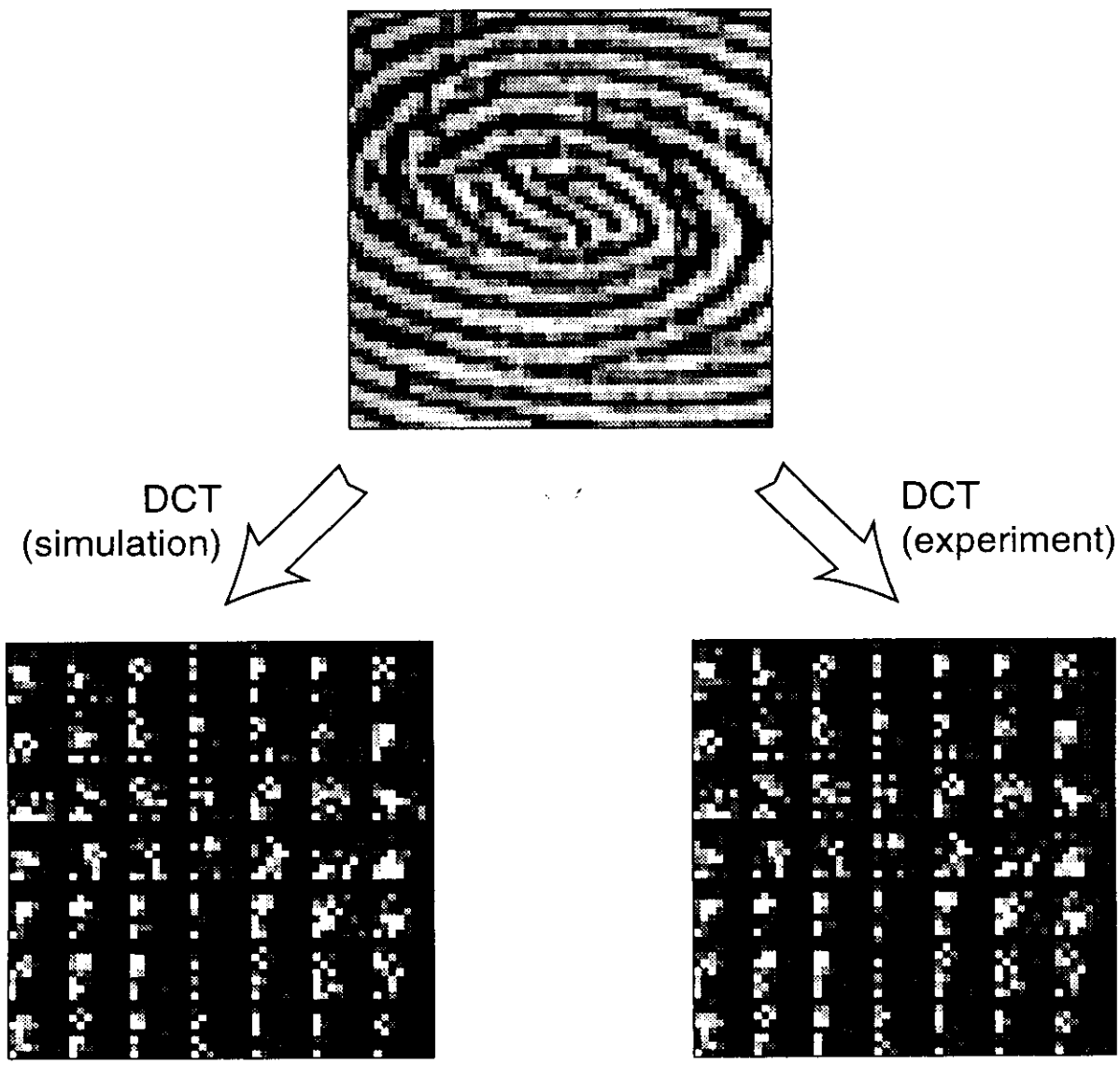
AR: Image Compression

Sensitivity patterns for discrete cosine transform of image blocks. Setting each block of eight VSPD rows to each of the sensitivity patterns yields the discrete cosine transformation in the vertical direction.



AR: Image Compression

Sensed image of a fingerprint and its blockwise cosine transforms. Simulation ans Experiment are in good agreement.



AR: Image Compression

JPEG image compression at compression ratios around ten. Decompression of the compressed images shows good agreement of simulation (a) and experiment (b).

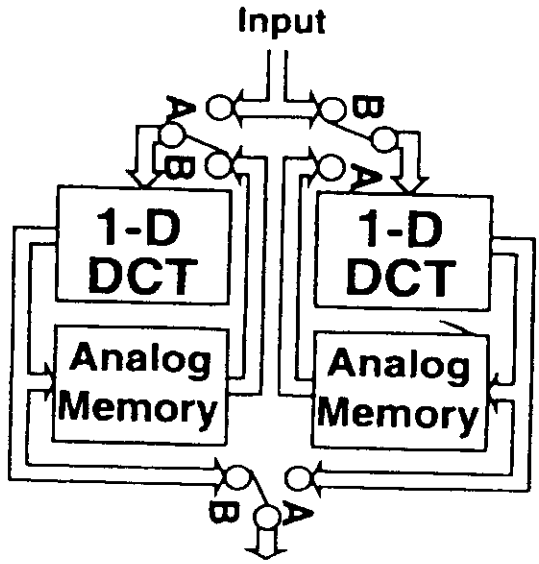
(a)

(b)

CMOS Analog Image Compression

Recently, an image sensor with integrated analog 2-D discrete cosine transform has been implemented in CMOS technology [Kawa 9

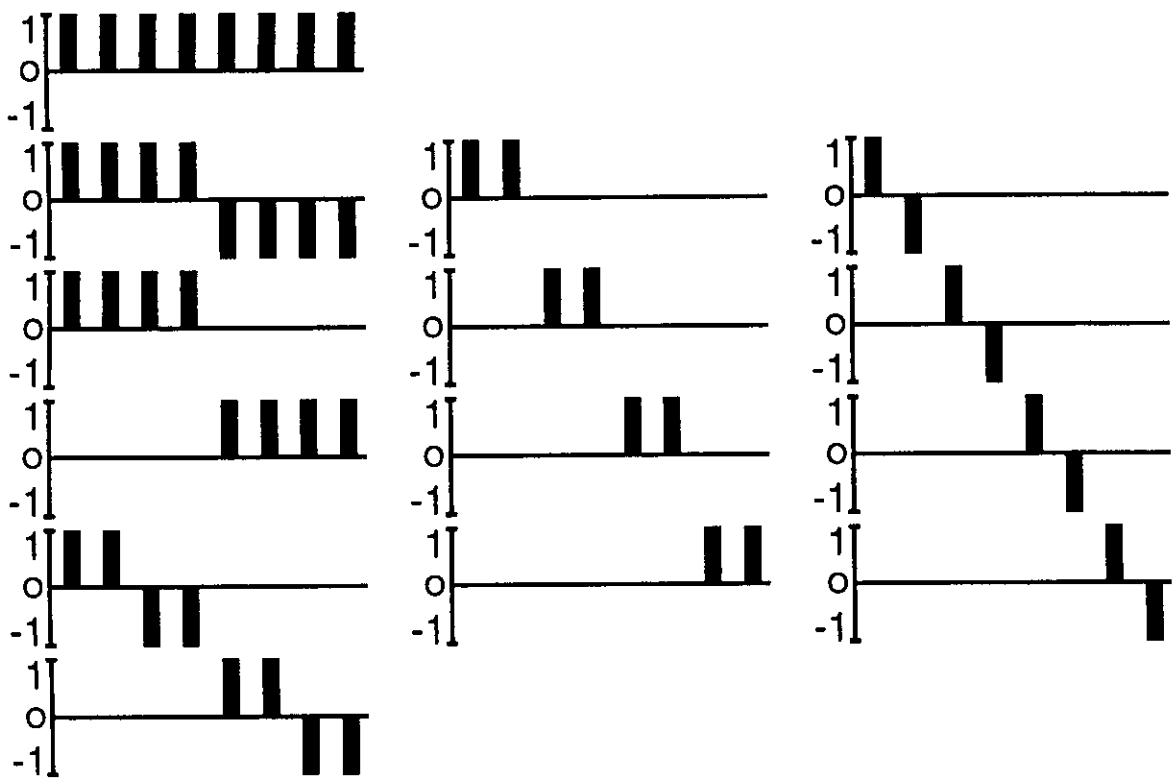
- 128×128 pixels, 30 Frames/s.
- Power dissipation 10mW (at 3V).
- Anaolg 1-D DCT cores in combination with analog memories implement 2-D DCT.



[Kawa 97]

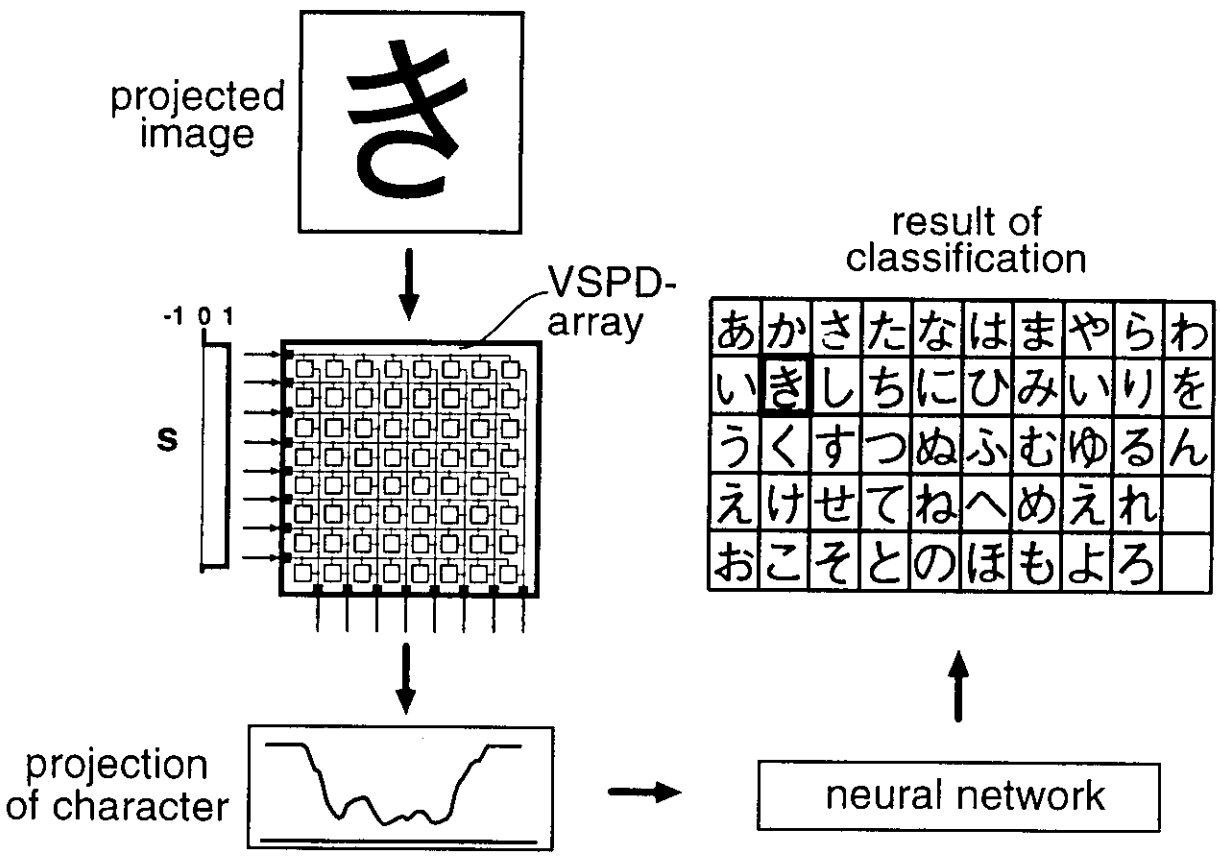
AR: Image Compression

Sensitivity patterns for Haar wavelet transformation.



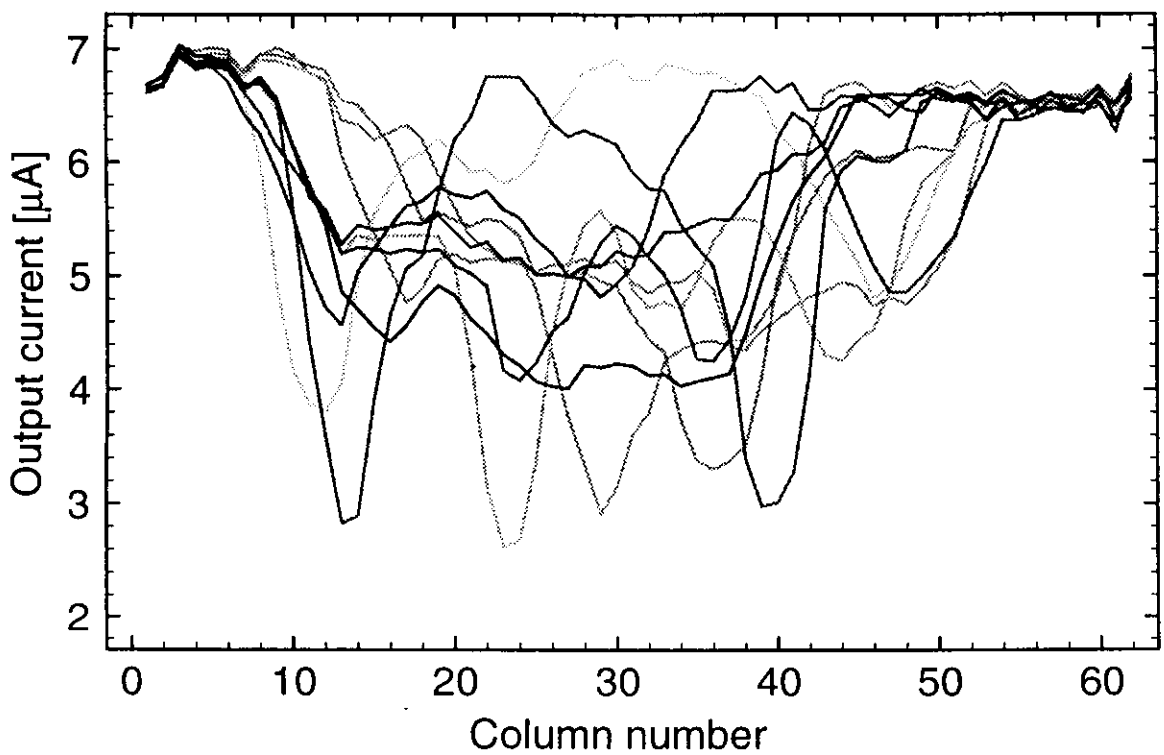
AR: Character Recognition

Character recognition system. The artificial retina directly senses the projection of the character in the vertical direction. A shift tolerant neural network recognizes the character using only this compact, compressed representation.



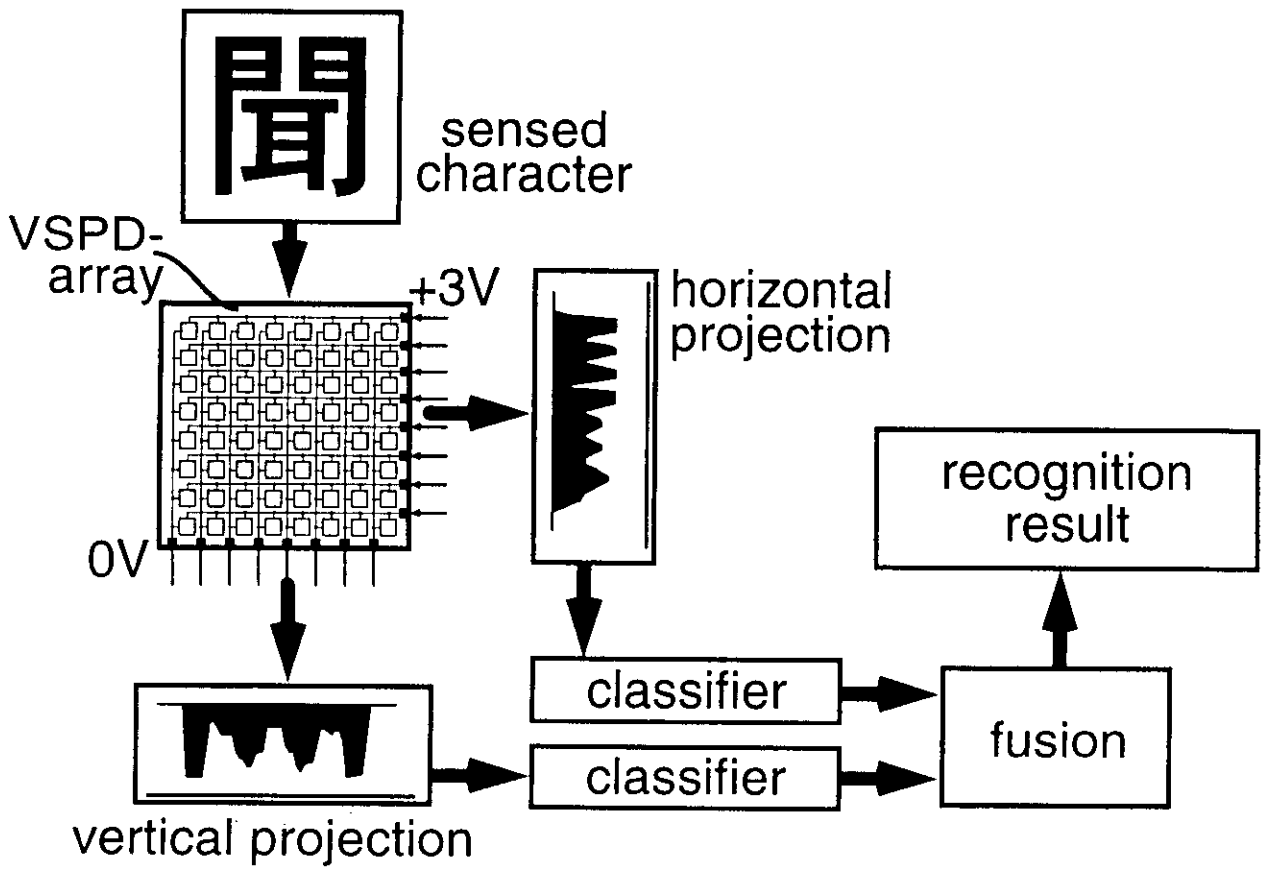
AR: Character Recognition

Character recognition system. The Projections of 10 characters from one of the Japanese syllabaries (hiragana) as sensed by the artificial retina device. The projections are quite different and retain a sufficient amount of information for recognition.



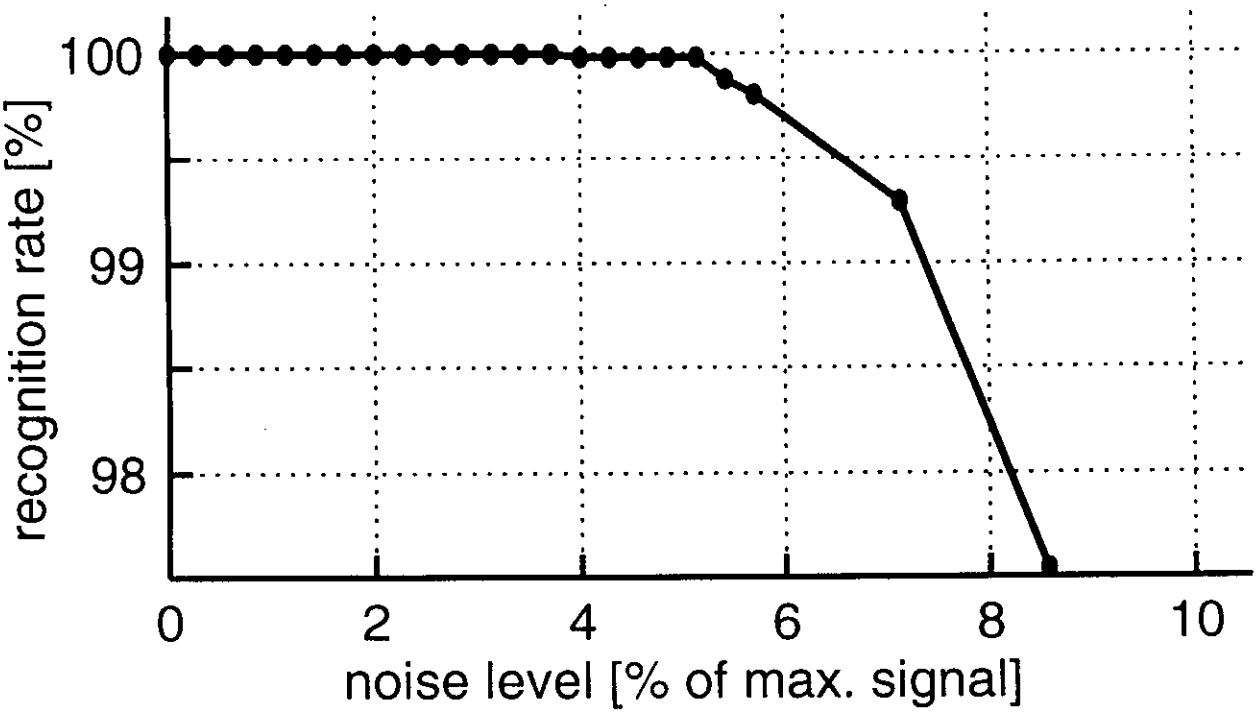
AR: Character Recognition

Two-directional projection mode of AR, applied to character recognition. Horizontal and vertical projections provide a sufficient amount if information to represent and recognize many different sensed character.



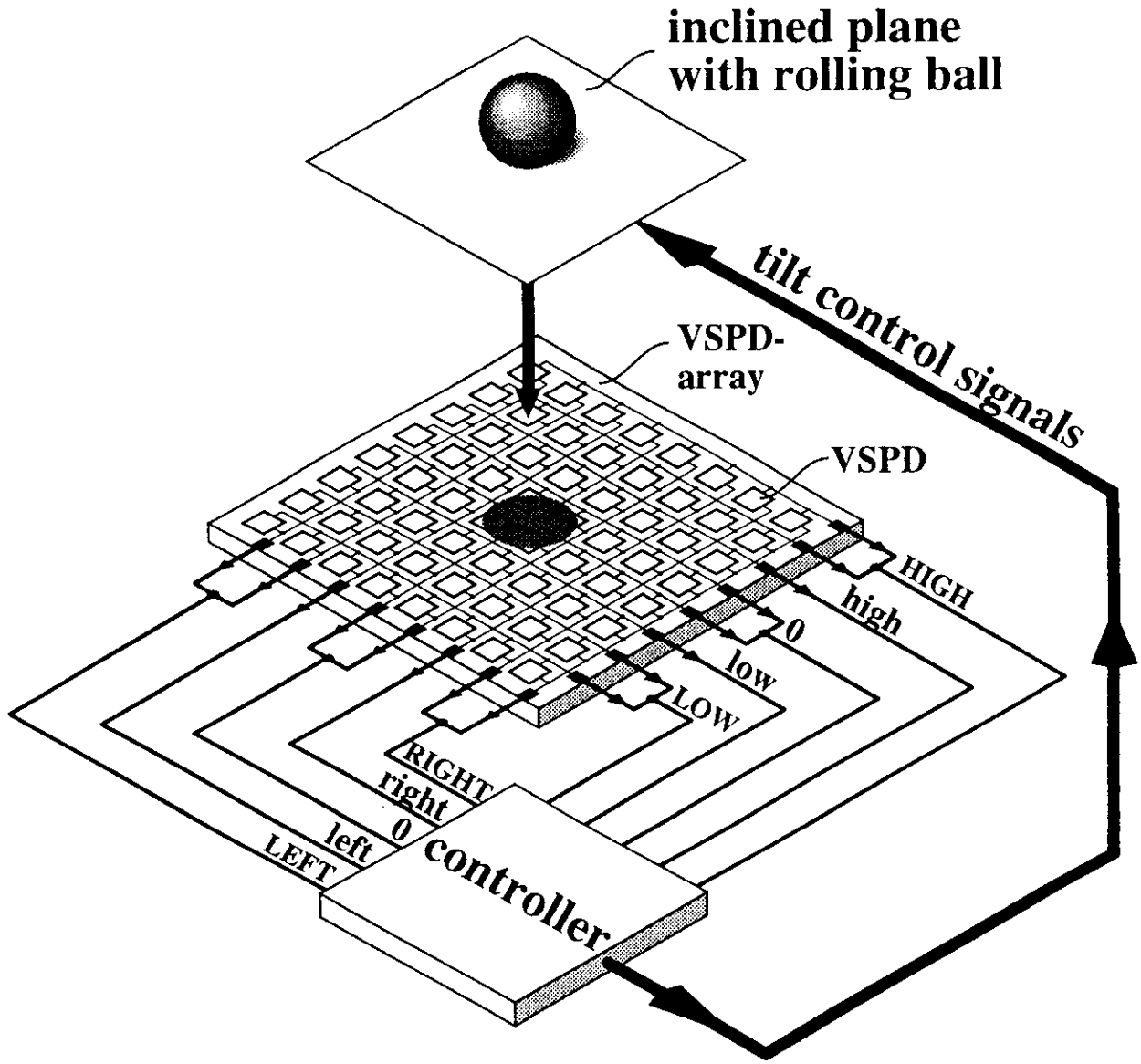
AR: Character Recognition

Character recognition performance in two-directional projection mode of AR. Using a set of 1945 Sino-Japanese ideographic characters, the system achieves recognition rates of up to 99.99 %.



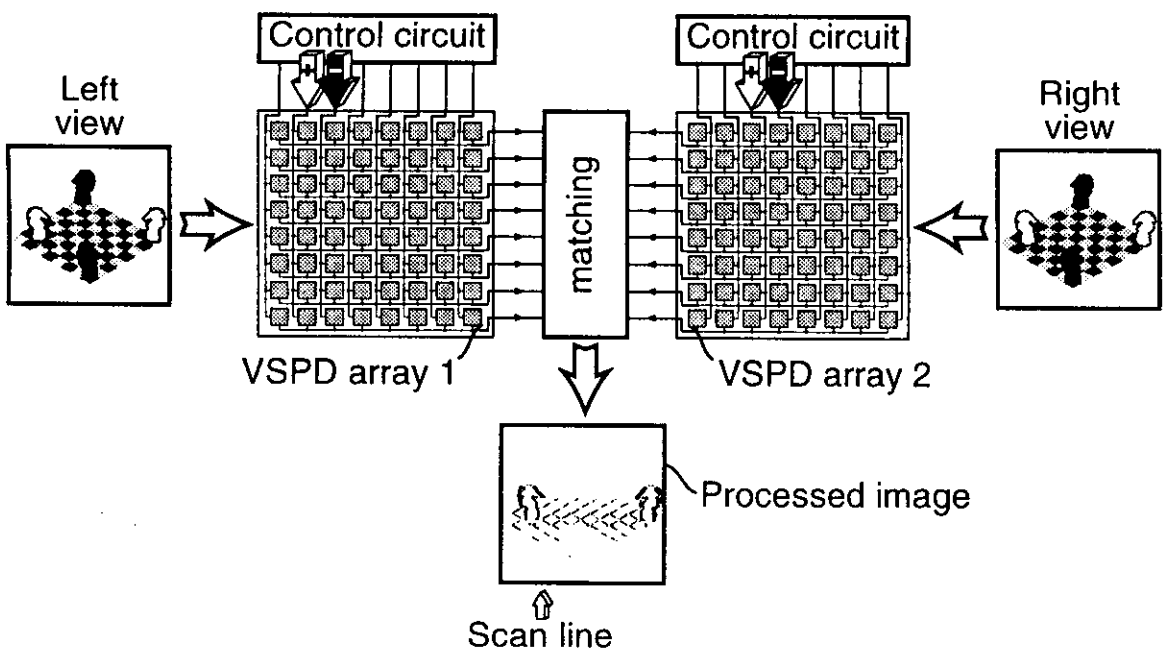
AR: Tracking

Demonstration of position control which utilizes the capability of VSPD arrays to concurrently measure the vertical and horizontal projection of an image.



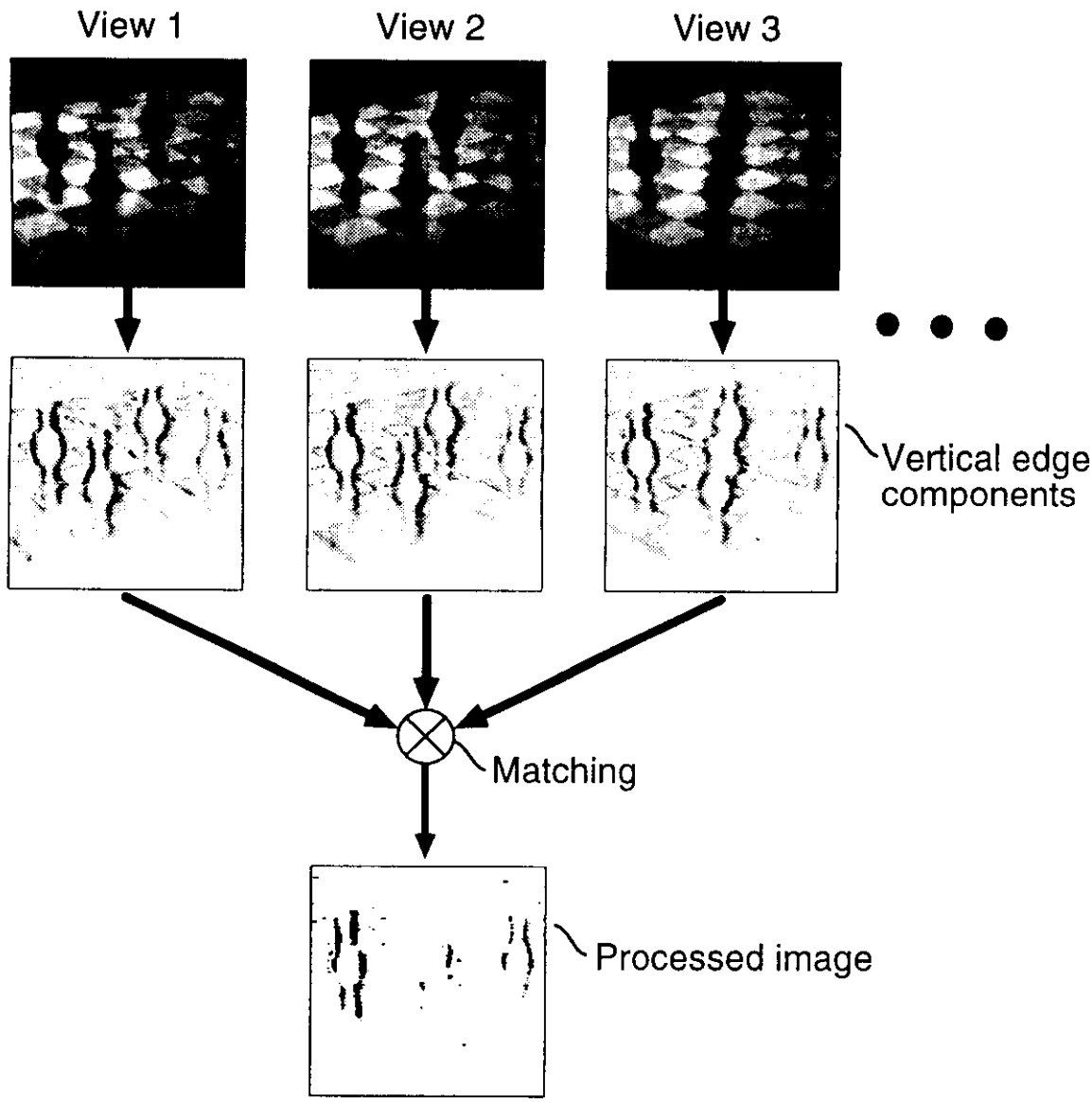
AR: Depth Perception

Architecture of a stereo vision system. The VSPD arrays perform edge enhancement and image shift. Pixel-by-pixel matching of image lines yields a processed image with the focus of attention on an arbitrary depth plane. In the simulation result shown, the focus of attention is set to the middle depth plane.



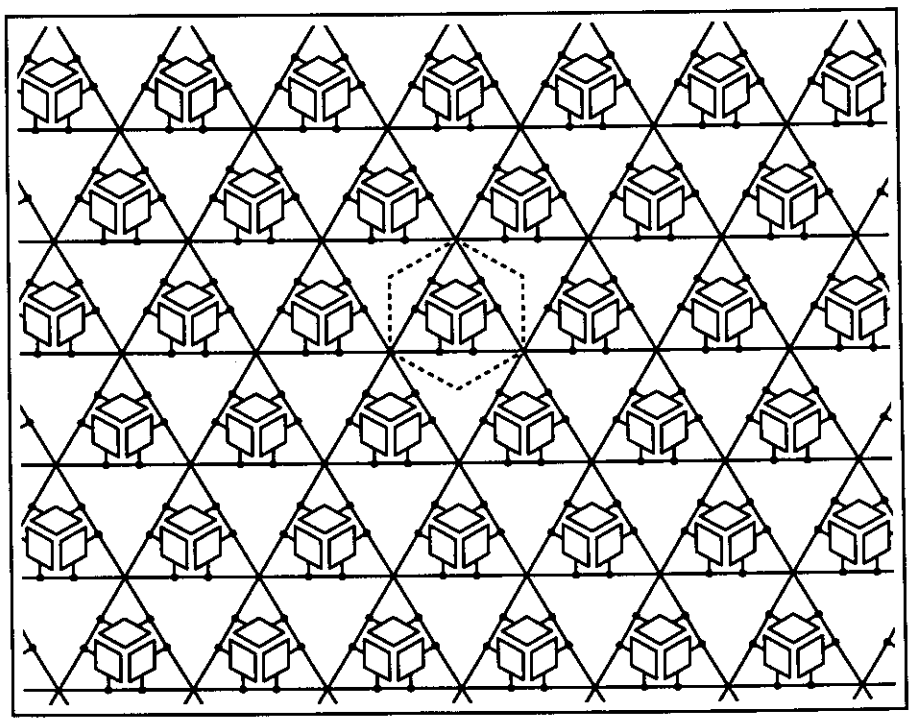
AR: Depth Perception

Experimental results of depth perception using matching of multiple views. Multiple views help to resolve correspondency problems.



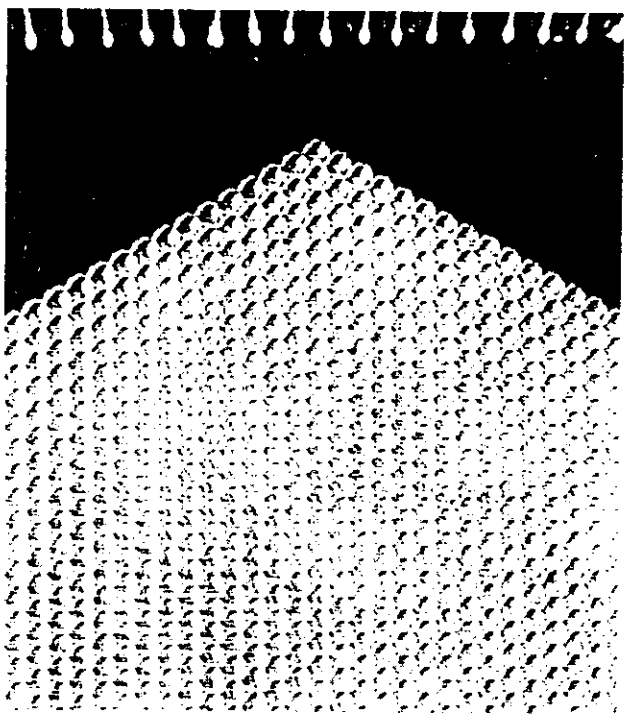
AR: Hexagonal Configuration

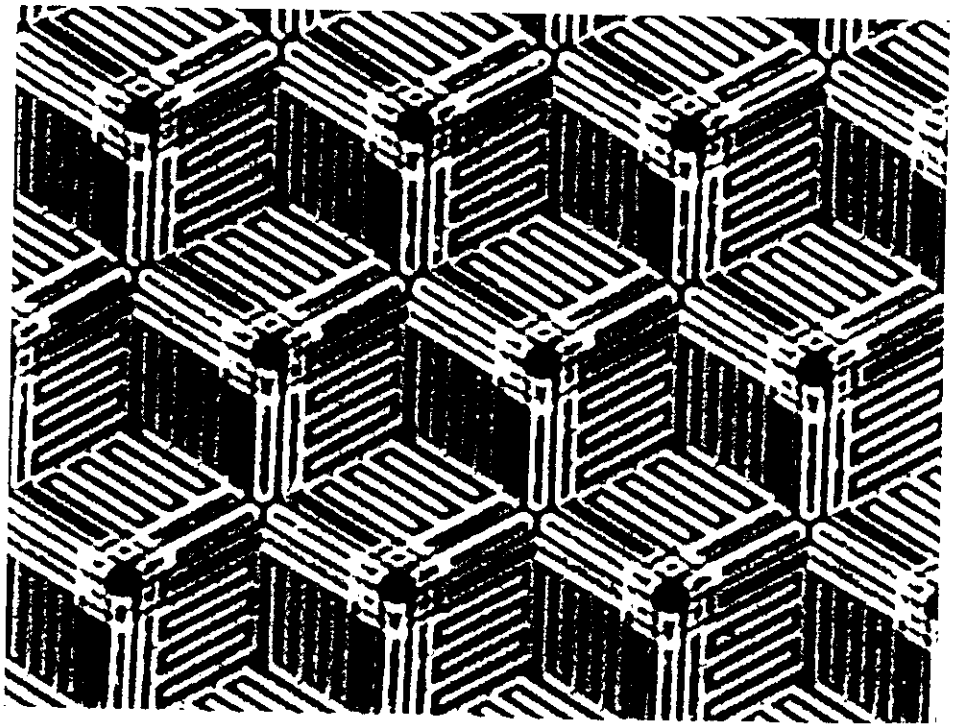
- VSPD arrays in hegagonal configuration implement three-directional scanning.
- Application example: concurrent measurement of three-directional image projections.
- Three image projections contain a sufficient amount of information for position and orientation computation (centroid and axis of least inertia) — a simple alternative to 2-D resistive grids.



AR: Hexagonal Configuration

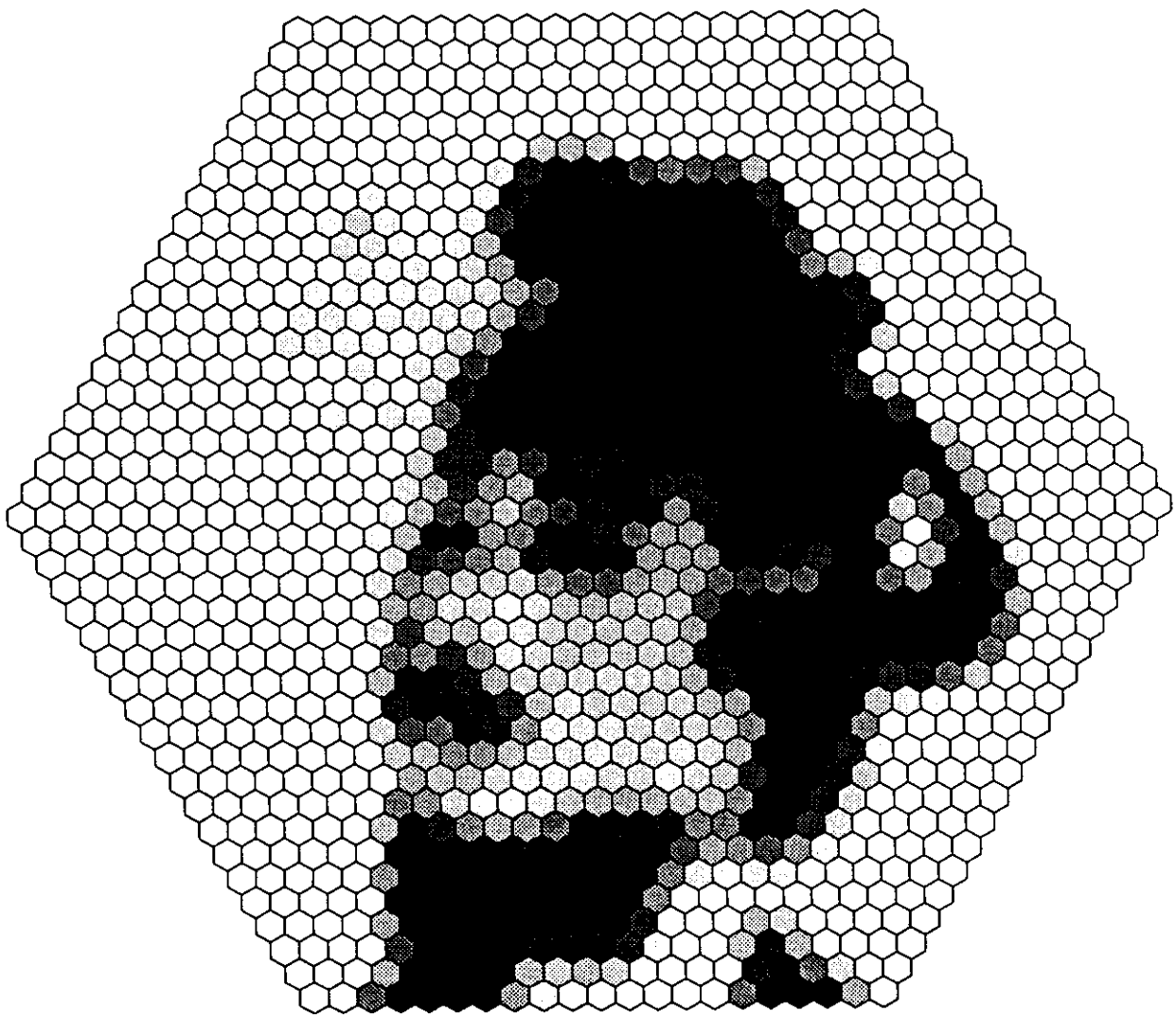
Device micrograph of hexagonal MSM-VSPD array.





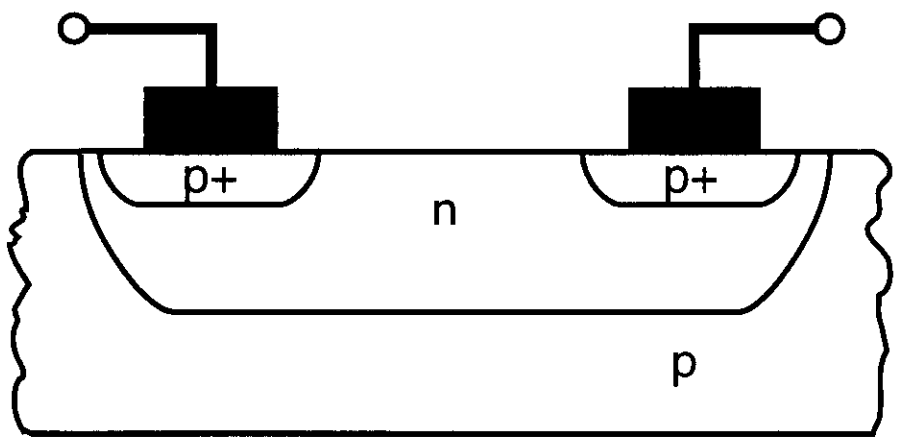
AR: Hexagonal Configuration

Image sensed in the TV-camera like operation mode of the hexagonal MSM-VSPD array.



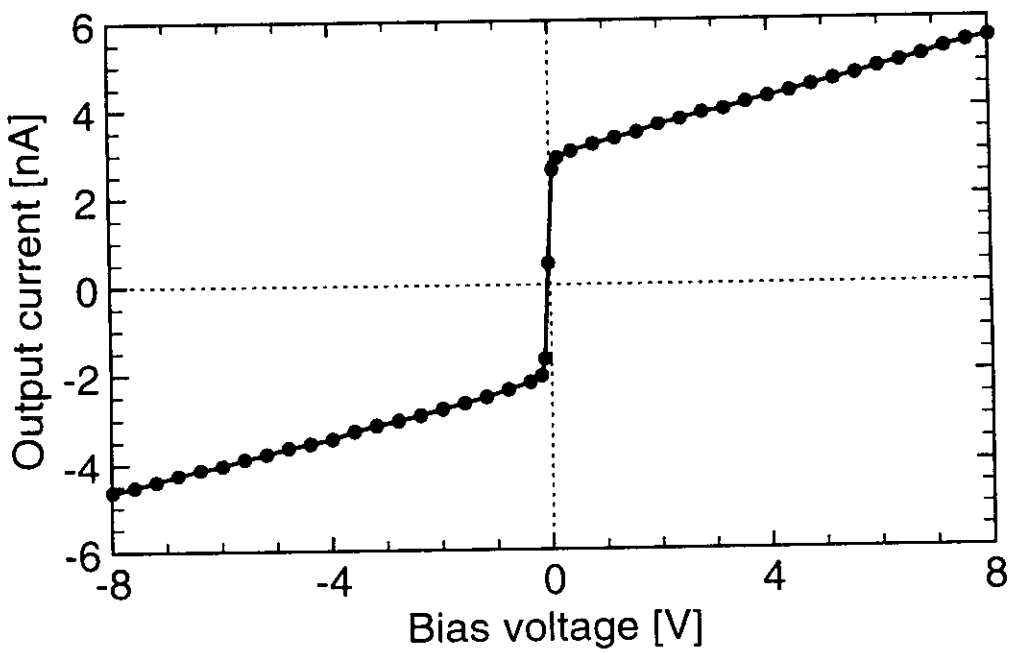
Detector Types: Silicon-VSPD

- Fabricated in a standard CMOS process.
- Internal gain bost output current by two orders of magnitude [Herm 94].



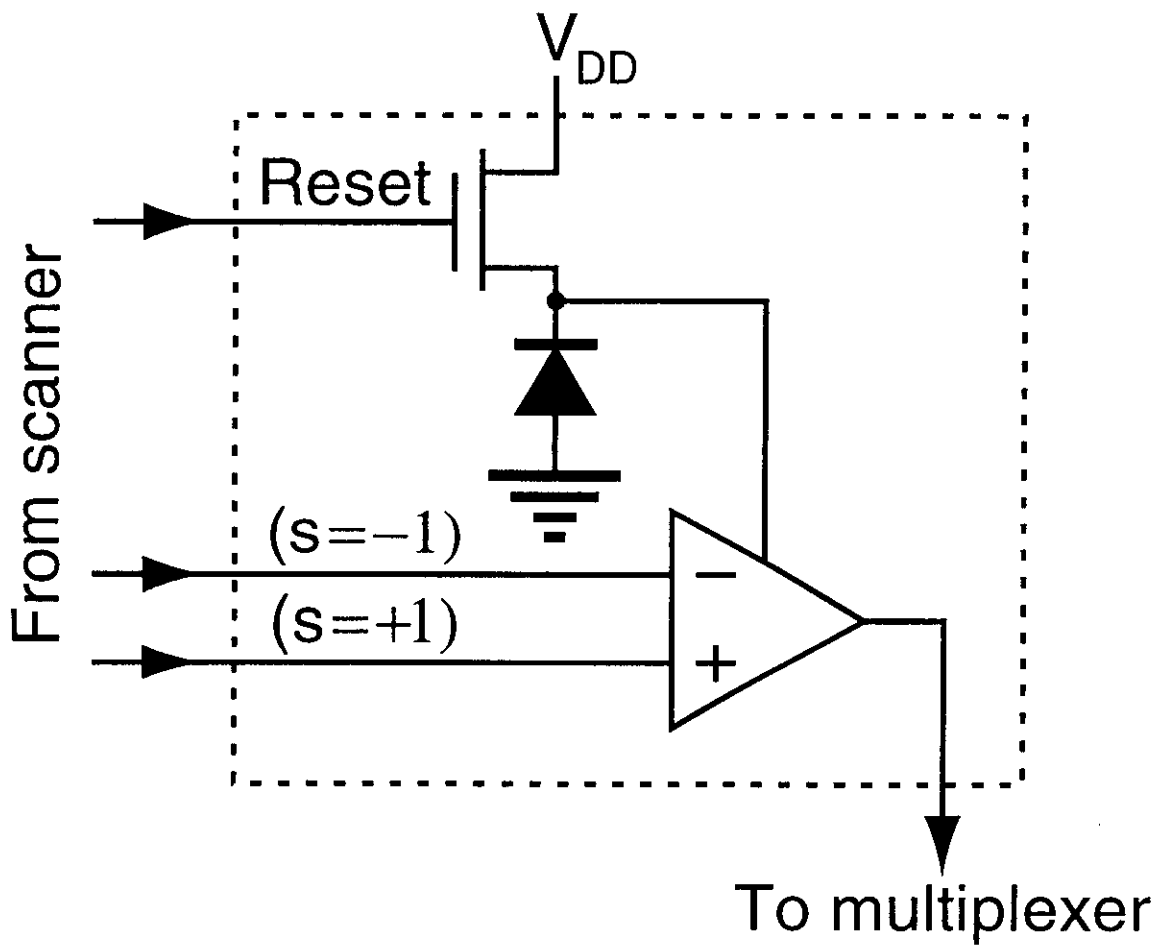
Silicon-VSPD Response Curve

- Steep response curve at small bias voltages.
- Suitable bias: three fixed voltages (± 3 V and 0 V, for example).



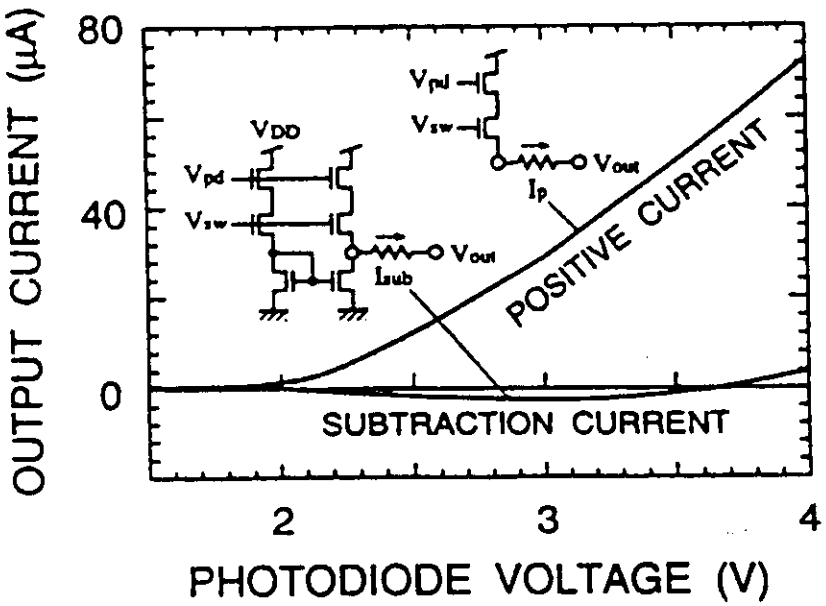
Detector Types: VSPC

Variable sensitivity photodetection cells combine charge integration and three-level sensitivity setting (positive, negative, zero) [Funa 95, Funa 97].



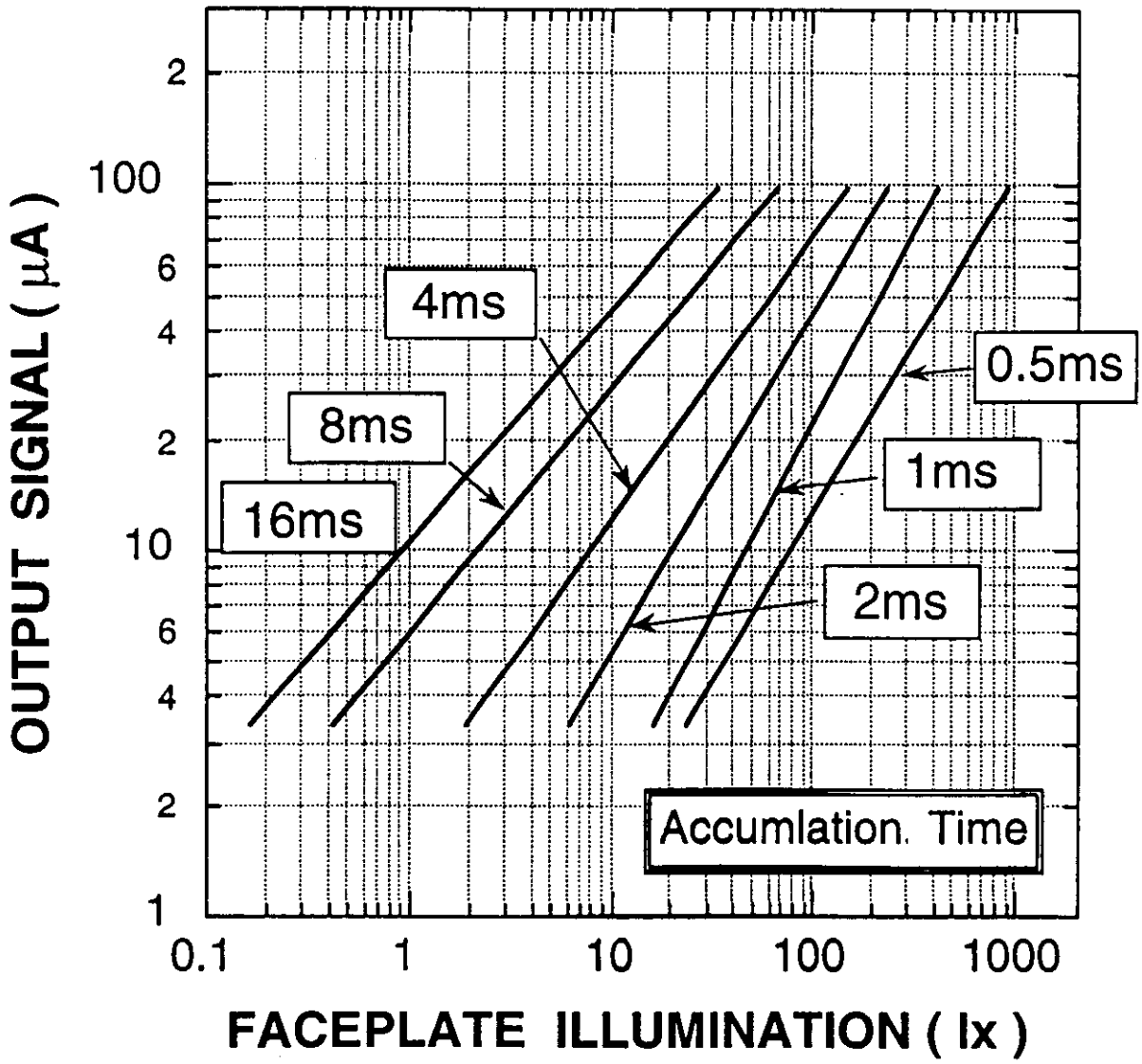
Detector Types: VSPC Response Curve

Simulated response of VSPC cells set to positive sensitivity (positive current), and difference between cells set to positive and negative sensitivity, respectively (subtraction current) [Funa 97]. Positve and negative currents cancel mostly, as intended (maximum deviation 4.8 %).

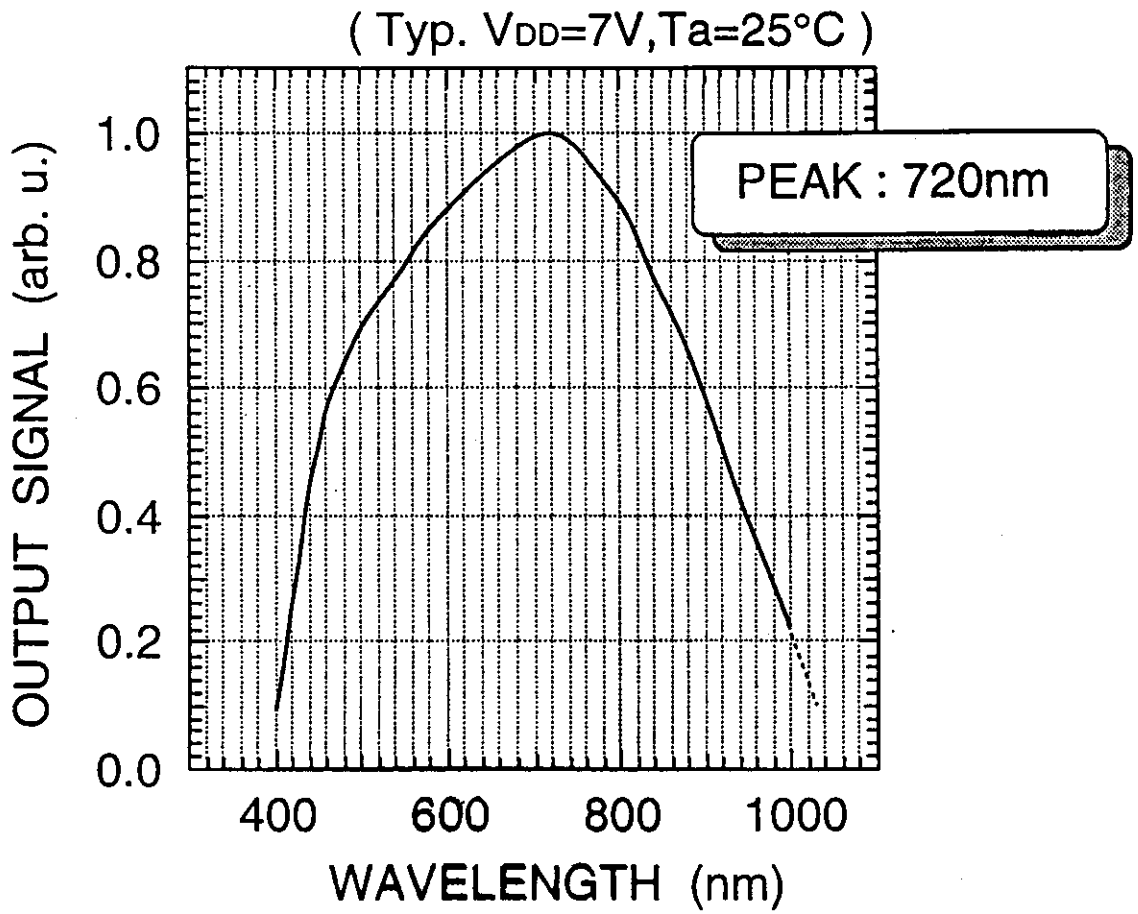


Detector Types: VSPC Photoconversion Characersitics

Variable sensitivity photodetection cells can be used over a wide range of illumination levels.

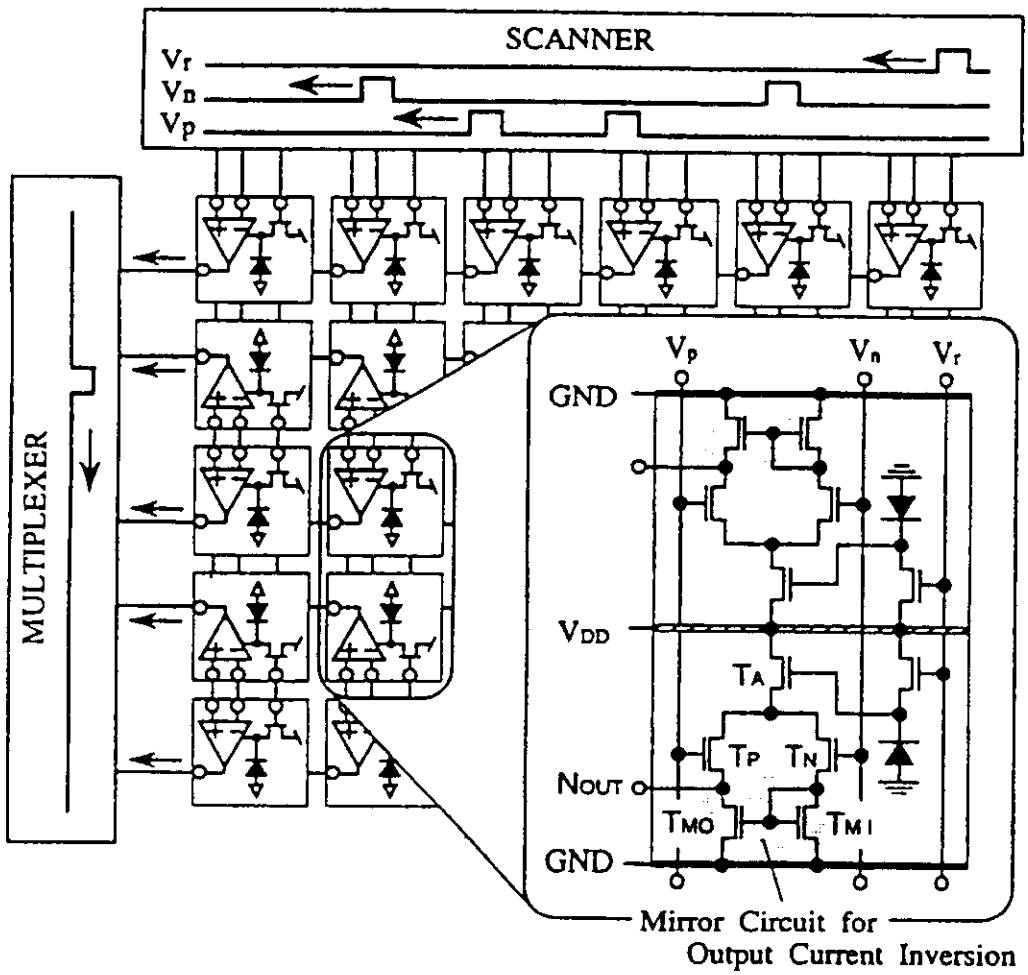


Detector Types: VSPC Spectral Response



CMOS-AR: Implementation Using VSPC-Array

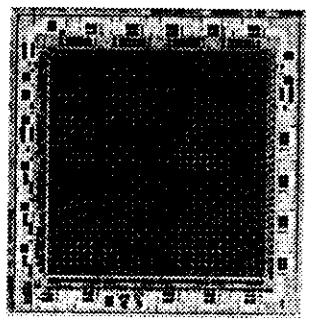
Implementation details of variable sensitivity photodetection cells, and schematic VSPC arrangement. The pulse pattern shown in the scanner results in a pattern matching operation [Funa 97].



CMOS-AR: Chip Specifications

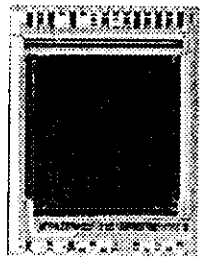
Resolution	32 x 32	128 x 128		352 x 288 (Under Development)
Chip Size	6.5mm x 6.5mm	6mm x 4.5mm	10mm x 10mm	10mm x 10mm
Function	1-D Filtering	1-D Filtering	2-D Filtering	2-D Filtering
Fabrication Technology	1.0 μm CMOS	0.8 μm CMOS	0.7 μm CMOS	0.5 μm CMOS
Sensitivity	~0.20 μA/lx・msec			
Dynamic Range	40dB (Input Light Power)			
Frame Rate	Variable:1msec~1000msec (1Hz~1000Hz)			
Accumulation Time	Variable:0.125msec~1000msec			

CMOS-AR: Chip Family



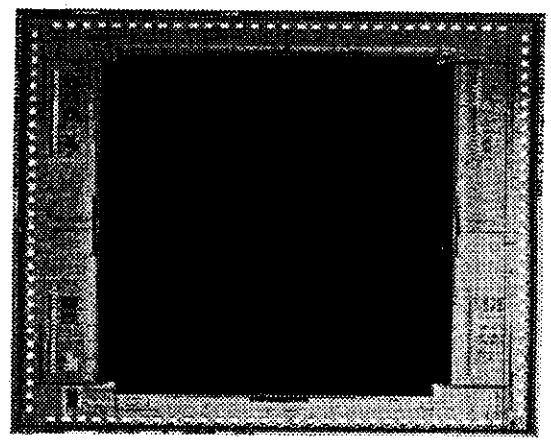
32x32-pixel

Chip size: 6.5x6.5mm²
Pixel size: 150x150μm²
Process Rule: 1.0μm
(Developed)



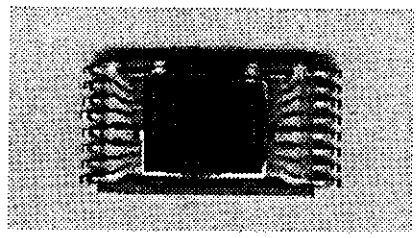
128x128-pixel

Chip Size: 6.0x4.5mm²
Pixel Size: 24x24μm²
Process Rule: 0.8μm
(Developed)



352x288-pixel

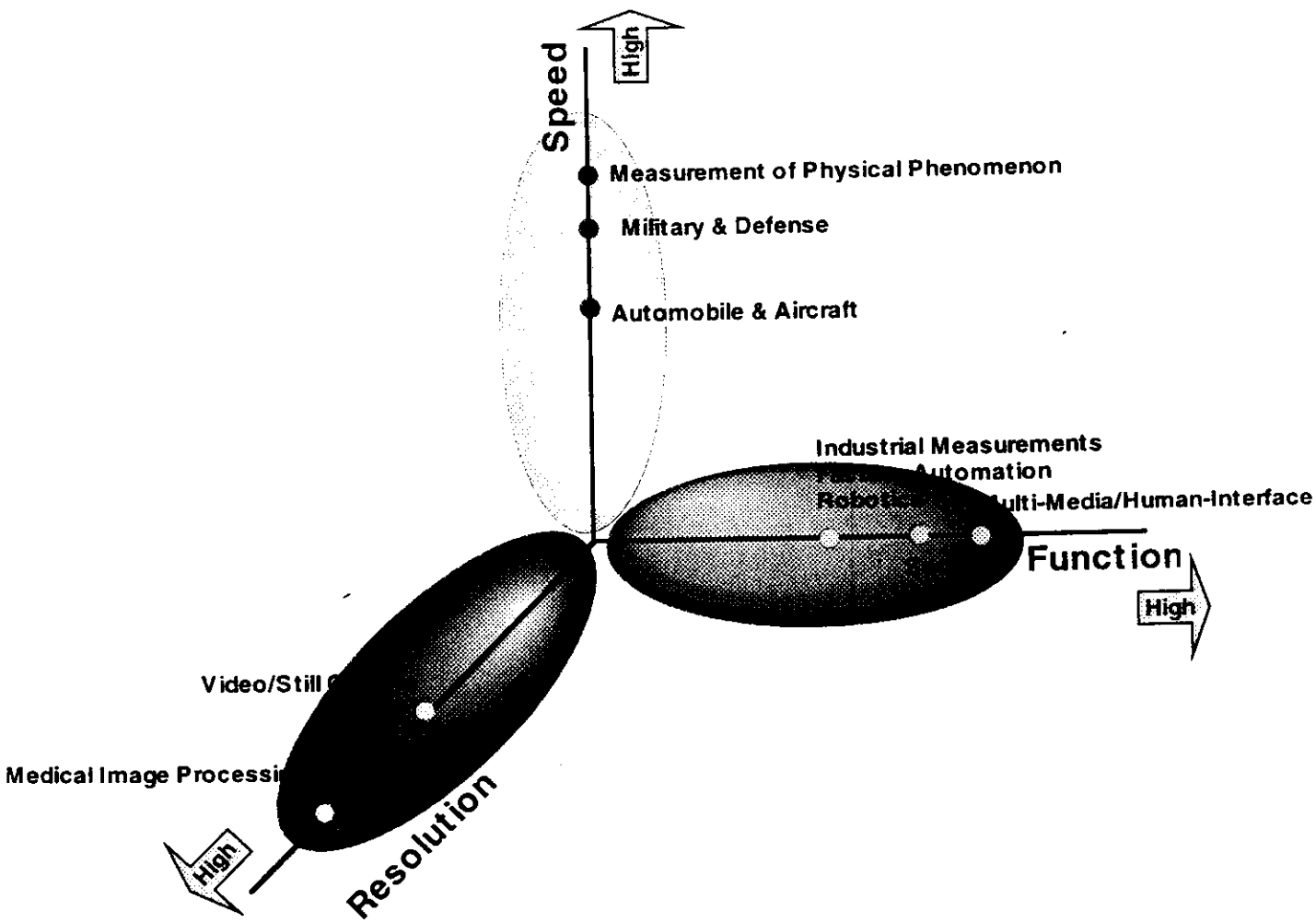
Chip Size: 10x12mm²
Pixel Size: 16x16μm²
Process Rule: 0.5μm
(Under Development)



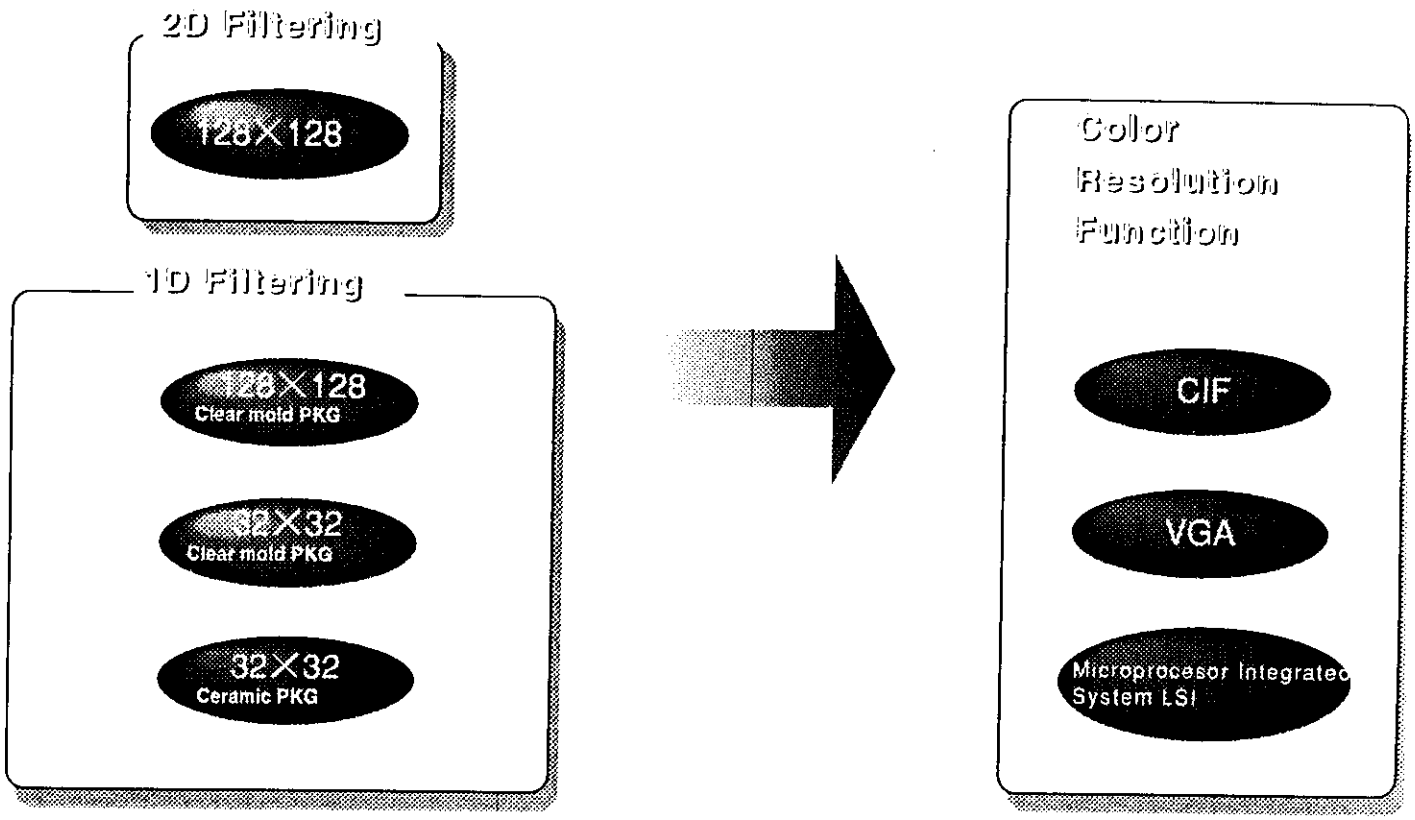
(Size : 11.1mm×6.9mm)

Graph of Artificial Retina LSI (M64282FP) (128×128-pixel)

CMOS-AR Application Fields

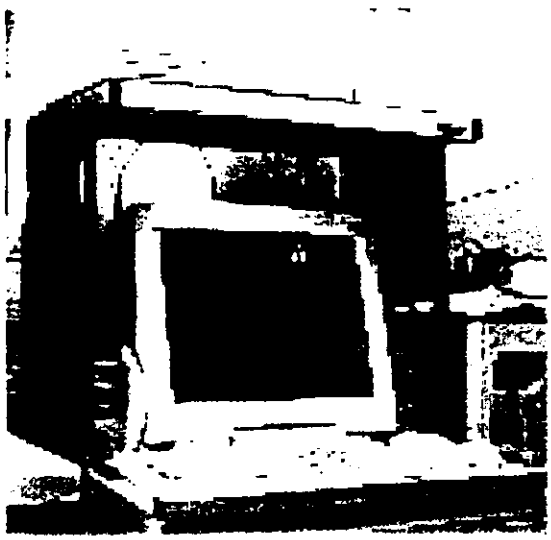


CMOS-AR: Road Map

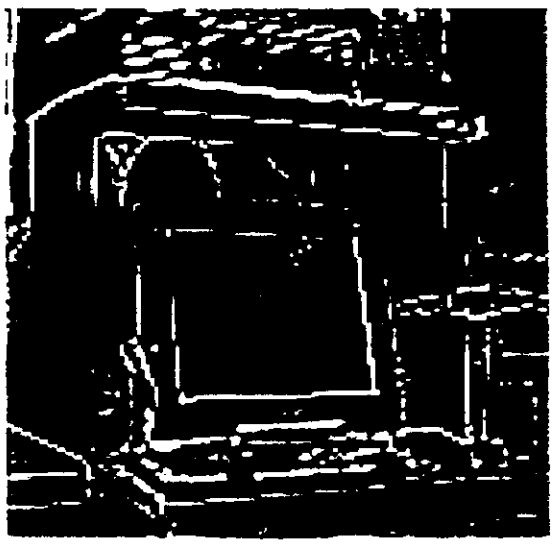


AR: 2-D Filtering Chip

Implements convolution with a 5×5 kernel (sensitivities: ±1 and 0); processing example:

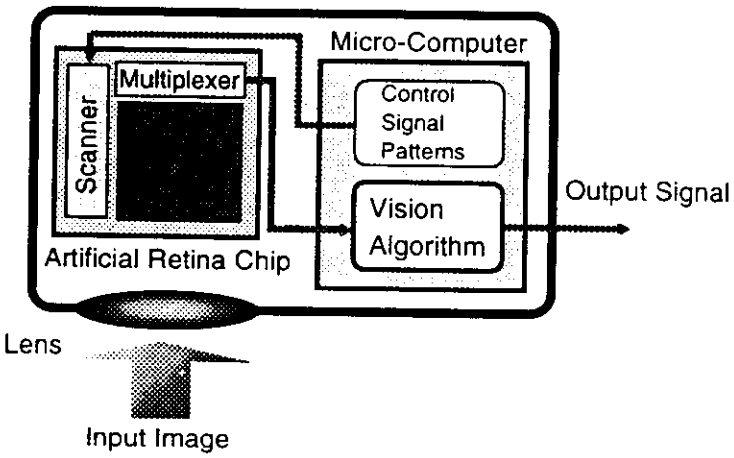


Original Image

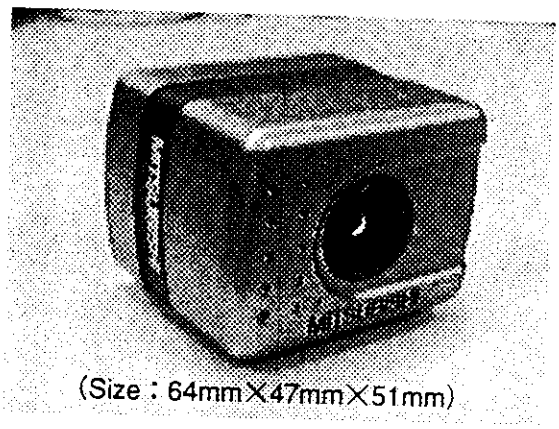


Edge Extracted Image

CMOS-AR Modul



(b) Block Diagram



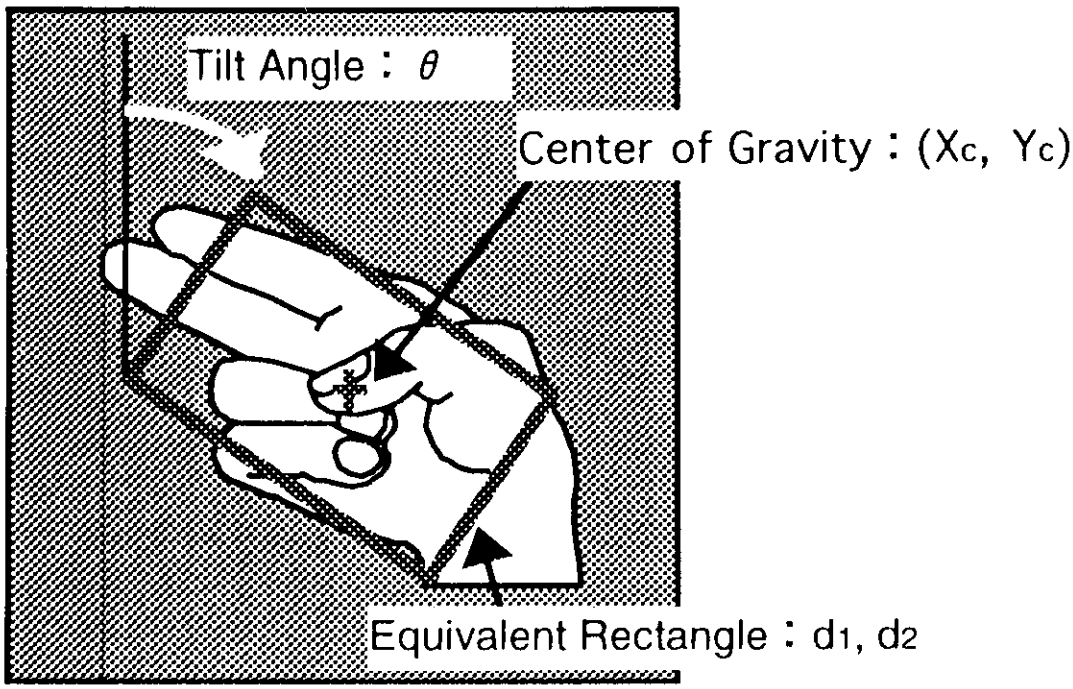
(a) Photograph

(c) Specifications

Frame rate	More than 100 frames/s
Interfaces	Serial (230kbps) Parallel (200kB/s)
Clock	10MHz
Power Supply	12VDC
Size	64mm×47mm×51mm
Sensitivity	10lx (F=2.3)

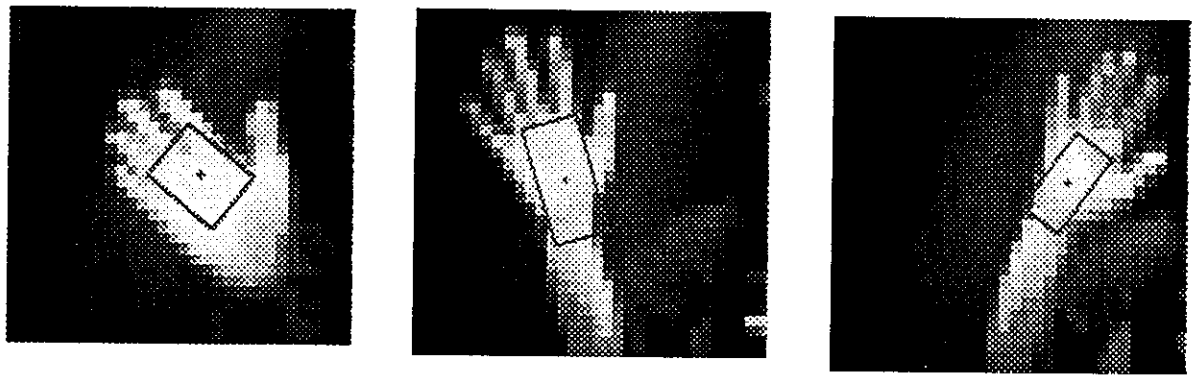
AR: Hand Gesture Recognition

Position and orientation sensing application: hand gesture recognition.



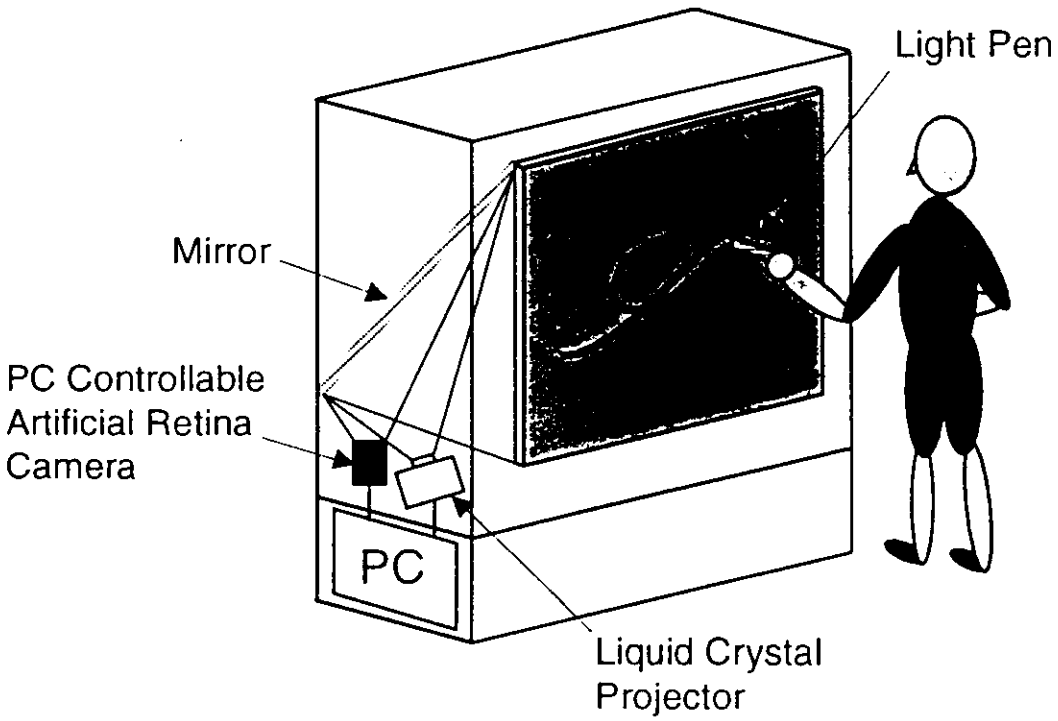
AR: Hand Gesture Recognition

Experimental results of hand gesture recognition. Image moments are used to calculate equivalent rectangles.

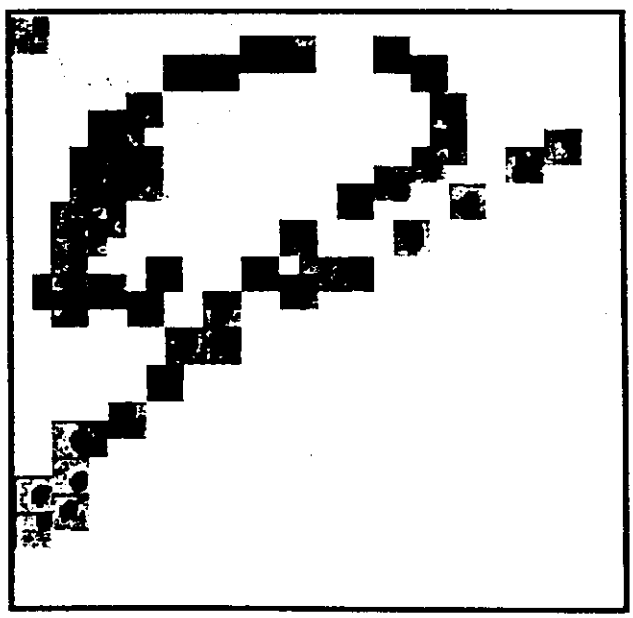


Experimental Results of Hand Gesture Recognition

AR: Target Tracking

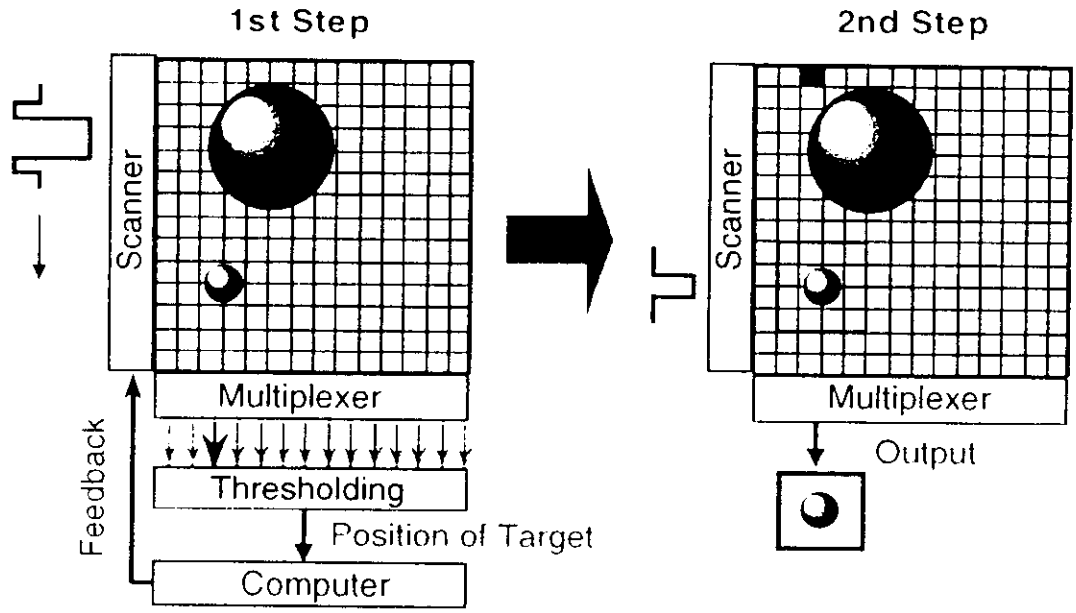


Experimental Setup

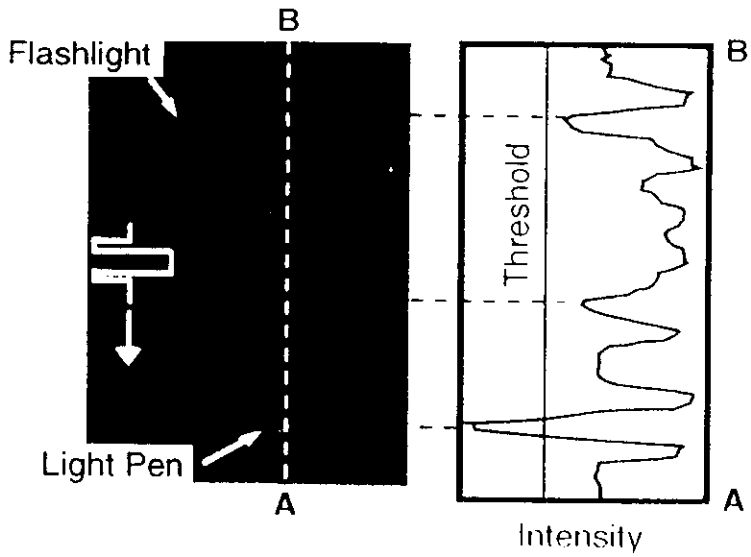


Light Spot Tracing

AR: Target Tracking

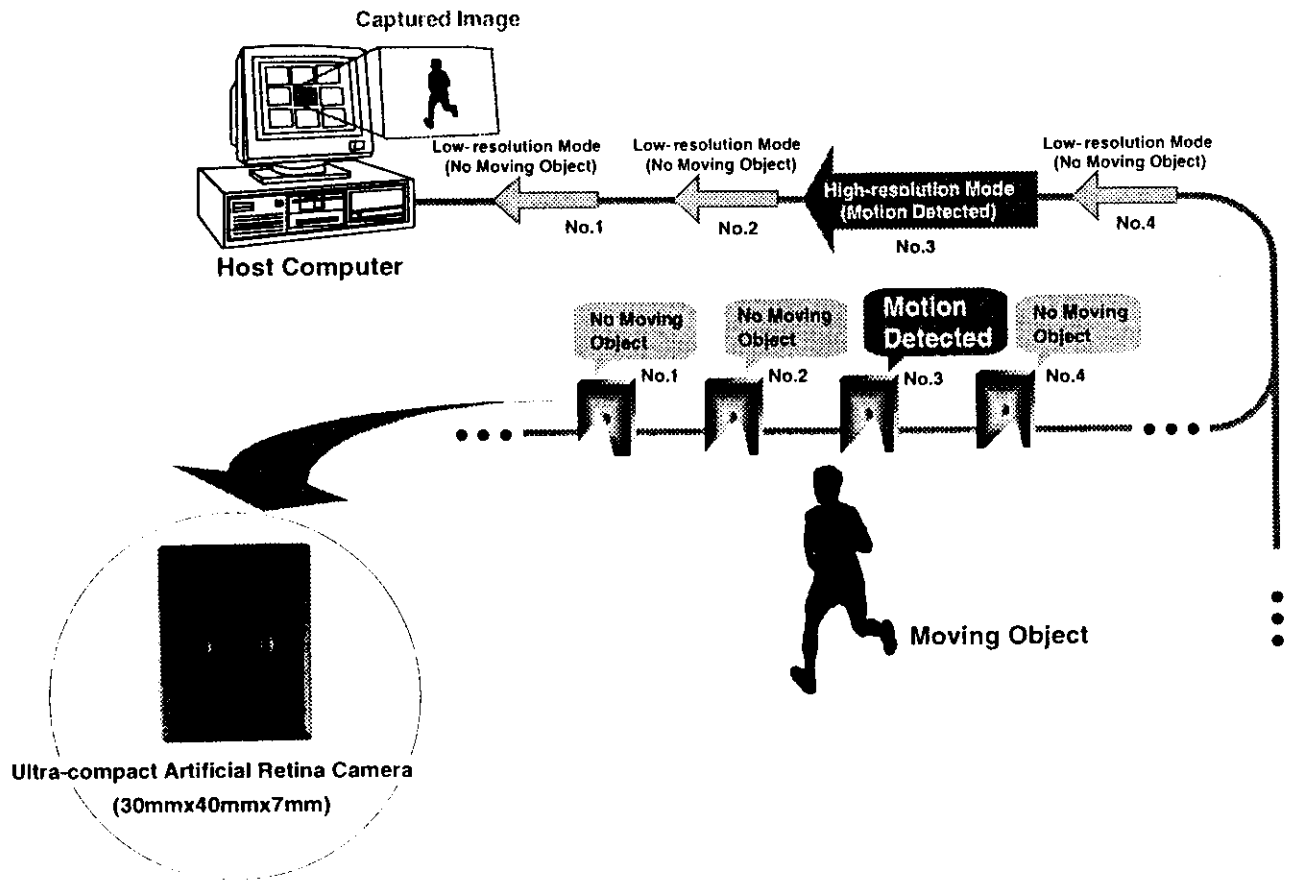


Pattern Matching **Random Access**

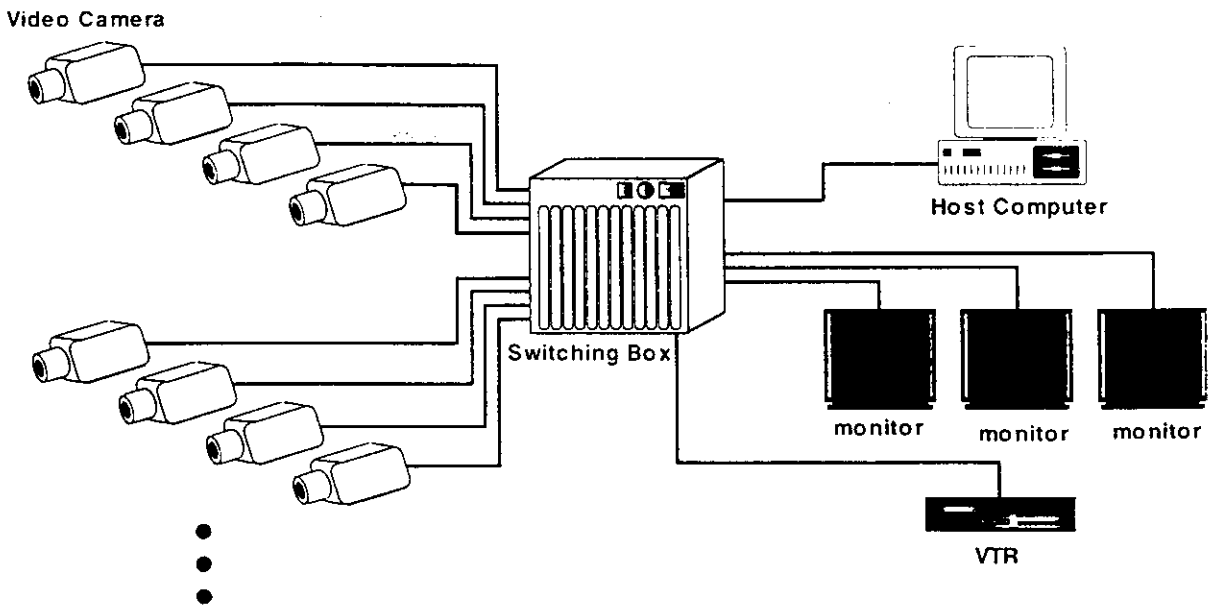


Experimental Result

AR: Security Network System



Present Monitoring System

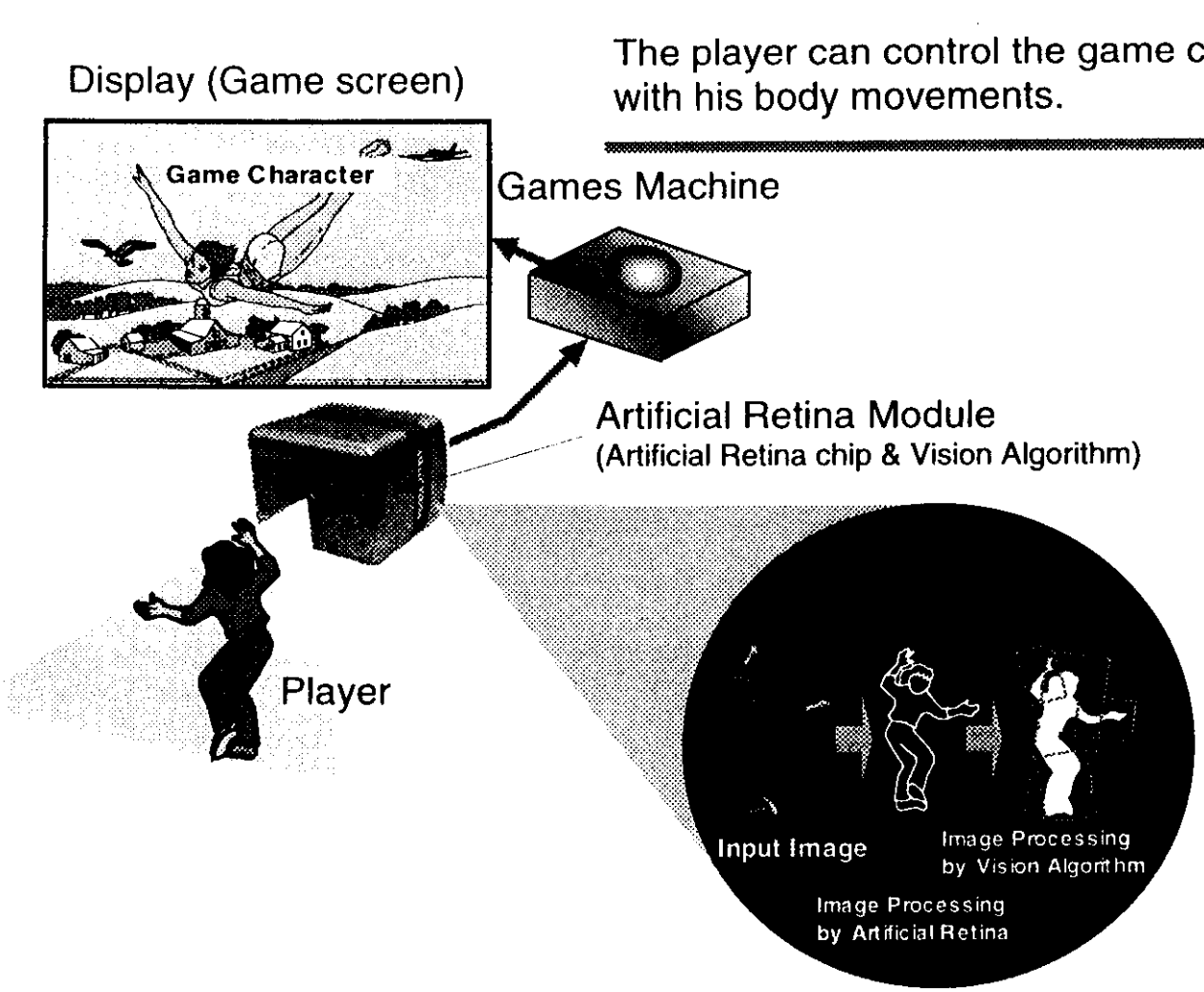


AR: Interactive Game

- Goal: immersion (requires fast feedback of visual gestures to game).
- Complete cycle (sensing, processing, feedback to game) takes only 17 ms.
- Good example for low-resolution image processing and extraction of significant information.

AR: Interactive Game

The player can control the game character with his body movements.

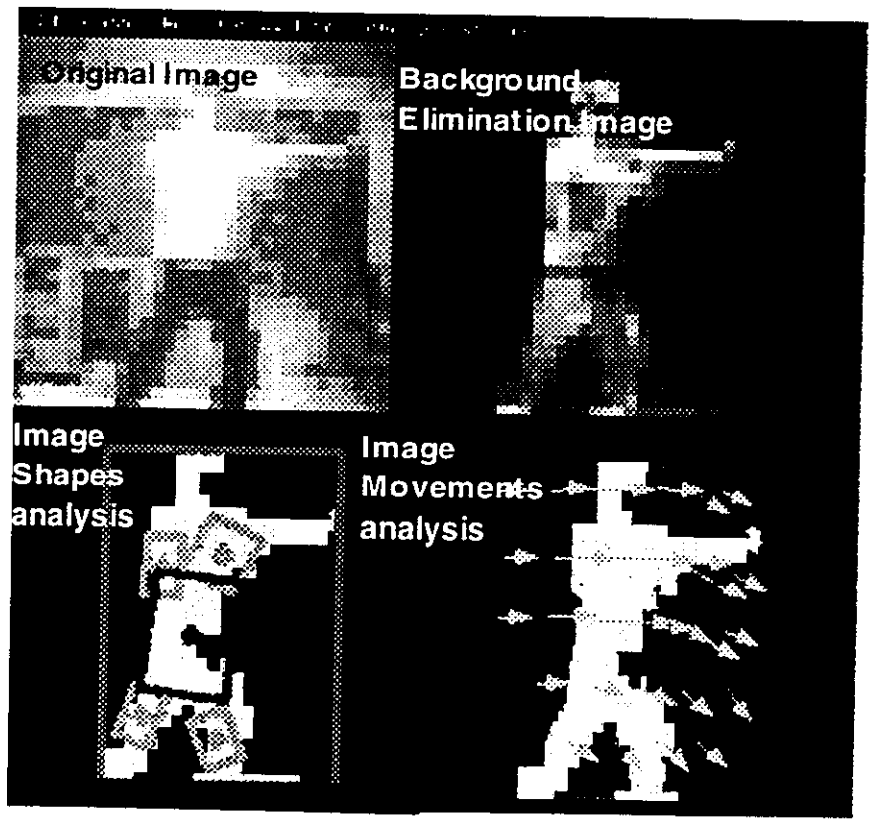


AR: Interactive Game

Real Time Vision Algorithm

The realtime recognition algorithm detects hand gestures and/or body actions with high-speed and high accuracy. It has the advantages of requiring only limited computing power and of being little affected by background.

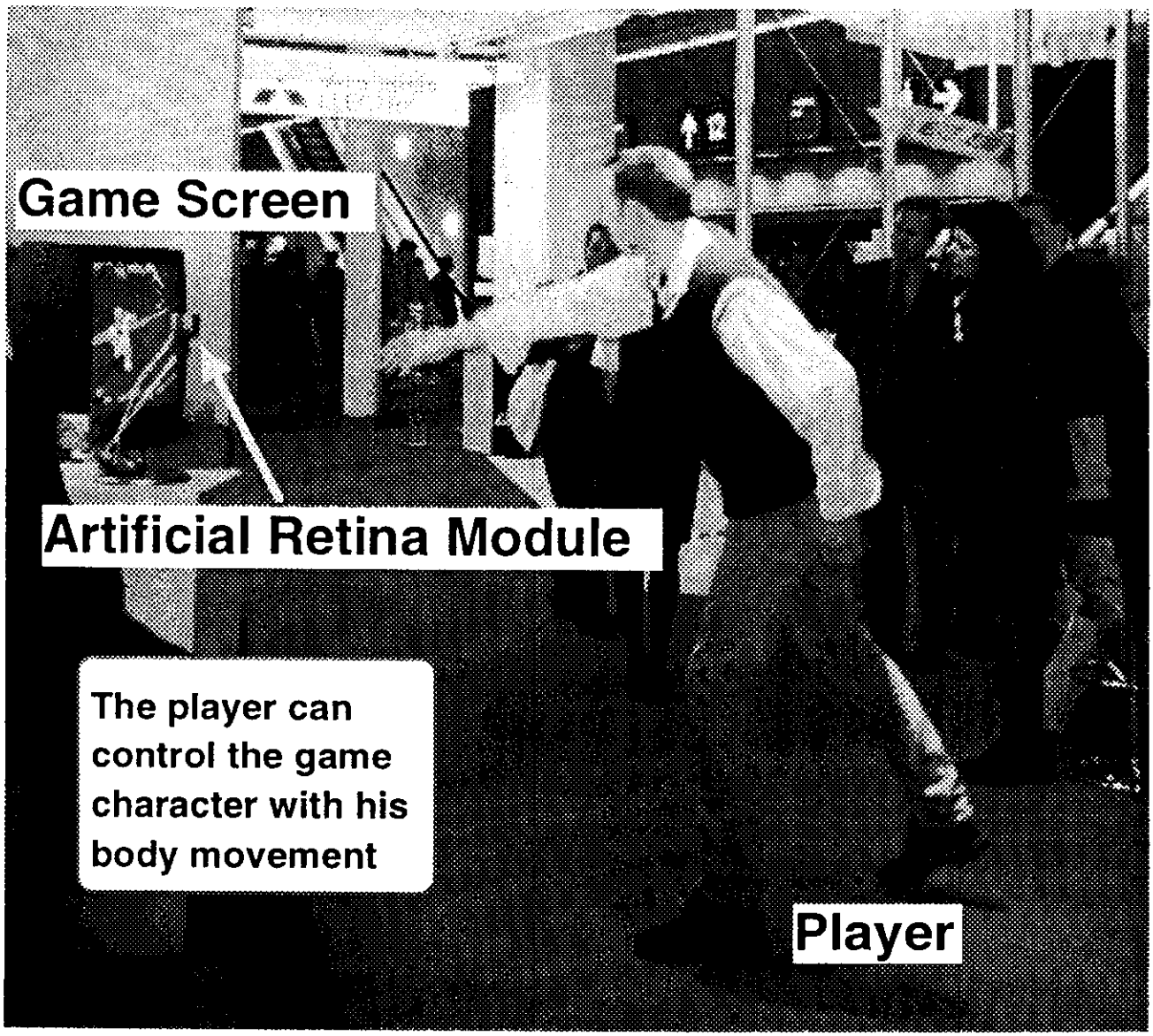
Image Processing Steps



Features of Model

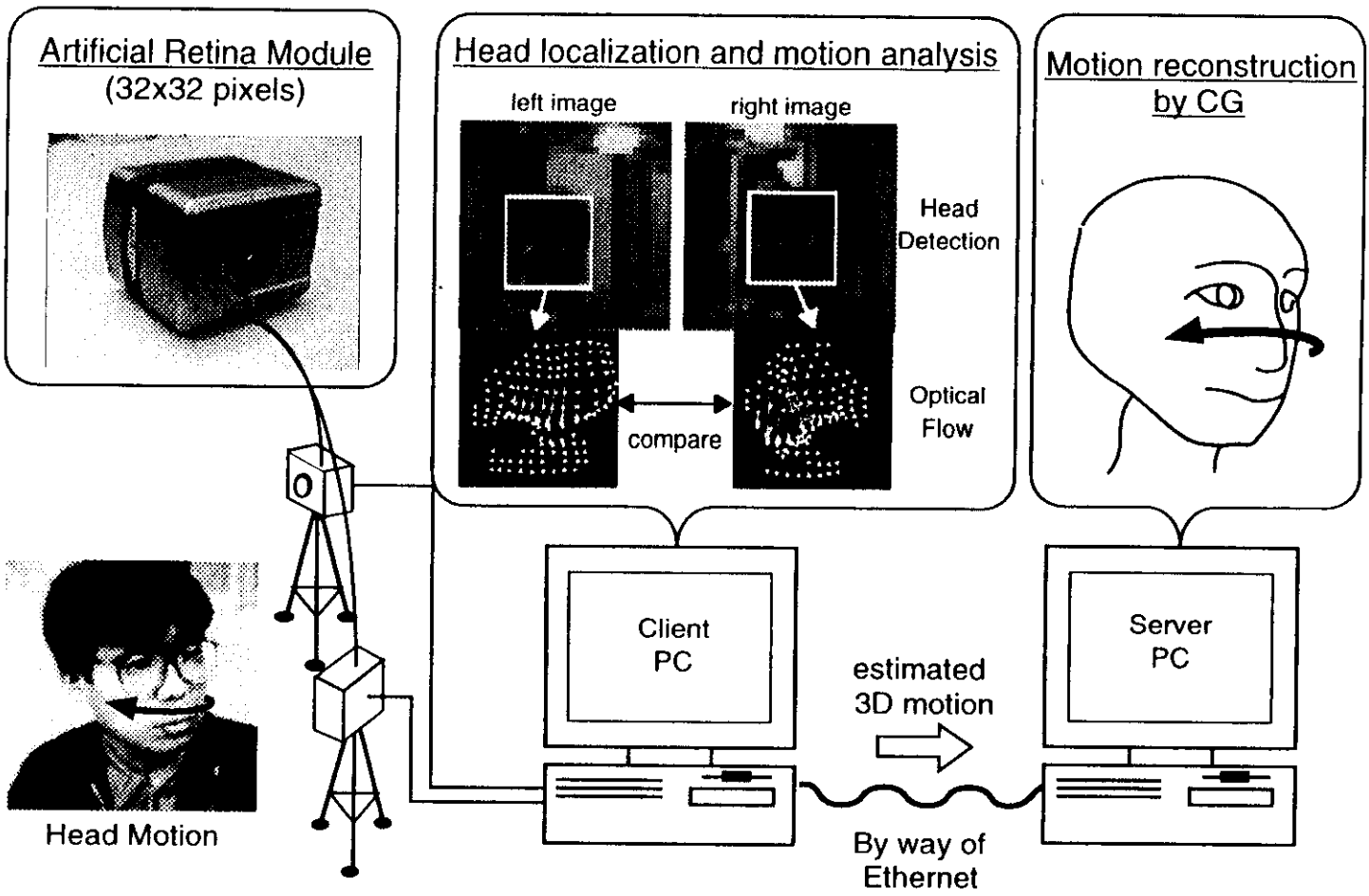
Types	Features
Image Shapes Analysis Model	• Analyze image shapes (Center of gravity, size, tilt angle, etc.) • Advantage of requiring only limited computing power
Image Movements Analysis Model	• Analyze image movements (direction & speed) • Being little affected by background

AR: Interactive Game



AR: 3-D Motion Tracking System

Goal: automatic motion recognition and computer generated reconstruction in real time (immersion).



Challenges and Chances

- Bottleneck turned inside out: computer network data transfer rates are beginning to exceed bus transfer rates (gigabit connections over copper wire).
- Shrinking devices: basically an advantage
  - Improves fill factors and/or processing functionality.
  - High-resolution active pixel sensors require $< 0.5\,\mu$m technology.

  But: below $< 0.25\,\mu$m technology, modifications of the CMOS process will be necessary (otherwise too low sensitivity).

Outlook

Possibilities for applying and designing vision chips:

- Collaboration with one of the research groups working on vision chips (c. f. listing in [Moin 97]) from biologically inspired chips to optically inspired chips?
- Wait for commercial availability of vision chips — for example, chip/memory/processor combinations (M32: 2Mbyte memory plus processor).

Reviews and collections: See [Koch 94] (paper collection) and [Moin 97] (200 page online review).

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