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Fifth Course on Basic VLSI Design Techniques

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ANALOGUE VLSI DESIGN

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Notes on Analogue VLSI Design

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Most of the presented material has been extracted from "CMOS Analog Circuit Design" by P. E. Allen & D.R.Holberg

Course outline

1. The pn junction
2. Direct current in the junction
3. The MOS transistor

4. Passive components
5. CMOS large-signal model
6. CMOS small-signal model

7. Devices and models in SPICE for CMOS
8. Current mirrors and voltage references
9. Simple amplifiers
10. Design case

1. The pn junction

•The ***pn junction*** plays a fundamental role in all semiconductor devices.

•A pure intrinsic silicon crystal is made as a tridimensional array of atoms: ***crystal lattice***.

•Atoms are held in place by the ***valence electrons*** that form bonds among the atoms.

•At zero absolute temperature all these electrons are frozen firmly in place. At room temperature the lattice vibrates and this ***thermal motion*** makes some electrons loose from the parent atom.

•They then become ***free electrons*** that can move across the crystal.

•Each free electron leave a ***hole*** in the parent atom and the atom next to it could supply a valence electron to fill that hole and the next to next could do the same.

•As a result we can think to a ***moving hole*** that carries a positive charge.

•When a wondering around electron meets a wondering around hole they annihilate; this is called ***recombination.***

•The volume concentration of free electrons and holes in the intrinsic silicon are equal

$$n_i = n_p = 1.45 \cdot 10^{10}\ \mathrm{cm}^{-3}$$

•Because there are $5 \cdot 10^{22}\ \mathrm{cm}^{-3}$ atoms in a silicon crystal only **3** out of every **10 13** of these atoms contribute to an electron-hole pair. Electrons and holes are called ***carriers***.

•It is possible to make the number of free electrons different from that of the holes inserting foreign atoms, ***impurities***, in the lattice crystal.

•This process is called ***doping*** and the crystal becomes then ***extrinsic***.

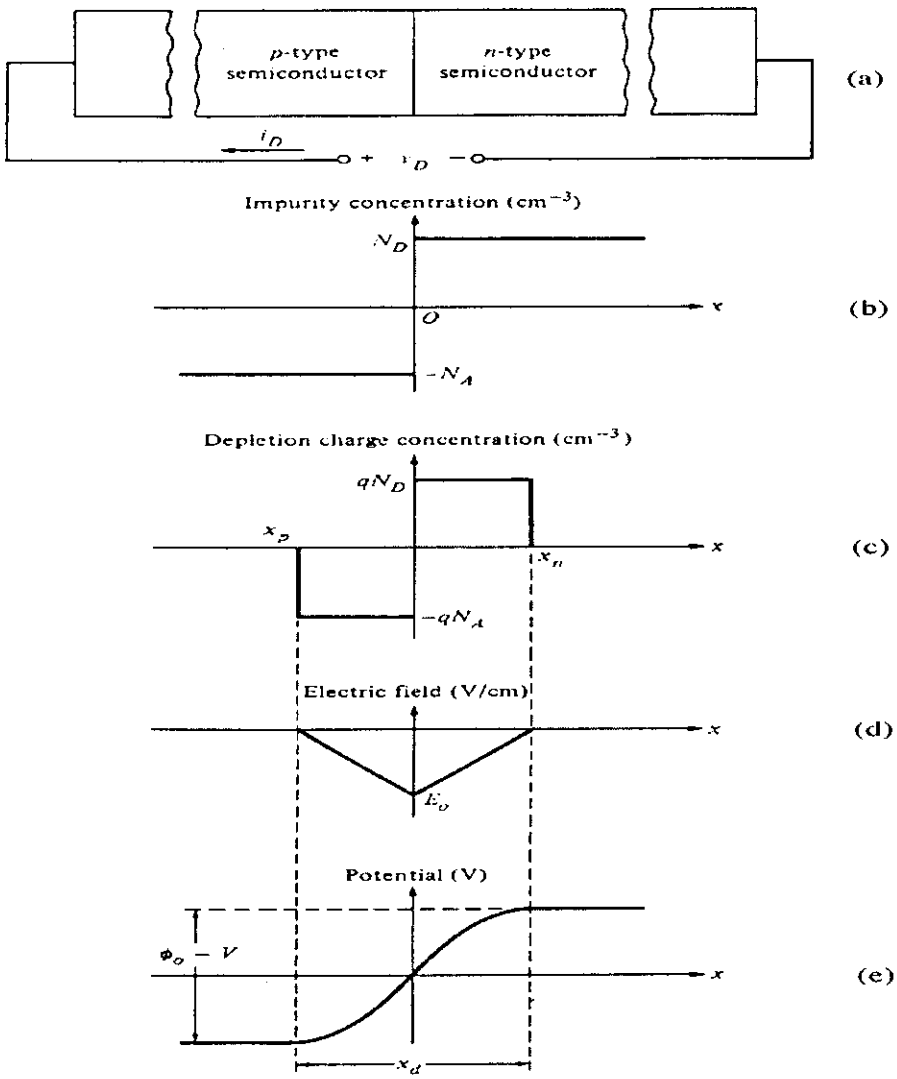
•To enrich the population of free electrons, the dopant is chosen to have one electron more than those required to bond to the neighborough atoms in the crystal.

•The dopant atoms in this case are called ***donors*** (phosphorous, arsenic, antimony) and the extrinsic silicon is ***n-type***. Electrons are ***majority*** cariers and hole ***minority.***

•To enrich the population of holes, atoms with one electron less than those required for perfect bonding are inserted.

•The dopant atoms in this case are called ***acceptors*** (boron, gallium, indium) and the extrinsic silicon is ***p-type***. Holes are ***majority*** cariers and electrons ***minority.***

•The donor ***concentration*** is called N_D, while the acceptor concentration is called N_A. They are several order of magnitude higher than n_i.



- Typically there are one donor or acceptor atom out of every **10^8** atoms of silicon.

- In the figure a physical model of a ***pn junction*** is given. We assume that the impurity concentration changes abruptly from N_D, donors in n-type, to N_A, acceptors in p-type.

- This is called ***step junction***.

- When the junction is formed, the two types of carriers ***diffuse*** across the junction.

- It should be noted that diffusion takes place everytime there is a different ***concentration*** of particles or a gradient in the concentration and it does not imply any electric field (smoke in the air, color in the water etc.).

- When electrons diffuse across the junction they leave positive charged donors, near the junction, $q \cdot N_D$. Similarly holes leaving the p side, generate a charge $-q \cdot N_A$ negative near the junction.

- Due to these charges of opposite sign but same in absolute value, an electrical field E_0 is created that tends to cause an opposite carrier movement (***drift current***) of free electrons and holes.

•When the current due to the free carrier diffusion equals the drift current due to E_0

the junction is in equilibrium with $V_D = 0$ and $i_D = 0$.

•The ***depletion region, x_d***, is defined as the region around the juction which is depleted of free carriers:

$$x_d = x_n - x_p \tag{1.1}$$

Because of electrical neutrality:

$$qN_D x_n = -qN_A x_p \tag{1.2}$$

where $q = 1.6 \cdot 10^{-19}$ **C**, electron charge.

•From Gauss' law:

$$E_0 = \frac{qN_A x_p}{\varepsilon_{Si}} = -\frac{qN_D x_n}{\varepsilon_{Si}} \tag{1.3}$$

where ε_{Si} is the ***dielectric constant*** of Si: $\varepsilon_{Si} = 11.7 \bullet \varepsilon_0$ where $\varepsilon_0 = 8.85 \bullet 10^{14}$**F/cm.**

•The voltage is found by integrating:

$$\phi_0 - V_D = \frac{-E_0(x_n - x_p)}{2} \qquad (1.4)$$

where V_D is the externally applied voltage. ϕ_0 is the ***barrier potential*** and is given as

$$\phi_0 = \frac{kT}{q} \cdot \ln \frac{N_A N_D}{n_i^2}$$

$$= V_t \cdot \ln \frac{N_A N_D}{n_i^2} \qquad (1.5)$$

where $k = 1.38 \cdot 10^{-23}$ **J/°K** is the Boltzmann constant and n_i is the intrinsic concentration of Si. V_t at 300°K is **25.9 mV**.

•From (1.2), (1.3) and (1.4) we get:

$$x_n = \left[\frac{2\varepsilon_{Si}(\phi_0 - V_D)N_A}{q\,N_D(N_A + N_D)} \right]^{1/2} \tag{1.6}$$

$$x_p = -\left[\frac{2\varepsilon_{Si}(\phi_0 - V_D)N_D}{q\,N_A(N_A + N_D)} \right]^{1/2} \tag{1.7}$$

and then:

$$x_d = \left[\frac{2\varepsilon_{Si}(\phi_0 - V_D)(N_A + N_D)}{qN_A N_D}\right]^{1/2}$$

$$= \left[\frac{2\varepsilon_{Si}(N_A + N_D)}{qN_A N_D}\right]^{1/2} \cdot (\phi_0 - V_D)^{1/2} \qquad (1.8)$$

•From (1.8) we understand that the depletion width is proportional to the square root of the difference between barrier potential and externally applied voltage. x_d extends with the junction inverse biasing.

•We see also that:

$x_d \approx x_n$ if $N_A >> N_D$
or
$x_d \approx x_p$ if $N_D >> N_A$.

That means that the depletion region will extend further into the lightly doped semiconductor than it will into the heavily doped semiconductor.

•We also define the depletion charge that is equal to the magnitude of the fixed charge on either side of the junction:

$$Q_j = |A\,q\,N_A x_p| = A\,q\,N_D x_n$$

$$= A \cdot \left[\frac{2\varepsilon_{Si} q N_A N_D}{N_A + N_D}\right]^{1/2} \cdot (\phi_0 - V_D)^{1/2} \qquad (1.9)$$

where ***A*** is the cross section area of junction in **cm²**.

•Substituting (1.6) or (1.7) in (1.3) we get:

$$E_0 = \left[\frac{2qN_A N_D}{\varepsilon_{Si}(N_A + N_D)}\right]^{1/2} \cdot (\phi_0 - V_D)^{1/2} \qquad (1.10)$$

•(1.8), (1.9) and (1.10), here summarized, are the key relations to understand the pn junction

$$x_d = \left[\frac{2\varepsilon_{Si}(N_A + N_D)}{qN_A N_D}\right]^{1/2} \cdot (\phi_0 - V_D)^{1/2} \qquad (1.8)$$

$x_d \approx x_n$* if *$N_A >> N_D$*, *$x_d \approx x_p$* if *$N_D >> N_A$

$$Q_j = A \cdot \left[\frac{2\varepsilon_{Si} q N_A N_D}{N_A + N_D} \right]^{1/2} \cdot (\phi_0 - V_D)^{1/2} \quad \textbf{(1.9)}$$

$$E_0 = \left[\frac{2qN_A N_D}{\varepsilon_{Si}(N_A + N_D)} \right]^{1/2} \cdot (\phi_0 - V \quad \textbf{(1.10)}$$

.

•The depletion region of a pn junction forms a capacitance called depletion-layer capacitance. Its value can be found by (1.11):

$$C_j = \frac{dQ_j}{dV_D} = A \cdot \left[\frac{\varepsilon_{Si} q N_A N_D}{2(N_A + N_D)} \right]^{1/2} \cdot \frac{1}{(\phi_0 - V_D)^{1/2}}$$

$$= \frac{C_{j0}}{[1 - (V_D / \phi_0)]^m} \quad (1.11)$$

where $C_j = C_{j0}$ at $V_d = 0$ and m is the grading coefficient.
$m = 1/2$ for step junction, in practice
$m = 1/3 \div 1/2$.

Exercise

Let's calculate x_p, x_n, x_d, ϕ_0, C_{j0}, and C_j at Vd = -4V, ambient temperature, for a step junction:
being $N_A = 5 \cdot 10^{15}$ cm^{-3}, $N_D = 10^{20}$ cm^{-3}, A = 10 • 10 μm^2.
We know that if $N_D >> N_A$ then:

$$x_d = x_p = -\left[\frac{2\varepsilon_{Si}(\phi_0 - V_D)}{q N_A}\right]^{1/2}$$

where

$$\phi_0 = 25.9 \cdot 10^{-3} \cdot \ln \frac{5 \cdot 10^{35}}{(1.45)^2 \cdot 10^{20}}$$

$$= 917 \text{ mV}$$

$$x_p = x_d = \left[\frac{2 \cdot 11.7 \cdot 8.85 \cdot 10^{-14} \cdot 4.917}{1.6 \cdot 10^{-19} \cdot 5 \cdot 10^{15}}\right]^{1/2}$$

$$= 1.128 \, \mu\text{m}$$

$$C_j = A\left[\frac{\varepsilon_{Si} q N_A}{2}\right]^{1/2} \frac{1}{(4.917)^{1/2}}$$

$$= 10^{-6}\left[\frac{11.7 \cdot 8.85 \cdot 10^{-14} \cdot 1.6 \cdot 10^{-19} \cdot 5 \cdot 10^{15}}{2 \cdot 4.917}\right]^{1/2}$$

$$= 9.178 \cdot 10^{-15} \text{ F}$$

$$C_{j0} = 9.178 \cdot 10^{-15}\left[1 + \frac{4}{0.917}\right]^{1/2}$$

$$= 21.25 \cdot 10^{-15} \text{ F}$$

•The voltage breakdown of a reverse biased ($V_d < 0$) junction is determined by the maximum electric field that can exist across the depletion region.
For silicon the maximum electric field is about:

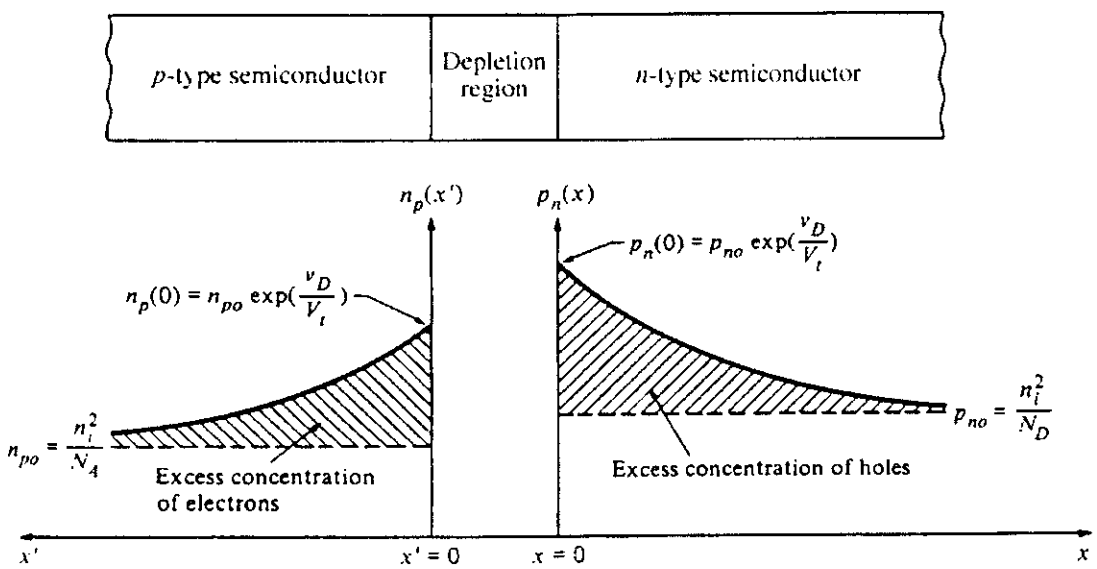
$$Emax \approx 300 \text{ kV/cm}$$

•We can use the (1.10) where $V_d < 0$, much larger than ϕ_0, to compute the breakdown voltage in the same case of the previous exercise:

$$V_{D_{breakdown}} = E_{max}^2 \cdot \frac{\varepsilon_{Si}(N_A + N_D)}{2q\,N_A\,N_D} \approx 58.2 \text{ V}$$

2.Direct current in the junction

- The total current of direct biased junction is



Minority carrier concentrations in a forward-biased pn junction.

made of four components: holes and electrons ***drift currents*** and hole and electrons ***diffusion currents*** . In our analysis we assume that V_d is sustained entirely at the junction.

- Then the total junction voltage will be $(\phi_0 - V_d)$. In forward bias $V_d > 0$, so the applied voltage reduces the barrier to the

diffusion flow of ***majority carriers*** at the junction.

•The reduced barrier permits transfer of holes from p-side to n-side and electrons from n-side to p-side.

•When these carriers enter the quasi-neutral region they become ***minority carriers*** and they are quickly neutralised by the majority carriers entering from ohmic contacts.

•The majority carriers act only as suppliers of minority carriers current or as neutralisers in the quasi-neutral region.

•The excess of minority carriers concentration on each side of the junction is shown by the curves. The concentration starts at a maximum and decreases to the value n_{p0} or p_{n0} that are the equilibrium concentrations of the ***minority*** carriers in the p-type and n-type semiconductors.

•The equilibrium concentration can be evaluated according to the following

considerations; as the free electrons concentration increases the chance of recombination with a hole increases. The hole concentration decreases by the same factor.

•Hence the product $p_{n0} \bullet N_D$, in the n-type, remains the same as in the intrinsic case, n_i^2, where $p_i = n_i$. The same applies to the product $n_{p0} \bullet N_A$, in the p-type.

•Then

$$p_{n0} \bullet N_D = n_i^2 \quad \text{and}$$

$$p_{n0} = n_i^2 / N_D \qquad (2.1)$$

$$n_{p0} N_A = n_i^2 \quad \text{and}$$

$$n_{p0} = n_i^2 / N_A \qquad (2.2)$$

.

•As V_d is increased, the excess minority concentration is increased. For $V_d = 0$ there is no excess, for $V_d < 0$ the minority

carrier concentration is depleted below its equilibrium value.

•The current that flows in the junction is proportional to the slope at ***x = 0***

$$J_p(x) = -qD_p \left.\frac{\partial p_n}{\partial x}\right|_{x=0} \qquad (2.3)$$

$$J_n(x) = qD_n \left.\frac{\partial n_p}{\partial x}\right|_{x=0} \qquad (2.3a)$$

being

$$p_n(0) = p_{n0} \cdot e^{V_D/V_t} \qquad (2.4)$$
$$n_p(0) = n_{p0} \cdot e^{V_D/V_t}$$

and D_p and D_n are the ***diffusion constants*** of the hole in n-type and electron in p-type.

•The diffusion constants are related to the mobility μ by the Einstein relationship $D=\mu V_t$, where mobility is constant of

proportionality between the electric field and the carrier velocity $\boldsymbol{v_d = \mu E}$.

- With some manipulation we get that

$$I_D = qA\left[\frac{D_p p_{n0}}{L_p} + \frac{D_n n_{p0}}{L_n}\right](e^{VD/Vt} - 1)$$

$$= I_S(e^{VD/Vt} - 1) \approx I_S \cdot e^{VD/Vt}$$

where $\boldsymbol{L_p}$ and $\boldsymbol{L_n}$ are the diffusion lengths for holes in n-type and electrons in p-type.

Example

Let's calculate I_S, saturation current, using the (2.3), for a junction where
$N_A = 5 \cdot 10^{15}$ cm^{-3}, $N_D = 10^{20}$ cm^{-3}
$D_n = 20$ cm^2/s, $D_p = 10$ cm^2/s, $L_n = 10 \cdot 10^{-4}$ cm, $L_p = 5 \cdot 10^{-4}$ cm
and
A = $1000 \cdot 10^{-8}$ cm^2.

$$I_S = 1.6 \cdot 10^{-19} \left[\frac{10 p_{n0}}{5 \cdot 10^{-4}} + \frac{20 n_{p0}}{10 \cdot 10^{-4}} \right] \cdot 10^{-5}$$

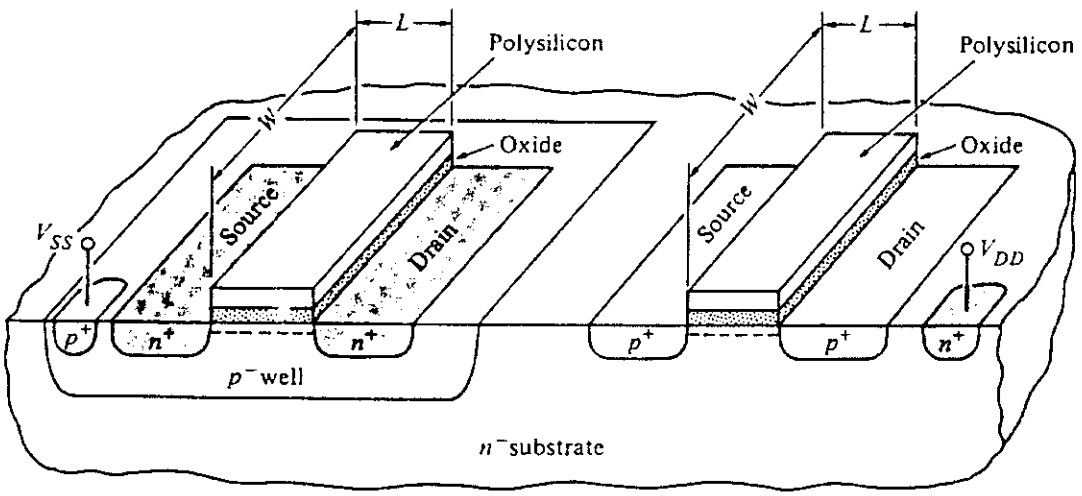
$$n_{p0} = \frac{n_i^2}{N_A} = \frac{(1.45)^2 \cdot 10^{20}}{5 \cdot 10^{15}} = 4.2 \cdot 10^4$$

$$p_{n0} = \frac{n_i^2}{N_D} = \frac{(1.45)^2 \cdot 10^{20}}{10^{20}} = 2.1$$

$$I_S = 1.34 \cdot 10^{-15} \text{ A}$$

3.The MOS transistor

•The physical structure of n-channel and p-channel MOS, using ***p-well technology*** is shown in the figure.



Physical structure of an NMOS and PMOS transistor in a p-well, CMOS technology.

p⁻ and ***n⁻*** means lightly doped while ***p⁺*** and ***n⁺*** means heavily doped silicon.

•The substrate, either well or bulk, form a junction with source and drain. Because source and drain are separated by two inverse junctions the resistance in between is of the order of $10^{12}\ \Omega$. The gate and the

substrate are separated by SiO_2 and form a capacitance whose value is $C_{ox}\ L\ W$. Assuming to consider the n-type MOS, at the left in the figure, when a voltage is applied to the gate (positive) the positive charges of the p^- substrate are pushed away, that is equivalent to a negative charge created underneath the gate.

•The mobile charge ***dQ*** of holes originally contained in an infinitesimal horizontal layer of p-type material below the gate is given by

$$dQ = q(-N_A)\, dx_d \tag{3.1}$$

the change in potential required to displace the charge is

$$d\phi_S = -x_d\, dE = -x_d \frac{dQ}{\varepsilon_{Si}}$$

that substituting (3.1), becomes

$$d\phi_S = \frac{x_d\, q\, N_A\, dx_d}{\varepsilon_{Si}} \qquad (3.2)$$

that can be easily integrated

$$\phi_S = \frac{x_d{}^2\, q\, N_A}{2\varepsilon_{Si}} + \phi_F \qquad (3.3)$$

where the integration constant ϕ_F is the equilibrium electrostatic potential that for p-type is

$$\phi_F = V_t \cdot \ln \frac{n_i}{N_A} \qquad (3.4)$$

and for n-type is

$$\phi_F = V_t \cdot \ln \frac{N_D}{n_i} \qquad (3.5)$$

•Assuming $\phi_S \geq \phi_F$ the (3.3) can be used to compute x_d

$$x_d = \left[\frac{2\varepsilon_{Si}|\phi_S - \phi_F|}{q N_A} \right]^{1/2} \tag{3.6}$$

From (3.1), the immobile charge of the acceptor ions stripped of their mobile holes is

$$Q = -q\, N_A\, x_d \tag{3.7}$$

where x_d is the thickness of depleted region. Combining (3.6) and (3.7) we get

$$Q = -q\, N_A \left[\frac{2\varepsilon_{Si}|\phi_S - \phi_F|}{q N_A} \right]^{1/2}$$

$$= -\sqrt{2q\, N_A\, \varepsilon_{Si}|\phi_S - \phi_F|} \tag{3.8}$$

•When the gate voltage reaches a value called ***threshold voltage*** , V_T, the substrate underneath becomes inverted. Consequently a (p/n) channel exists between source and drain that allows carriers to flow. This phenomenon is

known as ***strong inversion*** . In order to achieve this inversion the surface potential must increase from its original negative value to a positive value. The value of gate-source voltage necessary to cause this change in surface potential is the threshold voltage.
The threshold voltage will be discussed in some more detail, dealing with CMOS models.

4. Passive components

•The value of integrated capacitors is given by

$$C = \frac{\varepsilon_{ox} A}{t_{ox}} = C_{ox} A$$

where ε_{ox} is the dielectric constant of silicon dioxide ($\approx 3.45 \bullet 10^{-5}$ pF/μm), t_{ox} is the thickness and A is the area of capacitor.

•It is always desirable that ratios of capacitors rather than absolute capacitor values define circuit performance.

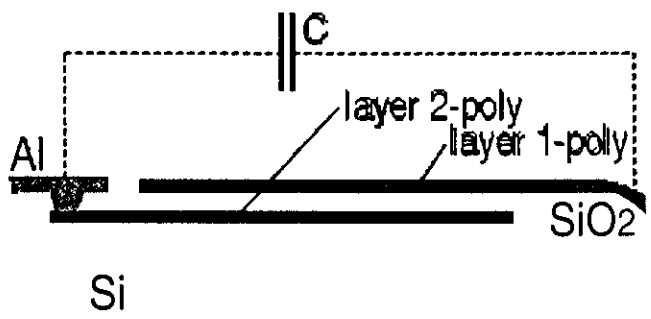
•In order to match two capacitors as precisely as possible, it is desirable that the errors associated with each are also matched.

•Let C_1' be defined as

$$C_1' = C_1 \pm \Delta C_1$$

and C_2'

$$C_2' = C_2 \pm \Delta C_2$$



•The ratio of C_2' to C_1' can be expressed as

$$\frac{C_2'}{C_1'} = \frac{C_2 \pm \Delta C_2}{C_1 \pm \Delta C_1}$$
$$= \frac{1 \pm \Delta C_2/C_2}{1 \pm \Delta C_1/C_1} \cdot \frac{C_2}{C_1}$$
$$\approx \frac{C_2}{C_1}$$

that is true if the errors of C_1 and C_2 are the same.

•In general it is desirable to obtain capacitor ratios using the same "***unitary***" capacitor. For instance the ratio

$$3.5 = \frac{3.5\ \text{pF}}{1\ \text{pF}} = \frac{7 \cdot 0.5\ \text{pF}}{2 \cdot 0.5\ \text{pF}}$$

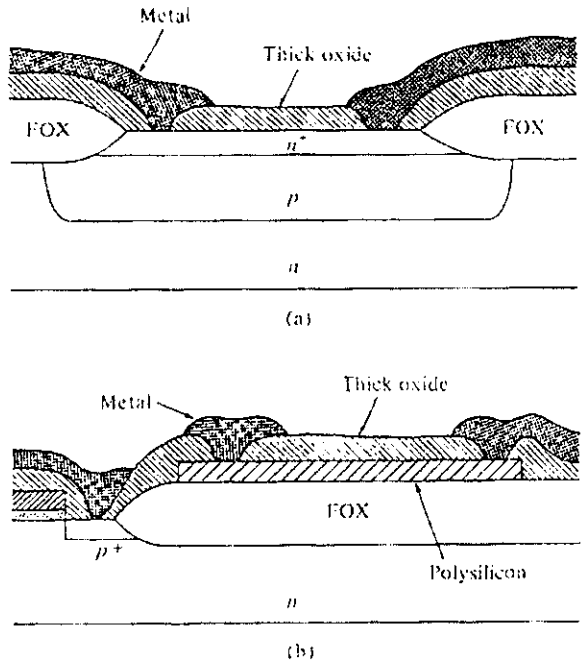
or

$$3.7 = \frac{6 \cdot 0.5\ \text{pF} + 0.7\ \text{pF}}{2 \cdot 0.5\ \text{pF}} .$$

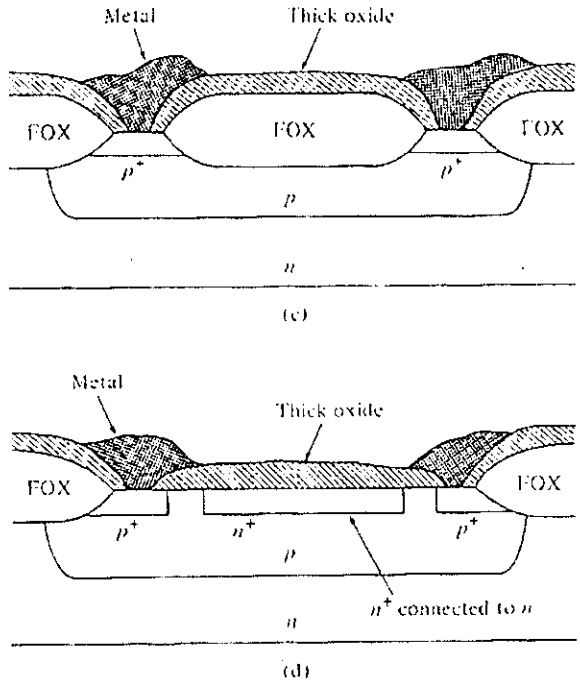
- The ***tempco*** of these capacitors is in the range of 20÷50 ppm/°C while the voltage coefficient is in the range of -10 to -200 ppm/V.

- The other passive component compatible with MOS technology is the ***resistor*** . Even though we shall use primarily circuits containing only MOS active devices and capacitors, some applications use the resistor.

Resistors compatible with MOS technology include:
diffused, ***polysilicon***, ***p-well*** (or ***n-well***) and ***pinched resistors***.



Resistors. (a) Diffused. (b) Polysilicon. (c) P-well. (d) Pinched



Approximate Performance Summary of CMOS Passive Components.

Component Type	Range of Values	Relative Accuracy	Temperature Coefficient	Voltage Coefficient	Absolute Accuracy
Poly/poly capacitor	0.3-0.4 fF/μ^2	0.06%	25 ppm/°C	50 ppm/V	20%
MOS capacitor	0.35-0.5 fF/μ^2	0.06%	25 ppm/°C	20 ppm/V	10%
Diffused resistor	10-100 ohms/sq.	2% (5 μm width)	1500 ppm/°C	200 ppm/V	35%
Poly resistor	30-200 ohms/sq.	2% (5 μm width)	1500 ppm/°C	100 ppm/V	30%
Ion impl resistor	0.5-2k ohms/sq.	1% (5 μm width)	400 ppm/°C	800 ppm/V	5%
p-well resistor	1-10k ohms/sq.	2%	8000 ppm/°C	10k ppm/V	40%
pinch resistor	5-20k ohms/sq	10%	10k ppm/°C	20k ppm/V	50%

- The ***sheet resistance*** of **diffused** is in the range of 10 to 100 ohm/square.

Polysilicon has a sheet resistance of 30 to 600 ohm/square and can be trimmed (laser trimming).

The ***p-well*** (or n-well) have high sheet resistance (1 to 10 Kohm/square) but poor accuracy.

Pinched resistors are some like JFET with gate tied to a positive supply (in the case of the figure being n^+ connected to n^-).They require proper modeling.

5. CMOS LARGE-SIGNAL MODEL

•Modeling is defined as the process by which the electrical properties of a semiconductor device or a group of interconnected devices (active and passive) are represented by means of mathematical equations or tables.

•***"A model is an artifice that gives one the illusion of knowing more about a process than one actually does"*** (Alva Archer from Datel Linear).

•The primary application of a ***large-signal model*** is to simulate or solve the large-signal behavior, that includes the ***biasing*** of the active devices.

•Once the bias points have been established, a ***small-signal model*** can be used to determine the small-signal performance.

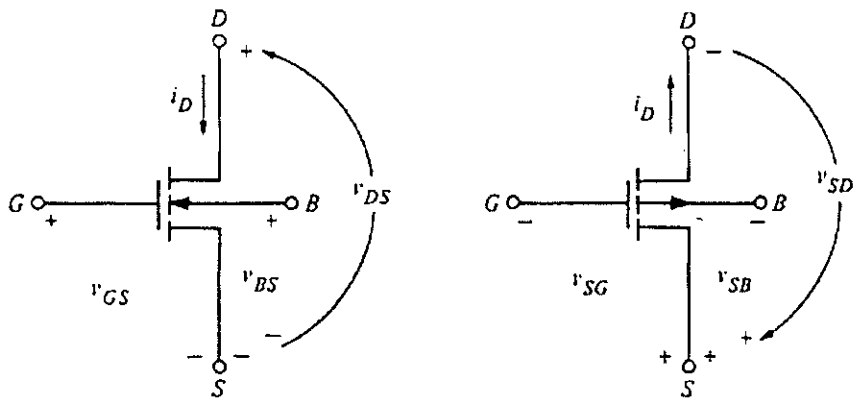
•Since most of the parameters of the small-signal model depend on the large-signal

voltages and currents (biasing), the small-signal model depends heavily upon the large-signal variables.

•A large-signal model, for ***strong inversion*** (***saturation region***), that includes ***second-order effects*** is presented next.
Second order effect are required to increase the accuracy in many cases as short-channel devices or high currents.

•When operating in ***sub-treshold*** region the strong inversion model is not accurate anymore.
Sub-threshold operation is suitable for extremely low power circuits. This subject will not be presented here.

•All large-signal models will be developed for the n-channel MOS device with positive polarities as shown in the following figure, part *a*. The same model can be use for p-channel MOS device if all voltages and currents are multiplied by -1, and the absolute value of the p-channel is used. This is equivalent to use voltages and currents as in the part *b* of the figure.



Positive sign convention for (a) n-channel, and (b) p-MOS transistor.

•Lower case variables, with capital subscripts, will be used for the large-signal models, and lower-case variables with lower-case subscripts will be used for the variables of small-signal models. When a current or a voltage is a ***model parameter*** it will be designated by an upper-case variable and an upper-case subscript. When the length and width of the MOS device is grater than 10μm and the substrate doping is low, the model suggested by Sah (also used in SPICE) is very appropriate.

•The i_D is described by the following relationresult is

$$i_D = \frac{\mu_o C_{ox} W}{L}\left[(v_{GS} - V_T) - v_{DS}/2\right] v_{DS}(1 + \lambda v_{SD}) \qquad (5.1)$$

where:

μ_o = surface mobility of the channel ($cm^2/V \cdot s$),

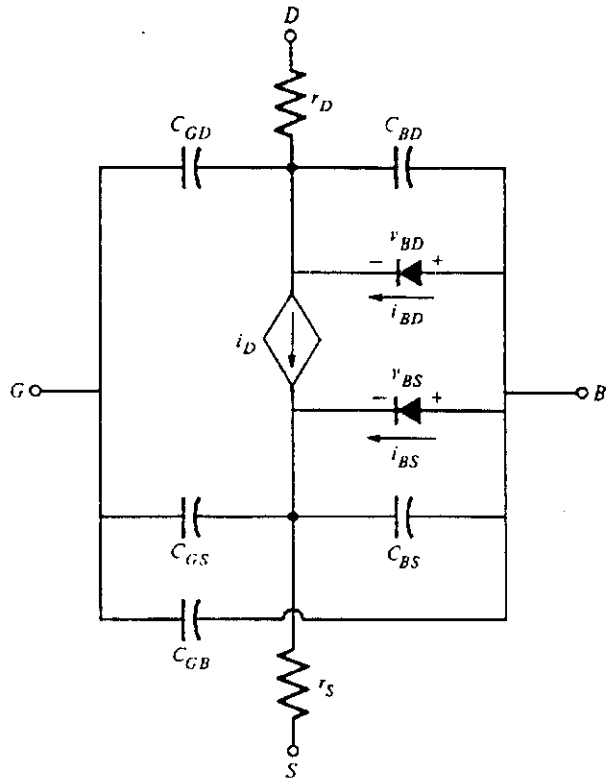
$C_{ox} = e_{ox}/t_{ox}$ = capacitance per unit areas of the gate oxide (F/cm^2),

W = effective channel width,

L = effective channel length,

l = channel length modulation parameter (V^{-1}),

V_T is the ***threshold voltage***.



Complete large-signal model for the MOS transistor.

- The ***threshold voltage*** is given as V_{T0}, as a typical process parameter, in the case of $V_{BS} = 0$, that is the most usual case in most applications.

- In the realm of circuit design it is more desirable to express the i_D in terms of electrical parameters rather than physical parameters. For this reason the (5.1) becomes

$$i = \beta\left[\left(v_{GS} - V_T\right) - \left(v_{DS}/2\right)\right]v_{DS}\left(1 + \lambda v_{DS}\right) \tag{5.2}$$

where

$$\beta = K' \frac{W}{L} \cong (\mu_o C_{ox}) \frac{W}{L} \qquad (5.3)$$

K' is called ***transconductance parameter*** and is normally given as a model parameter.

It is equal to $\mu_o C_{ox}$, only in non saturated region, in saturated region, is usually smaller. ***K'*** is given in $\mu A/V^2$.

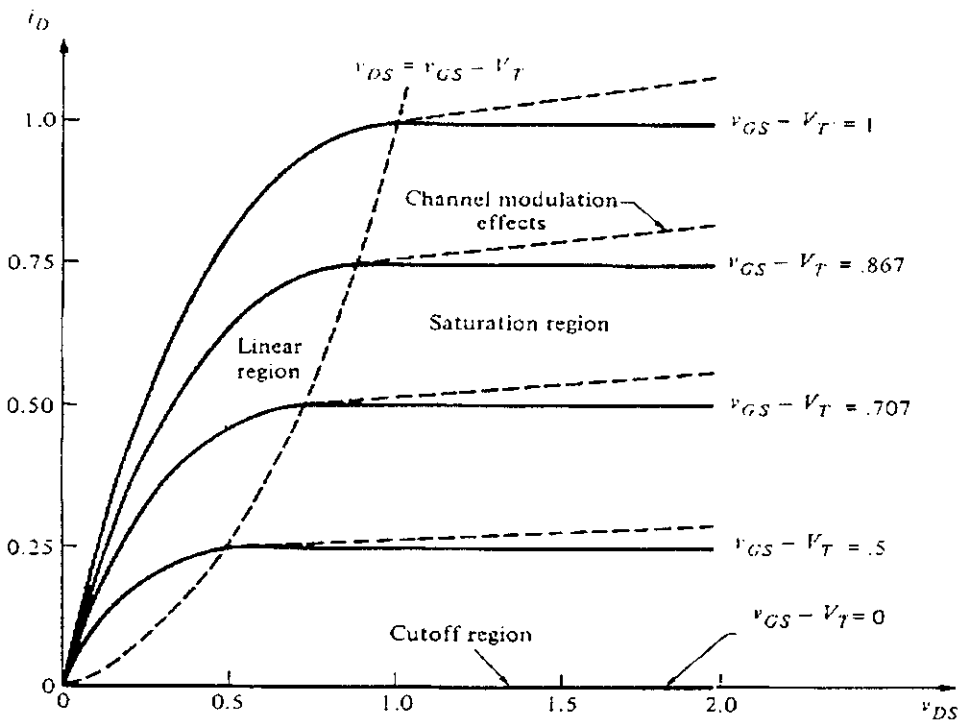
•The saturation region begins as soon as

$$v_{DS(sat)} = v_{GS} - V_T \qquad (5.4)$$

therefore replacing in (5.2) v_{DS} defined as in (5.4), but leaving the terms that accounts for channel-length modulation, we get

$$i_D = K' \frac{W}{2L} (v_{GS} - V_T)^2 (1 + \lambda v_{DS}) \qquad (5.5)$$

•In the saturation region the i_D is independent from v_{DS}, except for the channel-length modulation, that somehow reminds the Early effect in bipolar transistors. The i_D, v_{DS} characteristic is shown in the figure.



Output characteristics of the MOS device.

Example

Assume that two MOS transistors, one n-type and another p-type, have a *W/L* ratio of 100μm/10μm and the large signal model parameters are those give in the table, let's find the i_D current in the case that drain, gate, source, and bulk voltages of NMOS is 5V, 3V, 0V,and 0V while the ones for PMOS are the same with opposite sign.

From (5.4) we get that

$$v_{DS\,(sat)} = v_{GS} - V_{T0} = 3V - 1V = 2V$$

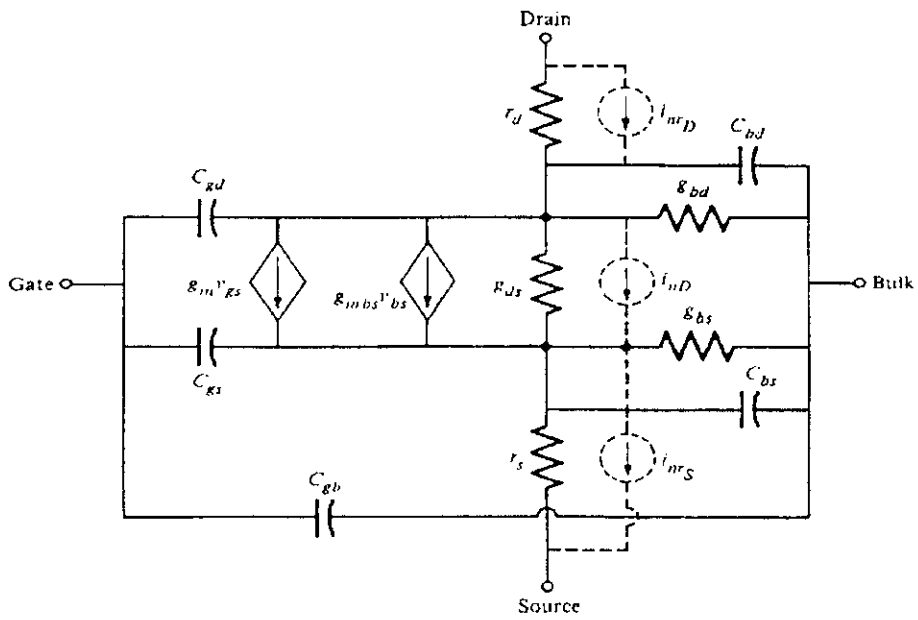
Since v_{DS} is 5V, the transistor operates in saturation region then using the (5.5) and the values in the table:

$$\begin{aligned} i_D &= K' \frac{W}{2L}(v_{GS} - V_T)^2(1 + \lambda v_{DS}) \\ &= \frac{17 * 10^{-6} * 100}{2 * 10}(3-1)^2(1 + .01 * 5) \\ &= 357\mu A \end{aligned}$$

Also the PMOS is in saturation, so we get:

$$\begin{aligned} i_D &= K' \frac{W}{2L}(v_{SG} - V_T)^2(1 + \lambda v_{SD}) \\ &= \frac{8 * 10^{-6} * 100}{2 * 10}(3-1)^2(1 + .02 * 5) \\ &= 176\mu A \end{aligned}$$

6. CMOS SMALL-SIGNAL MODEL



Small-signal model of the MOS transistor.

- The figure shows a small-signal model for MOS transistor at low frequency. Remind that small-signal parameters will have lower case subscripts.

- The small signal parameters are defined in terms of the ***ratio of small perturbations of the large-signal variables*** or as ***partial differentiation of one large-signal variable with respect to another***.

•The channel conductances, g_m, g_{mbs}, and g_{ds} are defined as

$$g_m = \frac{\partial i_D}{\partial v_{GS}} \tag{6.1}$$

$$g_{mbs} = \frac{\partial i_D}{\partial v_{BS}} \tag{6.2}$$

$$g_{ds} = \frac{\partial i_D}{\partial v_{DS}} \tag{6.3}$$

calculated at quiescent point.
Eventually

$$gbd = \partial i_{BD}/\partial v_{BD} \approx 0$$

$$gbs = \partial i_{SB}/\partial v_{SB} \approx 0$$

being bulk to drain and bulk to source junctions normally reverse biased.

•The (6.1) can be derived from (5.5), then substituting to i_D, I_D and to v_{DS}, V_{DS} as we consider small perturbations, given a certain operating point.

$$g_m = \frac{\partial i_D}{\partial v_{gs}}$$

$$= \frac{K' W}{2L} 2(v_{GS} - V_T)(1 + \lambda v_{DS})$$

$$= \sqrt{2K' W/L}\sqrt{I_D}\sqrt{1 + \lambda V_{DS}}$$

$$\cong \sqrt{I * (2K' W/L)} \qquad (6.1a)$$

If we rewrite the (6.2) as

$$g_{mbs} = \frac{-\partial i_D}{\partial v_{SB}} = -\frac{\partial i_D}{\partial V_T}\frac{\partial V_T}{\partial v_{SB}}$$

remembering that we said that V_T is a function of the bulk-source voltage and noting that

$$\frac{\partial i_D}{\partial v_{GS}} = -\frac{\partial i_D}{\partial V_T}$$

we get

$$g_{mbs} = g_m \eta \qquad (6.2a)$$

where η is the derivative of V_T that is written as

$$\eta = \frac{\gamma}{2\sqrt{(2\Phi_F + V_{SB})}} \qquad (6.4)$$

where γ, ***bulk threshold*** , and $2 \bullet \Phi_F$, ***surface potential*** at strong inversion, are model parameters (see table).
The (6.3) can be rewritten, deriving (5.5) we get

$$g_{ds} = \lambda I_D \qquad (6.3a)$$

Constants for Silicon.

Constant Symbol	Constant Description	Value	Units
V_{Go}	Silicon bandgap (27°C)	1.205	volts
k	Boltzmann's constant	1.381×10^{-23}	Joules/°K
n_i	Intrinsic carrier concentration (27°C)	1.45×10^{10}	cm^{-3}
ϵ_{si}	Permittivity of silicon	1.0359×10^{-12}	Farads/cm
ϵ_{ox}	Permittivity of SiO_2	3.45×10^{-13}	Farads/cm

Example

Find the values of g_m , g_{mbs} , g_{ds} using the large signal model parameters given in the table for both NMOS and PMOS devices assuming a dc value of the drain current of 50μA and a bulk-source voltage of 5V. The W/L ratio is 1, being W =10μm.
Using (6.1a) we get for NMOS,

Model Parameters for a Typical CMOS Bulk Process Suitable for Hand Calculations Using the Simple Model. These Values Are Based upon a 5 μm Silicon-Gate Bulk CMOS p-Well Process.

Parameter Symbol	Parameter Description	Typical Parameter Value NMOS	PMOS	Units
V_{t0}	Threshold Voltage ($V_{bs} = 0$)	1 ± 0.2	−1 ± 0.2	volts
K'_{sat}	Transconductance Parameter (in saturation)	17.0 ± 10%	8.0 ± 10%	μA/volt²
K'_{nonsat}	Transconductance Parameter (in nonsaturation)	25.0 ± 10%	10.0 ± 10%	μA/volt²
γ	Bulk threshold parameter	1.3	0.6	$(volts)^{1/2}$
λ	Channel length modulation parameter	0.01 (L = 10 μm) 0.004 (L = 20 μm)	0.02 (L = 10 μm) 0.008 (L = 20 μm)	$(volts)^{-1}$
$2\lvert\phi_f\rvert$	Surface potential at strong inversion	0.7	0.6	volts

For PMOS:

$$g_m = \sqrt{I_D(2K' W/L)}$$
$$= \sqrt{50(2*8)}*10^{-6}$$
$$= 28.3\mu A/V$$

From (6.4) we get

$$\eta = \frac{\gamma}{2\sqrt{2\Phi_F + V_{SB}}}$$
$$= \frac{1.3}{2\sqrt{(.7+5)}}$$
$$= .27$$

for NMOS, then, using (6.2a), we get g_{mbs} =11.2 μA/V.
For PMOS we have g_{mbs} = 3.58 μA/V.
Using the (6.3a) we get

$$g_{ds} = I_D\lambda$$
$$= 50*10^{-6}*.01$$
$$= .5\mu A/V$$

(45)

that means an output resistance $r_{ds} = 2M\Omega$ for the NMOS and

$$\begin{aligned} g_{ds} &= I_D \lambda \\ &= 50 * 10^{-6} * .02 \\ &= 1 \mu A / V \end{aligned}$$

that means an output resistance $r_{ds} = 1M\Omega$ for the PMOS.

7. DEVICES AND MODELS IN SPICE FOR CMOS

•For CMOS simulation in SPICE, there are ***devices*** lines (statements), and ***models*** lines (statements).

•The purpose of the ***device*** statement is to identify the device ***name*** , describe the topological ***connections*** of it, identify the ***model*** of the device, that contains the circuit and physical parameters, provide up to 8 ***geometric parameters*** , and 1 device ***multiplier*** which simulates the effect of multiple devices in parallel (default value = 1).

•CMOS device general form is:

M<name>
+<drain node> <gate node>
+<source node> <bulk node>
+<model name>
+[L=<value>] [W=<value>]
+[AD=<value>] [AS=<value>]
+[PD=<value>] [PS=<value>]
+[NRD=<value>] [NRS=<value>]
+[NRG=<value>] [NRB=<value>]
+[M=<value>]

- **M<name>** can be any name that starts with M: eg. M1, MNMOS, MPMOS, M4MOS etc.

L and **W** are channel length and width in meters (default value = 100μm).
AD and **AS** are the drain and source diffusion areas in square meters (default value = 0). They can be calculated according the technology information.
PD and **PS** are drain and source diffusion perimeters in meters (default value = 0).
NRD,and **NRS** (default value = 1), **NRG**, and **NRB** (default value = 0) are the relative resistivities of the drain, source, gate, and substrate in squares.

M is the device multiplier (default value = 1).

•Obviously not all the information can be entered until the device is geometrically defined. In the early phase of simulation only **L** and **W** are entered usually.

•Examples:

```
M1 14 2 13 0 PNOM L=25u W=12u
**********
MSTRONG 15 3 0 0 NSTRONG
**********
MTWICE 15 3 0 0 NSTRONG M=2
**********
MIN 2 3 4 4 NWEAK L=33u W= 12u
+AD=288p AS=288p PD=60u PS=60u
+NRD=14 NRS=24 NRG=10
**********
```

•Model general form

```
.MODEL
+<model name>
+NMOS (or PMOS)
```

+[model parameters]

•The ***model statement*** is preceded by a ***period*** to flag the program that is not a component, then there is the model ***name*** followed by the model ***type*** (NMOS or PMOS). The model ***parameters*** list starts with model ***level*** definition and provides ***electrical*** and ***process*** parameters.

Example
.MODEL MYMOS NMOS
+(LEVEL=1 VTO=.7 BF=30)
****

•The four most popular SPICE models for CMOS differ from the formulation of the I-V characteristic.
The **LEVEL**=1model uses the (5.1) or (5.2) to compute the drain current (large-signal). It is also called Shichman-Hodges model.
LEVEL=2 (Extended Model) and
LEVEL=3 are respectively geometry based analytic model (small-signal), and semi-empirical short-channel model. The

second takes into account ***second order effects*** .
In **Level**=4 or **BSIM** [**B**erkeley **S**hort-channel **I**gfet (isolated gate field effect transistor) model for **M**OS transistor] all parameters are obtained from process characterization.

Unlike the other models **BSIM** is designed for use with a ***process characterization system*** that provides all parameters: most of the SPICEs do not use any default for these parameters.

•The **level 1** parameters, covered in section 5, are the zero-bias threshold voltage **VT0,** the intrinsic transconductance parameter **KP**, the bulk threshold parameter **GAMMA**, the surface potential at strong inversion **PHI**, and the channel length modulation parameter **LAMBDA**. These were in given in the

table repeated here with the proper units.

Model Parameters for a Typical CMOS Bulk Process Suitable for Hand Calculations Using the Simple Model. These Values Are Based upon a 5 μm Silicon-Gate Bulk CMOS p-Well Process.

Parameter Symbol	Parameter Description	Typical Parameter Value NMOS	PMOS	Units
V_{TO}	Threshold Voltage (V_{BS} = 0)	1 ± 0.2	−1 ± 0.2	volts
K'_{sat}	Transconductance Parameter (in saturation)	17.0 ± 10%	8.0 ± 10%	μA/volt²
K'_{nonsat}	Transconductance Parameter (in nonsaturation)	25.0 ± 10%	10.0 ± 10%	μA/volt²
γ	Bulk threshold parameter	1.3	0.6	$(volts)^{1/2}$
λ	Channel length modulation parameter	0.01 (L = 10 μm) 0.004 (L = 20 μm)	0.02 (L = 10 μm) 0.008 (L = 20 μm)	$(volts)^{-1}$
$2\lvert\phi_f\rvert$	Surface potential at strong inversion	0.7	0.6	volts

- Other parameters are included to complete the model at level 1, all depending on the geometrical dimensions (see later).

- As already said the **level 2** requires additional parameters, not discussed so far, to take into account second order effects.

- Level 1 is almost not used while level 2 and 3 are the most used ones. Some examples of real models level 2 and 3 from a very popular process follow. Level 4 is more difficult to find from fundries.

```
*
*     LIBRERIA DI COMPONENTI MOS BRAND_X
* PROCESSO DA 2um ANALOGICO DOPPIO METAL, DOPPIO POLY
*                  ALIMENTAZIONE 5V
*                          2_CUBA BRAND_X
*
*************************************************************
*************************************************************
*         2_CUBA 2um CMOS
*************************************************************
* typical  parameters
*
.MODEL 2_CUBAN NMOS LEVEL=2
+ CGSO  =0.370E-09  CGDO  =0.370E-09  CGBO  =0.064E-09
+ CJ    =0.350E-03  MJ    =0.440E+00  CJSW  =0.150E-09  MJSW  =0.300E+00
+ JS    =0.500E-03  PB    =0.800E+00  RSH   =33.00E+00  XQC   =1E+00
+ TOX   =29.70E-09  XJ    =0.570E-06  LD    =0.303E-06  WD    =0.564E-06
+ VTO   =0.804E+00  NSUB  =26.80E+15  NFS   =1.160E+12  NEFF  =6.310E+00
+ UO    =552.0E+00  UCRIT =21.00E+04  UEXP  =0.181E+00  UTRA  =0.000E+00
+ VMAX  =066.0E+03  DELTA =1.660E+00
*
.MODEL 2_CUBAP PMOS LEVEL=2
+ CGSO  =0.370E-09  CGDO  =0.370E-09  CGBO  =0.064E-09
+ CJ    =0.320E-03  MJ    =0.490E+00  CJSW  =0.150E-09  MJSW  =0.260E+00
+ JS    =0.200E-03  PB    =0.700E+00  RSH   =65.00E+00  XQC   =1E+00
+ TOX   =29.70E-09  XJ    =0.472E-06  LD    =0.313E-06  WD    =0.561E-06
+ VTO   =-.776E+00  NSUB  =12.60E+15  NFS   =1.020E+12  NEFF  =2.560E+00
+ UO    =174.0E+00  UCRIT =20.20E+04  UEXP  =0.245E+00  UTRA  =0.000E+00
+ VMAX  =045.6E+03  DELTA =3.100E+00
*************************************************************
*************************************************************
*
*     LIBRERIA DI COMPONENTI MOS BRAND_X
* PROCESSO DA 2um ANALOGICO DOPPIO METAL, DOPPIO POLY
*                  ALIMENTAZIONE 5V
*                          2_CUBAQ BRAND_X
*
*************************************************************
*************************************************************
*         2_CUBAQ 2um CMOS
*************************************************************
* typical  parameters
*
.MODEL 2_CUBAQN NMOS LEVEL=2
+ CGSO  =0.560E-09  CGDO  =0.560E-09  CGBO  =0.165E-09
+ CJ    =0.400E-03  MJ    =0.500E+00  CJSW  =0.390E-09  MJSW  =0.060E+00
+ JS    =0.020E-03  PB    =0.860E+00  RSH   =30.00E+00  XQC   =1E+00
+ TOX   =31.10E-09  XJ    =0.054E-06  LD    =0.338E-06  WD    =0.644E-06
+ VTO   =0.770E+00  NSUB  =33.10E+15  NFS   =0.293E+12  NEFF  =3.560E+00
+ UO    =582.0E+00  UCRIT =20.90E+04  UEXP  =0.235E+00  UTRA  =0.000E+00
+ VMAX  =86.00E+03  DELTA =0E+00
*
.MODEL 2_CUBAQP PMOS LEVEL=2
+ CGSO  =0.560E-09  CGDO  =0.560E-09  CGBO  =0.165E-09
+ CJ    =0.360E-03  MJ    =0.500E+00  CJSW  =0.310E-09  MJSW  =0.010E+00
+ JS    =0.040E-03  PB    =0.790E-00  RSH   =81.00E+00  XQC   =1E+00
+ TOX   =31.10E-09  XJ    =0.021E-06  LD    =0.315E-06  WD    =0.731E-06
```

```
+ VTO   =-.804E+00  NSUB  =11.80E+15  NFS   =0.337E+12  NEFF  =2.030E+00
+ UO    =180.0E+00  UCRIT =19.70E+04  UEXP  =0.219E+00  UTRA  =0.000E+00
+ VMAX  =41.20E+03  DELTA =1.040E+00
* * * * * * * * * * * * * * * * * * * * * * * * * * * * * * * * * * * * * * * * * * * * * * * * * * * *
*
* worst case power parameters
*
.MODEL 2_CUBAWCPN NMOS LEVEL=2
+ CGSO  =0.370E-09  CGDO  =0.370E-09  CGBO  =0.064E-09
+ CJ    =0.300E-03  MJ    =0.440E+00  CJSW  =0.100E-09  MJSW  =0.300E+00
+ JS    =0.500E-03  PB    =0.800E+00  RSH   =25.00E+00  XQC   =1E+00
+ TOX   =28.00E-09  XJ    =0.570E-06  LD    =0.475E-06  WD    =0.450E-06
+ VTO   =0.650E+00  NSUB  =18.00E+15  NFS   =1.160E+12  NEFF  =6.310E+00
+ UO    =590.0E+00  UCRIT =21.00E+04  UEXP  =0.181E+00  UTRA  =0.000E+00
+ VMAX  =066.0E+03  DELTA =1.660E+00
.MODEL 2_CUBAWCPP PMOS LEVEL=2
+ CGSO  =0.370E-09  CGDO  =0.370E-09  CGBO  =0.064E-09
+ CJ    =0.280E-03  MJ    =0.490E+00  CJSW  =0.100E-09  MJSW  =0.260E+00
+ JS    =0.200E-03  PB    =0.700E+00  RSH   =50.00E+00  XQC   =1E+00
+ TOX   =28.00E-09  XJ    =0.472E-06  LD    =0.475E-06  WD    =0.450E-06
+ VTO   =-.650E+00  NSUB  =08.50E+15  NFS   =1.020E+12  NEFF  =2.560E+00
+ UO    =190.0E+00  UCRIT =20.20E+04  UEXP  =0.245E+00  UTRA  =0.000E+00
+ VMAX  =045.6E+03  DELTA =3.100E+00
* * * * * * * * * * * * * * * * * * * * * * * * * * * * * * * * * * * * * * * * * * * * * * * * * * * *
* worst case speed parameters
*
.MODEL 2_CUBAWCSN NMOS LEVEL=2
+ CGSO  =0.370E-09  CGDO  =0.370E-09  CGBO  =0.064E-09
+ CJ    =0.400E-03  MJ    =0.440E+00  CJSW  =0.200E-09  MJSW  =0.300E+00
+ JS    =0.500E-03  PB    =0.800E+00  RSH   =45.00E+00  XQC   =1E+00
+ TOX   =32.00E-09  XJ    =0.570E-06  LD    =0.175E-06  WD    =0.750E-06
+ VTO   =0.950E+00  NSUB  =38.50E+15  NFS   =1.160E+12  NEFF  =6.310E+00
+ UO    =520.0E+00  UCRIT =21.00E+04  UEXP  =0.181E+00  UTRA  =0.000E+00
+ VMAX  =066.0E+03  DELTA =1.660E+00
*
.MODEL 2_CUBAWCSP PMOS LEVEL=2
+ CGSO  =0.370E-09  CGDO  =0.370E-09  CGBO  =0.064E-09
+ CJ    =0.360E-03  MJ    =0.490E+00  CJSW  =0.200E-09  MJSW  =0.260E+00
+ JS    =0.200E-03  PB    =0.700E+00  RSH   =80.00E+00  XQC   =1E+00
+ TOX   =32.00E-09  XJ    =0.472E-06  LD    =0.175E-06  WD    =0.750E-06
+ VTO   =-.950E+00  NSUB  =18.00E+15  NFS   =1.020E+12  NEFF  =2.560E+00
+ UO    =160.0E+00  UCRIT =20.20E+04  UEXP  =0.245E+00  UTRA  =0.000E+00
+ VMAX  =045.6E+03  DELTA =3.100E+00
* * * * * * * * * * * * * * * * * * * * * * * * * * * * * * * * * * * * * * * * * * * * * * * * * * * *
* typical parameters with tolerances
*
.MODEL 2_CUBATOLN NMOS LEVEL=2
+ CGSO  =0.370E-09                    CGDO  =0.370E-09
+ CGBO  =0.064E-09                    CJ    =0.350E-03  DEV  =0.050E-03
+ MJ    =0.440E+00                    CJSW  =0.150E-09  DEV  =0.050E-09
+ MJSW  =0.300E+00                    JS    =0.500E-03
+ PB    =0.800E+00                    RSH   =35.00E+00  DEV  =10.00E+00
+ XQC   =1E+00                        TOX   =30.00E-09  DEV  =02.00E-09
+ XJ    =0.570E-06                    LD    =0.325E-06  DEV  =0.150E-06
+ WD    =0.600E-06  DEV  =0.150E-06   VTO   =0.800E+00  DEV  =0.150E+00
+ NSUB  =28.25E+15  DEV  =10.25E+15   NFS   =1.160E+12
+ NEFF  =6.310E+00                    UO    =555.0E+00  DEV  =035.0E+00
```

```
+ UCRIT =21.00E+04                    UEXP  =0.181E+00
+ UTRA  =0.000E+00                    VMAX  =066.0E+03
+ DELTA =1.660E+00
*
.MODEL 2_CUBATOLP PMOS LEVEL=2
+ CGSO  =0.370E-09                    CGDO  =0.370E-09
+ CGBO  =0.064E-09                    CJ    =0.320E-03  DEV   =0.040E-03
+ MJ    =0.490E+00                    CJSW  =0.150E-09    DEV   =0.050E-09
+ MJSW  =0.260E+00                    JS    =0.200E-03
+ PB    =0.700E+00                    RSH   =65.00E+00    DEV   =15.00E+00
+ XQC   =1E-00                        TOX   =29.70E-09    DEV   =02.00E-09
+ XJ    =0.472E-06                    LD    =0.325E-06    DEV   =0.150E-06
+ WD    =0.600E-06  DEV   =0.150E-06  VTO   =-.800E+00    DEV   =0.150E+00
+ NSUB  =13.25E+15  DEV   =04.75E+15  NFS   =1.020E+12
+ NEFF  =2.560E+00                    UO    =175.0E+00    DEV   =015.0E+00
+ UCRIT =20.20E-04                    UEXP  =0.245E+00
+ UTRA  =0.000E+00                    VMAX  =045.6E+03
+ DELTA =3.100E+00
**************************************************************
**************************************************************
*
*    LIBRERIA DI COMPONENTI MOS BRAND_X
* PROCESSO DA 4um ANALOGICO SINGOLO METAL, DOPPIO POLY
*                 ALIMENTAZIONE 11V
*                        CCF BRAND_X
*
**************************************************************
**************************************************************
*       4um CMOS
**************************************************************
* typical parameters
*
.MODEL CCFN NMOS LEVEL=2
+ CGSO  =0.310E-09  CGDO  =0.310E-09  CGBO  =0.100E-09
+ CJ    =0.350E-03  MJ    =0.850E+00  CJSW  =0.520E-09  MJSW  =0.260E+00
+ JS    =6.500E-03  PB    =0.670E+00  RSH   =24.30E+00  XQC   =0.400E+00
+ TOX   =46.10E-09  XJ    =1.000E-06  LD    =0.552E-06  OXETCH=-1.27E-06
+ VTO   =0.824E+00  TCV   =1.880E-03  NSUB  =16.80E+15  NFS   =0.522E+12
+ UO    =636.0E+00  FRC   =14.90E-13  FSB   =1.070E-04  VST   =320.0E+07
+ ECV   =3.910E+06  SCM   =0.191E+00  ASPNWM=0.754E+00
*
.MODEL CCFP PMOS LEVEL=2
+ CGSO  =0.310E-09  CGDO  =0.310E-09  CGBO  =0.100E-09
+ CJ    =0.170E-03  MJ    =0.500E+00  CJSW  =0.400E-09  MJSW  =0.270E+00
+ JS    =0.650E-03  PB    =0.670E+00  RSH   =68.00E+00  XQC   =0.400E+00
+ TOX   =46.10E-09  XJ    =1.500E-06  LD    =0.524E-06  OXETCH=-1.35E-06
+ VTO   =-.972E+00  TCV   =1.900E-03  NSUB  =02.82E+15  NFS   =1.000E+12
+ UO    =213.0E+00  FRC   =149.0E-13  FSB   =3.670E-04  VST   =500.0E+07
+ ECV   =6.030E+06  SCM   =1.020E+00  ASPNWM=0.408E+00
**************************************************************
```

•Level 3

```
*****************************************************************
*
*    LIBRERIA DI COMPONENTI MOS (PROCESSO DA 2um)
*          ricavata da L.A.Glasser e altri
*     "The Design and Analysis of VLSI Circuits"
*                  pg.  453-460
*
*****************************************************************
*****************************************************************
*       2um nMOS
*****************************************************************
* Worst-case slow parameters
*
.MODEL NENHS NMOS LEVEL=3 RSH=50 TOX=330E-10 LD=0.19E-6 XJ=0.27E-6
+ VMAX=13E4 ETA=0.25 KAPPA=0.5 NSUB=5E14 UO=650 THETA=0.1
+ VTO=0.946 CGSO=2.43E-10 CGDO=2.43E-10 CJ=6.9E-5 CJSW=3.3E-10
+ PB=0.7 MJ=0.5 MJSW=0.3 NFS=1E10
*
.MODEL NZEROS NMOS LEVEL=3 RSH=50 TOX=330E-10 LD=0.19E-6 XJ=0.27E-6
+ VMAX=13E4 ETA=0.25 KAPPA=0.5 NSUB=40E14 UO=680 THETA=0.1
+ VTO=0.526 CGSO=2.43E-10 CGDO=2.43E-10 CJ=6.9E-5 CJSW=3.3E-10
+ PB=0.7 MJ=0.5 MJSW=0.3 NFS=1E10
*
.MODEL NDEPS NMOS LEVEL=3 RSH=50 TOX=330E-10 LD=0.19E-6 XJ=0.27E-6
+ VMAX=13E4 ETA=0.25 KAPPA=0.5 NSUB=50E14 UO=650 THETA=0.04
+ VTO=-2.078 CGSO=2.43E-10 CGDO=2.43E-10 CJ=6.9E-5 CJSW=3.3E-10
+ PB=0.7 MJ=0.5 MJSW=0.3 NFS=1E10
*
*deltaLpoly(one  side)=-0.125U
*deltaW(one  side)=0.9U
*
*****************************************************************
*Typical
*
.MODEL NENHT NMOS LEVEL=3 RSH=35 TOX=300E-10 LD=0.21E-6 XJ=0.3E-6
+ VMAX=15E4 ETA=0.18 KAPPA=0.5 NSUB=3.5E14 UO=700 THETA=0.095
+ VTO=0.781 CGSO=2.8E-10 CGDO=2.8E-10 CJ=5.75E-5 CJSW=2.48E-10
+ PB=0.7 MJ=0.5 MJSW=0.3 NFS=1E10
*
.MODEL NZEROT NMOS LEVEL=3 RSH=35 TOX=300E-10 LD=0.21E-6 XJ=0.3E-6
+ VMAX=15E4 ETA=0.18 KAPPA=0.5 NSUB=2.75E14 UO=730 THETA=0.095
+ VTO=0.354 CGSO=2.8E-10 CGDO=2.8E-10 CJ=5.75E-5 CJSW=2.48E-10
+ PB=0.7 MJ=0.5 MJSW=0.3 NFS=1E10
*
.MODEL NDEPT NMOS LEVEL=3 RSH=35 TOX=300E-10 LD=0.21E-6 XJ=0.3E-6
+ VMAX=15E4 ETA=0.18 KAPPA=0.5 NSUB=35E14 UO=700 THETA=0.035
+ VTO=-2.231 CGSO=2.8E-10 CGDO=2.8E-10 CJ=5.75E-5 CJSW=2.48E-10
+ PB=0.7 MJ=0.5 MJSW=0.3 NFS=1E10
*
*deltaLpoly(one  side)=0U
*deltaW(one  side)=0.75U
*
*****************************************************************
*Fast
*
.MODEL NENHF NMOS LEVEL=3 RSH=20 TOX=270E-10 LD=0.23E-6 XJ=0.33E-6
+ VMAX=17E4 ETA=0.10 KAPPA=0.5 NSUB=2E14 UO=750 THETA=0.09
```

```
+ VTO=0.612 CGSO=3.4E-10 CGDO=3.4E-10 CJ=4.6E-5 CJSW=1.65E-10
+ PB=0.7 MJ=0.5 MJSW=0.3 NFS=1E10
*
.MODEL NZEROF NMOS LEVEL=3 RSH=20 TOX=270E-10 LD=0.23E-6 XJ=0.33E-6
+ VMAX=17E4 ETA=0.10 KAPPA=0.5 NSUB=1.5E14 UO=780 THETA=0.09
+ VTO=0.179 CGSO=3.4E-10 CGDO=3.4E-10 CJ=4.6E-5 CJSW=1.65E-10
+ PB=0.7 MJ=0.5 MJSW=0.3 NFS=1E10
*
.MODEL NDEPF NMOS LEVEL=3 RSH=20 TOX=270E-10 LD=0.23E-6 XJ=0.33E-6
+ VMAX=17E4 ETA=0.10 KAPPA=0.5 NSUB=20E14 UO=750 THETA=0.03
+ VTO=-2.384 CGSO=3.4E-10 CGDO=3.4E-10 CJ=4.6E-5 CJSW=1.65E-10
+ PB=0.7 MJ=0.5 MJSW=0.3 NFS=1E10
*
*deltaLpoly(one side)=0.125U
*deltaW(one side)=0.6U
*
```

- As already stated **L** and **W** are the parameters to be defined early in the simulation, however there are other parameters as **AD**, **AS**, **PD**, and **PS** that have a close relation to **L** and **W** so they can defined also at the beginning. In order to have a device definition that changes all these parameters as we need to change **L** and **W** during simulation, it is convenient to define a ***subcircuit*** that includes the device as in the example.

- In the example we change the other parameters as a function of **L** and **W** according to the process characteristic.

- Subcircuit definition requires a **.SUBCKT** instance and a statement that has the following structure:

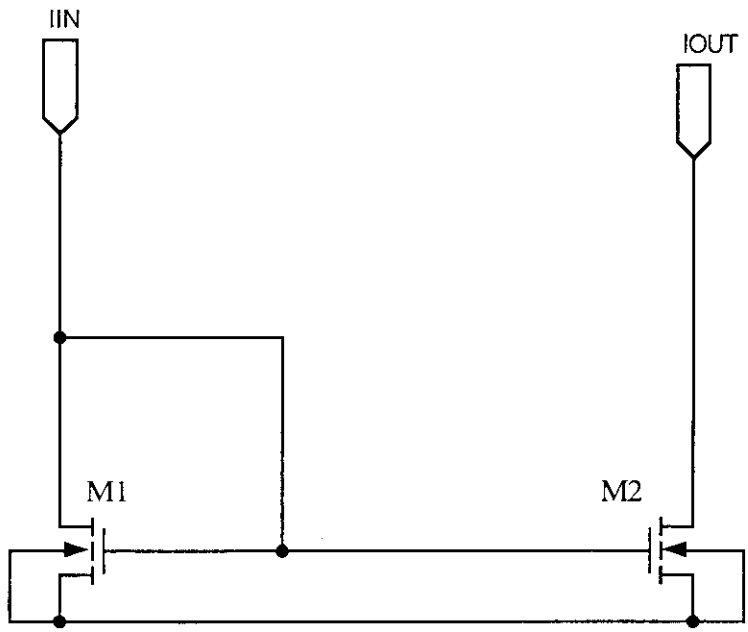
```
.SUBCKT <name>
+[list of nodes]
+[PARAMS :<name>=<value>]
+[TEXT]
.ENDS <name>
```

```
* * * * * * * * * * * * * * * * * * * * * * * * *
.SUBCKT TN_2_CUBAQb          D        G          S       PARAMS:   WN=3U      LN=2U
M1              D        G       S          S     2_CUBAQN W={WN}   L={LN}
+         AD={2U*WN}AS={2U*WN}PD={2U+(2*WN)}PS={2U+(2*WN)}
+        NRD={2U/WN}NRS={2U/WN}
.ENDS TN_2_CUBAQb
* * * * * * * * * * * * * * * * * * * * * * * * *
* PMOS_CAE
.SUBCKT TP_2_CUBAQb          D        G          S       PARAMS:   WP=3U      LP=2U
M1              D        G       S          S     2_CUBAQP W={WP}   L={LP}
+         AD={2U*WP}AS={2U*WP}PD={2U+(2*WP)}PS={2U+(2*WP)}
+        NRD={2U/WP}NRS={2U/WP}
.ENDS TP_2_CUBAQb
* * * * * * * * * * *
.SUBCKT   CAE_12N     D        G          S       PARAMS:   W=2U      L=2U
M1              D        G       S          0        MODN     W={W}     L={L}
+          AD={2U*W}AS={2U*W}PD={2U+(2*W)}   PS={2U+(2*W)}
+         NRD={2U/W}NRS={2U/W}
.ENDS CAE_12N
* * *
.SUBCKT   CAE_12P     D        G          S       PARAMS:   W=2U      L=2U
M1              D        G       S          S        MODP     W={W}     L={L}
+          AD={2U*W}AS={2U*W}PD={2U+(2*W)}   PS={2U+(2*W)}
+         NRD={2U/W}NRS={2U/W}
.ENDS CAE_12P
```

8. CURRENT MIRRORS AND VOLTAGE REFERENCES

•A very useful building block in CMOS analog design is the ***current mirror*** , already well known in bipolar technology.

•The current mirror uses the principle that ***if the gate source voltage of two identical MOS transistor are equal, the channel current should be equal.***



•Normally i_{in} is defined by a current generator or some other means and i_{out} is the mirrored current. **M1** is in saturated region as $v_{DS1} = v_{GS1}$.
Assuming that $v_{DS2} > v_{GS-VT2}$, we can use the equation (5.5) of the MOS transistor in the saturated region. So the ratio is

$$\frac{i_{out}}{i_{in}} = \frac{L_1 W_2}{L_2 W_1}\left(\frac{v_{GS} - V_{T2}}{v_{GS} - V_{T1}}\right)^2 \frac{1+\lambda v_{DS2}}{1+\lambda v_{DS1}} \frac{K_2'}{K_1'} \qquad (8.1)$$

•Normally the components are identical as they are processed on the same silicon area and thus the physical parameters are the same for both devices. Also assuming that λ effect is negligible ($v_{DS2} \approx v_{DS1}$), the (8.1) simplifies as

$$\frac{i_{out}}{i_{in}} = \frac{L_1 W_2}{L_2 W_1} \qquad (8.2)$$

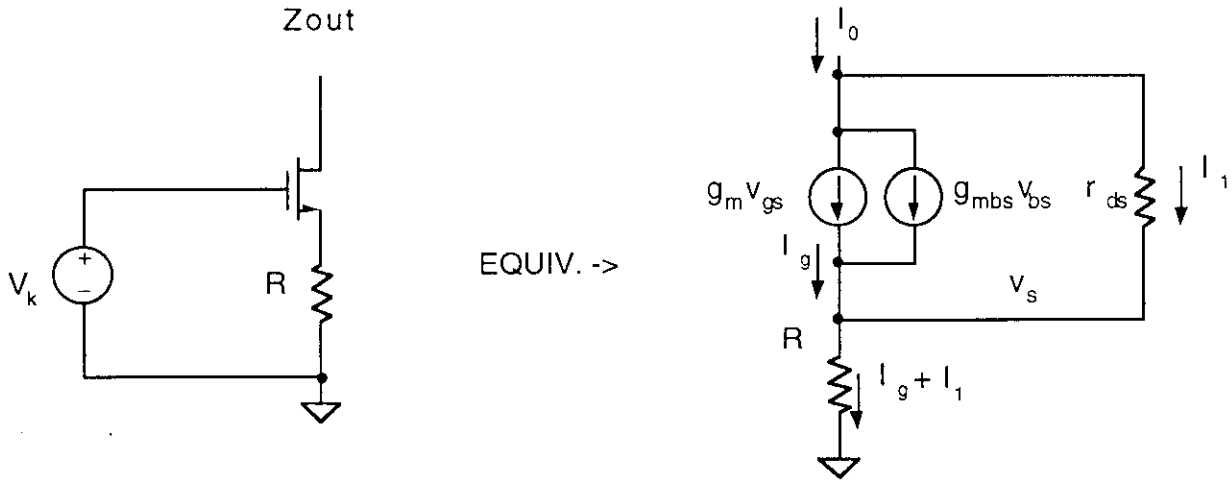
consequently i_{out}/i_{in} is a function of the ***aspect ratio*** under control of the designer. It

is evident that ***Zout*** seen from the drain of ***M2*** is equal to ***rds***.

•There are many techniques that allow tight control of the aspect ratio using suitable layouts and geometries.

•The current mirrors are widely used as amplifiers load as we'll see. It's then important to evaluate their dynamic impedance (load).

• We consider first the load impedance Z_{out} of the following simple circuit.



$$I_0 = I_g + I_1 \cdots\cdots\cdots I_0 = {}^{v_s}\!/_{R} \cdots\cdots\cdots I_1 = {}^{\left(V_0 - v_s\right)}\!/_{r_{ds}}$$

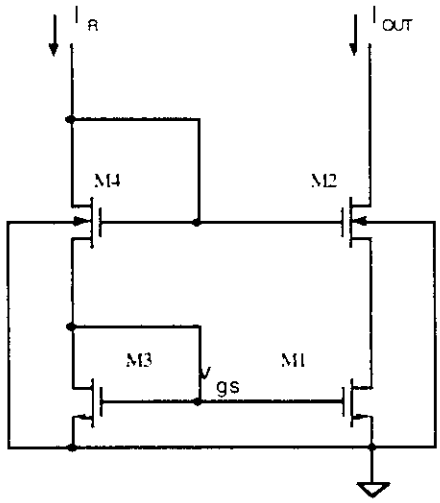
$$I_g = -g_m v_s - g_{mbs} v_s = -g_m R I_0 - g_{mbs} R I_0 = -R I_0 \left(g_m + g_{mbs}\right)$$

$$V_0 = I_1 r_{ds} + v_s = I_0 r_{ds} - I_g r_{ds} + I_0 R = I_0 r_{ds} + I_0 R r_{ds}\left(g_m + g_{mbs}\right) + I_0 R$$

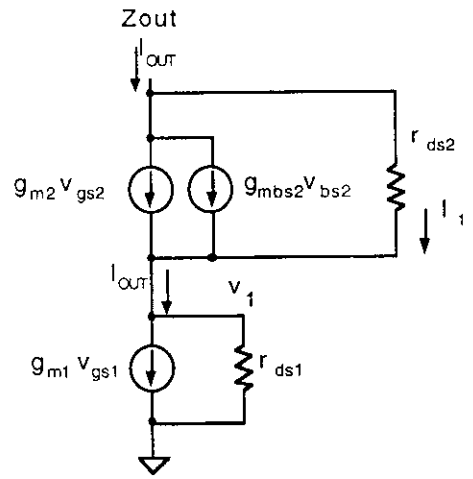
$$Z_0 = {}^{V_0}\!/_{I_0} = R + r_{ds} + R r_{ds}\left(g_m + g_{mbs}\right) \approx g_m R r_{ds}$$

(8.3)

- We can now try to improve the previous current mirror whose Z_{out} was equal to r_{ds} with the following ***cascode current mirror***.



EQUIV. ->



•We must remember that the small signal ***Vgs*** is ***zero*** as the voltage at the gate of ***M1*** is defined by the one on the ***M2*** gate.

The ***Zout*** is again given by (8.3) rewritten:

$$Z_0 = {}^{V_0}\!/_{I_0} = r_{ds1} + r_{ds2} + r_{ds1} r_{ds2} (g_{m2} + g_{mbs2}) \approx r_{ds1} + r_{ds2} + g_{m2} r_{ds1} r_{ds2} \tag{8.4}$$

•The current mirror in order to work properly must have the output transistors in ***saturation region***, that means, remembering the (5.4):

$$V_{DS(sat)} \geq V_{GS} - V_T = \Delta V \tag{8.5}$$

where ΔV is just the voltage on top of the V_T.

•Also we must remember that

$$i_D = K' \frac{W}{2L} (v_{GS} - V_T)^2 (1 + \lambda v_{DS}) \approx K' \frac{W}{2L} \Delta V^2 \tag{8.6}$$

Hence being the ***id*** the same, we have

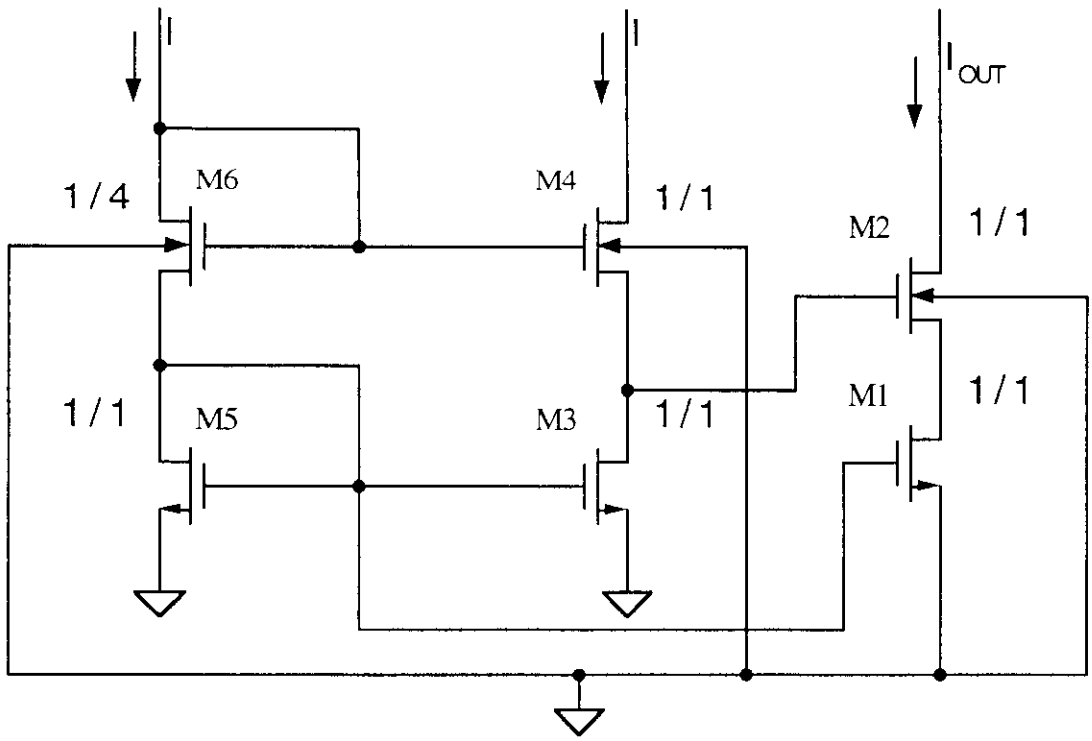
$$i_D = K' \frac{W_1}{2L_1} \Delta V_1^2 = K' \frac{W_2}{2L_2} \Delta V_2^2$$

and assuming ***M1*** and ***M2*** of the same type

$$\frac{W_1}{L_1} \Delta V_1^2 = \frac{W_2}{L_2} \Delta V_2^2 \qquad (8.7)$$

The aspect ratio ***W/L*** can be used to control ΔV.

•We show now a method to reduce V_{SAT} at minimum in a cascode current mirror.



•All the transistors have the same dimensions (aspect ratio) exception for ***M6*** that is 4 times longer, or 4 times more narrow.
Voltage in gate of ***M5*** is:

$$V_{g5}=V_T+\Delta V$$

Voltage in gate of ***M6***, rembering, (8.7) is:

$$V_{g6}=V_T+2\Delta V+V_{g5}=2V_T+3\Delta V$$

Voltage in gate of ***M2*** is:

$$V_{g2}=V_{g6}-V_T+\Delta V=V_T+2\Delta V$$

while voltage in gate of ***M1*** is:

$$V_{g1}=V_T+\Delta V$$

- In this case, remembering (8.6), we have for ***M2***:

$$v_{D2(sat)min}=v_{GS}-V_T=2\Delta V$$

Again it's worth to remember that ΔV is controlled by the aspect ratio of the transistors.

Example

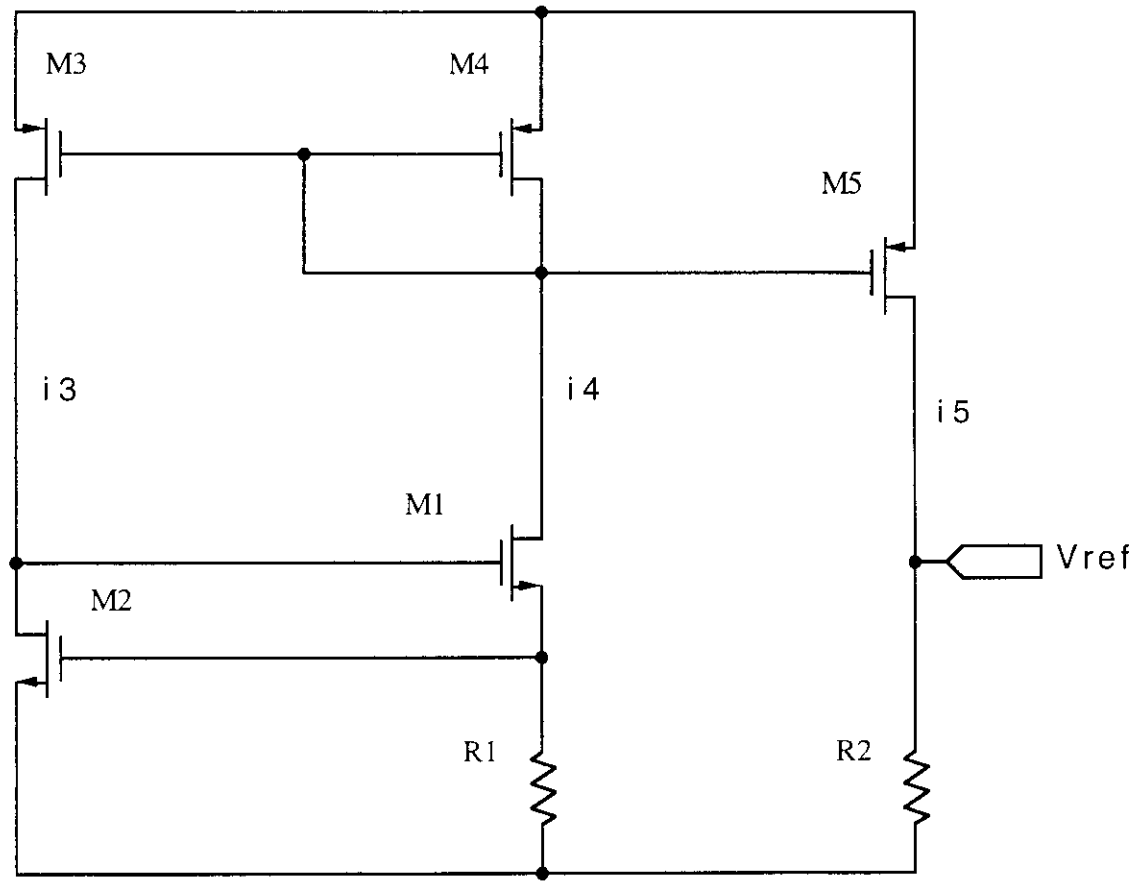
Calculate the aspect ratios for a cascode current mirror that allows ***Vmin = 0.8V***
with an output current of ***100μA.***

According to (8.6), and assuming the transistor parameters of pag. 7.12, we have for M1 to M5:

$$W/L=\frac{2i_{out}}{K'\,\Delta V^2}=\frac{2*100*10^{-6}}{17*10^{-6}*.16}=73,5$$

while for M6 we have *W/L*=18,4.

•To generate a reference voltage let's consider the following circuit that is called ***V_T referenced source***.



•Let's assume that **M3** and **M4** have the same aspect ratio, they are then a current mirror with $i_3 = i_4 = i$. let's now compute the

voltage drop across **R1**, using (5.5), where we ignore the λ effect.

$$i = K' \frac{W_2}{2L_2}\left(V_{GS2} - V_T\right)^2 = K' \frac{W_2}{2L_2}\left(V_{R1} - V_T\right)^2$$

$$V_{R1} = V_T + \sqrt{\frac{2iL_2}{K' W_2}} \cong V_T$$

The last approximation is correct for small ***i*** and W larger than L.
We can also write that

$$i = \frac{V_{R1}}{R_1} = \frac{V_T}{R_1}$$

The voltage drop across **R2** is obtained through the **M5** current mirror

$$V_{R2} = \frac{\left(W/L\right)_5}{\left(W/L\right)_3} V_T \frac{R_2}{R_1}$$

- The current mirror and voltage reference presented here have the objective of providing stable values with respect to changes in power supply and temperature. It is easy to understand that while power supply independence is obtained, satisfactory temperature performance could not with the presented design.

- References that offer good temperature performance will be presented later.