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# *Microprocessor Laboratory*
# *Sixth Course on Basic VLSI Design Techniques*
# *8 November - 3 December 1999*

A CASE STUDY

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# A Case Study:
# 4 μW 8b Algorithmic ADC

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# Outline

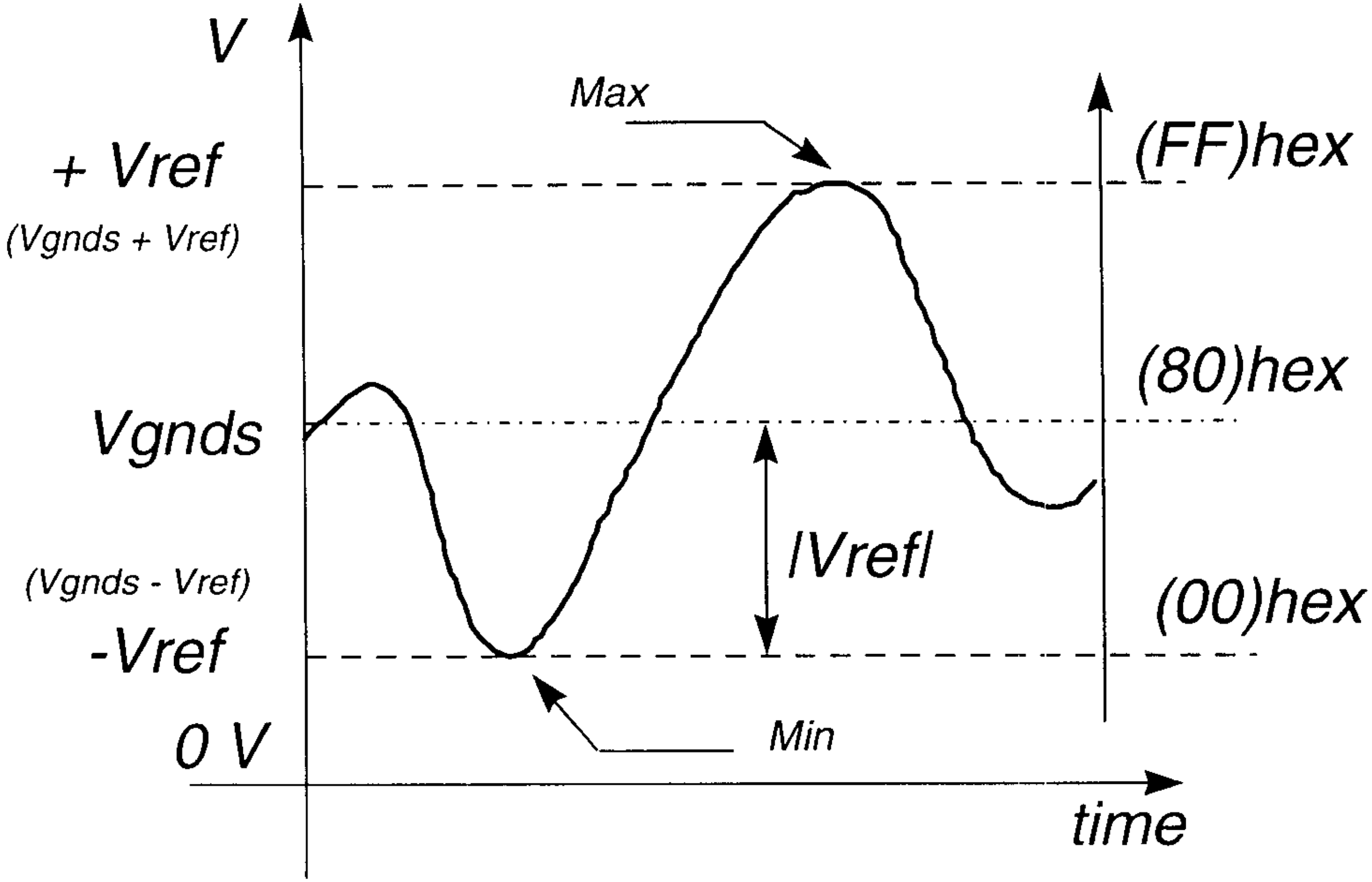
- Design Specifications;
- The algorithmic A/D converter;
- Numerical Model and Simulation
- Digital and Analog Design (Control logic, phases generator, OTAs, switches, capacitors)
- Layout
- Test set-up & Measurements

# Design specifications

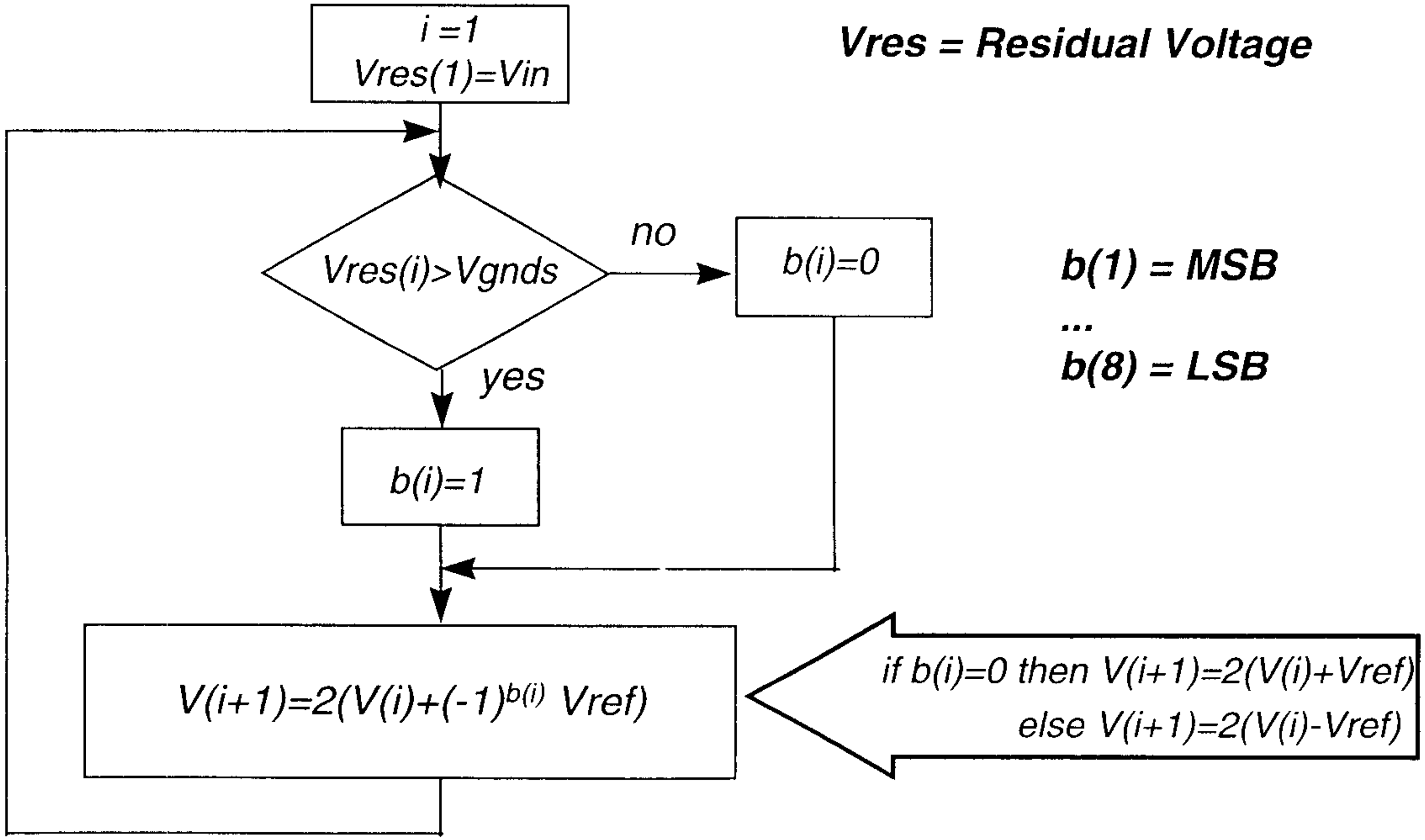
- Resolution: 8 bits
- Single Voltage Supply: 2V - 2.8V
- Bandwidth: 250Hz (Sample Rate Min. 500Hz)
- Bipolar input signal: Vgnds ± 400 mV
- Very Low Die Size
- Very Low Power Dissipation

⇒ *Pacemaker Application*

# “Bipolar” input signal



# The algorithmic A/D converter




***Vres = Residual Voltage***

***b(1) = MSB***

***...***

***b(8) = LSB***

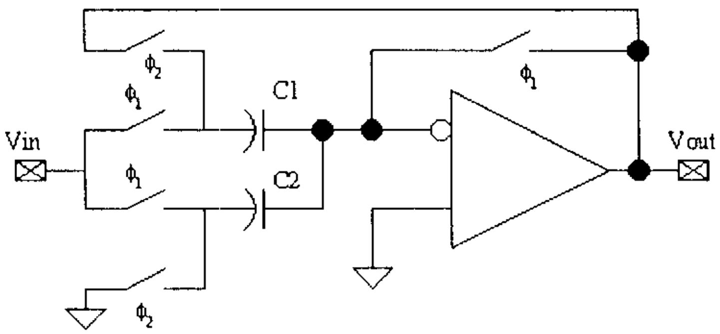
# What do I need to realise an algorithmic A/D converter ?

$$V(i+1)=2\,(V(i)+(-1)^{b(i)}\,Vref)$$

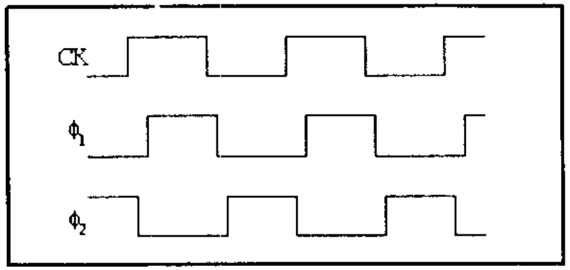
- Multiplier x 2
- Adder ± Vref
- Comparator

*if (Vres(i) > Vgnds) then ...*

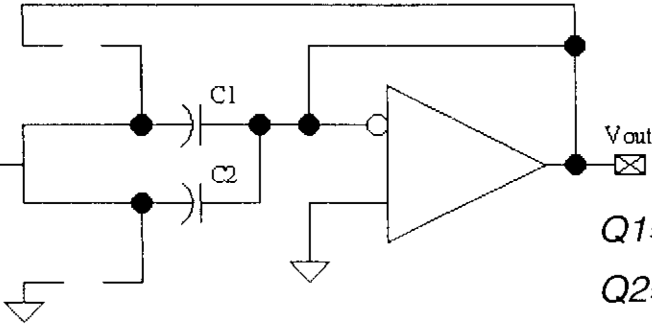
# Multiplier x 2




*Non Overlapping phases*



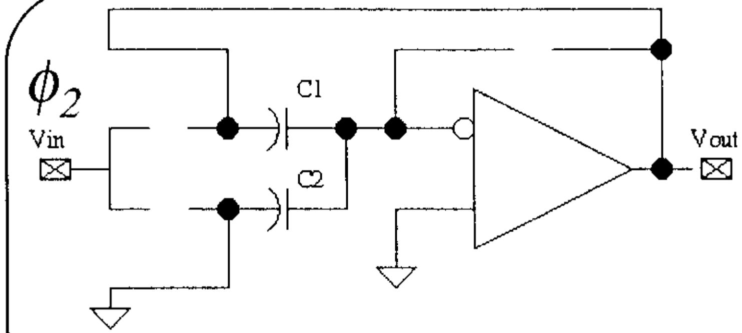

$\phi_1$




*Q1=C1 Vin*

*Q2=C2 Vin*

$\phi_2$



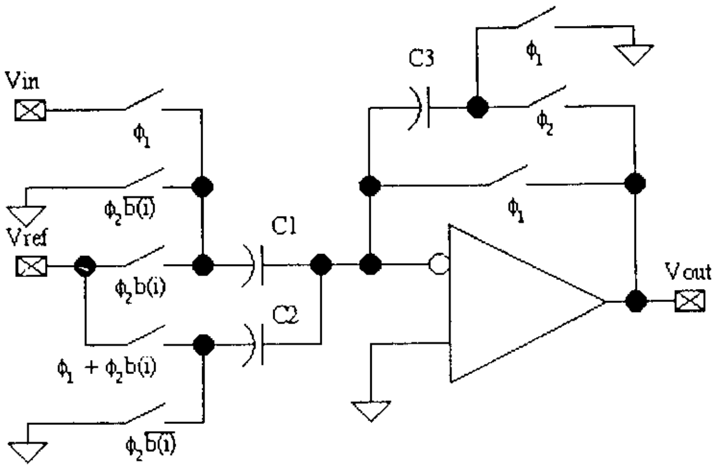

*<u>Q1'=Vout C2</u>* *<u>Q2'=0</u>*

*= Q1+Q2*

*= Vin (C1 + C2)*

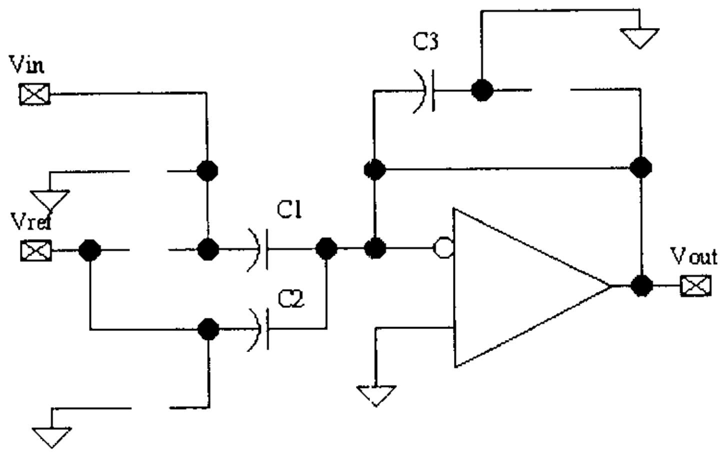
*if C1= C2 then **Vout = 2 Vin***

# Adder ± Vref



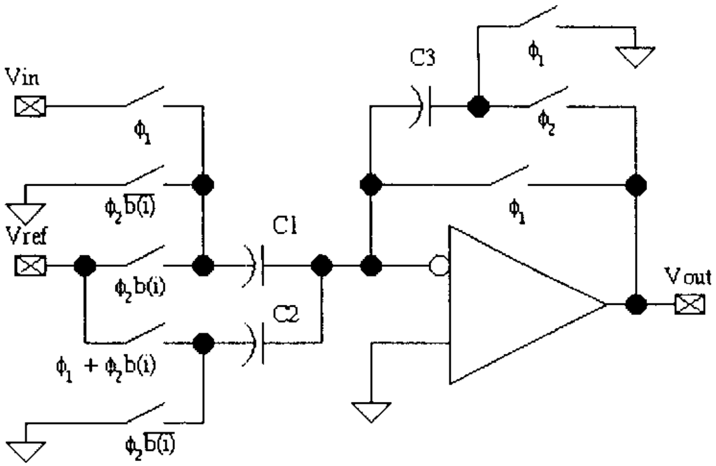

*b(i) is the last output bit elaborated*

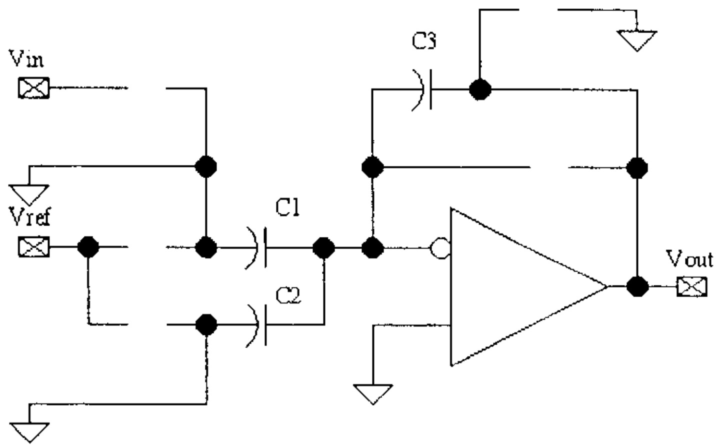
$\phi_1$




*Q1 = C1 Vin*
*Q2 = C2 Vref*
*Q3 = 0*

## $\phi_2$ **b(i) = 0**




*Q1' = 0*

*Q2' = 0*

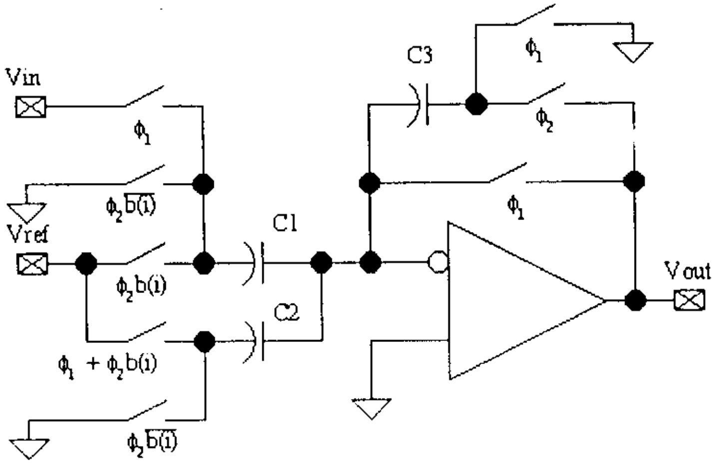
*Q3' = C3 Vout*

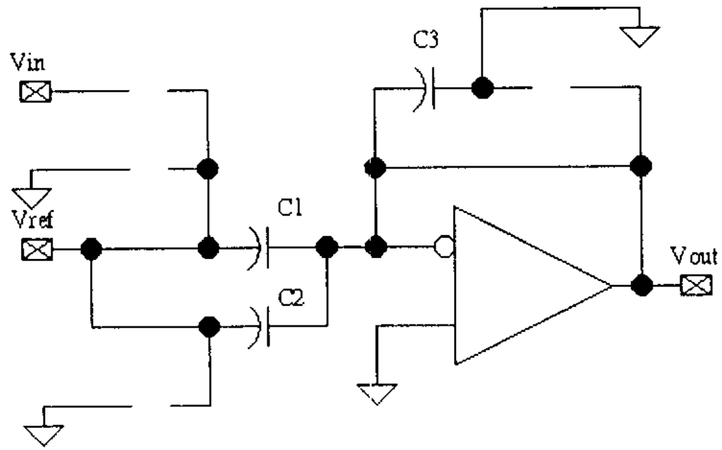
*= Q1 + Q2*

*= C1 Vin + C2 Vref*

*if C1=C2=C3 then* **Vout = Vin + Vref**

# $\phi_2 \quad b(i) = 1$

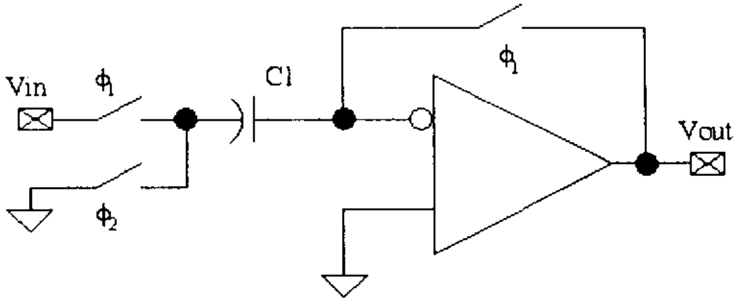


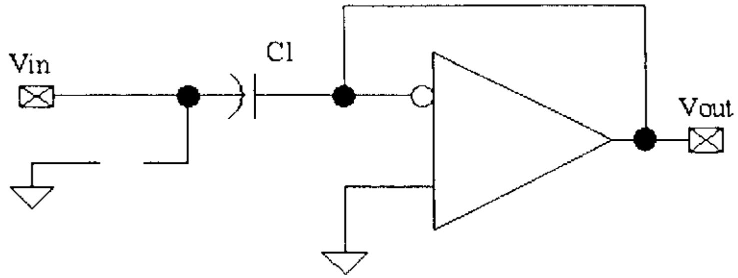




*Q1' = C1 Vref*
*Q2' = C2 Vref*
*Q3' = C3 Vout*
*Q1' + Q2' + Q3' = Q1 + Q2*
*C1 Vref + ~~C2 Vref~~ + C3 Vout = C1 Vin + ~~C2 Vref~~*

*if C1=C3 then* **Vout = Vin - Vref**

# SC Comparator with Offset Cancellation (Autozero)




$\phi_1$ Sample

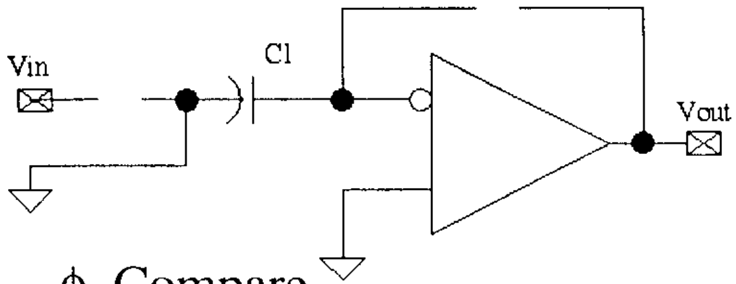
VC1= Vin - Voff

Voff = Offset Opamp

Av = Open Loop Gain

Vout = - Av [-(Vin - Voff) - Voff]

= Av Vin




$\phi_2$ Compare

# *Numerical Model and Simulation*

- Amplifiers: Open Loop Gain, offset, GBW?
- Capacitors: Minimum Value, mismatching?
- Comparator: Maximum Offset?

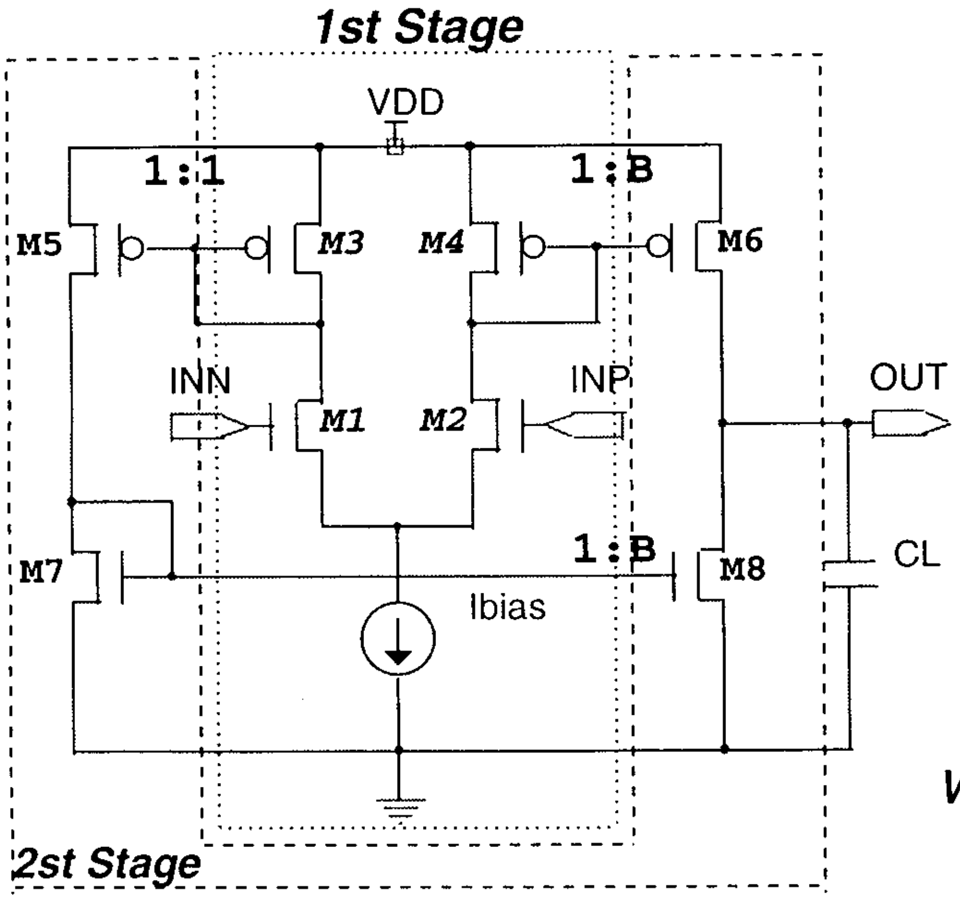
***The ADC has been fully described by a matematical model and simulated with MATLAB to define the specification for each component to reach the required performance.***

**DESIGN SPECIFICATIONS**

# *Analog and Digital Design*

- Digital Part: very simple (phases generation, counters, combination logic).
- Analog Part: OTA with Very low power dissipation (Mosfet in weak inversion), switches array and capacitors array.

# *O*perational *T*ransconduttance *A*mplifier




$$g_m = B\ g_{m1}$$

*1st Stage*

*M1=M2 (weak inversion)*
*gm is geometry independent*

*M3=M4 (strong inversion)*
*gm is geometry dependent*

*2st Stage*

*M5=M7 (strong inversion)*
*M6=M8 (strong inversion)*
*gm is geometry dependent*

*weak* $$g_m = \frac{I_D}{n U_T}$$

*strong* $$g_m = \sqrt{2\mu\ C_{ox} \frac{W}{L} I_D}$$

*M1 & M2 in weak inversion*

$$I_D < \boxed{\frac{W_{1(2)}}{L_{1(2)}}} 5nA$$

$$GWB = \frac{g_m}{C_L} = \frac{g_{m(1)}\, B}{C_L}$$

*GWB, $C_L$, B fixed* $\Longrightarrow g_{m1} \Longrightarrow Id_1 = g_{m1}\, n\, U_T \Longrightarrow \boxed{Ibias} = 2\, Id_1$

*Gain 1st stage*

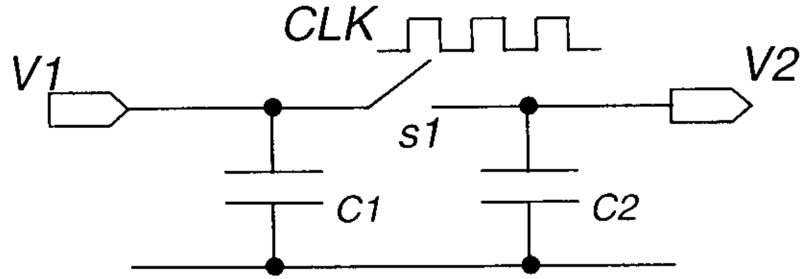
$$A_{1st} = \frac{dV_{D2(1)}}{dV_{in}} = \frac{dV_{D2(1)}}{dI_{D2(1)}} \frac{dI_{D2(1)}}{dV_{in}}$$

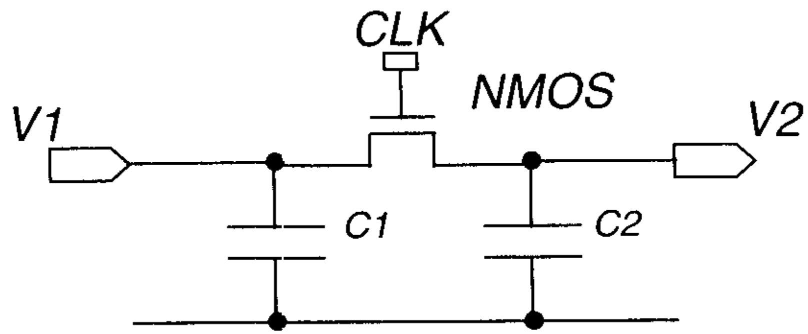
$$= \frac{g_{m1(2)}}{g_{m3(4)}} \Rightarrow g_{m3(4)} = \frac{g_{m1(2)}}{A_{1st}} \Rightarrow \boxed{\frac{W_{3(4)}}{L_{3(4)}}} = \frac{g^2_{m3(4)}}{2\mu\ C_{ox} I_D}$$

$$\boxed{\frac{W_5}{L_5}} = \frac{W_{3(4)}}{L_{3(4)}} \text{ and } \boxed{\frac{W_6}{L_6}} = B \frac{W_{3(4)}}{L_{3(4)}}$$

*for symmetry* $g_{m8} = g_{m6} = B\, g_{m3(4)} \Rightarrow \boxed{\frac{W_8}{L_8}} = \frac{g^2_{m8(6)}}{2\mu\ C_{ox} I_D}$ *and* $\boxed{\frac{W_7}{L_7}} = \frac{1}{B} \frac{W_8}{L_8}$

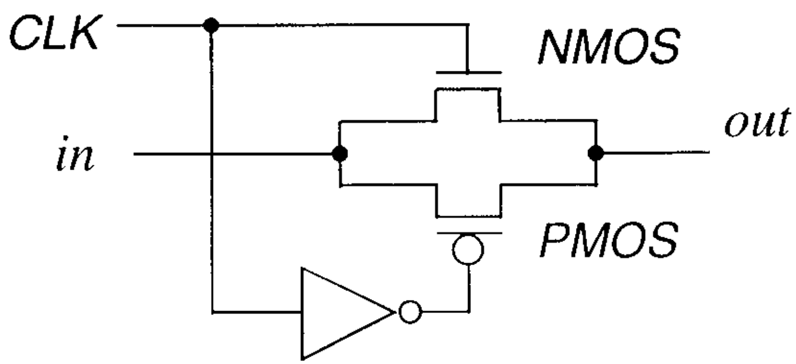
# Switches

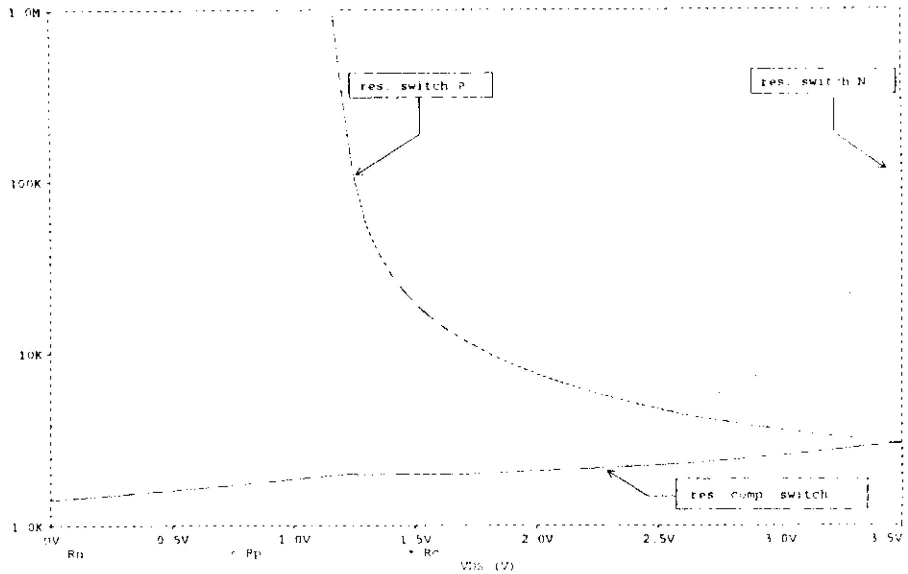



**Problem 1:** *"On" Conductance.*
*When the switch is turned on, the conductance depend on difference between the input and the clock voltage level.*

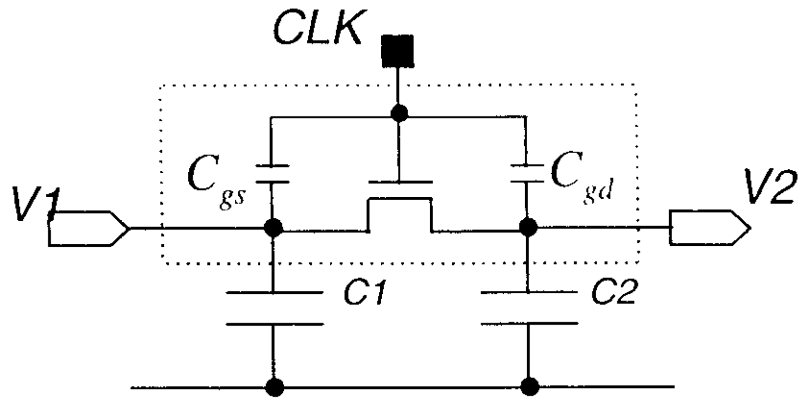
**Solution 1:** *Complementary swiches.*

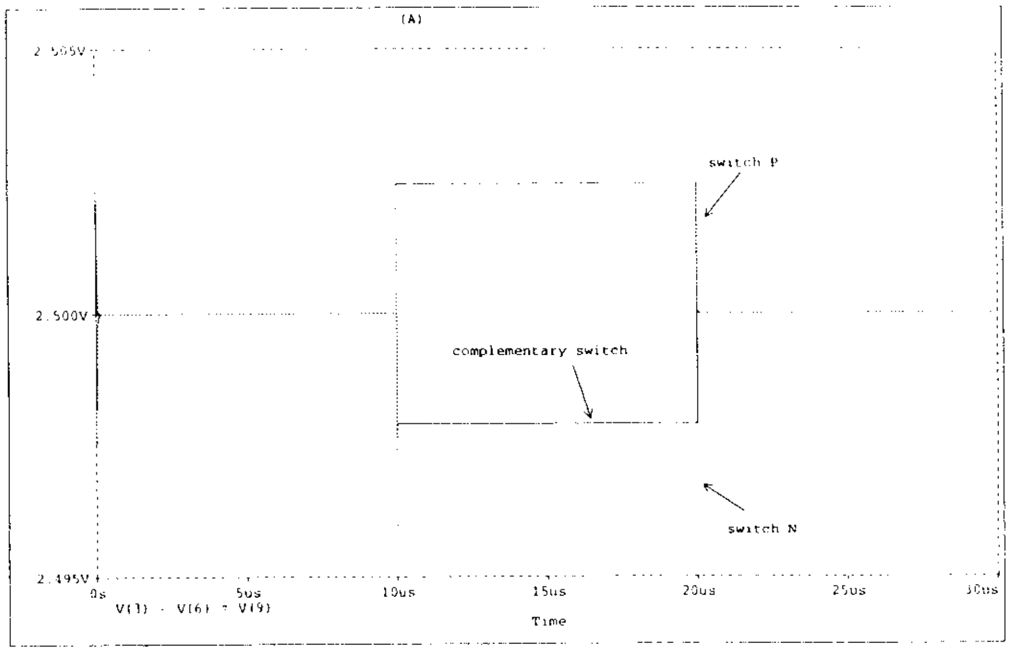


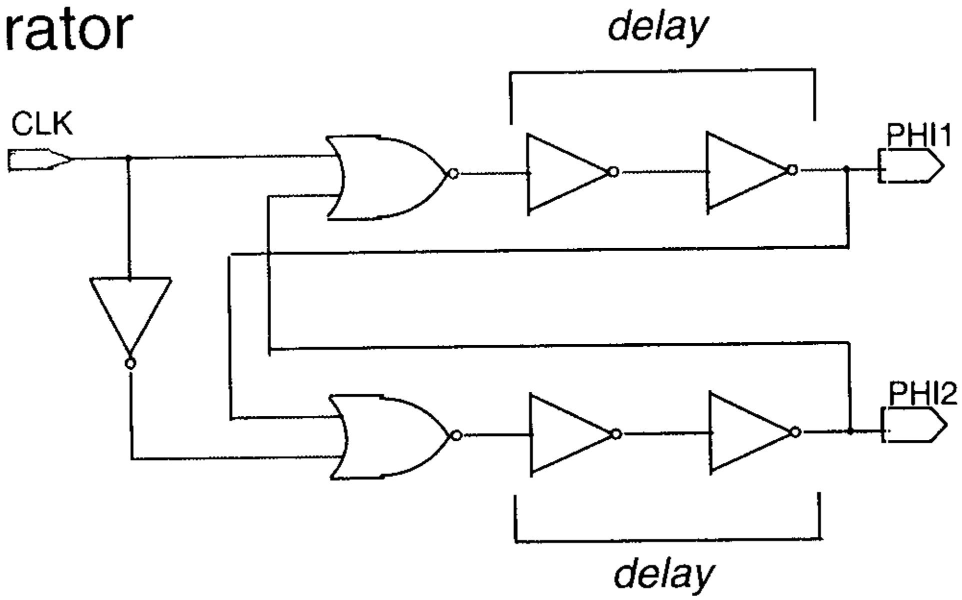
***Problem 2:*** *Clock Feedtrhough.*
*When the switch is turned off, a lot of charge is injected on capacitors (due to transistors channel charge and transistors parassitic capacitors ).*

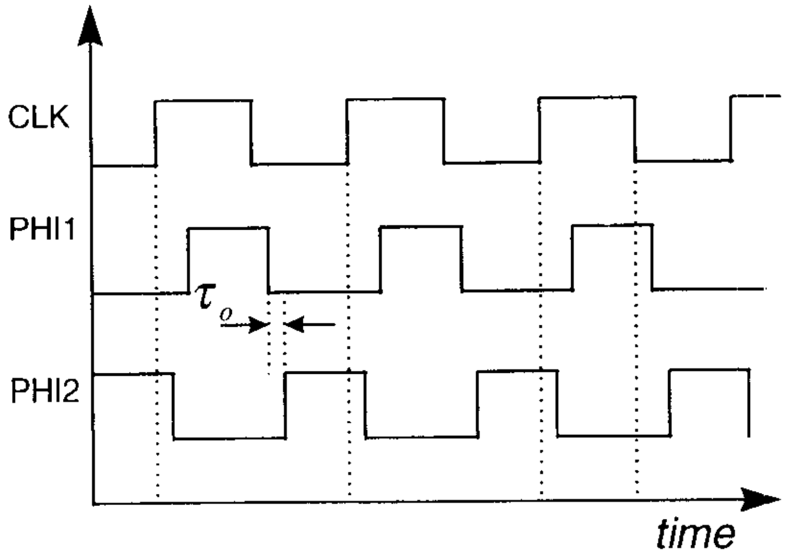
***Solution 2:*** *Partial Clock Feedtrhough cancellation with complemetary switch.*



# Phases Generator

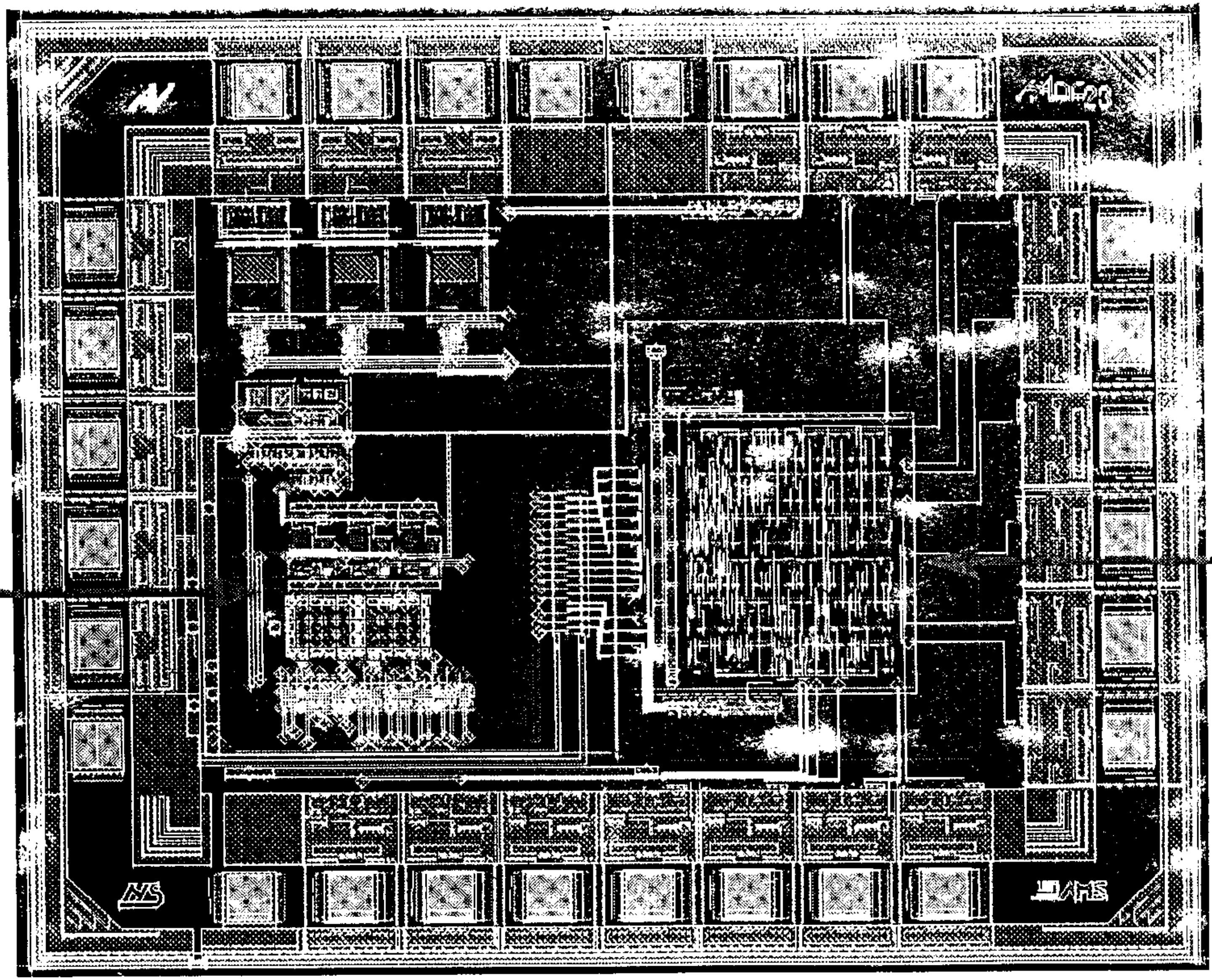



$\tau_o \cong 100ns$

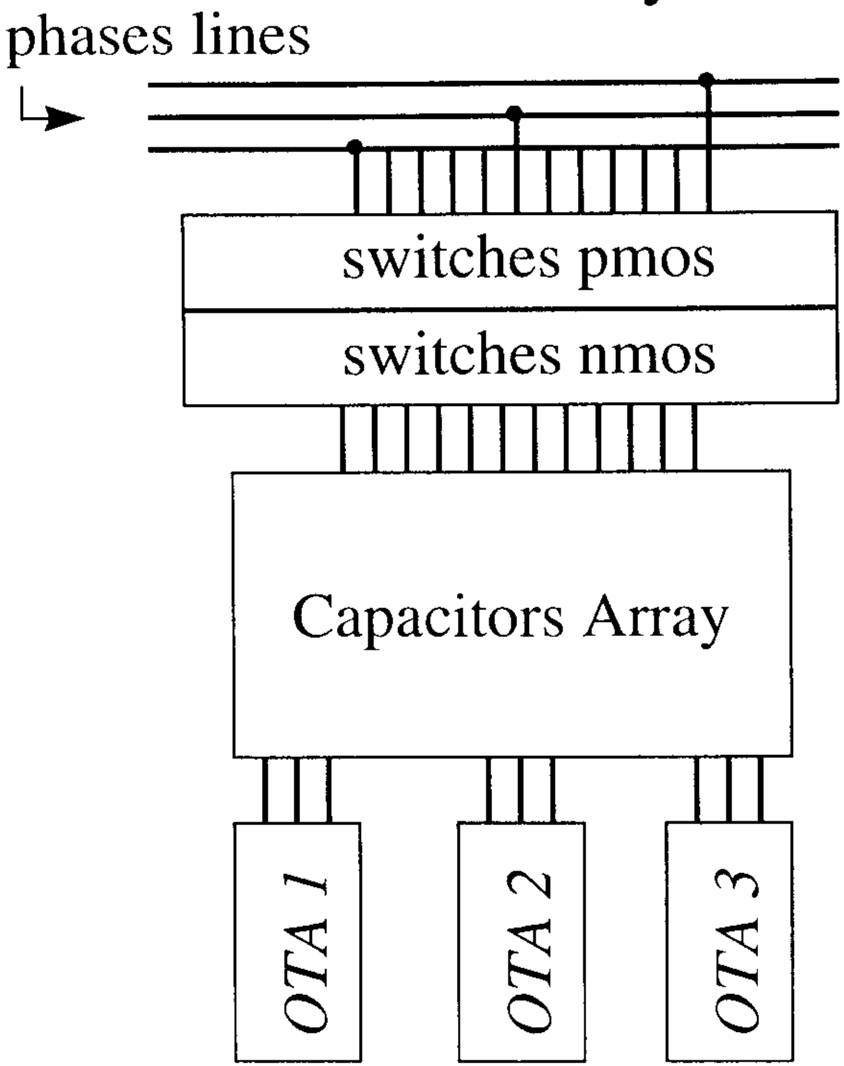
# Layout

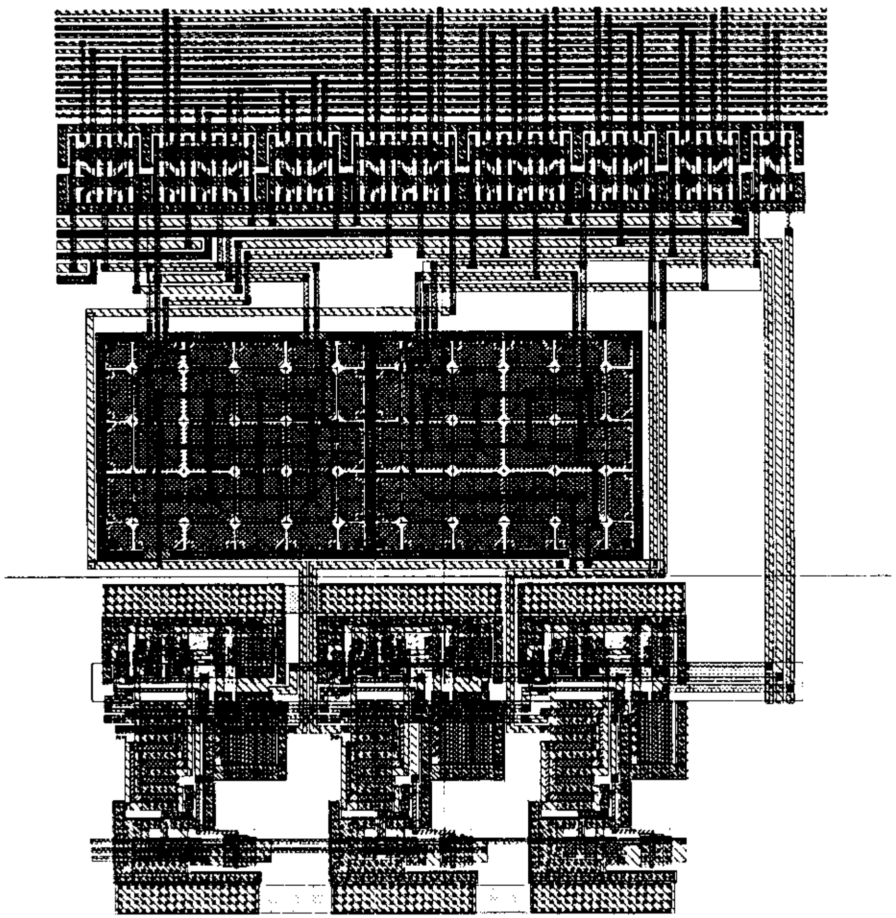
ANALOG PART



DIGITAL PART

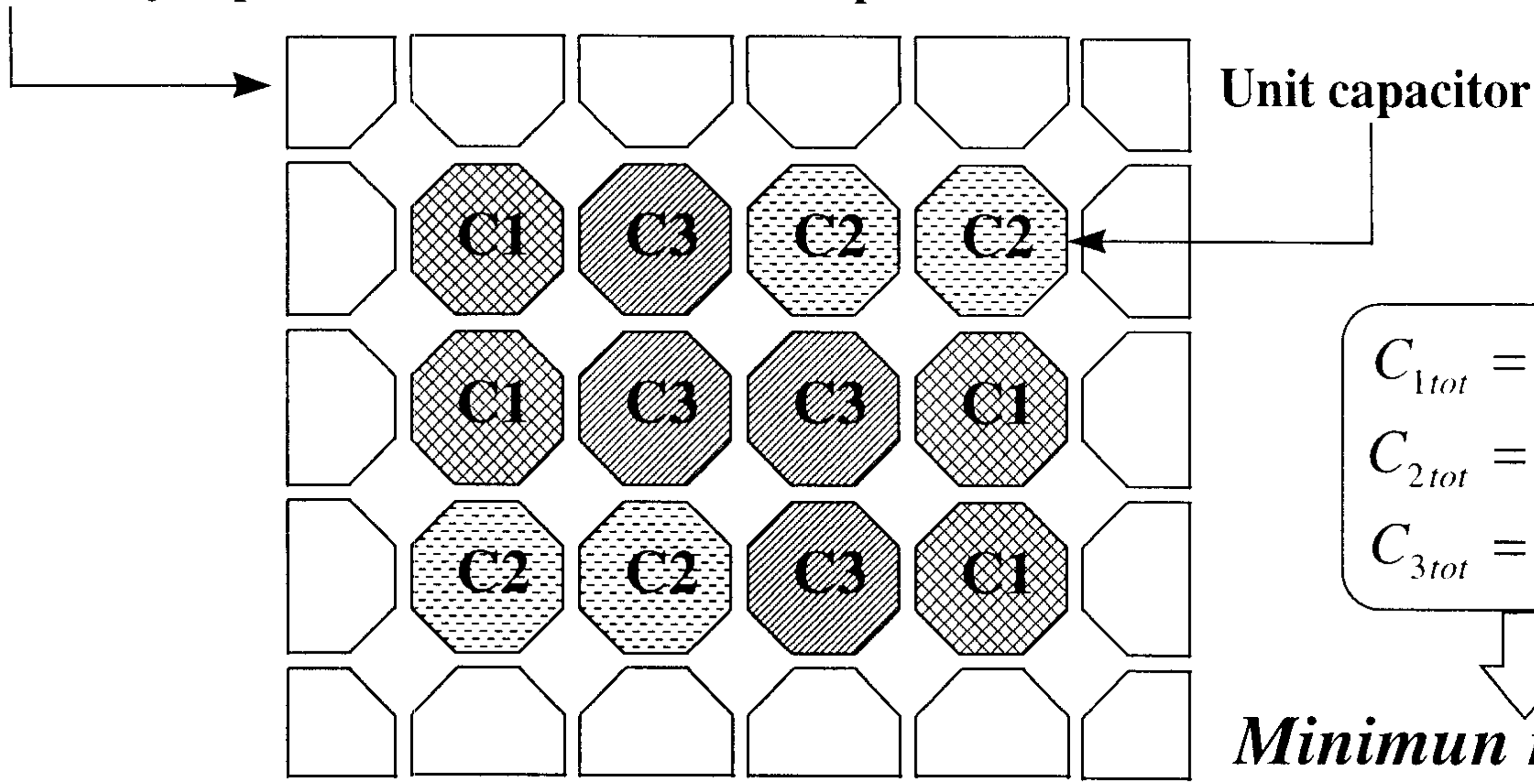
# Layout Analog Part



# Capacitors matching tecniques

**Dummy capacitors: solve border effect problem.**




$$C_{1tot} = 3 \times C_1$$
$$C_{2tot} = 3 \times C_2$$
$$C_{3tot} = 3 \times C_3$$

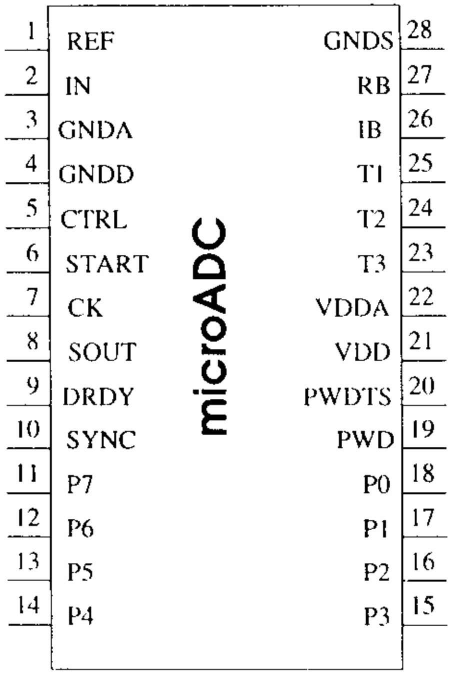
⇓

***Minimun mismatch***

- Exagonal shape of unit capacitors: Minimize geometry errors
- Barycentric structure: oxide thickness variation is mediate

# Test Results

*microADC*



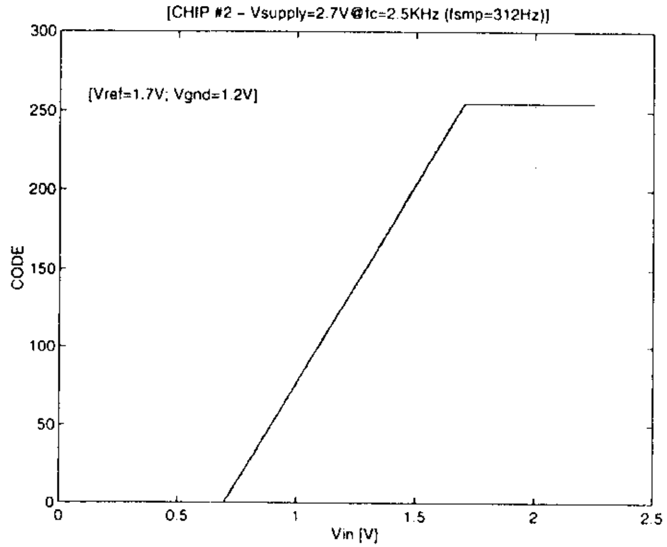

| N° Pin (Analogs pins) | NAME | Function |
|---|---|---|
| 1 | **REF** | Reference Voltage ($V_{REF}$) |
| 2 | **IN** | Input Voltage |
| 3 | **GNDA** | Analog Ground |
| 22 | **VDDA** | Analog Voltage Supply |
| 23 | **T1** | Test Out (Comparator) |
| 24 | **T2** | Test Out (Ampli x2) |
| 25 | **T3** | Test Out (Sub / Add) |
| 26 | **IB** | Test Ibias (Ibias is the Bias Current) |
| 27 | **RB** | R for Ibias |
| 28 | **GNDS** | Signal Ground |

| N° Pin (Digitals pins) | NAME | Function |
|---|---|---|
| 4 | **GNDD** | Digital Ground |
| 5 | **CTRL** | Control convertion type (ctrl=0 one shot, ctrl = 1 continuos sampling) |
| 6 | **START** | Start convertion |
| 7 | **CK** | Master Clock |
| 8 | **SOUT** | Serial Out |
| 9 | **DRDY** | Data ready |
| 10 | **SYNC** | Syncro out per (for **SOUT)** |
| 11 - 18 | **P<7-0>** | Parallel Out |
| 19 | **PWD** | Power down/ Logic Reset |
| 20 | **PWDTS** | Test Out Buffers Power down |
| 21 | **VDD** | Digital Voltage Supply |

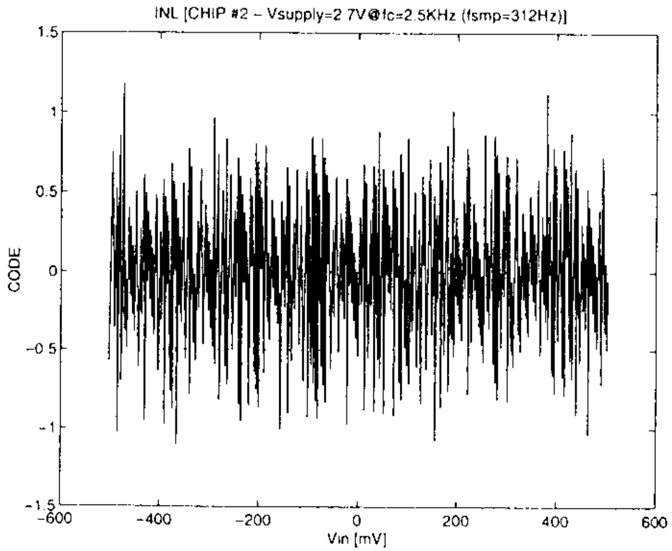
# Test Results

| | min | typ | max |
|---|---|---|---|
| **Vsupply** | 2.0 V | 2.7 V | 3.3 V |
| **$V_{ref}$** | | 1.7 V | |
| **$V_{gnds}$** | | 1.2 V | |
| **Range** | | $(V_{ref} - V_{gnds}) \div (V_{ref})$ | |
| **Isupply** | | 1.5μA | 2 μA |
| **N. bits** | | 8 | |
| **Clock frequency** | | 2.5 KHz | 20 KHz |
| **Sample frequency** | | 0.312 KHz | 2.5 KHz |
| **INL** | | < 1 LSB | < 2 LSB |
| **Gain error** | | 1 LSB | < 1.5 LSB |
| **Offset error** | | 0.5 LSB | < 2.5 LSB |

***DC TESTS (Vsupply = 2.7V, temp=25 C, f_clock=2.5 KHz (f_sample = 312Hz)***

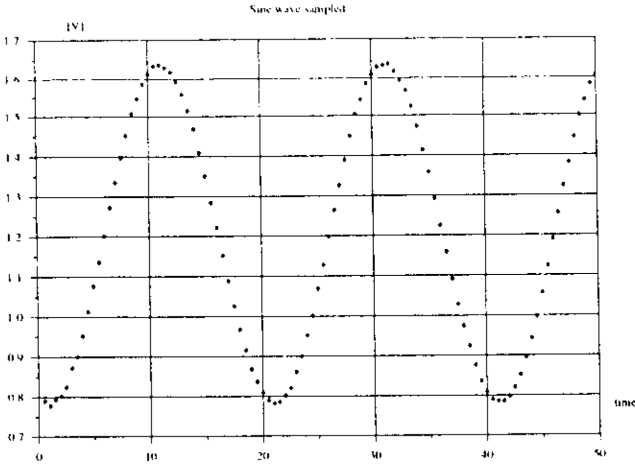


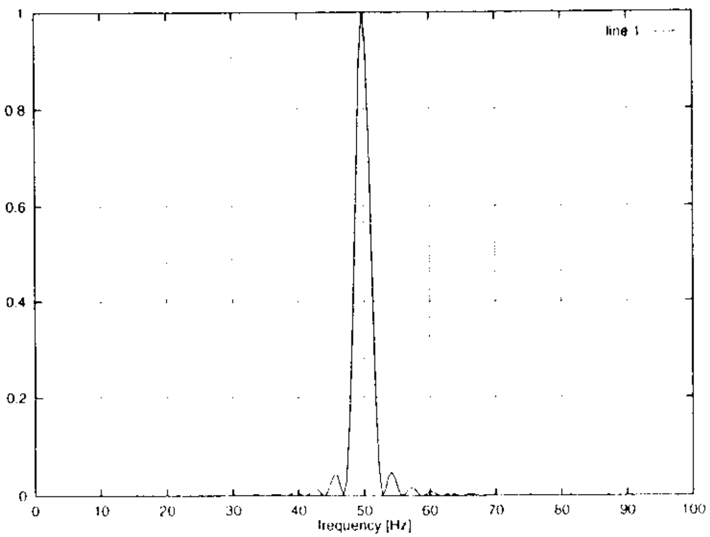

***Vin VS CODE OUT***



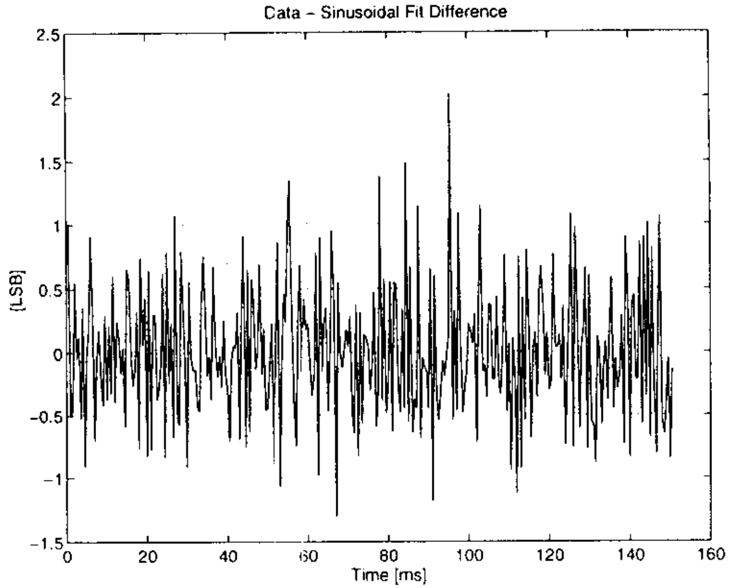

***INL error***

# *Dynamic Tests: Sine Wave Input*



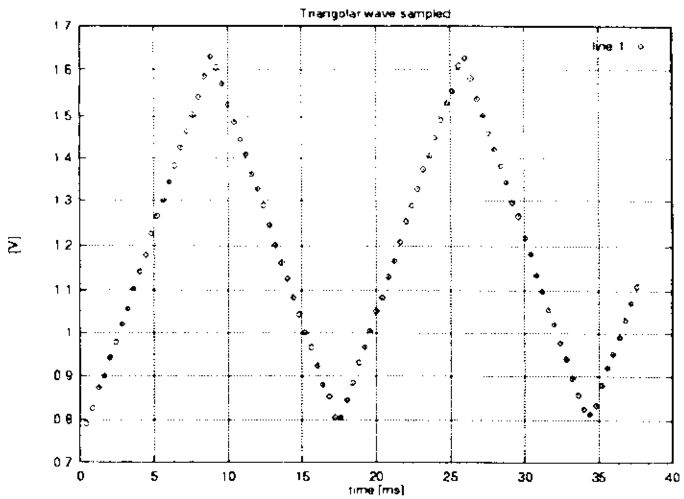



***FFT OF SAMPLED DATA***



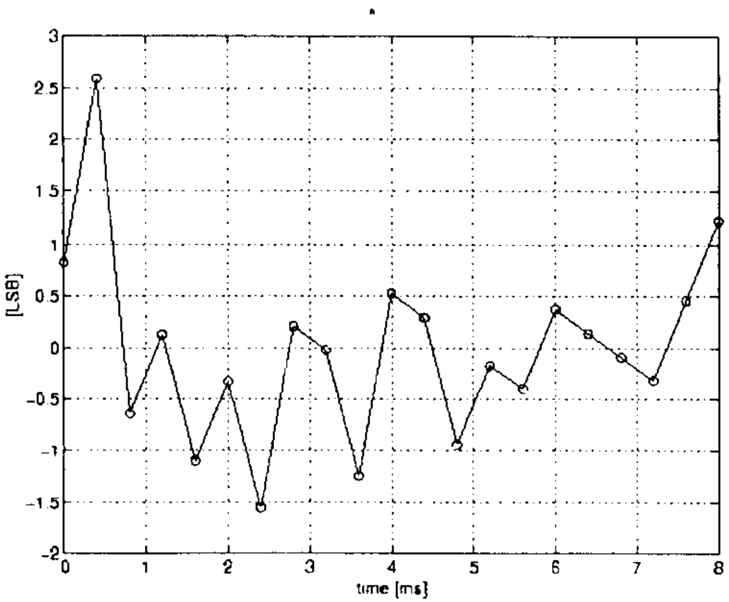

***SAMPLED DATA - SINUSOIDAL FIT DIFFERENCE***

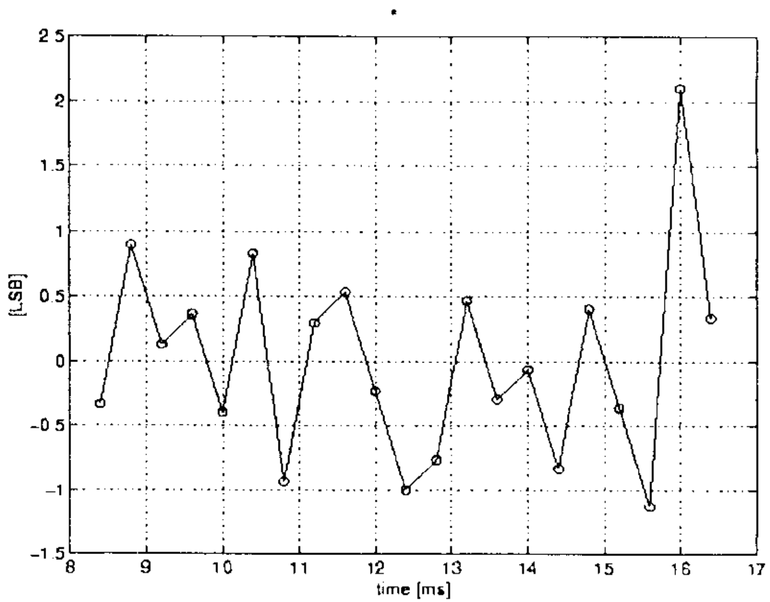
# *Dynamic Tests: Triangular Wave Input*




| input signal: Triangular wave | | |
|---|---|---|
| Freq. | = | 50 Hz |
| Voff | = | 1.190 V |
| Vmax | = | 1.640 V |
| Vmin | = | 0.780 V |
| Vpp | = | 860 mV |

| ADC sets | | |
|---|---|---|
| F_clock | = | 20 KHz |
| F_sample | = | 2.5 KHz |
| T_sample | = | 0.4 ms |
| Vsupply | = | 2.7 V |
| Temp | = | 25 °C |




*Sampled Data - Linear Fit Difference (Positive and Negative Slope)*

# APPLICATION INFORMATION