united nations educational, scientific and cultural organization
international atomic energy agency
the
abdus salam
international centre for theoretical physics

301/1152-5

Microprocessor Laboratory
Sixth Course on Basic VLSI Design Techniques
8 November - 3 December 1999

LOW POWER DESIGN
&
POWER ESTIMATION

Nizar ABDALLAH
Actel Corporation
955 East Arques Avenue
Sunnyvale, 94086-4533 California
U.S.A.

These are preliminary lecture notes intended only for distribution to participants.

Actel

Low Power Design
&
Power Estimation

Nizar Abdallah

Actel

Outline

- ❑ Motivation for Power Tools
- ❑ Low-Power Design Methodology
- ❑ Principles for Power Reduction
- ❑ Principles for Power Estimation
- ❑ Conclusion

Motivation for Power Tools

Deep-Submicron Technologies

↓

Higher Density and Performance Capabilities
(FPGAs: 100 000 Gates; 100 MHz Clock rates)

↓

Power Dissipation Problem

Motivation for Power Tools

4 times / 3 Years Increase for the last 20 Years

❑ PowerPC / Motorola	8.5 Watts
❑ Pentium / Intel	16 Watts
❑ Alpha / Dec	30 Watts
❑ Alpha 300 Mhz / Dec	50 Watts

Motivation for Power Tools

Power = Cost
For Major Applications Today

- Battery Lifetime (Cellular, Medical, ...)
- Packaging Cost
- Reliability (Time to Failure)
- Green PC program (< 30 Watts)

Motivation for Power Tools

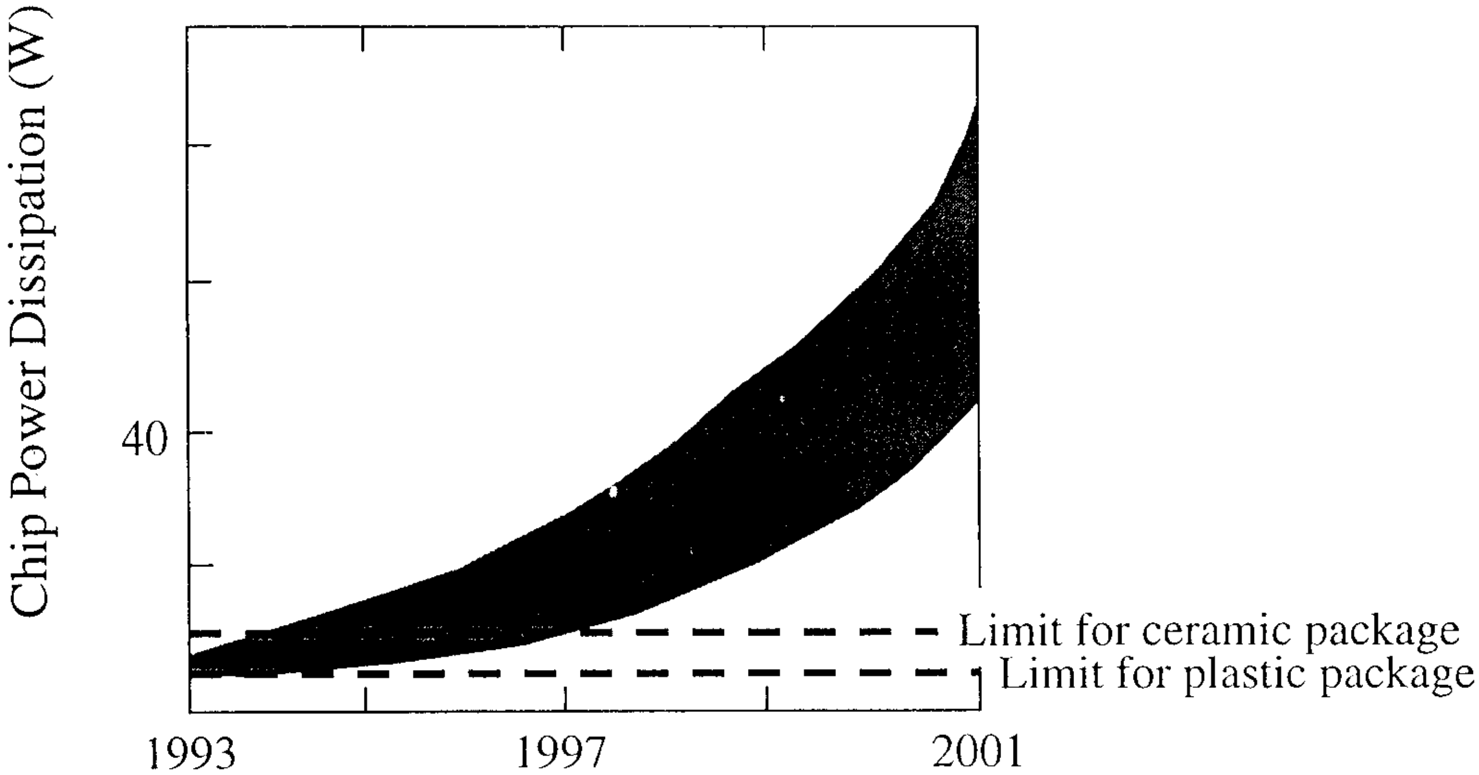
Power = Less Performance

- Clock Frequency
- Temperature Increase
- Electromigration

Nizar Abdallah

Motivation for Power Tools

Packaging Cost is an Issue



Actel Motivation for Power Tools

Today…

Design Win = f(performance, cost)

Tomorrow…

Performance = f(Power, ...)

cost = f(Power, ...)

Design Win will also be low-power dependent

Nizar Abdallah

Motivation for Power Tools

We Need...

✓ Low Power Design Methodology

✓ Power Estimation Tools

✓ Power Optimization Tools

Methodology

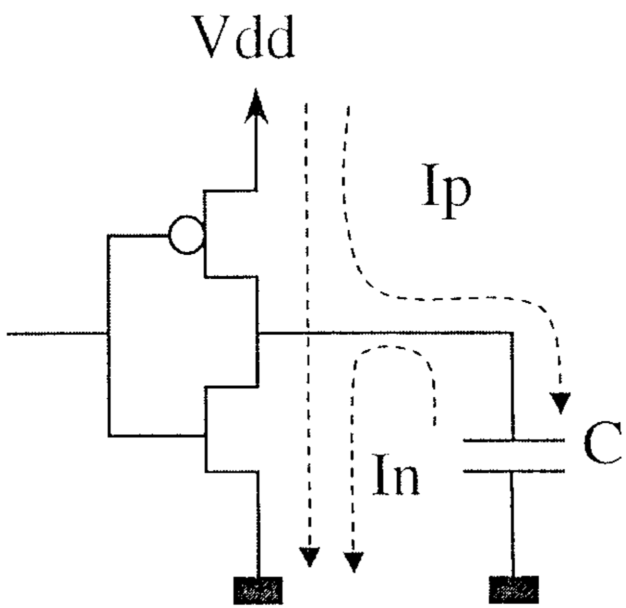
Analogous to Timing Methodologies

✓ All Levels of Abstraction

✓ Back-Annotation from physical Design

Sources of Power Consumption

- Dynamic Power (70-90%)
  (Switching activity)
- Short-Circuit Power (10-30%)
- Leakage Power (<5%)
  (Important for battery lifetime)



Nizar Abdallah

Expression for CMOS Power

- Gate Generating a Simple Clock Signal with Frequency f

$$P_{average} = C\,V_{dd}^{2}\,f$$

- In general, a signal with a transition density D

$$P_{average} = 1/2\,C\,V_{dd}^{2}\,D$$

Power Reduction

$$P_{average} = 1/2\ C\ V_{dd}^2\ D$$

- Reducing Switching Activity
  Prevent glitches (Architecture, Synthesis, ...)
  20% of power increase due to glitches

- Reducing Load Capacitance
  Gate sizing, Low-Power cell library
  Circuit techniques (Pass-Transistor, ...)

- Reducing Supply Voltage
  Drawback: Circuit delay increases

Nizar Abdallah

Two Problems

- Design Dependent
  Tools Should be Available to the Customer

- Input Pattern Dependent (more Central Problem)
  Difficult when the application is not known
  A good vector set may be very long

High-Level Power Estimation

- FPGA: Block Macromodels Available
  Problem to estimate net consumption
- Models for Logical Level, RTL Level, Behavioral Level
  Need for a power cost function

What About Accuracy and Improvements?

Assuming we Have a represetative Vector Set,

❑ Low-Level Timing Simulation	10% from Spice
❑ Low-Level Static Technique	20-60% from Spice
❑ Low-Level Dynamic Technique	10-20% from Spice

Improvement

❑ At the Logical Level is About	5%
❑ At the RTL Level May Reach	90%

Conclusion

- Power Consumption Issues Can no Longer be Ignored for High Density FPGA Design
- Timing / Power : The same challenge
  - Input pattern dependency
  - All abstraction levels
  - Power and timing constraints
  - Net consumption is becoming very significant
- DPCS IEEE 1481 is also for Power
- A Balance between Power, Area, and Delay
- Absolute Accuracy is not a Critical Issue

FPGA Solutions

Nizar Abdallah

Motivation

- Cost (Small Series, New Designs, ...)
- Rapid Prototyping
- Emulators
- Development Time
- Test Time

Motivation

- Relatively High Density (100 000 Gates)
- Relatively High Performance Capabilities (100MHz)

Nizar Abdallah

Actel

Motivation

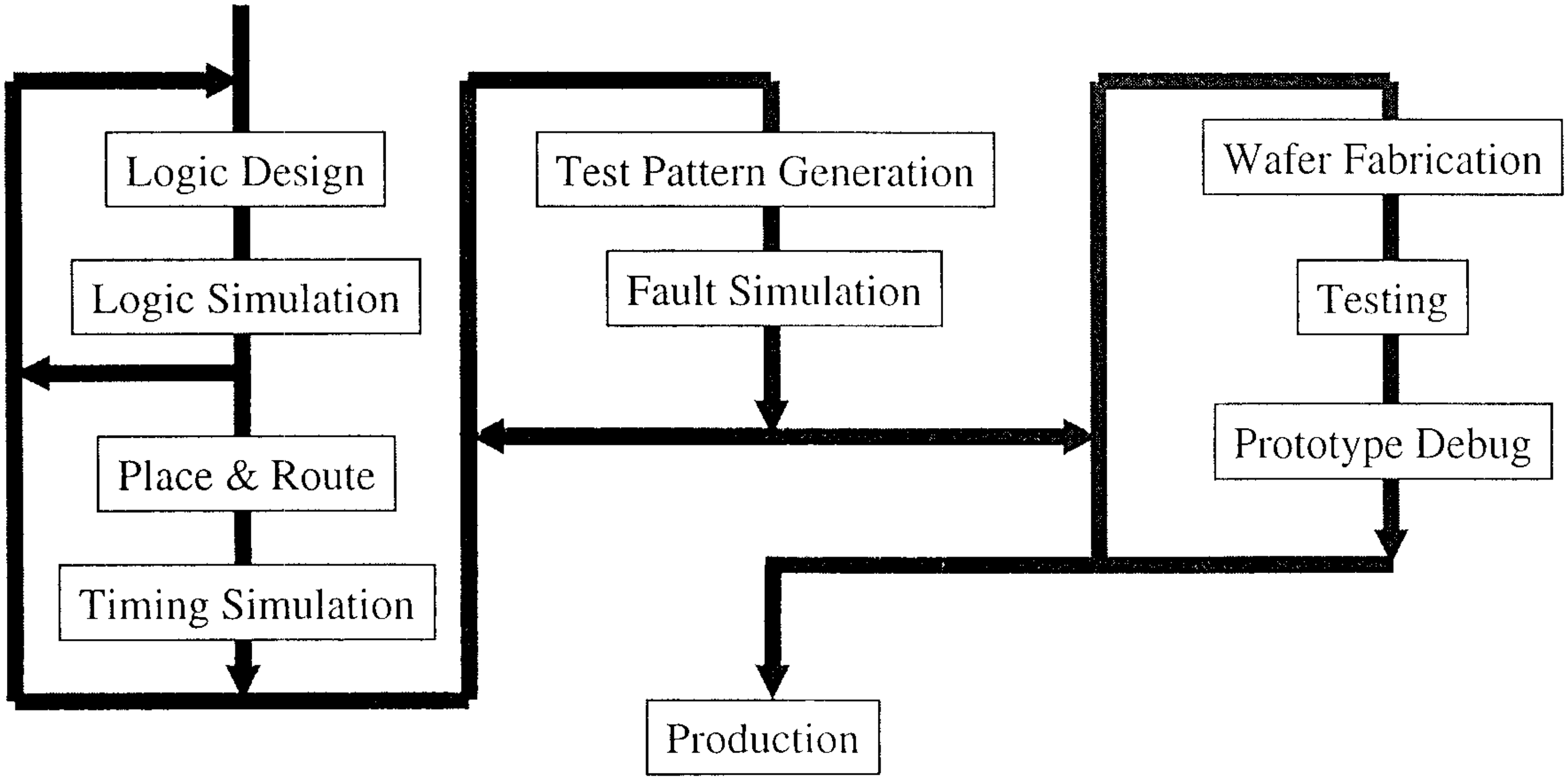
- Market in 1993 : $539M
- Market in 1998 : $2124M
- Annual Growth Rate of 32%

Nizar Abdallah

Sales

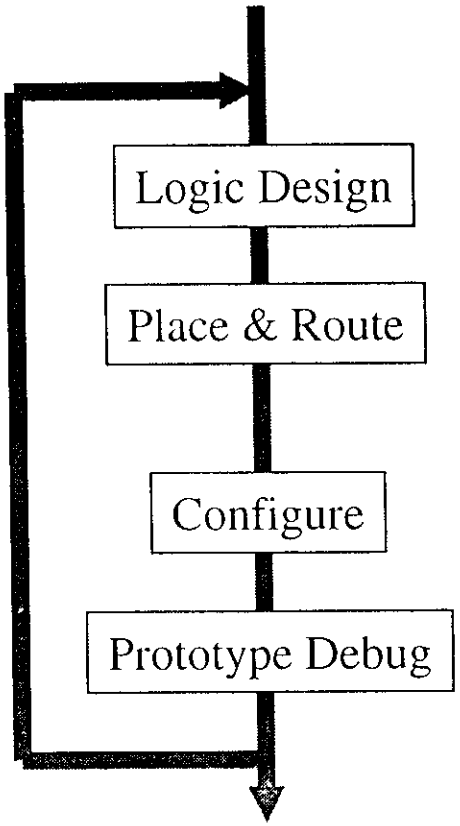
❑ Actel	$151.3M
❑ Altera	$639.0M
❑ Xilinx	$610.6M

Typical ASIC



Nizar Abdallah

FPGA



Actel

Performance

- Relatively High Density (100 000 Gates)
- Relatively High Performance Capabilities (100MHz)

Nizar Abdallah

Actel

Memory Based Architecture

Can be ...

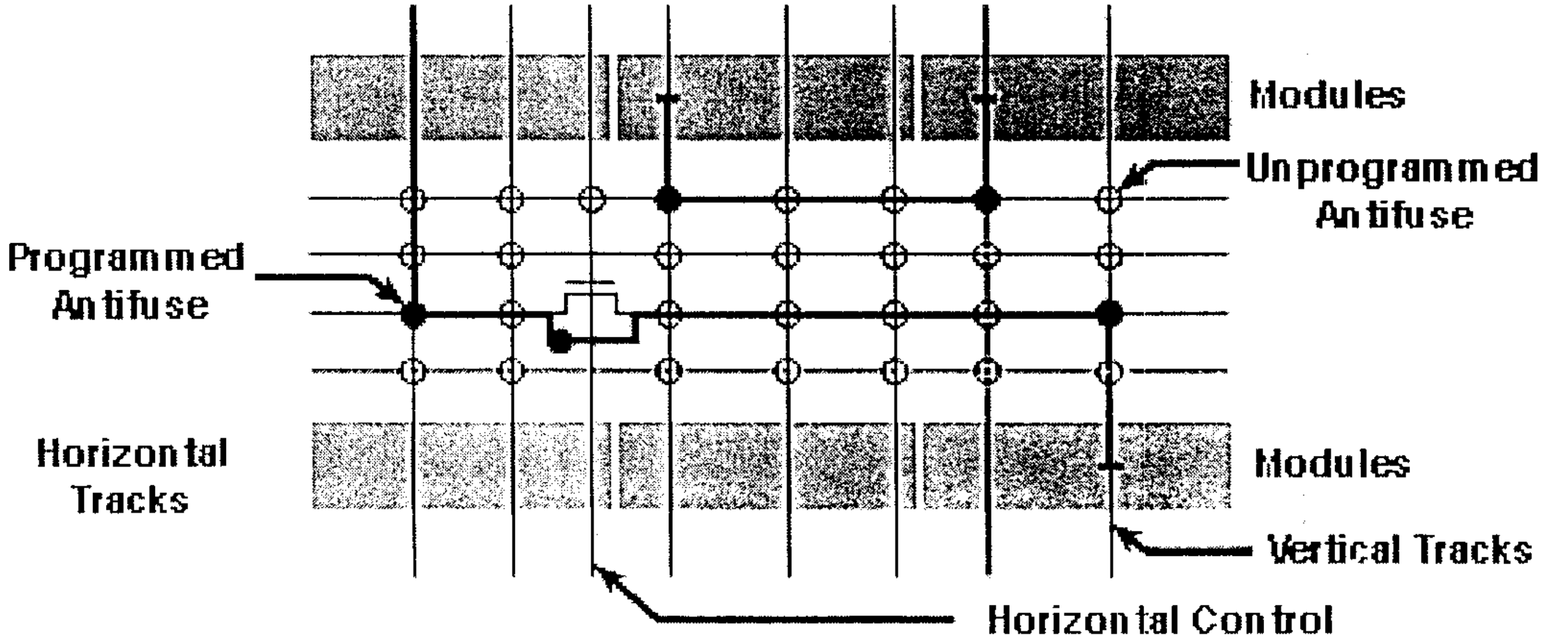
- ❑ Changed During the Development
- ❑ Updated after Delivery to the Customer
- ❑ Purchased in Larger Quantities
- ❑ Reused (No Inventory if not Sold)
- ❑ Fully Tested Prior to Delivery

One-Time Architecture (Antifuse)

Have ...

- Higher Speed (Less RC Delays on the Interconnections)
- High Reliability
- No Time-Delay to Reload the Interconnection Information (Available Immediately on Power-Up)

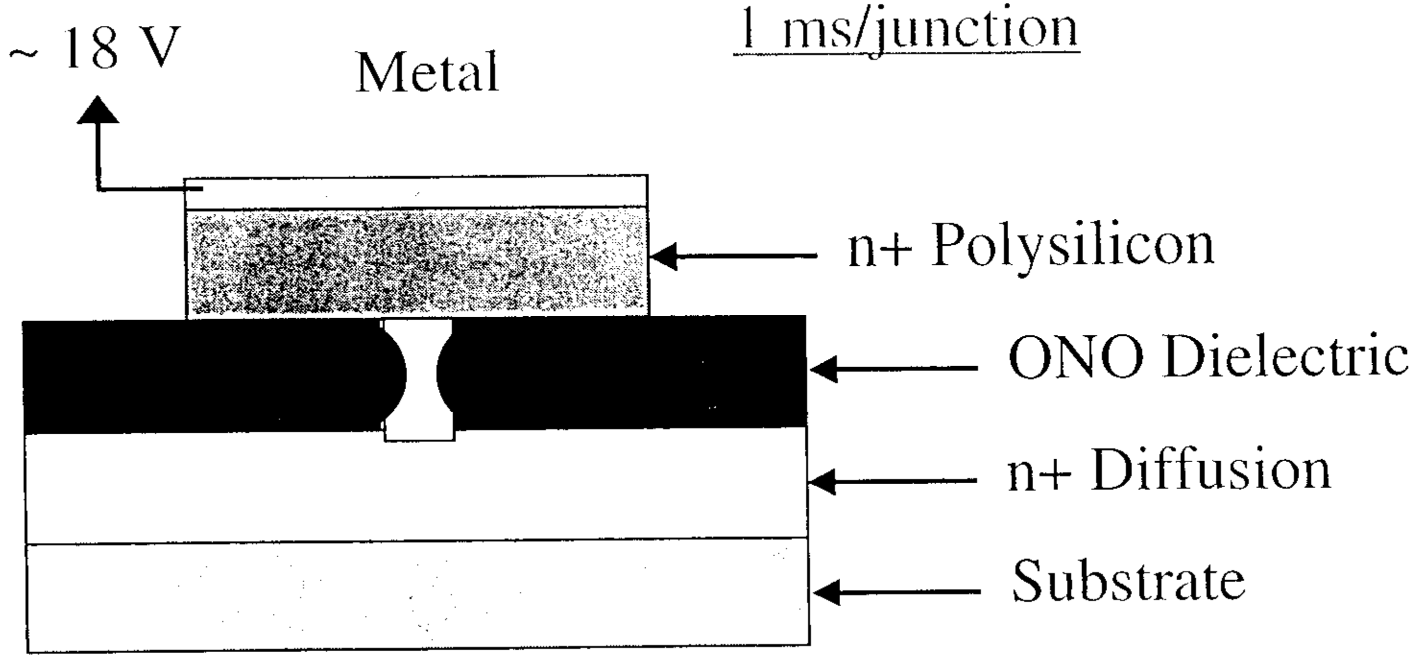
Actel Antifuse



Nizar Abdallah

Actel PLICE Antifuse

Programmable Low Impedance Circuit Element



Open Resistance = 10s of MOhms
Short Resistance = 500 Ohms

Nizar Abdallah

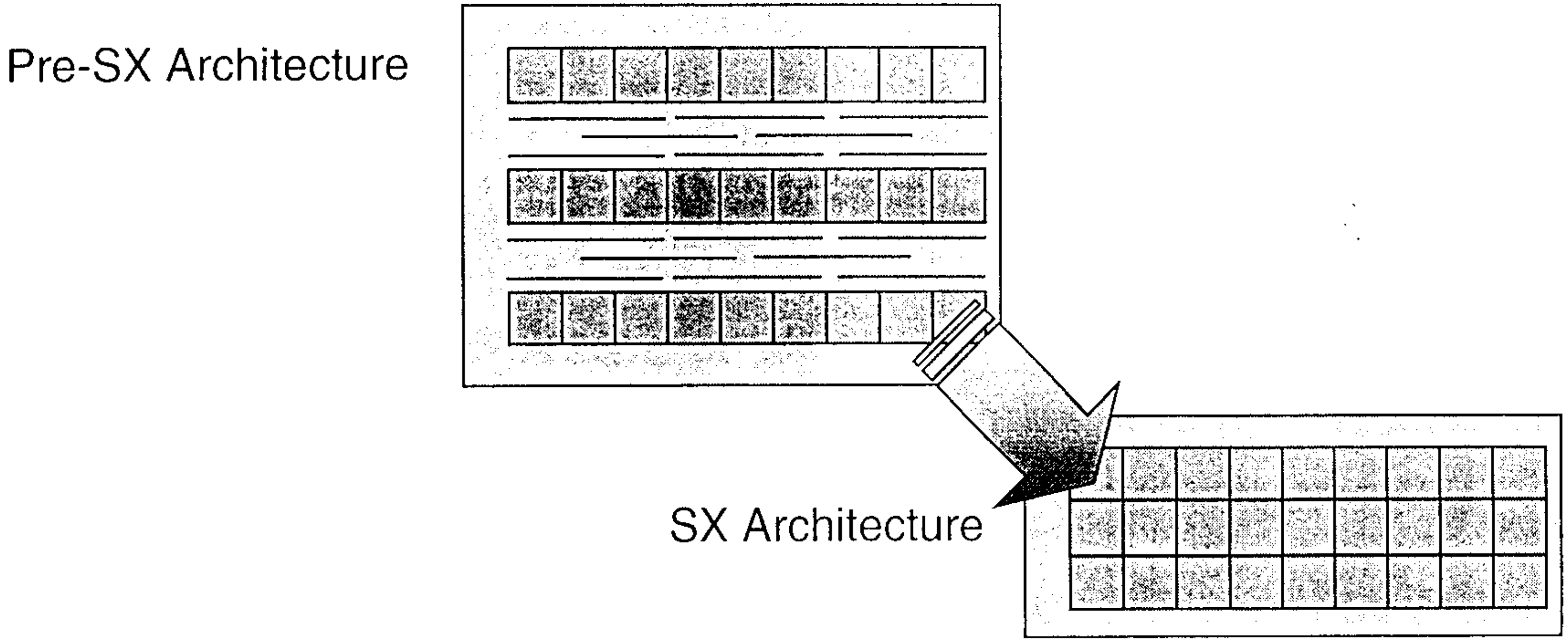
Features

- ❑ 2 Global Clocks
- ❑ PCI Compliant I/O
- ❑ Mixed Voltage Operation
- ❑ Built-In JTAG

- ❑ More Routing Resources
- ❑ New Antifuse
- ❑ New Architecture

SX Family

Routing Interconnects are Above Logic Modules



A 0.6 Micron Technology

SX Routing Resources

Direct Connects

- Connects Combinatorial Cell (C-Cell) to its Adjacent Sequential Cell (R-Cell)
- No Antifuses
- 0.1 ns Routing Delay

SX Routing Resources

Fast Connects

- Every Cell Output Connects to One
- Accessible by Cells in the Same Cluster or the One Below by One Antifuse
- 0.4 ns Routing Delay

SX Parts

Part#	SX08	SX16	SX16P	SX32	SX64
Gates	8,000	16,000	16000	32,000	64,000
MaxIO	129	177	177	246	340
Rcells	256	528	528	1080	2160
CCells	512	924	924	1800	3600
Availb.	98	98	98	98	99

ALLIANCE Web Site

http://www-asim.lip6.fr

Nizar Abdallah

Good Luck...