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THIRD COLLEGE ON MICROPROCESSORS:
TECHNOLOGY AND APPLICATIONS IN PHYSICS

7 October - 1 November 1985

SYNCHRONOUS AND ASYNCHRONOUS MACHINES

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Synchronous and asynchronous machines

All processors are normally made of two types of fundamental blocks:

- MASTER
- SLAVES

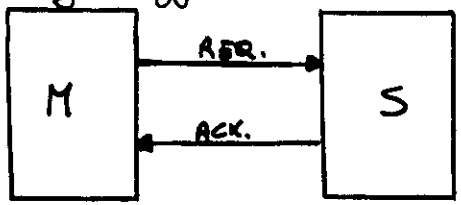
Master units (CPUs , DMA controllers etc) govern the data movement in the system.
Slave units (memory , I/O) are normally storage of data to be used by masters.

How can we connect masters and slaves in order to assure proper data transfer between them?

- SYNCHRONOUS
- ASYNCHRONOUS

- SYNCHRONOUS: In a synchronous system the data transfer between a M and a S (read or write) is simply started from the M who assumes to have an answer from the S within a guaranteed time. That implies that systems have to be built such that the slowest S governs the speed of it.

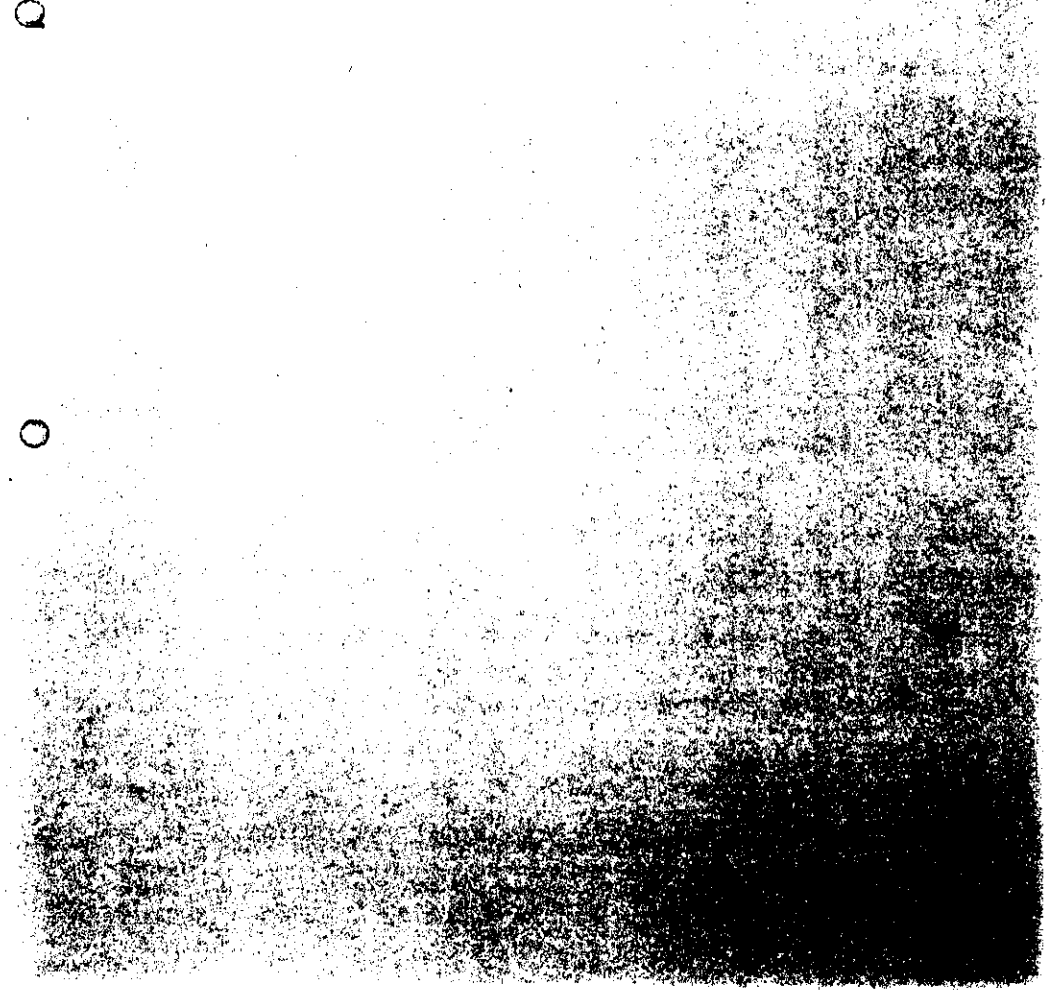
- ASYNCHRONOUS: For asynchronous systems data transfer operations are also started from the M, but now he waits until the S responds (acknowledges) that the desired operation has been performed. In this way the master adapts automatically to the speed of different slave units.



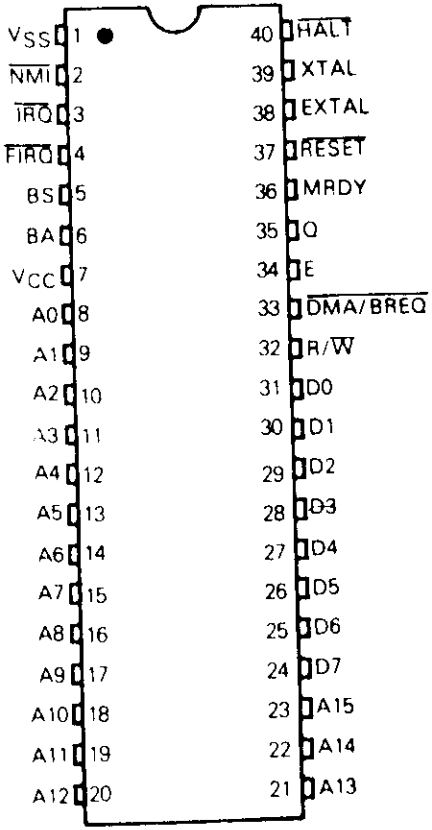
M 6809

- Non-multiplexed address-data lines
- Linear addressing to 65536 memory locations
- Synchronous processor
- No need for external bus controller
- No need for external timing controller

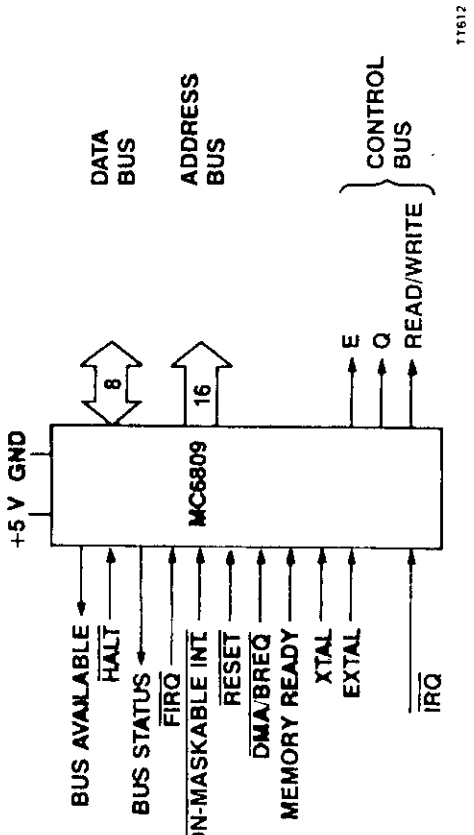
} HARDWARE IS SIMPLE



PIN ASSIGNMENT



MC6809 BUS & CONTROL SIGNALS



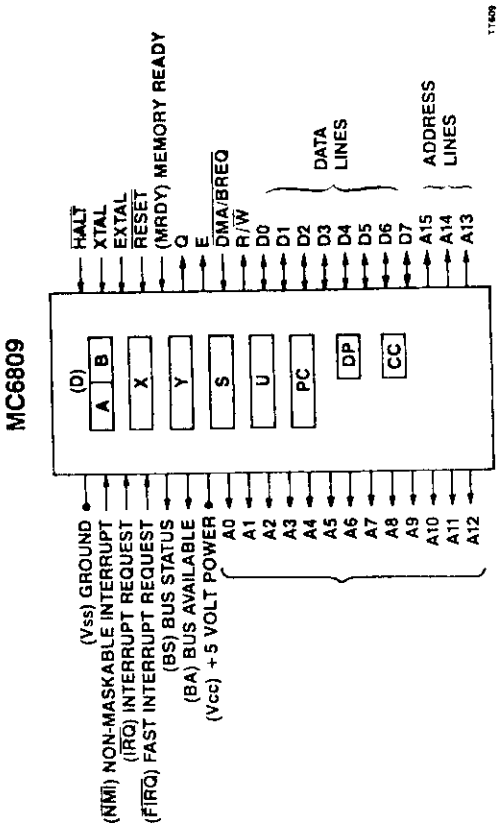
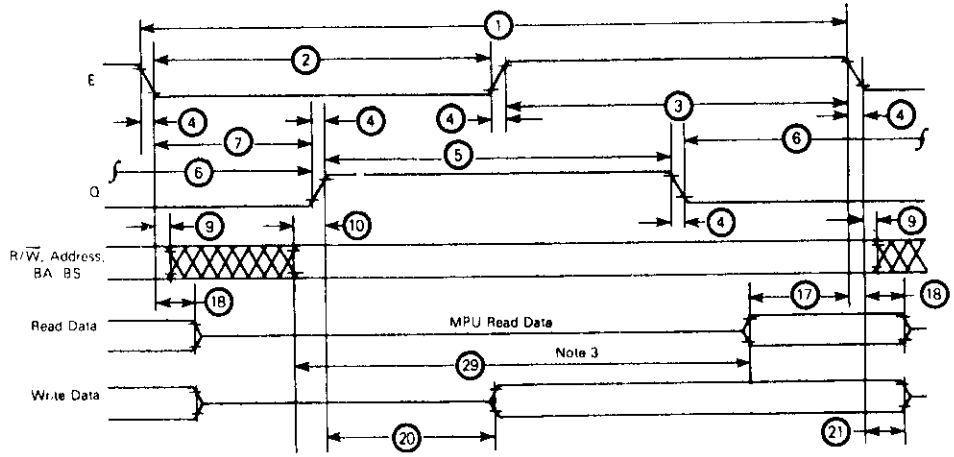


FIGURE 1 – BUS TIMING



BUS TIMING CHARACTERISTICS (See Notes 1 and 2)

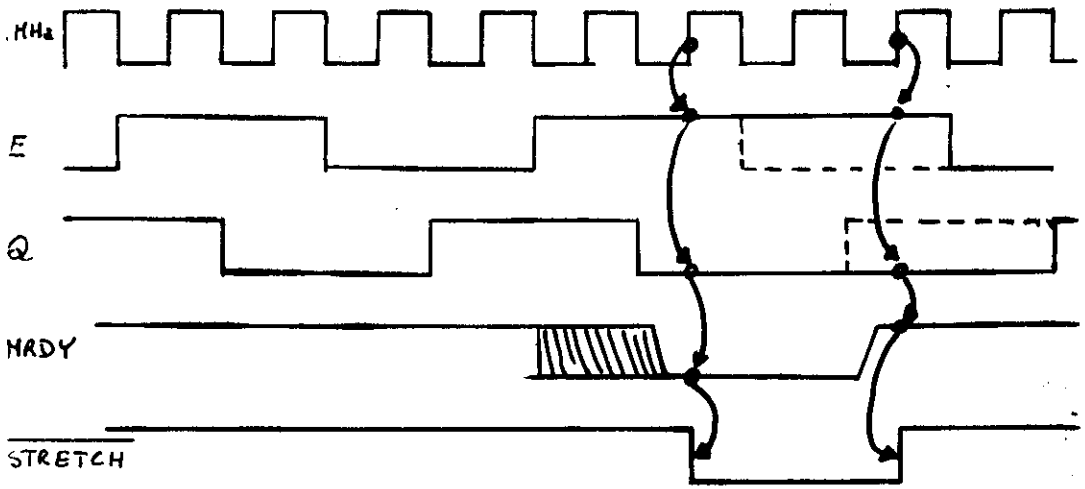
Ident. Number	Characteristics	Symbol	MC6809 Min	MC6809 Max	MC68A09 Min	MC68A09 Max	MC68B09 Min	MC68B09 Max	Unit
1	Cycle Time (See Note 5)	t_{cyc}	1.0	10	0.667	10	0.5	10	µs
2	Pulse Width, E Low	PW_{EL}	430	5000	280	5000	210	5000	ns
3	Pulse Width, E High	PW_{EH}	450	15600	280	15700	220	15700	ns
4	Clock Rise and Fall Time	$t_{r,\,tf}$	–	25	–	25	–	20	ns
5	Pulse Width, Q High	PW_{QH}	430	5000	280	5000	210	5000	ns
6	Pulse Width, Q Low	PW_{QL}	450	15600	280	15700	220	15700	ns
7	Delay Time, E to Q Rise	t_{AVS}	200	250	130	165	80	125	ns
9	Address Hold Time* (See Note 4)	t_{AH}	20	–	20	–	20	–	ns
10	BA, BS, R/W, and Address Valid Time to Q Rise	t_{AQ}	50	–	25	–	15	–	ns
17	Read Data Setup Time	t_{DSR}	80	–	60	–	40	–	ns
18	Read Data Hold Time*	t_{DHR}	10	–	10	–	10	–	ns
20	Data Delay Time from Q	t_{DDQ}	–	200	–	140	–	110	ns
21	Write Data Hold Time*	t_{DHW}	30	–	30	–	30	–	ns
29	Usable Access Time (See Note 3)	t_{ACC}	695	–	440	–	330	–	ns
	Processor Control Setup Time (MRDY, Interrupts, DMA/BREQ, HALT, RESET) (Figures 6, 8, 9, 10, 12, and 13)	t_{PCS}	200	–	140	–	110	–	ns
	Crystal Oscillator Start Time (Figures 6 and 7)	t_{RC}	–	100	–	100	–	100	ms
	Processor Control Rise and Fall Time (Figures 6 and 8)	t_{PCr}, t_{PCf}	–	100	–	100	–	100	ns

*Address and data hold times are periodically tested rather than 100% tested.

NOTES:
1. Voltage levels shown are $V_L \le 0.4$ V, $V_H \ge 2.4$ V, unless otherwise specified.
2. Measurement points shown are 0.8 V and 2.0 V, unless otherwise specified.
3. Usable access time is computed by 1 – 4 – 7 max + 10 – 17
4. Hold time (9) for BA and BS is not specified
5. Maximum t_{cyc} during MRDY or DMA/BREQ is 16 µs.

Peripherals need also to be faster.

MC 6809E CLOCK GENERATOR TIMING



MC 6809E Special signals

E, Q are input signals

TSC (Three state control) used in multiprocessor applications

LIC (Last instruction cycle) indicates instruction fetch cycle

AVMA (Advanced VMA) indicates that the MPU will use the next bus cycle

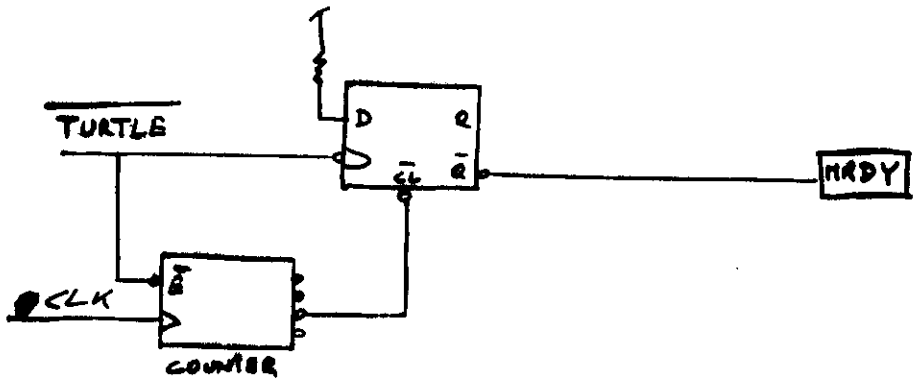
BUSY indicates the need of the bus by the MPU during complex instructions (like RMW and indirect instructions) used for arbitration in multiple MPU systems

MC6809 and Slow devices

If you plan to connect to your 6809 system a very slow device ($t_{acc} > 500$ ns) it is possible to make the 6809 look like a semi-asynchronous machine by using the MRDY signal.

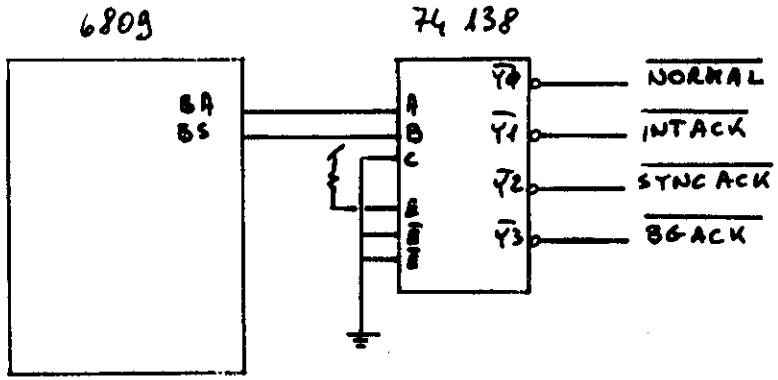
The MRDY line, when pulled down, stretches the current memory cycle. The MRDY line is sampled from the processor at a speed of 4x Basic clock.

Practical implementation:

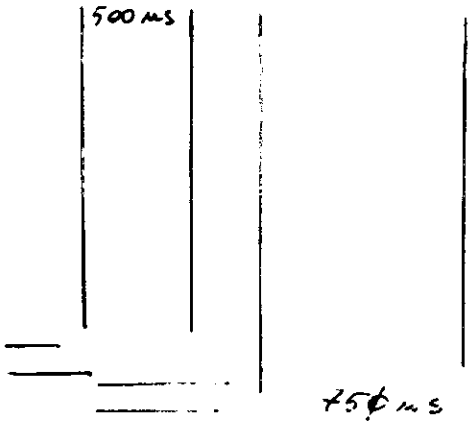


MPU State Definition

BA	BS	MPU State
ϕ	ϕ	NORMAL
ϕ	1	INTERRUPT OR RESET ACK.
1	ϕ	SYNC ACK.
1	1	HALT OR BUS GRANT ACK



On a 1 MHz system



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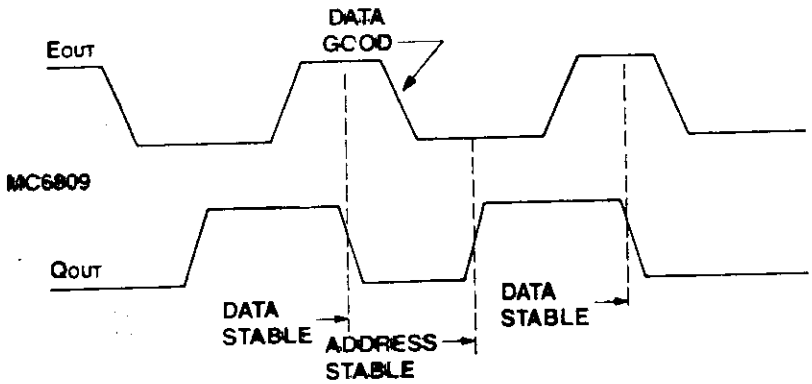
MPU CLOCK WAVE FORM



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INSTRUCTIONS TIMING

The MC6809 is a synchronous machine.

☞ timing is very easily known

A 4 MHz clock quartz a 1 MHz system clock, so the basic machine cycle is 1µs.

How to find execution timing:

1. MC6809 reference card
2. Assembler listing

Example:

INSTR	#bytes	#cycles
CMPA <$F3	2	4
LEAY 5,Y	2+0	4+1
LDA #1	2	2
LDA [$200,PCR]	2+2	4+8
SWI	1	13

CHARACTERISTICS OF THE MC6809

Example for a delay loop:

```
DELAY   EQU  *          _
        PSHS X          _
        LDX  #N         _
LOOP    LEAX -1,X       _
        BNE  LOOP       _
        PULS X,PC       _
                        ____
```

µs

CYCLE BY CYCLE OPERATION

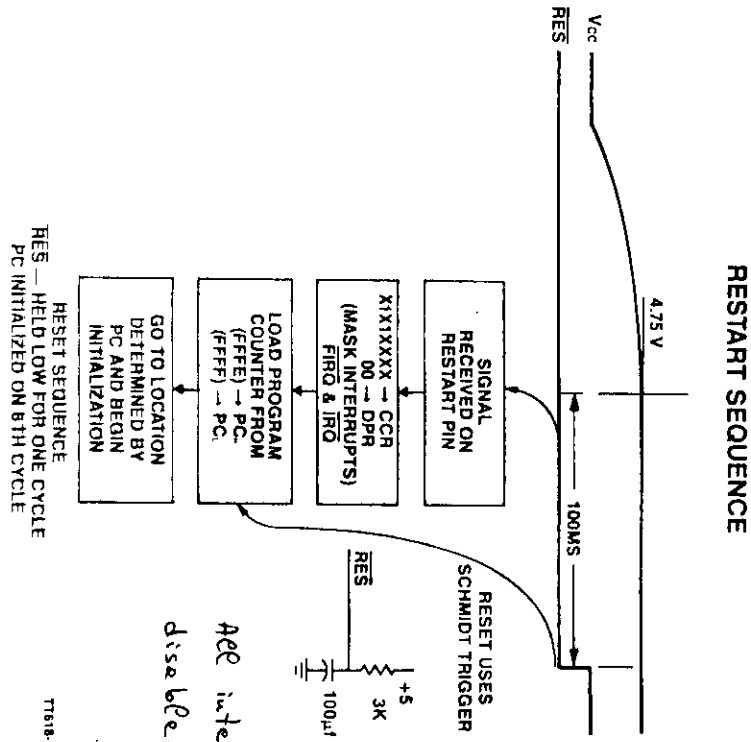
$1000 ASL $3000

⋮

$3000 $01

CYCLE#	ADDRESS	DATA	R/$\overline{W}$	
1	1000	78	1	OPCODE FETCH
2	1001	30	1	OPERAND ADDRESS
3	1002	00	1	...
4	FFFF	*	1	$\overline{VMA}$ CYCLE
5	3000	01	1	DATA READ
6	FFFF	*	1	$\overline{VMA}$ CYCLE
7	3000	02	ϕ	DATA WRITE

RESTART SEQUENCE



ACC interrupts are disabled until first LDS !

6809E CLOCK GENERATOR