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INTERNATIONAL CENTRE FOR THEORETICAL PHYSICS

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24 - 26 July 1972

(SUMMARIES)

INTERNATIONAL ATOMIC ENERGY AGENCY

UNITED NATIONS EDUCATIONAL, SCIENTIFIC AND CULTURAL ORGANIZATION

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Please note that copies of papers referred to may be obtained direct from the authors and not from the ICTP.

COINCIDENT REDUNDANT MULTIPLEX TRANSMISSION OF INFORMATION IN NEURAL NETWORKS

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Although it was known from the works of von Neumann that all complex automata, and neural networks especially, must work redundantly, it has never been explained how redundant transmission of information in neural networks is performed and how one communication line can be used as the communication line for many information sources.

The solution of this problem was found in the coincident redundant multiplex transmission of the information by which one communication line transmits simultaneously the signals from many information sources (multiplexy!) but at the same time signals from every information source are transmitted by means of many communication lines (redundancy!). At the end of the redundant multiplex transmission of information many combinations of exit lines are performed. In every combination where the signals from the same information source appear (reaching the combination through different lines) there is a precise time coincidence between gemini signals (coincidence!). This time coincidence of the redundant (i.e. gemini) signals performs the very original, simple and effective demultiplex operations at the end of the coincident redundant multiplex transmission of information.

The theory of the coincident redundant multiplex has its implications in perceptron theory, the creation of Hebb's cell assemblies, the processing and coding of information in neural networks, and telecommunication measurements with many parameters, for instance, in artificial satellites and prototypes of intercontinental missiles.

The proof for the theory of the coincident redundant multiplex is found in physiological data and is illustrated in two diagrams and in a hardware model.