INTERNATIONAL ATOMIC ENERGY AGENCY
UNITED NATIONS EDUCATIONAL, SCIENTIFIC AND CULTURAL ORGANIZATION

INTERNATIONAL CENTRE FOR THEORETICAL PHYSICS
34100 TRIESTE (ITALY) - P.O.B. 586 - MIRAMARE - STRADA COSTIERA 11 - TELEPHONE: 2240-1
CABLE: CENTRATOM - TELEX 460392-1

SMR.300 - 13

COLLEGE ON MEDICAL PHYSICS

10 October - 4 November 1988

Scintillation Detector System

Y. XIE
IAEA, Siebersdorf Laboratory, Austria

APPENDIX 1

SCINTILLATION DETECTOR SYSTEM

1. General

The detector supplied with the Single Channel Analyzer Eurocard System is a 2" x 2" NaI(TC) crystal, coupled to a 2" photomultiplier and built within a single container (mfg. BICRON Corp., Newburg USA, model no. 2M2/2-X). Also supplied a BICRON PM-tube base with Voltage Divider and Preamplifier model PA-14. The description and circuit diagram of the PA-14 is included as annex, also a data sheet of the photomultiplier. In case of troubles together with the amplifier 102 of the single channel analyzer system the PM-tube base with voltage divider and preamplifier PA-14 has to be modified. A filter is inserted in the high voltage line and/or the charge sensitivity of the preamplifier has to be reduced.

2. Modification of the PM-tube base assembly (see circuit diagrams)

2.1 Ripple Filter

- unscrew the two small nuts from the gain pot. (R2) and focus pot. (R1) on the top of the PA-14 and remove carefully the metal can.
- remove (unwind) the insulation tape.
- remove (unsolder) C1 underneath the gain pot. R2.
- remove the connection from R2 to the HV plug.
- insert the resistor R22 (220 kohms/0.3W) between HV-plug and pin 1 (pin 2) of R2 (use one lead of R22 to shorten pin 1 to pin 2).
- place the capacitor C10 (0.01µF/3kV) underneath R2. Solder one lead to pin 1 of R1 (ground) as short as possible, solder the other lead to pin 3 of R2.
- wrap the thin plastic sheet or insulation tape around the assembly and put it carefully back into the metal can.
- screw on and tighten the two nuts to fix the can.
- plug the dynode chain assembly onto the PMT.

The detector is now ready for use with an amplifier 102.

2.2 Charge sensitivity resp. decay time constant of the preamplifier

It is recommended to apply a HV-voltage of 600 - 800 Volts to the photomultiplier. For higher γ-energies the min. gain of the Amplifier 102 is still too high, therefore the charge sensitivity of the preamplifier should be reduced.

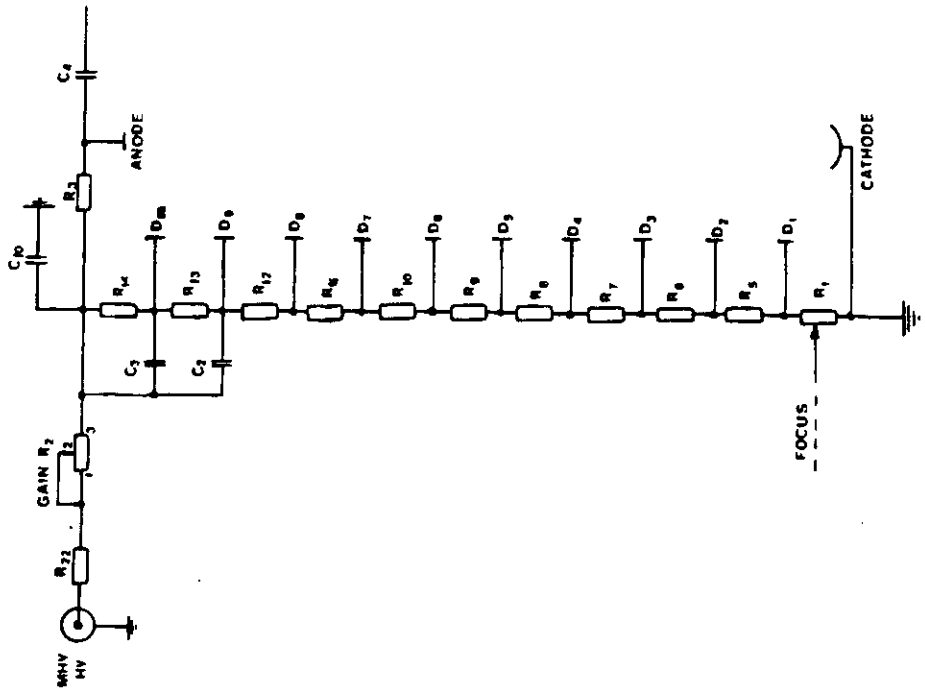
recommended values:

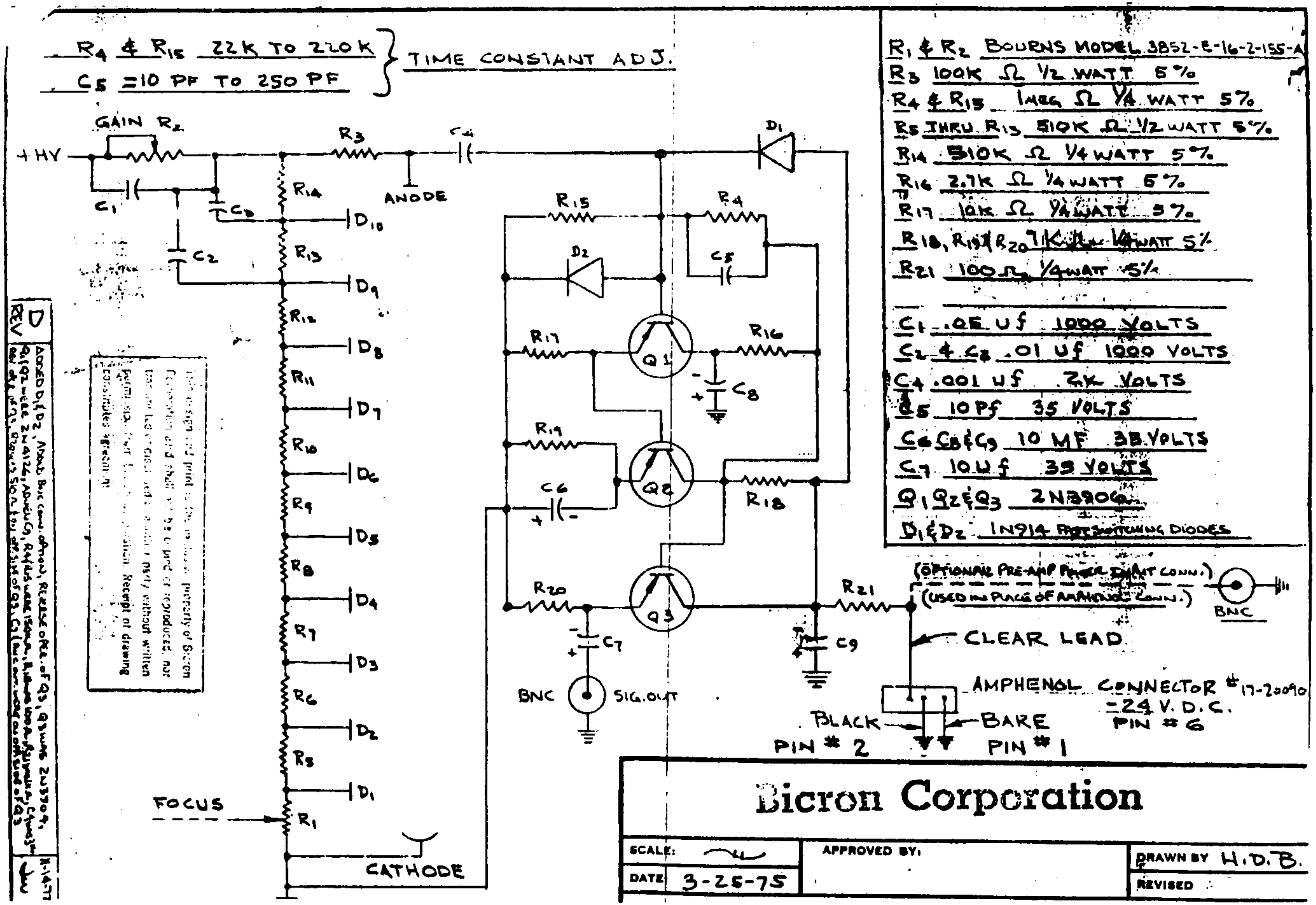
charge sensitivity	20mV/pico coulomb
decay time constant	2 - 4 µs

Note: Don't change the ratio of R4/R15

shaping time of 102	1 - 2 µs

Modified circuit diagramm of PA-14




R4 & R15 22K TO 220K
C5 =10 PF TO 250 PF
TIME CONSTANT ADJ.
GAIN R2
+HV
R3
C4
ANODE
C1
C3
C2
R14 R13 R12 R11 R10 R9 R8 R7 R6 R5 R1
D10 D9 D8 D7 D6 D5 D4 D3 D2 D1
FOCUS
CATHODE
R15
R4
D2
C5
D1
R17
R16
Q1
C8
R19
Q2
C6
R18
R20
Q3
C7
BNC
SIG.OUT
C9
R21
(OPTIONAL PRE-AMP POWER INPUT CONN.)
(USED IN PLACE OF AMPHENOL CONN.)
BNC
CLEAR LEAD
AMPHENOL CONNECTOR #17-20090
-24 V.D.C.
PIN #6
BLACK
BARE
PIN # 2
PIN # 1
R1 & R2 BOURNS MODEL 3852-E-16-2-155-A
R3 100K Ω 1/2 WATT 5%
R4 & R15 1MEG Ω 1/4 WATT 5%
R5 THRU R13 510K Ω 1/2 WATT 5%
R14 510K Ω 1/4 WATT 5%
R16 2.7K Ω 1/4 WATT 5%
R17 10K Ω 1/4 WATT 5%
R18, R19 & R20 1/4 WATT 5%
R21 100 Ω 1/4 WATT 5%
C1 .05 uf 1000 VOLTS
C2 & C3 .01 uf 1000 VOLTS
C4 .001 uf 2K VOLTS
C5 10 Pf 35 VOLTS
C6 C8 & C9 10 MF 35 VOLTS
C7 10 uf 35 VOLTS
Q1 Q2 & Q3 2N3906
D1 & D2 1N914 FAST SWITCHING DIODES
REV D
Bicron Corporation
SCALE:
APPROVED BY:
DRAWN BY H.D.B.
DATE 3-25-75
REVISED

APPENDIX 2

BICRON CORPORATION
MODEL PA-14
SCINTILLATION VOLTAGE DIVIDER & PREAMPLIFIER

DESCRIPTION:

Socket: Standard 14 contact Plug-on Cinch 3M-14
Voltage Divider: 10 Stage, directly compatible with all 2, 3, and 5 inch diameter PM tubes used in standard Bicron detectors.
Controls: F Focus, one turn potentiometer should be adjusted for best pulse height resolution. Note: If PM tube has an internal fixed focus, this adjustment will have no effect.
G Gain, one turn potentiometer, adjust for desired signal output amplitude.
Connectors: HV High Voltage Input
A. MHV KV-79-15 bulkhead receptacle mates with MHV plug KV-59-24 or equivalent.
or B. SHV Kings 1704-1 bulkhead receptacle. Mates with SHV plug Kings 1705-6 or equivalent.
S Signal Output: Positive polarity, BNC KC-79-43 bulkhead receptacle. Mates with BNC plug KC-59-296 or equivalent.
DC Preamp Power
A. BNC KC-79-43 bulkhead receptacle. Center conductor D.C. voltage. Coaxial braid common mates with BNC plug KC-59-296 or equivalent.
or B. Amphenol min. rac 17-90090-15 plug. Pin 6 D.C. voltage, Pin 1 common mates with amphenol min rack 17-80090-15 receptacle.

POWER REQUIREMENTS:

Pre-amp: -12V or -24V at 10 milliamps
PMT Tube Voltage Divider Bias: (Positive voltage only) Typical +500 to +1000 Volts at 150 micro-ampere. See PM tube data sheet for maximum ratings.

PREAMP SPECIFICATIONS:

Noise: Less than 50 Microvolts RMS referred to input.
Input: Direct connection from photomultiplier tube anode to charge integrating preamplifier input circuit, negative charge.
Conversion Gain: 5×10^{-11} coulombs per volt with NaI(Tl) or faster scintillators. (Gain of approximately 20)
Rise Time: 100 Nano seconds
Decay Time: 4 microseconds (internally adjustable)
Output Impedance: 92 ohms
Gain Stability: 0.25%/C from 0^{o} to 50^{o}C.
Linearity: 0.25%

PHYSICAL DIMENSION
Size: 3" long x 2¼" diameter
Weight: 6 ounces

BICRON CORPORATION
12345 Kinsman Road
Newbury Ohio 44065
(216) 564-2251

12/78

1. GENERAL DESCRIPTION

The spectroscopy amplifier 102 is two IAEA module wide unit, designed on a printed circuit board according to Eurocard format (160 x 100 mm) with the standard 64 pin connector DIN 41612c.

It can accept input pulses of the negative or the positive polarity, either in the form of the exponential function with time constant greater than 40 µs, or in the form of step functions superimposed to the ramp voltage. The later is the typical signal, when the optically coupled charge sensitive preamplifier is used. The adaptation to the "normal" or "optical" coupled charge sensitive preamplifier is made by using the front panel mode switch.

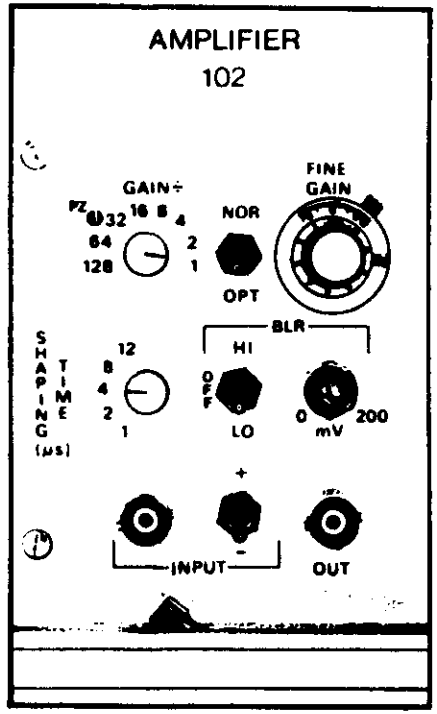


Fig. 1.1 Front panel of 102

The output pulses are unipolar with presetable width. The pulse forming is achieved through one differentiation followed by four approximate integrations with the same time constants.

There is a selection of 5 different time constants: 1,2,4,8 and 12 μs. The width of the output pulses is 2.2 x selected time constants, measured at the half of the maximum.

The true unipolar output is achieved by using the pole/zero cancellation control.

The maximum selectable gain is 3000, the minimum is 12. It can be set by division of 2 at 8 steps: 3000, 1500, 750, 375, 190, 95, 48 and 24 by the coarse gain control. Among these values, and down to 12 the gain can be varied continuously by using the fine gain control knob.

In order to keep the output DC level as stable as possible an AC coupling with a large time constant of 660 ms is introduced after the main amplification has been done. To avoid the shift problems of an ac-coupled amplifier a base line restoration system (BLR) is introduced. With the BLR active a constant current is injected into the coupling capacitor restoring the output voltage back to zero at two different rates.

It should be pointed out that the output stage is sensitive to capacitive loads. It might oscillate if too long coaxial cables are used at the output. Try to avoid them.

2. SPECIFICATIONS

Amplification	3000
Coarse regulation	Attenuated in 8 steps, by division of 2 (reduced in powers of 2)
Fine regulation	1 to 2 by ten turn potentiometer
Pulse shaping	1,2,4,8 and 12μs time constants. One active differentiation, four active integrations.
Input pulse polarity	Positive or negative
Input pulse shape	Exponential: from a normal charge sensitive preamplifier with a decay time constant > 40 μs Saw tooth, with step functions superimposed; from an optically coupled charge sensitive preamplifier
Output pulse	Unipolar, positive, saturation at 11 Volts into 1 kohms load
Base line restorer (BRL)	Modes: HIGH, OFF, LOW

3. CIRCUIT DESCRIPTION & THEORY OF OPERATION

3.1 Block diagram

The amplifier consists from 8 main building blocks shown in fig. 3.1. There are two options for the pulse processing depending on the selection of the charge sensitive preamplifier, which may by either normal or optically coupled.

At first, the processing corresponding to the pulses from the normal charge sensitive amplifier will be considered. In the first stage the amplification A=3.0 is obtained. By ten-turn pot P1 the amplification can be increased for an additional factor of 2.1.

Between this stage and the next one is an attenuator, dividing the output signal by 2,4,8 or 16. The next stage is a differential amplifier with gain A=5.7, providing the proper polarity of the output pulses by the corresponding selection of the sign of the amplification.

In the third stage with IC3 and IC4 the differentiation together with the approximate integrations is performed. In some way also the amplification A=3 can be described to this stage. As amplification, the ratio between the output pulse height and the height of the input step function is introduced.

In the next stage designed with IC5 the further variable amplification together with the pole/zero cancellation is performed. The full amplification of 6.6 can be reduced by factors of 2, 4 or 8 by a rotary switch control.

The next stage titled BLR is capacitively coupled to the previous one. The gain of this stage is 2. The gated BLR amplifier inspects the output of the BLR stage and inject a constant current charging the input capacitor and moving the BLR output voltage toward zero when the base line deviation from zero exceeds the preset value.

The BLR output signal is applied to the next stage IC11 performing double approximate integration. Due to the attenuation of the signal in this stage the gain of the output stage was selected as 1.85.

In the mode adapted to the optically coupled preamplifier the input signal enters through a capacitor providing an approximate differentation. The transfer function of this stage is FA_1^*. In this way the saturation of the first and the second stage by the ramp voltage with an amplitude of approx. 2 volts from the optically coupled charge sensitive preamplifier is avoided. However, the step function-like pulses arising from the detection of the nuclear radiation are converted into exponential tail pulses with a decay constant of 33 µs. Therefore a filter with the inverse transfer function F^{-1} is introduced in the stage 4, following the pulse shaping stage. By this filter the unipolar pulse shape is restored.

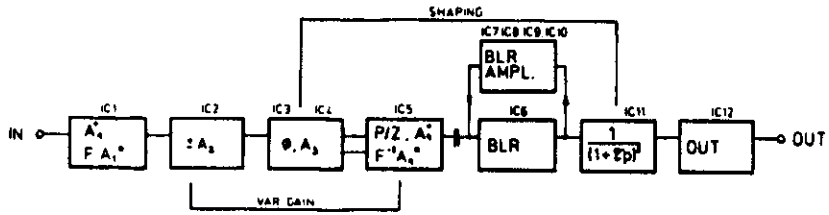


Fig. 3.1 Amplifier; block diagram

3.2 Detailed Scheme

The detailed scheme is given in Fig. 6.3. The first stage is the inverting amplifier when operating in the "NORMAL" mode. The gain is determined by the (R2+P1)/R1 ratio. By the ten turn potentiometer P1 the fine gain can be set. The ultra low noise operational amplifier OP 37 is used in this stage; its replacement by the standard version like TL 07I would increase the noise by a factor of 2.

A fraction of the output signal is applied to the input of the next stage, which is a differential amplifier. The 8 position rotary switch SW1a is used for the attenuation of the output signal. The gain of this stage is determined by the ratio of R8/R10 = R9/R11. By the capacitor C2 some frequency compensation is introduced. By the toggle switch SW3 the signal is applied either to the inverting or to the noninverting input providing the positive output pulse. As operational amplifier IC2 also the ultralow noise OP 37 is used.

The stage with IC3 (LM 318) performs differentiation together with two approximate integrations. The input signal is connected to the inverting input through R12 while the noninverting input is grounded.

Three types of the feedback are employed in this stage. The first feedback is made through resistor R13 and trimmer P2. The second feedback is introduced through capacitor C3. The degree of this feedback is selected by the rotary switch SW3b, applying the reduced voltage to the C3. In order to reduce the impedance of the resistor dividing network (R22 to R26) a source follower T1 (FET 2N3819) is used. The third contribution to the feedback is the signal taken from the output of the IC3, then integrated by using the noninverting active integrator designed with IC4 (LF 356) and returned to the inverting input of IC3 through the changeable resistor network R15 to R19. The overall transfer function of this stage T (p) is:

$$T_{(p)} = \tau_p / (1 + \tau_p)^2$$

For the satisfactory operation of the noninverting integrator the time constants R21C5 and (P3+R20)C4 should be exactly balanced. This is realised by P3.

The shaped and smoothed signal from the output of IC3 is applied to the inverting amplifier IC5 (LF 357). A part of the signal determined by P4 is added from the output of the operational amplifier IC4 when the toggle switch SW5 is in the "NORMAL" operating mode. Through the combination of both signals the pole/zero cancellation is achieved with respect to the properties of the selected charge sensitive amplifier. P4 can be adjusted through a hole in the front panel (PZ). In the "OPTICAL" mode of the operation the same combination of both signals is realised, but the admixture of the signal from IC4 is controlled through the trimpot P9 on the PCB. This setting for the compensation of the input differentiation depends on the C1R1 product; it does not depend on the choice of the optically coupled charge sensitive preamplifier.

The amplification of this stage can be changed by the rotary switch SW1b by taking only a fraction of the output signal to supply the feedback resistor R29. At the lower gain ranges LF357 could oscillate. This tendency is reduced by the capacitor C6.

By P5 zero voltage at TP4 is set in the absence of the input signal. With the IC6 (LF 357) a noninverting amplifier with a gain of 2 is made. The feedback resistor R36 is bypassed by C7 to achieve stable operation. The output voltage of the IC6 is inspected by the base line restoration system and a corresponding current is injected into C8. However, by the toggle switch SW4 the BLR system can be made inactive, and then is no current into C8.

Additional filtering of the provided signal is obtained by using a second order active filter with the transfer function R(p):

$$R_{(p)} = 1/(1+ \tau_p)$$

Such filtering provides the stage IC11 if the time constants R50xC10 and R55xC11 are equal. Different resistor pairs matched to the resistor sets R15 to R19 and R22 to R26 are selected by SW2c and SW2d running in parallel with SW2a and SW2b.

As the gain in this stage is lower than 1, the output signal from IC11 is amplified by a factor of 1.85 (R61/R60) by the output stage IC12 (LF357). The feedback resistor R61 is bypassed by capacitor C12 to ensure a stable operation.

The DC offset from IC6, IC11 and IC12 is compensated by P8.

The base line restoration system (BLR) is composed from the clamping amplifier IC7 (TL071), single channel analyser IC8, IC9; (LF357 both) and the gated current source IC10 (CA3080).

The signal from IC6 is applied through R37 to the inverting input of the IC7. For small signals there is the (R38/R37) = 2.7 amplification. For signals exceeding the diode threshold voltage of 0.6 V approx. at the output of IC7, the output voltage depends logarithmically on the input voltage. Therefore small deviations of input signal from zero are well observed, while pulses are clamped. However, in the midposition of the toggle switch SW4 this stage is inactive due to the -15V superimposed to the noninverting input of IC7 through the resistor R 39.

The signal from IC7 is attached to inputs of IC8 and IC9 as discriminators. By using the resistor dividing network R40, R41, R42 and R43 attached to the +15 V and to -15 V the thresholds of (-250 mV and +250 mV) are defined when potentiometer P7 has its full value. Therefore at the output of IC8 the high state appears when the input signal is smaller than -250 mV. Also the output of IC9 goes high when the input signal is greater than +250 mV. However, these limits can be reduced practically down to zero by changing the setting of P7. Because of diodes D3 and D4 forming OR-gate the signal at TP7 is high if either IC8 output or IC9 output goes high.

The high state at TP7 allows the current to enter into the control pin of the transconductance amplifier IC10 (CA3080) through the zener diode VR1 and serially connected R46 or R47.

The current released by IC10 is proportional to the current into the control pin, and to the signal at its noninverting input. The clamped signal from IC 7 is taken after being attenuated to few tens of mV by the resistor dividing network R44, R45.

The output resistor R49 of IC10 has no influence; it helps to convert the current signal into a voltage signal for the possible inspection.

By two different resistors R46 and R47 two different output currents from IC10 can be programmed.

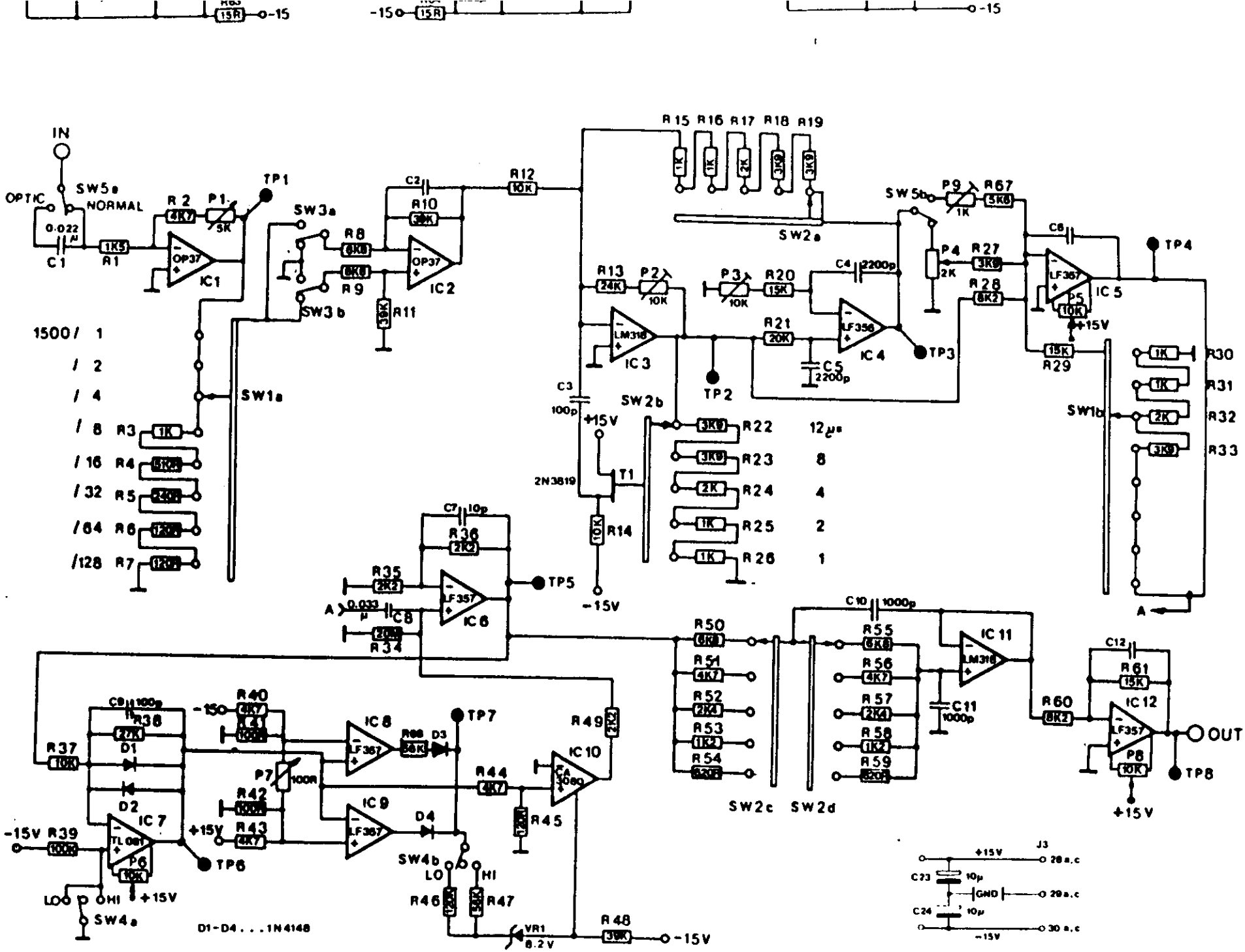


Fig. 6.3 Circuit diagram 102

APPENDIX 3

1.1 GENERAL DESCRIPTION

The timing single channel analyser TSCA 301 is an 8 unit width module of a Nuclear Instrument KIT System, using Eurocard format (160 x 100 mm).

The TSCA 301 analyzes the amplitude of pulses from a spectroscopy amplifier (e.g. 102) by generating a logic output pulse with a walk less than 20 ns for the specified dynamic range. It accepts either unipolar or bipolar input pulses.

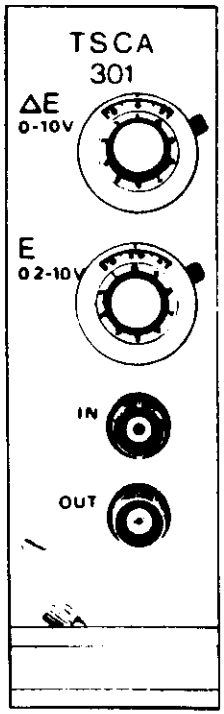


Fig.1.1 Front Panel

2. SPECIFICATIONS

Input			
Signal input	0 to +10 volts, unipolar or bipolar (positive portion leading), input impedance 4kOhms, dc-coupled		
Dynamic range	50 : 1		
Pulse width	> 500 ns, at half amplitude		
Controls			
Lower level (LLD)	0.2 to 10 volts (positive), front panel 10-turn potentiometer		
Upper level (ULD/ΔE)	0 to 10 volts (positive) front panel 10-turn potentionmeter		
Output	positive TTL pulse, 500 ns width		
Time shift versus pulse height (walk)	less than 20 ns for the specified dynamic range		
Power requirements	+15V	-15V	+5V
	50mA	35mA	30mA
Size	8 unit of IAEA Eurocard modul		

3. CIRCUIT DESCRIPTION AND THEORY OF OPERATION

3.1 Theory of operation

The aim of the timing single channel analyser TSCA is to release TTL compatible output pulses as a response to the input pulse of the preselected height interval that is between E and E+ΔE. The time relations between the ouput pulses follow the time relations between the input pulses assuming that the input pulses are of the same shape. In this type of SCA, the output pulse is delivered at the moment when the top of the input pulse is reached (Fig. 3.1).

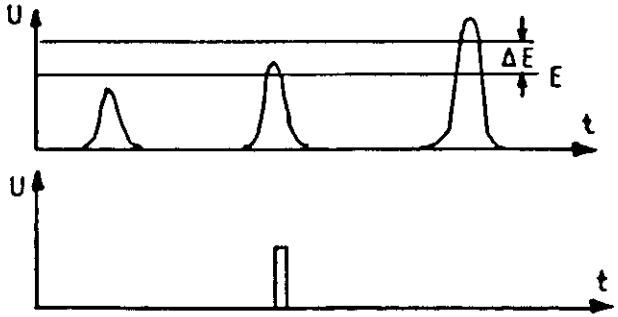


Fig.3.1 Input-output relations in TSCA

By setting ΔE to its maximum value (which is 10V in this case) the unit can be used also as the timing discriminator with the discriminator level at the voltage E. The operation of the presented TSCA can be followed by using the block diagram represented in Fig.3.2 as well as the signal forms given in Fig.3.3

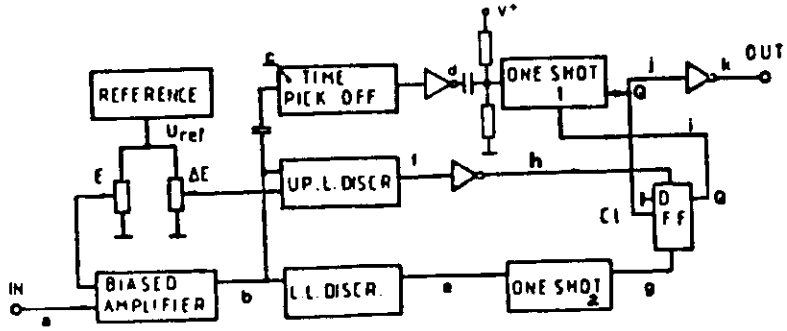


Fig.3.2 Block diagram

The positive input pulses (Fig.3.3a) are shifted in the negative direction for the amount of E/2 and amplified by a factor of 0.5, when passing through the BIASED AMPLIFIER. The obtained signal (Fig.3.3b) is connected in parallel to the input of the TIME PICKOFF DISCRIMINATOR, UPPER LEVEL DISCRIMINATOR and LOWER LEVEL DISCRIMINATOR. In the TIME PICKOFF DISCRIMINATOR the signal is time differentiated; for bi-polar pulses a pole-zero cancellation network is added (jumper B) to cancel the third pole (Fig.3.3c). The produced output signal exhibits the 1-0 transition at the moment when the input pulse has reached the top (Fig.3.3d). By this transition the ONE SHOT 1 is fired and the Q pulse (Fig.3.3j) is inverted in the output stage to give the positive output pulse (Fig.3.3k). However, the firing of the ONE SHOT 1 is allowed only when the input pulse height is within the height interval between E and E+ΔE. This single channel operation is realised if the Q output of the D flip-flop is set to the high state. Such high state (Fig.3.3i) is achieved if D flip-flop has been set by ONE SHOT 2 pulse (Fig.3.3g) followed the LOWER LEVEL DISCRIMINATOR pulse (Fig.3.3e) and not yet reset by the UPPER LEVEL DISCRIMINATOR pulse (Fig.3.3f) which is inverted by nand gate 1/4 74LS37 (Fig.3.3h) indicating that the pulse being analysed is bigger than E+ΔE. However, in the absence of the UPPER LEVEL DISCRIMINATOR pulse (Fig.3.3h) the D flip-flop would remain in the high state (Fig.3.3i). Therefore, the corresponding reset is assured through the clock input of the D flip-flop by the 0-1 transition of the ONE SHOT 1 pulse (Fig.3.3j).

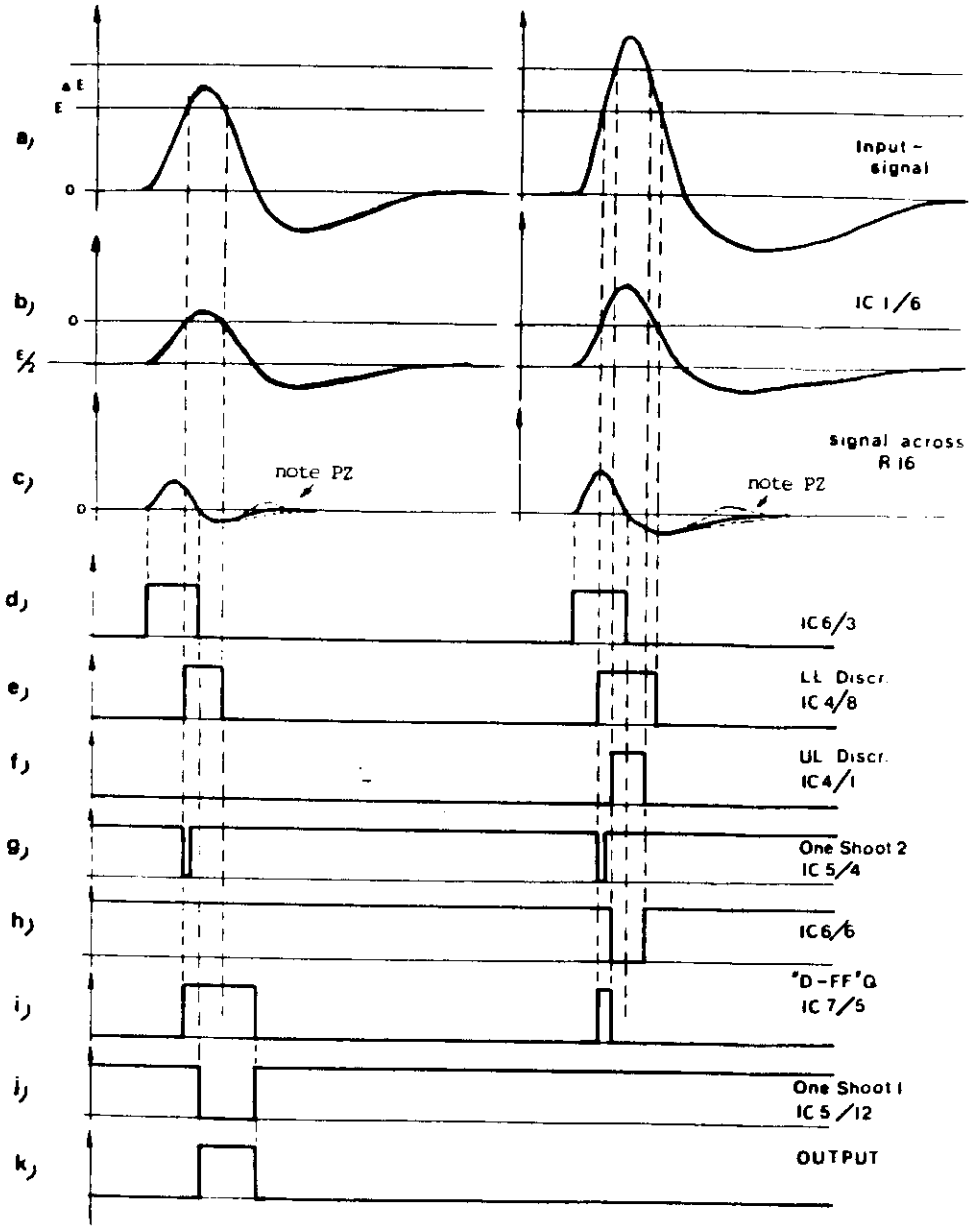


Fig.3.3 Signal Forms

3.2 Circuit description (refer to page 301-13, Fig.7.1)

The operational amplifier IC1 LM318 is used as input amplifier. The signal connected to the non-inverting input is attenuated to 0.25 of the initial value by the passive network R1, R2 to be later amplified twice. Due to the equal values of resistors R3 and R4, the voltage from the slider of the P1 gives equal voltage of the reversed polarity at the output of IC1. Therefore, by setting the upper end of this potentiometer to 5V, the output voltage of IC1 can be shifted to -5V. In parallel with the feedback resistor R4, two capacitances C1 and C* are connected in order to optimise the frequency response of this stage. For this purpose the rectangular positive pulses of few µs connected to the input are observed while searching for the optimal output signal of IC1, by adjusting the capacitance C1 (see assembling instructions, para 5.4)

In the voltage reference stage the operational amplifier LF356 is used as IC2. This stage is a voltage follower with adjustable gain (set by P3 from 1 to 1.18) to get a reference voltage of 5V from the Zener reference source of 4.7V. The output current capability of the reference voltage source is increased by using transistor T1. Some integration is introduced through capacitors C6 and C7 to make the operation of this stage stable. Ten turn potentiometers P1 and P2, connected in parallel are decoupled by using RC filters (R7+P1)C4 and R9C5, respectively. By the resitor R8 the minimal threshold E is limited to 200mV. R13 is normally bypassed by a jumper to give a zero window width. For R13 = 10 ohms the minimum window width is 100mV with respect to input signal if P2 is in zero position.

As comparators IC3 and IC4 the dual comparators TL 820CN are employed instead of the popular 710 due to their higher gain. Through this choice an adequate sensitivity of the time pickoff discriminator is assured. To the input of the comparator the time differentiated signal is applied through the passive network C8,R16, with the time constant τ = 0.26 µs.

If the input pulse is bi-polar a pole zero cancellation network P5 R10 (C21) is added (by jumper B) to cancel the third pole. The dotted line in Fig.3.3e shows misadjustment of the pole-zero potentiometer.

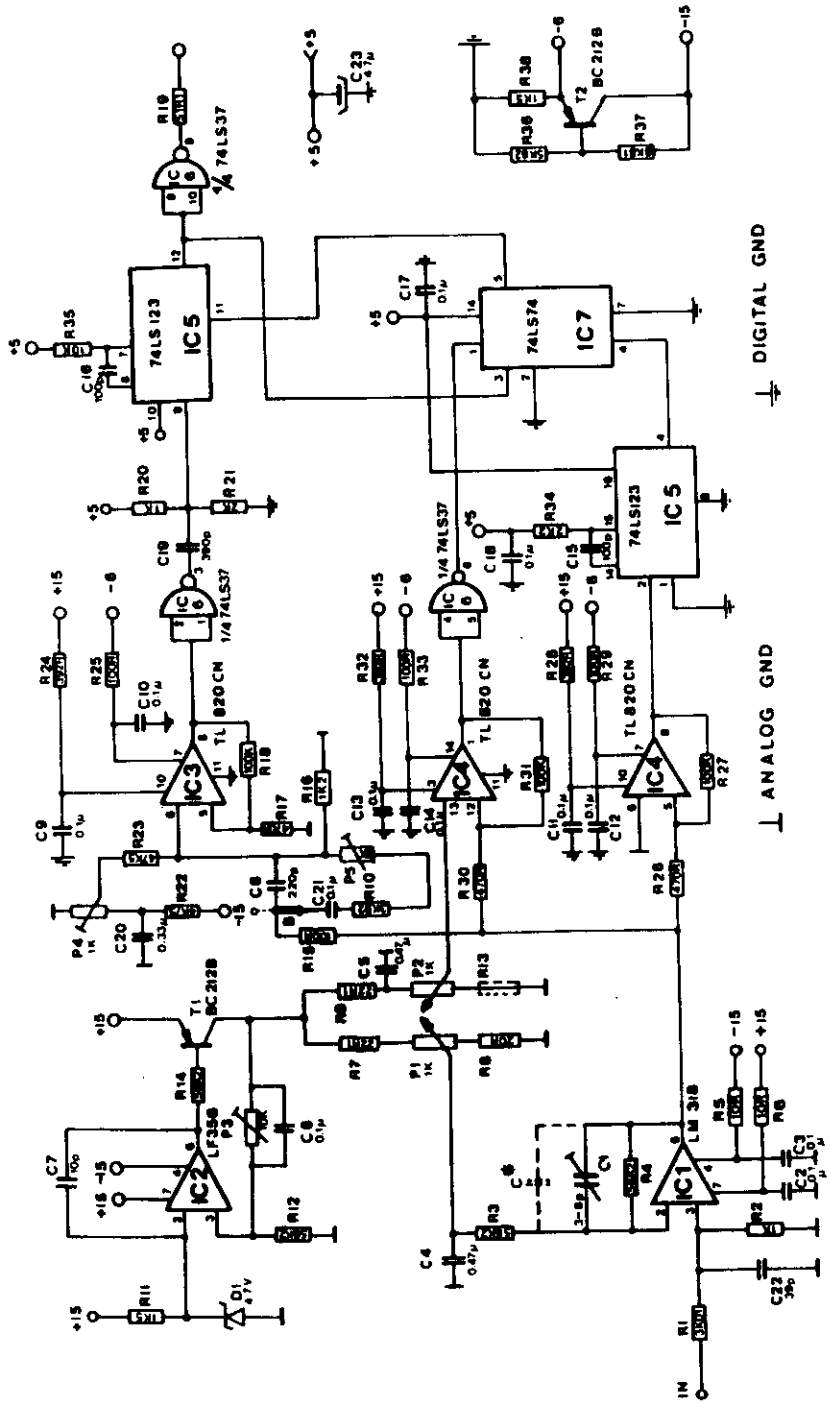
Note: Input pulses coming from a spectroscopy amplifier which is connected to a photomultiplier system are bipolar for decay time constants less than 40µs. To avoid double pulses at output of IC3, it is necessary to cancel the third pole. In case of troubles change R10.

By the resistor combination R16,R23 and P4 a variable reference voltage (0 - 60mV) is introduced to inverting input of IC3 in order to set the optimal condition for the timing pulse (see para 5.5). In general, it should be set to get the output 1 - 0 transition when the differentiated signal is crossing zero. By resistors R17 and R18 connected to the non inverting input of the comparator, 20mV of hysteresis is introduced. Resistors R24 and R25 as well as capacitors C9 and C10 placed close to the IC3 to form the usual decoupling filters.

The output pulses from IC3 are inverted in the 1/4 of SN74LS37 (IC6) and applied across C19 and the voltage divider R20, R21 to the trigger input of the dual one shot SN74LS123 (IC5). The width of the output pulses (500 ns) is determined by R35 and C16. The Q pulses are finally inverted into the positive pulses by NAND gate IC6.

The upper and lower level discriminator (IC4) are of the same construction: standard decoupling filters, and 20mV of hysteresis assured through the resistor divider network R30,R31 and R26,R27, respectively. While pulses from the upper level discriminator are inverted in 1/4 of SN74LS00 pulses from the lower level discriminator are used for triggering one of the two one shots of IC5 (SN74LS123) to give output pulses of 100 ns duration. In the place of IC7 one D flip-flop SN74LS74 is used while the second one is not employed.

The negative voltage source for comparators operation is an emitter follower made from transistor T2 with the resistor dividing network R36 and R37 defining the output voltage at about 6.8V.



7.1 Circuit diagram 401

APPENDIX 4a

1. GENERAL DESCRIPTION

The 402 Scaler Timer with RS232 printer interface is a 16 unit width IAEA Eurocard nuclear instrumentation module. It counts and displays input pulses up to a predetermined time and sends data out to a printer. The scaler-timer board (PCB 402-1) consists of two 6 decade cascaded counters. One is used for counting positive TTL pulses up to a count rate of 1 MHz with 250 ns pulse pair resolution. The other one works as a timer on a 1 Hz time base. Reset for timer and counter is generated automatically each time the START switch is pressed and at power up. During count operation no reset is possible except if counting is stopped first. Interface board (PCB 402-2) is designed to interface scaler-timer (PCB 402-1) to a printer with RS232 interface standard. It converts the parallel BCD data from the scaler to serial one and transmits it to the connected printer. Selection of data per line can be predetermined. All functions are controlled by switches on the front panel.

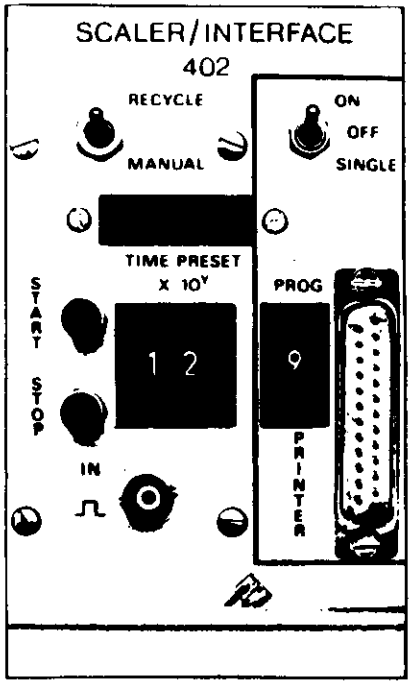


Fig. 1.1: Front Panel

2. SPECIFICATIONS

Presetable scaler-timer 402-1

1. Input

Count Input	: - front panel BNC connector insulated - Impendance: 50 Ohm (if R1 is inserted), DC coupled - Polarity: positive - Amplitude: TTL logic level (low<+0.8V/high>+2V), ± 50V maximum - Width: ≥250ns

2. Controls

Start	: - front panel pushbutton to begin count accumulation. Counter and timer automatically reseted at same time.
Stop	: - front panel pushbutton to terminate accumulation.
Preset time	: - front panel thumbwheel switch $X.10^{Y}$ [s] 1≤X≤9 0≤Y≤5
Manual/Recycle	: - front panel two-position toggle switch selects single or recycle mode of operation upon reaching time preset condition.

3. Performance

Count capacity	: - six decades allowing a count of 10^{6}-1 (999,999)
Indicator	: - six digit LED display

4. Power

Consumption	: - +15V, max. 80mA (without option)

5. Physical

Size	: - 16 units width Eurocard module

6. Option

Printer Interface	: - front panel 25 pin connector RS232 asynchronous serial, unidirectional

Option printer interface 402-2

1. Input

Data Input	: - 4 bit BCD parallel, digit serial, internal connected

2. Output

RS232 Interface	: - front panel 25 pin connector - operation mode: asynchronous serial unidirectional - Baud rate: 4800 bps - word lenght: start bit 1 bit data bit 7 bit parity bit none stop bit >1 bit - handshaking: none

3. Controls

Print mode select	: - front panel three position toggle switch selects single, continous (on) or no printing (off)
Printing format	: - front panel thumbwheel switch selects 1 to 9 readings per line. Each reading consists of a 6 digit number, 2 or 3 spaces and one carriage return
Reset	: - internal by power on

4. Power

Consumption	: - +12V, max. 70mA -15V, max. 50mA
RS232 driving capability	: - Mark = logic "1" (-15V to -3V) can sink 40mA Space = logic "0" (+3V to +10V) can source 60mA

3. CIRCUIT DESCRIPTION

3.1 PCB 402-1

As shown in the block diagram, Fig. 3.1 the module has six main functional blocks; a time base generator, control logic, timer, counter, input shaper and a six digit display.

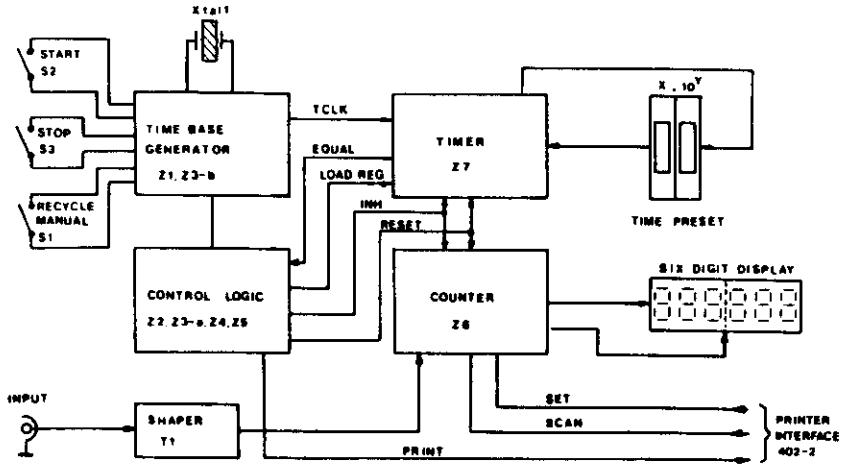


Fig. 3.1: Block diagram

Quartz crystal driven Z1 is an oscillator and a frequency divider. The oscillator frequency of 32,768 kHz is divided to 2 Hz and output at Z1/3. Z3-b works as divider by 2 to obtain 1 Hz (TCLK).

Control logic consists of a sequencer, a power up reset circuit and flip-flops to control the process. Sequencer is based on the Z2 (4017, decade counter) and generates the operation sequences. The control logic circuit Z2, Z3-a and Z4 (flip-flops) is reset by either power-up or

pressing the STOP button. The sequencer is prepared to start. If START button is pressed, Z3-a changes the state and enables Z2. Z2 starts control sequence triggered by the time base generator Z1/1. Z2/2 sends a pulse to reset the timer and the counter. As next it sends a pulse to the timer Z7 to load the registers with the preset time interval from the thumbwheel switches on the front panel. The output Z2/7 activates Z4-a/11. Output Z4-a/12 goes low and disables Z2. At the same time it prepares Z4-b to be set with TCLK pulse to synchronize. Positive leading edge of TCLK sets output Z4-b/1 high. This enables (INH) timer Z7 and counter Z6 after a short delay (by R19 and C8) and inversion of Z5-a.

If timer Z7 is equal to preset value, it generates an EQUAL signal to clear Z4 and to enable the sequencer Z2. Z2/10 sends a PRINT pulse to printer interface (PCB 402-2). If REC-MAN switch S1 is closed (MAN), reset is generated. Via Z5-d and Z5-c Z2, Z3, and Z4 goes back to initial state to be ready for next START.

If S1 is open (RECYCLE), Z2 advances till step "9", returns to step "0" and repeats the above-mentioned cycle.

Preset time value is transfered to internal comparision register of Z7 at beginning of every cycle. Decimal thumbwheel switch selects the power (0≤Y≤5), BCD thumbwheel selects the multiplication factor (0≤X≤9).

Z7 accumulates TCLK pulses (1 Hz) and generates EQUAL signal when preset time is reached.

Counter Z6 receives pulses from IN-BNC via T1 (pulse shaper) and displays the current count. T2 to T7 are digit driver transistors. Z6 also provides output to the printer interface.

3.2 PCB 402-2

As shown in the block diagram, Fig 3.2 this module consists of six main functional blocks; a clock generator, control logic, readings per line counter, latch, serializer and output driver.

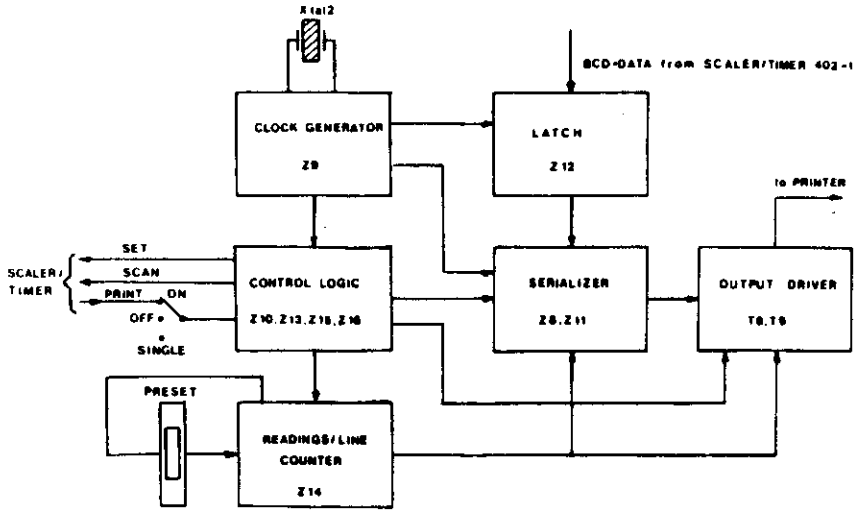


Fig 3.2: Block diagram

If S4 is at ON (PRINT ON), Z2/10 generates a print command at the end of the preset acqusition time. Flip-flop Z13-a/1 starts the sequence of serializing. The 4-bit BCD data is serialized and sent to the printer.

When output Z13-a/1 goes high, sequencer Z16 and scaler Z6 are triggered by clock pulses coming from Z9/3 via Z10-b and Z10-c. High at output Z10/11 loads the data to the shift registers Z8 and Z11. When Z10/11 goes low, data is shifted with the positive going clock pulses on inputs Z8/10 and Z11/10. The parallel BCD data is serialized and sent via T8, T9 to the printer.

Sequencer Z16 controls the data transfer from Z6 to Z12 digit by digit. The sequencer Z16 sends at the beginning a SET pulse to the scaler Z6 to output 6th digit first to Z12. The following clock pulses are sent to Z6 as scan pulses and the next lower digit is latched into Z12 until 6th clock pulse is finished. Then Z16 triggers Z13-b and generates a space by resetting Z12 and pulling Z11/6 to low. As Z11/7 is at high, three spaces (ASCII code 20H) are sent out. The next step of Z16 increments readings per line counter Z14 by one. At the same time Z13 and Z16 are reset and prepared for the next print signal from Z2. When the preset number of readings per line is reached, Z15/11 goes low and after two spaces a Carriage Return (ASCII code 0DH) is generated at Z11 and sent out.

Z9 is an oscillator (2.4576 MHz) and a divider. For 4800 bits per second at Z9/13 a frequency of 4800 Hz is continuously available. Whenever S4 is pressed to SINGLE the momentary reading is transferred to the printer. If S4 is at OFF no printing takes place.

3.3 Typical wave forms are shown in the following drawings on page 402-8 and 402-9.

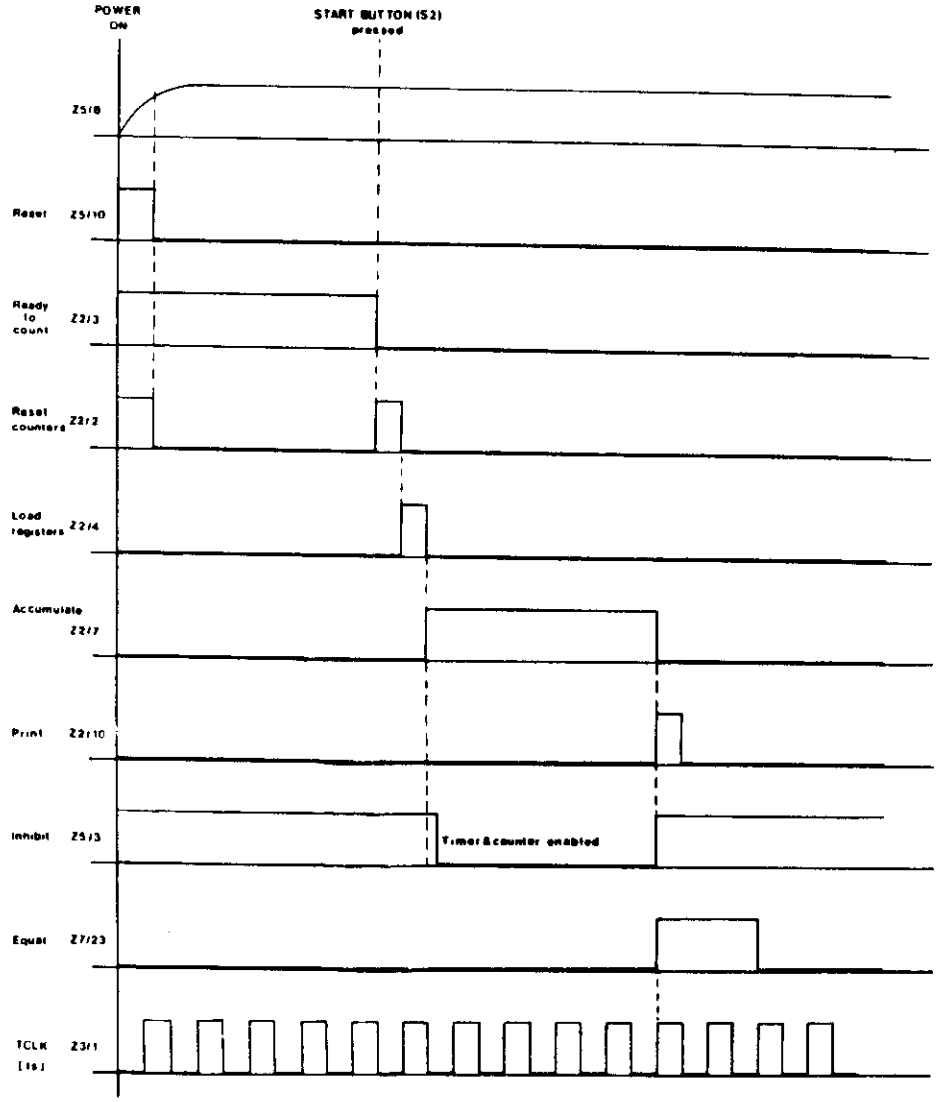


Fig 3.3: Timing sequence on PCB402-1

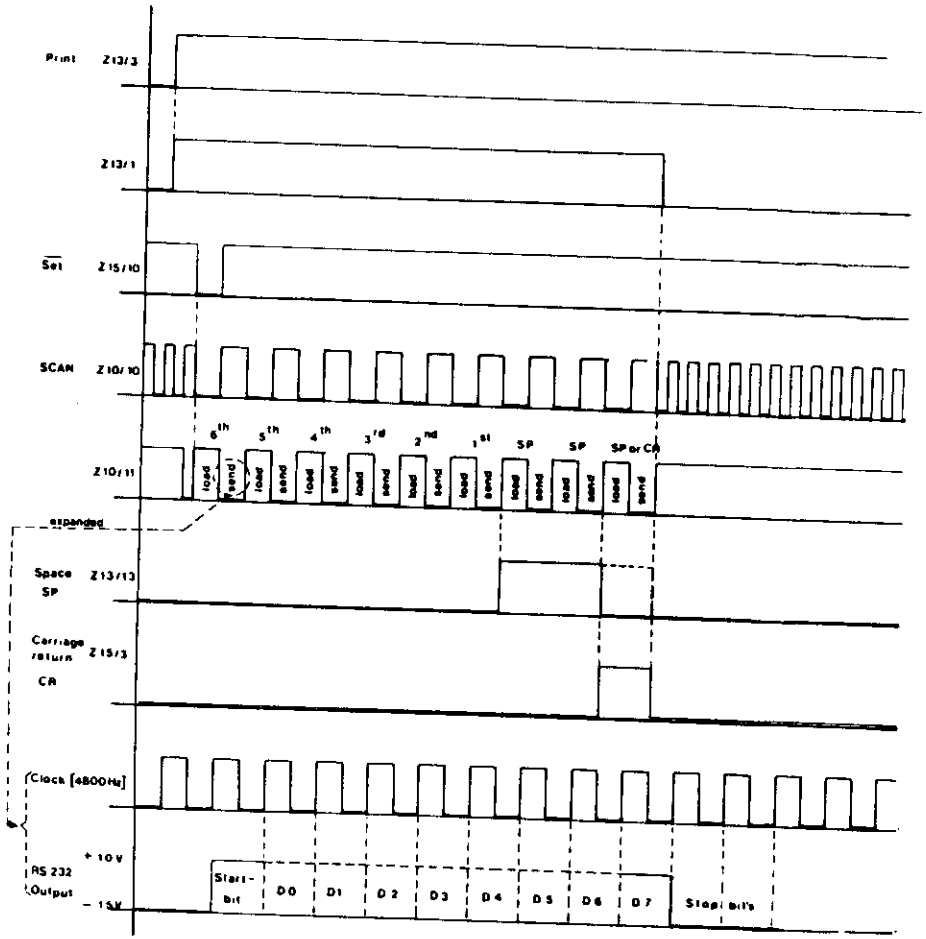
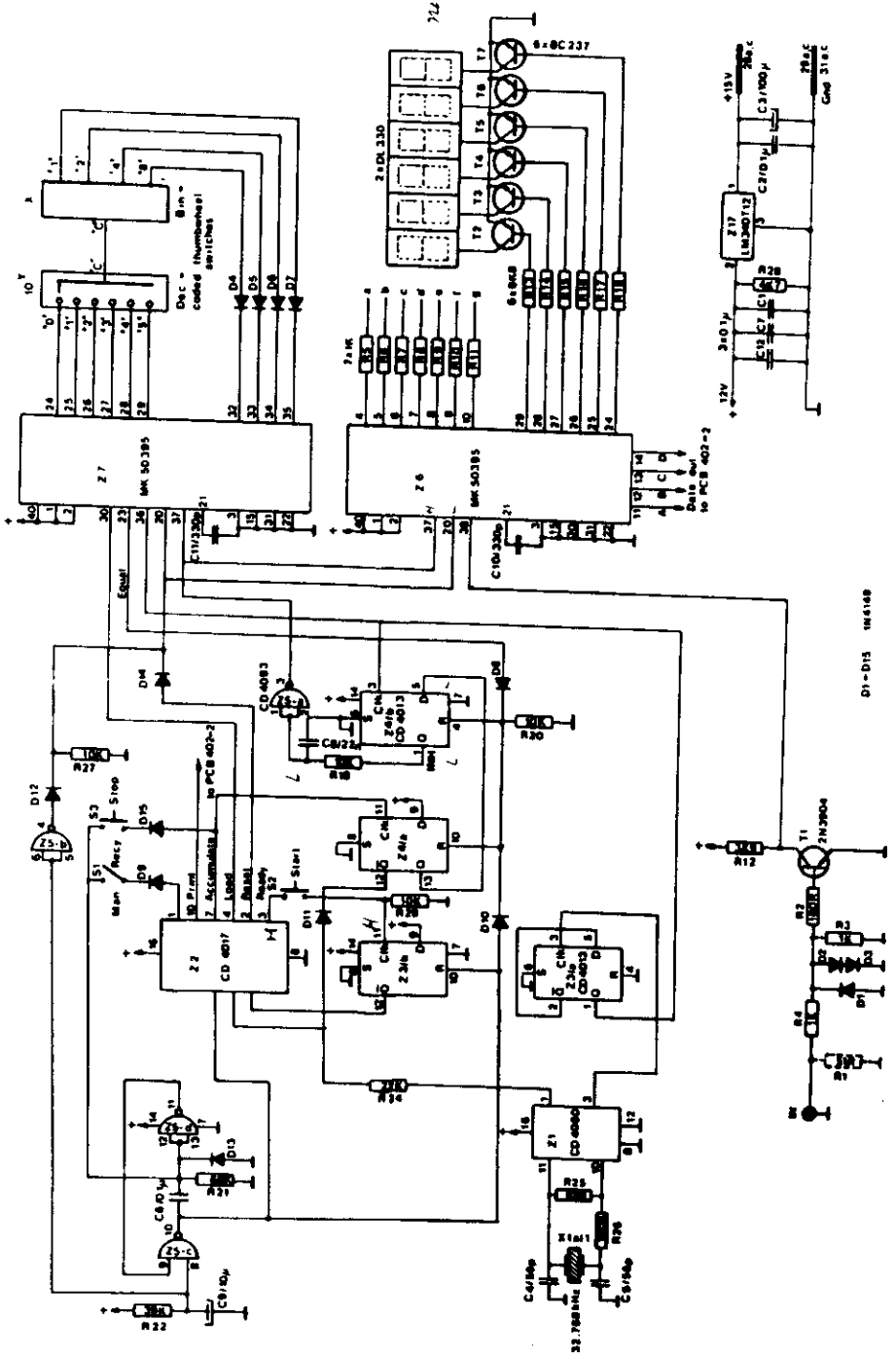


Fig 3.4: Timing sequence on PCB402-2



10.1 Circuit diagram PCB402-1

APPENDIX 4b

1. GENERAL DESCRIPTION

The Lin-Log Ratemeter 501 is a module of the IAEA Eurocard Nuclear Instrumentation System. The unit serves for measuring the rate of input pulses passing discriminators. It consists of two separate measuring circuits: a linear and a logarithmic one. Both outputs - full scale of 10V - can be connected to the front panel meter by means of the mode switch.

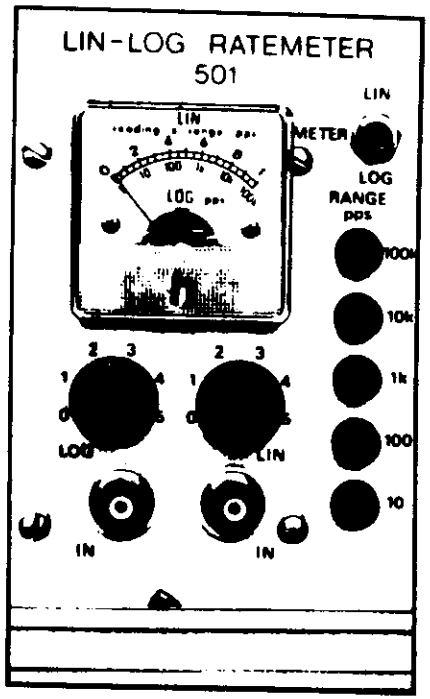


Fig. 1.1 Front-Panel of LIN-LOG Ratemeter

2. SPECIFICATIONS

2.1 Linear ratemeter

Measuring ranges 10 V full scale	Time constant	Accuracy at 25°C	Linearity
10 pps	10 s	5%	better than 2%
100 pps	10 s	5%	
1 kpps	5 s	3%	better than 1%
10 kpps	1 s	2%	
100 kpps	0.1 s	2%	

Stability at full scale output voltage

Range/pps	%/°C	% day at 25°C
10	0.2	0.1
100	0.2	0.1
1 k	0.1	0.05
10 k	0.1	0.05
100 k	0.1	0.05

2.2 Logarithmic ratemeter

Measuring range: 1 pps to 10^5 pps

Voltage output: 0 V/1pps to 10V/10^5pps

Time constant: 15s/1pps to 2ms/10^5pps

Stability:

Between 10pps and 10^5pps range: 0.2%/°C, 0.1%/day (of full scale output voltage)

2.3 General (for both ratemeters)

Input pulse - polarity	positive
- amplitude	0 V to +5V max. (linear discrimination range)
- width	0.2 µs min.
Input resistance:	10 kOhm up to 5V, only
Discriminator threshold level	Adjustable by front panel potentiometer from 0.2 to +5.0V
Pulse output	positive TTL pulse
fan out	10 TTL
Voltage output	
voltage range	0 V to 10 V
	R_{LOAD}, 1kOhm
Voltage outputs short-circuit proof	
Power Requirements	+15V 90 mA max
	-15V 60 mA max
	+ 5V 60 mA max
Supply voltage ranges	+13V to +17V
	-13V to -17V
	+4.75V to +5.25V
Operating temperature range	0°C to +50°C
Suggested temperature range	15°C to +35°C

3. CIRCUIT DESCRIPTION

3.1 Linear Ratemeter (refer to Fig. 3.1 and circuit diagram of linear ratemeter, page 501-17)

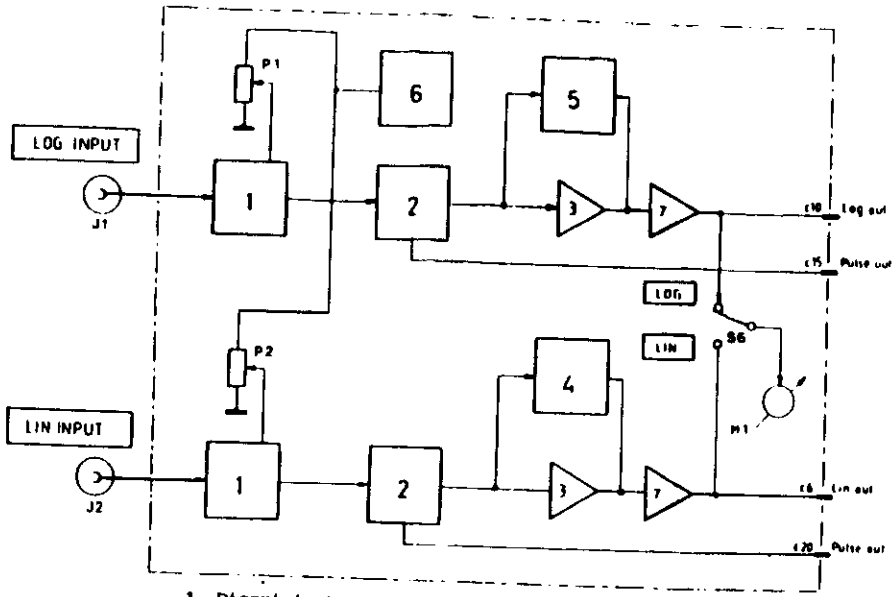
Positive input pulses from the BNC-connector (J2) are fed through the resistor R30, passing R1,V1 as a limiting circuit directly into the inverting input of the comparator A1. The comparator threshold can be set by the front panel potentiometer R2. The positive output pulse of A1 triggers the monostable multivibrator A2 (SN74121). The monoflop provide negative output pulses (TTL) with stable duration. The pulse width is 5 µs for the lowest range only (10 pulses/sec) and 0.5 µs for all other ranges from 100p/s to 100kp/s. The 5 µs pulse is selected by S1 in connection with the relay K ; width adjustment by R10. The 0.5 µs pulse duration can be adjusted with the trimpot R11 (K1 is activated, when switch 14-8 is closed). The output pulse from A2 is fed through R13,C5 and changes transistor V2 from saturation into the non-conducting condition. During this period a very stable current of 2 mA is flowing through R15, V3, V4 R16 into the linear amplifier A3 (LF356). Mean current (pulsewidth x pulse current x countrate) multiplied by the selected feedback resistor (R17 to R20) gives the output voltage on A3 (1V by full range); so the output voltage is proportional to the rate of the input pulses.

The feedback condensors (C7 to C10) give the suitable time constants. R22 is for zero-offset adjustment of A3. Operational amplifier A4 inverts the output voltage of A3 with an amplification factor of 10 (10V positive, full range). The output voltage of this linear ratemeter is applied to the panel meter M1 through switch S6.

3.2 Logarithmic ratemeter (refer to Fig. 3.1 and circuit diagram of log. ratemeter, page 501-15)

Positive input pulses from the BNC-connector (J1) are fed through the resistor R36, passing R1,V1 as a limiting circuit directly into the inverting input of the comparator A1. The comparator threshold can be set by the front panel potentiometer P1 The positive output pulse of A1

triggers the monostable multivibrator A2 (SN74121). This monoflop provides a Q pulse with stable duration. The pulse width is 0.5 µs; adjustable with potentiometer R9. The output pulse from A2 is fed through R13,C5 and changes transistor V3 from saturation into the non-conducting condition. During this period a very stable current of 2mA is flowing through R15,V4,V5 R20 into the amplifier A3 (LF356). This amplifier gives the output signal to the resistor chain R24,R25; R26,R27,R28. An adjustable part (R27) of this signal is fed into the logarithmic current generator consisting of: V6 (a temperature compensated emitter coupled transistor pair) in connection with the operational amplifier A4 (LF356) and the reference voltage generated by V2 (ZPD 5.6). This logarithmic current generator feeds the signal back to the inverting input of the amplifier A3. This arrangement forms a logarithmic output signal depending on the applied input current to A3 over a range of 5 decade .



1. Discriminator
2. One shot and current generator
3. Amplifier
4. Linear feedback
5. Logarithmic feedback
6. Voltage source
7. Output amplifier

Fig. 3.1 Block Diagram 501

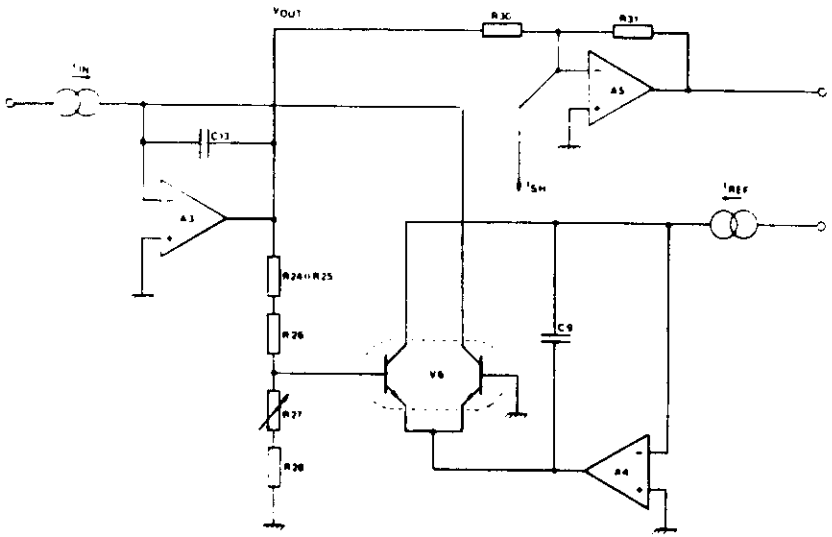


Fig. 3.2 Logarithmic converter (stages 3, 5 and 7)

Dynamic ranges: $10^{-9}A<5.10^{-7}A<10^{-4}A$

5 decades

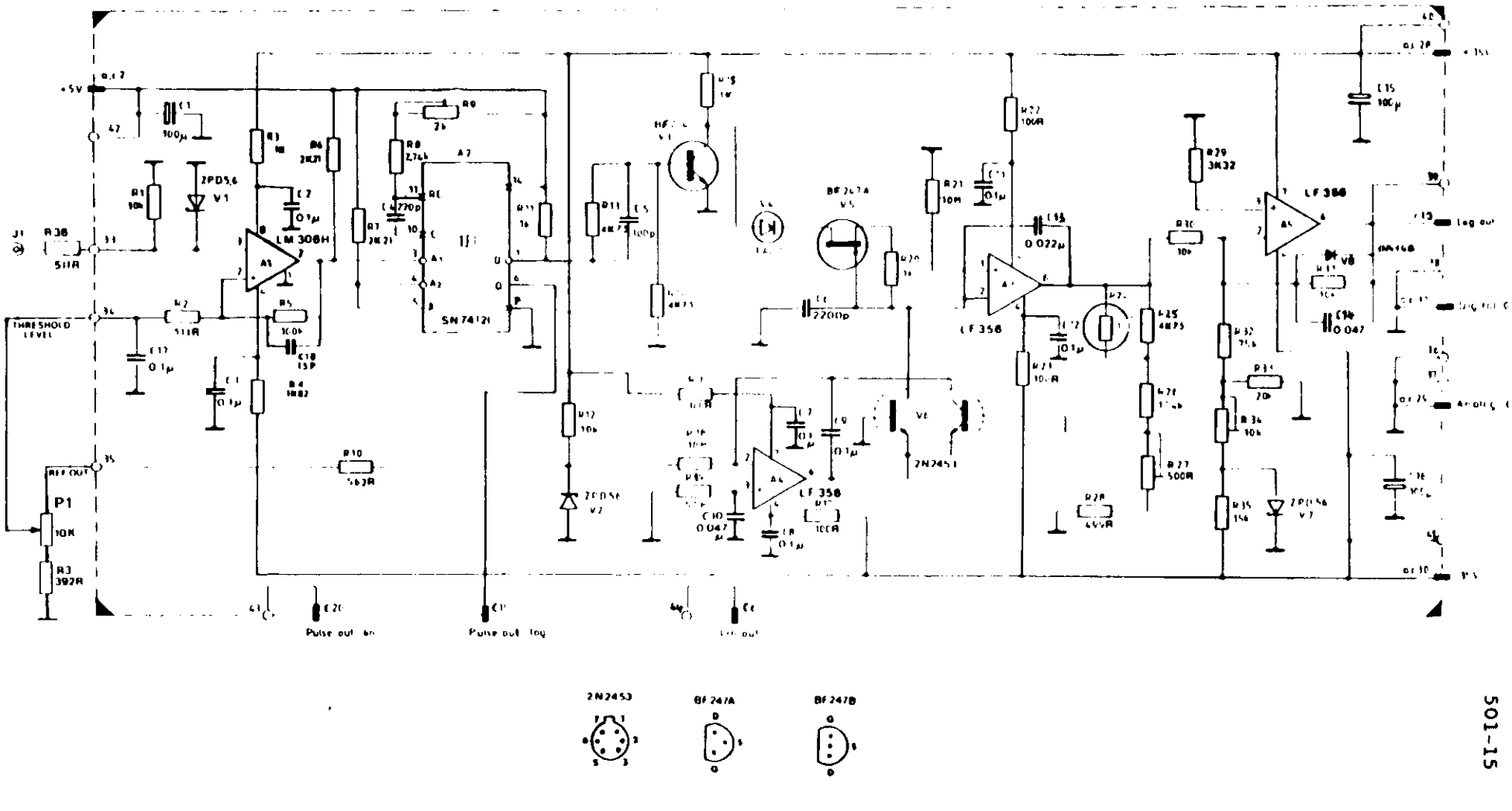
$|V_{OUT}|$ = 2V/decade

$V_{OUT} = -K\log(I_{IN}/I_{REF})$

K = scaling factor

I_{IN} = average current

The amplifier A5 (LF 356) inverts the input signal to a positive output. The resistor chain R32,R33,R34 together with the reference voltage (V7) is for the zero voltage adjustment (R34). The diode V8 avoids an overload of the panelmeter in the opposite direction if no input pulses are applied. The output voltage of this logarithmic ratemeter is applied to the panelmeter M1 through switch S6.



501-15

Fig. 6.2 Circuit diagram 501-1-LOG