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I.C.T.P., P.O. BOX 586, 34100 TRIESTE, ITALY, CABLE CENTRATOM TRIESTE

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FIFTH COLLEGE ON MICROPROCESSORS: TECHNOLOGY AND APPLICATIONS IN PHYSICS

2 - 27 October 1989

Microprocessor Interfacing the 6809

A. COLAVITA
Microprocessors Laboratory, ICTP, Trieste

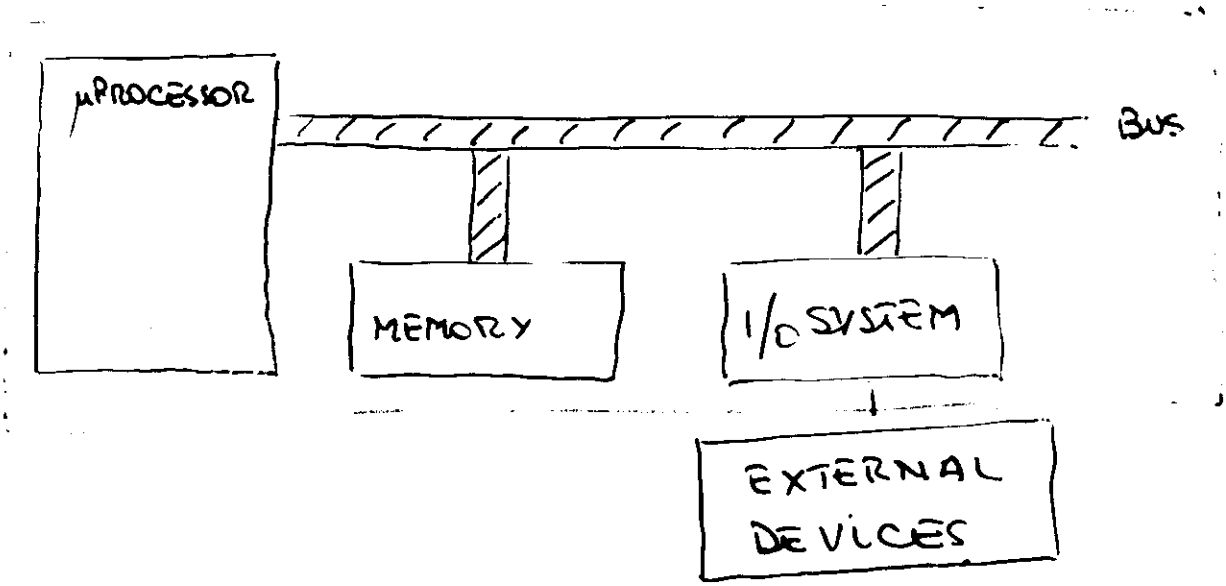
OVERVIEW OF THE LECTURES

- BASIC I/O CONCEPTS
- PARALLEL PORTS USING THE PIA (MC 6821)
- SERIAL PORTS USING THE ACIA (MC 6850)
  THE RS-232C STANDARD.
- MORE ADVANCED I/O TECHNIQUES.

BASIC CONCEPTS – LECTURE 1.

- BASIC MICROCOMPUTER STRUCTURE
- BUS FUNCTIONS
- 6809 BASIC READ, WRITE TIMING
- ISOLATED AND MEMORY MAPPED I/O
- I/O PORTS AND I/O TRANSACTIONS
  PROGRAM CONTROLLED AND INTERRUPT DRIVEN.
- I/O DRIVERS

THERE ARE THREE PARTS: (ONE MASTER SYSTEM)



I) µPROCESSOR: CONTAINS THE CONTROL LOGIC AND ALU OF THE SYSTEM.

II) MEMORY: HOLDS DATA AND PROGRAM.

III) I/O SYSTEM: IT HAS "PORTS" THAT CONNECT THE COMPUTER TO EXTERNAL DEVICE SUCH AS:

- TERMINALS
- DISPLAYS
- DISKS
- TAPE UNITS
- PRINTERS
- MODEMS
- SENSORS
- ACTUATORS
- ETC.

1 BUS.

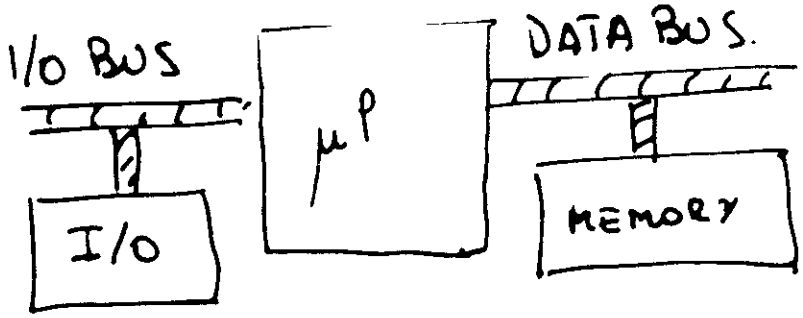
- THE μPROCESSOR INITIATES ALL ACTIVITY ON THE BUS BY ISSUING COMMANDS TO THE MEMORY AND I/O SYSTEMS.
- THE BUS EXECUTES A TRANSACTION AT A TIME.
- THE MEMORY AND I/O RESPOND TO THE COMMANDS.
- THERE ARE TWO TYPES OF COMMANDS ON THE BUS:

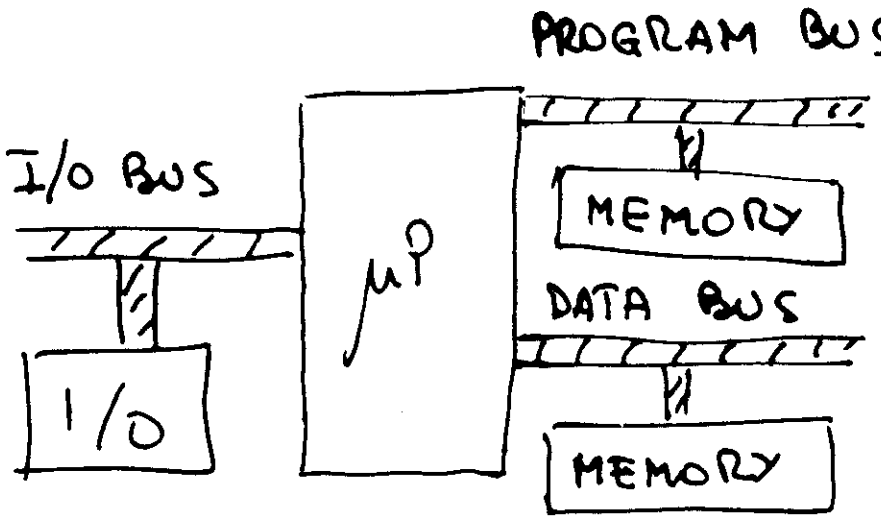
A) THE μP INSTRUCTS THE DESTINATION TO ACCEPT DATA
DATA FROM THE μP ACCOMPANIES THE COMMAND.

B) THE μP TELLS THE DESTINATION TO ISSUE DATA FOR THE PROCESSOR. THE DESTINATION REPLIES BY SENDING THE DATA TO THE μP.

THE DATA FLOWS FROM I/O AND MEMORY TO AND FROM THE μP UNDER THE COMMANDS ISSUED BY THE μP.

TO OBTAIN MORE THAN ONE TRANSACTION AT THE TIME WE NEED MORE BUSES. EXAMPLES.





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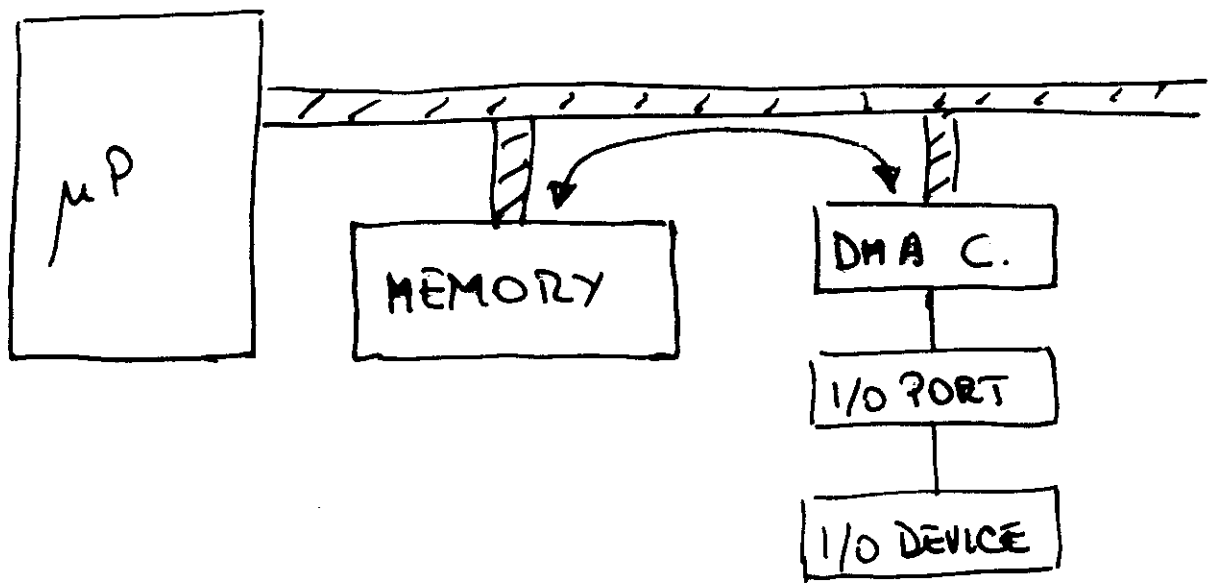
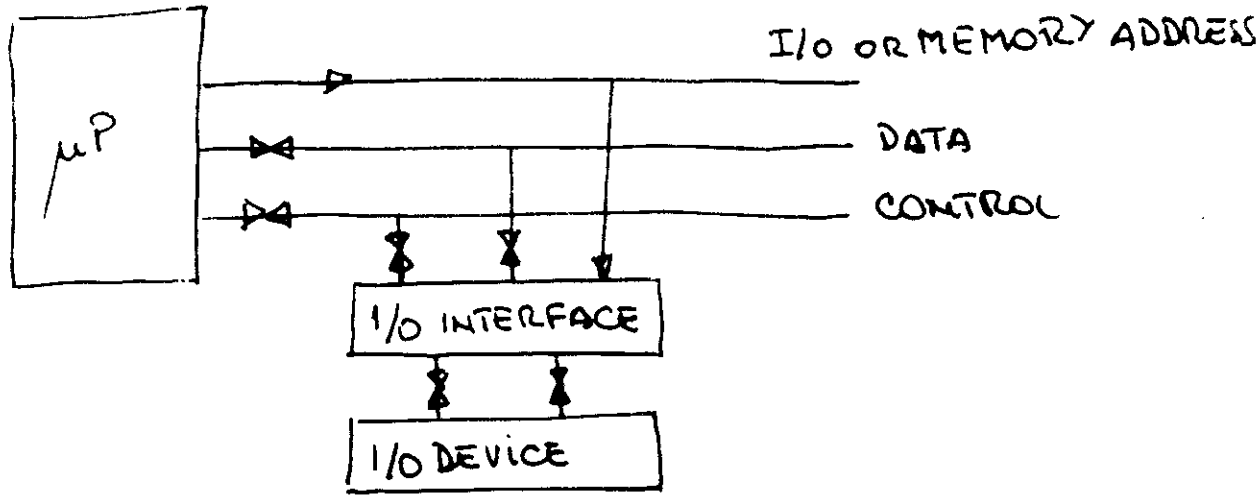
A DMA (DIRECT MEMORY ACCESS) CONTROLLER CAN TALK DIRECTLY WITH MEMORY
IT CAN ISSUE COMMANDS TO MEMORY THAT ARE IDENTICAL TO THE COMMANDS ISSUED BY THE MICROPROCESSOR.



BUS FUNCTIONS



- A BUS IS A COLLECTION OF SIGNAL LINES THAT ARE UNBROKEN AND THAT CARRY MODULE-TO-MODULE COMMUNICATION.
- MODULES SIMPLY TAP ONTO A BUS BY SIMPLY CONNECTING THEIR RESPECTIVE INPUTS AND OUTPUTS DIRECTLY TO CORRESPONDING BUS SIGNAL LINES.

THERE THREE BROAD CATEGORIES OF BUS LINES.

1) MEMORY OR I/O ADDRESS LINES
2) DATA (1, 2, 4, 8, 16, 24, 32)
3) CONTROL (READ, WRITE, STATUS, STROBE).

ADDRESS LINES ARE USED TO IDENTIFY THE MODULE, PORT OR CELL THE μP IS TALKING TO.

CONTROL LINES CAN BE DIVIDED INTO

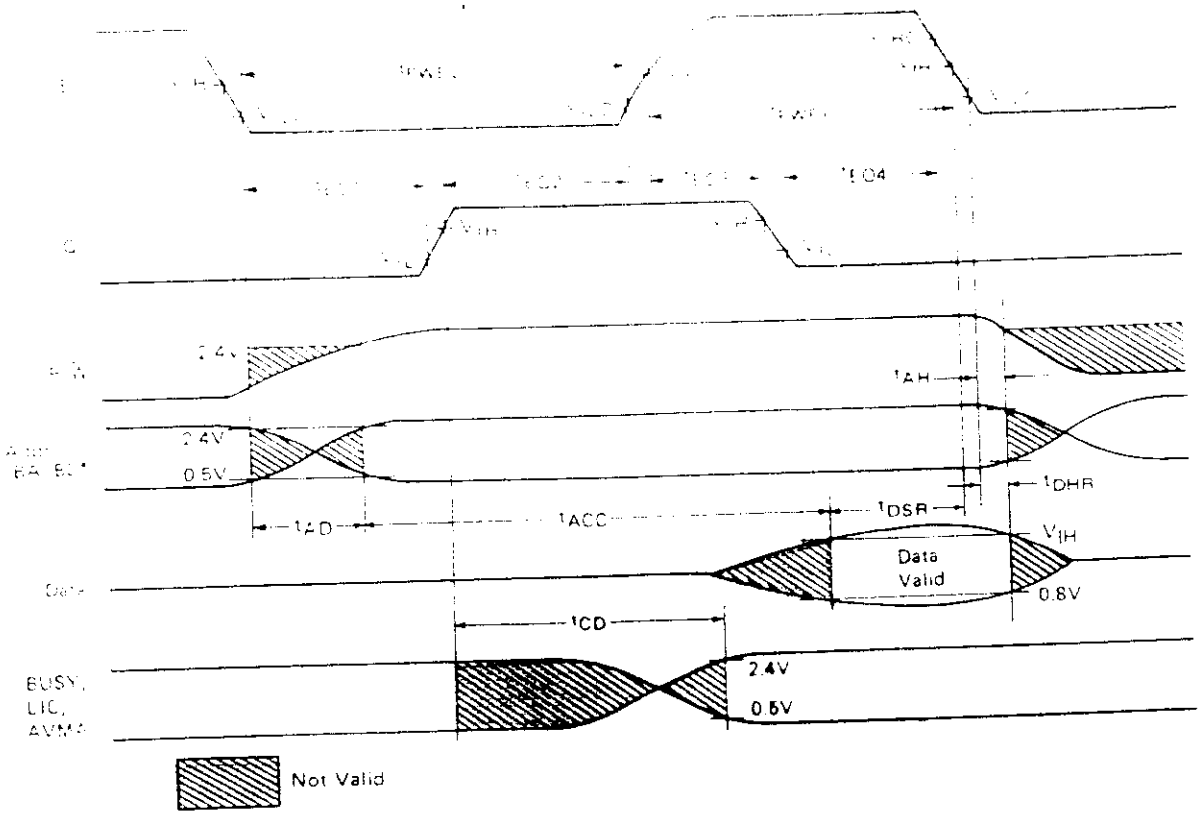
A) COMMANDS: READ, WRITE, R/$\overline{W}$, ETC., INST. FETCH, THIS GROUP CARRIES INFORMATION THAT ONE MODULE NEEDS TO CONVEY TO ANOTHER IN ORDER TO INVOKE A REMOTE FUNCTION OR RESPONSE

B) DATA HANDSHAKE LINES; CONTAIN SIGNALS THAT DICTATE WHEN EACH INDIVIDUAL DATA TRANSFER START AND ENDS. THE HANDSHAKE START AND STOPS TRANSACTIONS AND GENERALLY

EXERT THE SAME FUNCTIONAL CONTROL OF ALL TRANSACTIONS REGARDLESS OF THE TYPE. E, Q, ϕ_1, ϕ_2, ETC.

6809 READ, WRITE TIMING

READ

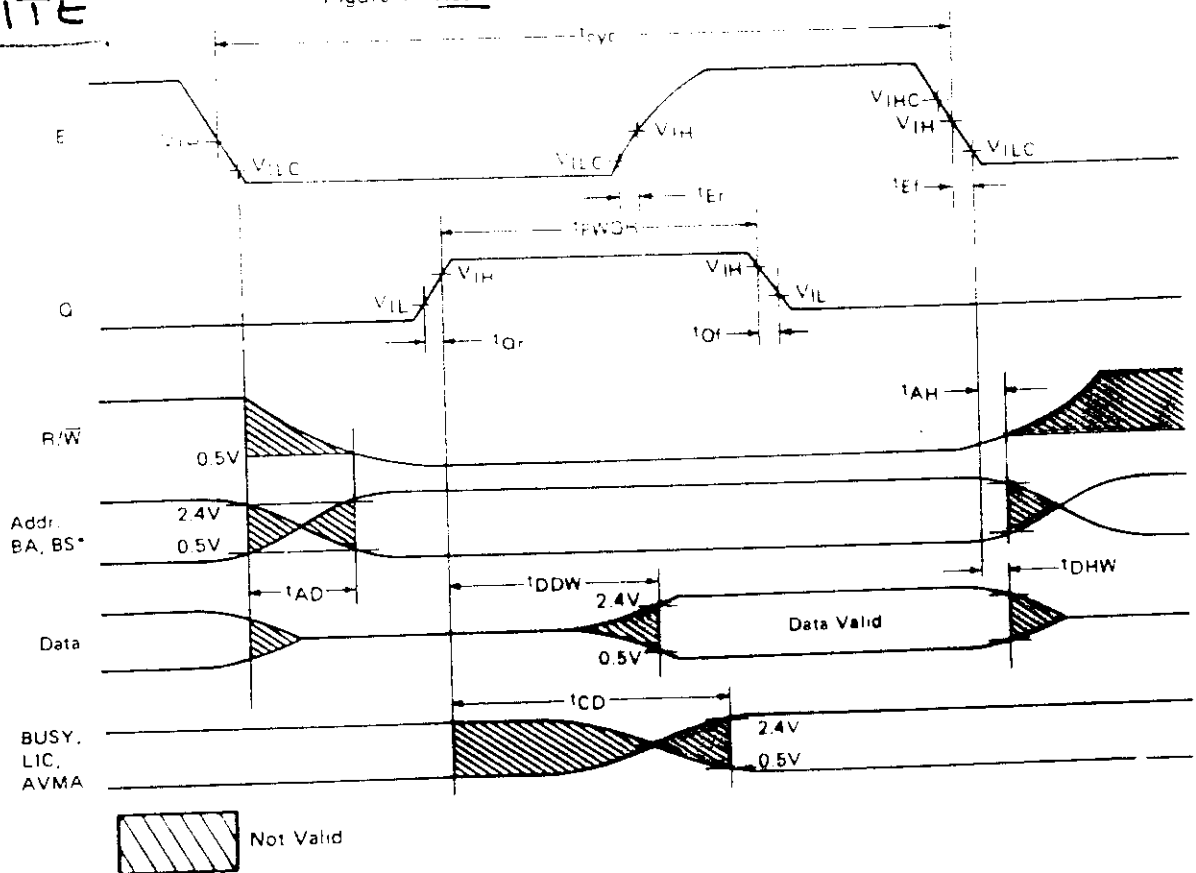


* Hold time for BA, BS not specified

(NOTE) Waveform measurements for all inputs and outputs are specified at logic "High" = V_{IHmin} and logic "Low" = V_{ILmax} unless otherwise specified.

Figure 1 Read Data from Memory or Peripherals

WRITE



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(NOTE) Waveform measurements for all inputs and outputs are specified at logic "High" = V_{IHmin} and logic "Low" = V_{ILmax} unless otherwise specified.

Figure 2 Write Data to Memory or Peripherals

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ISOLATED AND MEMORY MAPPED I/O

THIS TWO TYPES OF I/O HAVE THEIR CAMPIONS

INTEL (8080, 8086, ETC, Z-80).	ISOLATED
MOTOROLA (6809, 68000, ETC)	MEMORY MAPPED

ISOLATED I/O: MICROPROCESSORS SUCH AS Z-80, 8080 ETC. HAVE SPECIAL COMMAND LINES TO INDICATE WHETHER AN I/O OR A MEMORY ACCESS IS BEING EXECUTED. THIS HAS THE EFFECT OF SEPARATING THE I/O AND MEMORY SPACES.
THIS COMMAND LINES ARE ACTIVATED (FOR I/O) BY SPECIFIC INSTRUCTIONS:

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IN B     REGISTER, PORT_ADDRESS
OUT B    PORT_ADDRESS, REGISTER
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THE ADVANTAGES OF SUCH AN APPROACH ARE THAT AS I/O PORT ARE FEWER THAN THE MEMORY ADDRESSES THE PORT ADDRESS DECODING IS DONE USING FEWER ADDRESS LINES SIMPLIFYING THE DECODING CIRCUITS. ALSO THAT NO I/O PORT CAN BE ACCIDENTALLY ACTIVATED BY ADDRESSING MEMORY DUE TO A PROGRAMMING MISTAKE.

MEMORY MAPPED I/O: MOTOROLA MACHINES SUCH AS 6809, 68000, ..., 68040 AND DIGITAL'S PDP-11 MAKE NO DIFFERENCE BETWEEN I/O AND MEMORY ACCESS. I/O AND MEMORY COEXIST IN THE SAME ADDRESS SPACE CONSEQUENTLY PART OF THE SPACE HAS TO BE RESERVED FOR THE I/O PORTS

I/O PORTS AND MEMORY ARE ACCESSED USING THE SAME INSTRUCTIONS AND ADDRESSING MODES.

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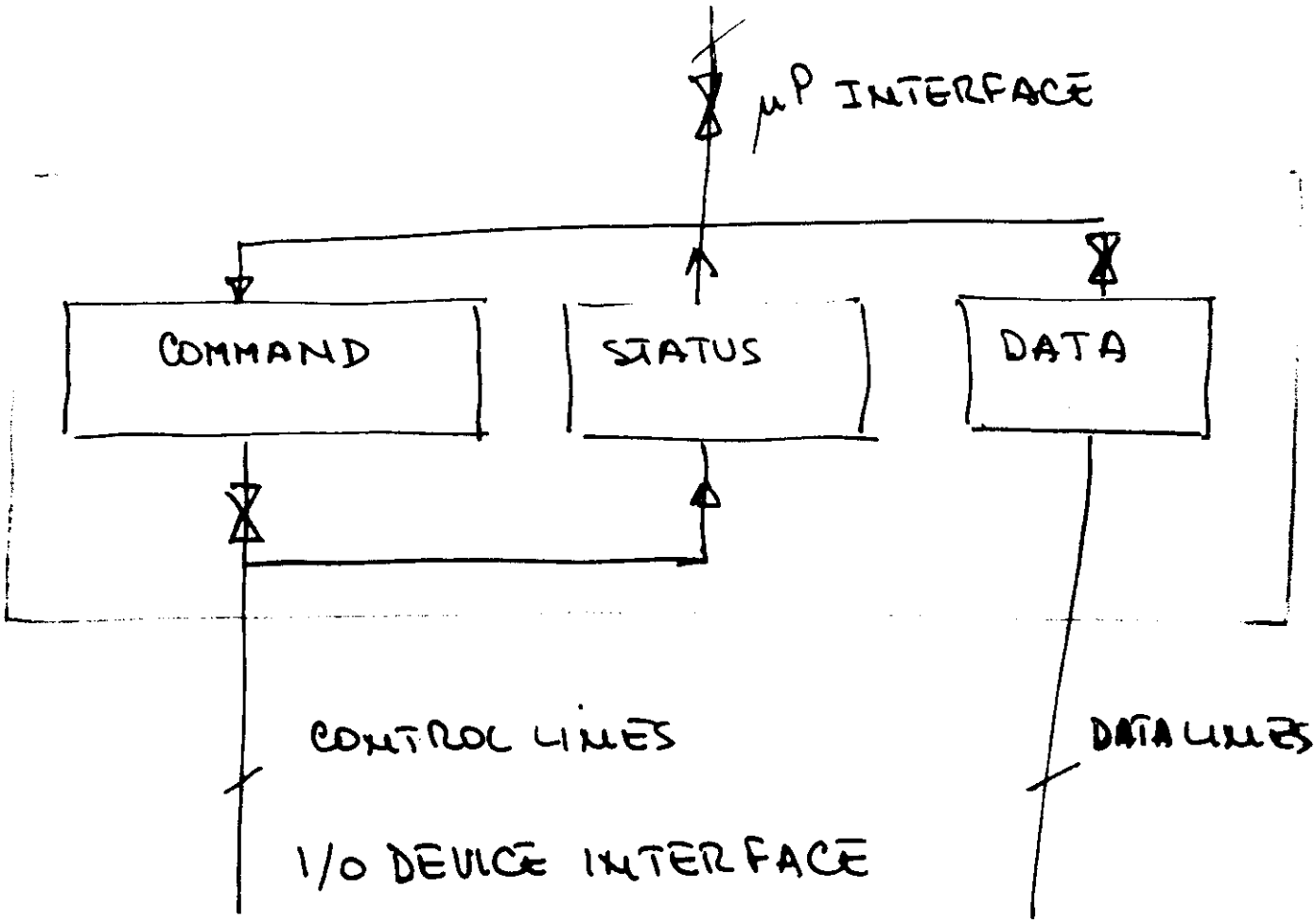
ADVANTAGES OF THIS MODE ARE.

- NO SPECIAL OP-CODES ARE NEEDED SIMPLIFYING THE INTERNAL STRUCTURE OF THE μP.
- LARGE NUMBER OF I/O PORTS ARE POSSIBLE
- MORE SYSTEMATIC HARDWARE STRUCTURE
- ALL ADDRESSING MODES CAN BE USED.

I/O PORTS AND I/O TRANSACTIONS

THE STRUCTURE OF A SIMPLE I/O PORT IS SHOWN.



FOR THE PROGRAMMER THERA THREE MAIN VISIBLE REGISTERS:

- A REGISTER TO HOLD COMMAND ISSUED BY THE μP
- A STATUS REGISTER SO THAT THE μP CAN MONITOR THE ACTIVITY OF THE PORT
- A DATA REGISTER THAT HOLDS THE DATA TO BE TRANSFERED TO/FROM THE μP.

THERE CAN BE OTHER REGISTERS IF NEEDED SUCH AS IN THE CASE OF A FLOPPY DISK CONTROLLER.

I/O TRANSACTIONS

1) PROGRAM-CONTROLLED: THE TRANSACTION IS INITIATED BY AN EXECUTING PROGRAM.

2) INTERRUPT DRIVEN: THE TRANSACTION IS INITIATED BY THE PORT.

THE DIFFERENCE BETWEEN THE TWO IS THE MECHANISM FOR DETECTING WHEN AN I/O PORT HAS COMPLETED AN OPERATION

- IN (1) THE μP INTERROGATES THE PORT
- IN (2) THE PORT GENERATES A SIGNAL CALLED INTERRUPT REQUEST. THE μP RESPONDS TO THIS REQUEST AFTER THE COMPLETION OF THE OPERATION BEING EXECUTED. IT PASSES CONTROL OF THE EXECUTION TO A PIECE OF CODE WRITTEN FOR THE SERVICE OF THE I/O PORTS THAT CAN INTERRUPT. GENERALLY THERE ARE HIERARCHIES OF INTERRUPTS (NMI, FIRQ, IRQ IN 6809 PARLANCE).

I/O DRIVERS

AN I/O DRIVER IS A PIECE OF CODE WRITTEN TO HIDE FROM THE HIGH LEVEL PROGRAMMER THE DETAILS AND PECULIARITIES OF THE I/O PORT (HARDWARE). THE WRITING OF THE I/O DRIVERS REQUIRE AN UNDERSTANDING OF THE MACHINE AND I/O PORTS HARDWARE.

GENERALLY, MACHINES COME WITH READY MADE I/O DRIVERS FOR STANDARD DEVICES SUCH AS

KEYBOARDS, FLOPPY DISKS, DISPLAYS, ETC. BUT IF A NON-STANDARD DEVICE HAS TO BE ADDED AN I/O DRIVER HAS TO BE WRITTEN.

A GOOD DRIVER SHOULD PROVIDE:

- A STANDARD SOFTWARE INTERFACE OR ENVIRONMENT
- PROTECTION AGAINST INCORRECT USES OF THE DEVICE OR PORT
- STANDARD ERROR REPORTING.
- PREVENT DEADLOCK SITUATIONS, CONTENTION BETWEEN USERS, ETC.

FOR SYSTEMS WITH MANY IDENTICAL I/O PORTS AND DEVICES, FOR INSTANCE TERMINALS, IT IS USUAL TO HAVE A SINGLE COPY OF THE DEVICE DRIVER AND TO COMMUNICATE A DEVICE DESCRIPTOR TO THE DRIVER. THIS DEVICE DESCRIPTOR CONTAIN INFORMATION SPECIFIC TO THE DEVICE SUCH AS ADDRESS, SPEED, ETC TO THE I/O DRIVER. THIS TYPE OF I/O DRIVERS ARE GENERALLY CALLED "SHARED DRIVERS".

WE WILL PRESENT, WITHOUT REFERENCE TO ANY SPECIFIC OPERATING SYSTEM, WHAT ARE THE STEPS TO FOLLOW TO PROGRAM AND USE A PROGRAM-CONTROLLED PORT.

AFTER INITIALIZING A PORT (SETTING, BAUD RATE, LINES SET AS INPUTS OR OUTPUTS, ETC) THERE ARE TWO MAIN OPERATIONS (TRANSACTIONS) READ & WRITE.

I/O READ

A) TEST STATUS REGISTER OF PORT AND WAIT FOR READY
B) PASS A READ COMMAND TO THE CONTROL REGISTER.
C) THE µP TEST THE STATUS REGISTER FOR READY
D) THE µP READS THE DATA.

I/O WRITE:

A) TEST THE STATUS REGISTER FOR READY.
B) IT WRITES DATA INTO THE DATA REGISTER
C) IT WRITES INTO THE COMMAND REGISTER A WRITE COMMAND.

SOME OF THESE OPERATIONS CAN BE ASSEMBLED TOGETHER BECOMING JUST ONE INSTRUCTION.

INTERRUPT-CONTROLLED.

THE INITIAL STEPS (BOOT) OF A SYSTEM WITH INTERRUPTS HAVE TO MAKE SURE THAT NO INTERRUPT COMES TO THE µP BEFORE IT IS READY TO ACCEPT THEM. THIS IS DONE EITHER BY A µP THAT UNABLES ITS INTERRUPTS UNTIL READY OR HAVING RESET DISABLE THE PORT INTERRUPT LINES. THE PORT INTERRUPTS ARE POSTERIOUSLY ENABLED UNDER INSTRUCTION COMING FROM THE µP.

I/O READ

A) THE PORT ASSERTS AN INTERRUPT REQUEST

B) WHEN THE µP RECEIVES THE IRQ IT IS GENERALLY IN AN UNINTERRUPTABLE STATE SUCH AS IN THE MIDDLE OF THE EXECUTION OF AN INSTRUCTION OR EXECUTING A PIECE OF CODE CALLED BY AN IRQ OF HIGHER PRIORITY.
AT A LATER TIME, WHEN INTERRUPTS ARE PERMITTED THE µP WILL ACKNOWLEDGE THE IRQ A START A DEVICE-IDENTIFICATION TRANSACTION. IT CAN BE DONE IN THREE DIFFERENT WAYS.

B.1) THE µP TRANSMITS AN ACKNOWLEDGE TO THE WHOLE SYSTEM. THE HIGHEST PRIORITY PORT WITH PENDING IRQ WILL RESPOND BY PLACING ITS IDENTIFIER ON THE BUS. THE µP THEN INITIATES EXECUTION AT AN ADDRESS THAT IS A FUNCTION OF THE IDENTIFIER

B.2) THE µP ISSUES A SIGNAL TO EACH PORT INDIVIDUALLY STARTING WITH THE HIGHEST PRIORITY PORT. THE IRQ PENDING PORT ACKNOWLEDGES THE INTERROGATION. THE µP BRANCHES TO THE PROPER SERVICE ROUTINE.

B.3) THE µP HAS AS MANY IRQ LINES AS THERE ARE I/O PORTS AND EACH ASSERTS A DIFFERENT LINES.

C) THE PROCESSOR EXECUTES A PROGRAM THAT ACCEPTS THE DATA. AT THE CONCLUSION OF AN I/O TRANSACTION THE PROCESSOR RETURNS TO THE INTERRUPTED PROGRAM.

I/O WRITE.

A) THE PROCESSOR ENABLES THE IRQ LINES OF THE PORT AND TRANSMIT THE DATUM AND WRITE COMMAND.

B) THE PROCESSO RETURNS TO OTHER ACTIVITIES WHILE THE PORT TRANSMIT THE DATUM TO THE I/O DEVICE. (WHEN THE I/O PORT HAS FINISHED IT ISSUES AN INTERRUPT REQUEST.

C) AT THE RIGHT TIME THE µP ISSUES AN ACKNOWLEDGE AFTER IDENTIFYING THE INTERRUPTING DEVICE.

D) IF THE µP HAS MORE DATA TO TRANSFER IT WILL REPEAT THE PREVIOUS STEPS. ELSE IT WILL CONTINUE THE EXECUTION OF THE INTERRUPTED PROGRAM.