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FIFTH COLLEGE ON MICROPROCESSORS: TECHNOLOGY AND APPLICATIONS IN PHYSICS

2 - 27 October 1989

Transputers

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TRANSPUTERS

(an introduction)

R.W. ROBINSON, CERN

AIM

- TO GIVE YOU THE FLAVOUR OF TRANSPUTER TECHNOLOGY

CONTENT

- DISCUSS MULTI μP SYSTEMS
- EXPLAIN WHAT IS A TRANSPUTER AND WHAT IS OCCAM
- TRANSPUTER CHIP AND BOARD PRODUCTS
- A TRANSPUTER SUPER COMPUTER
- WHATS GOOD, WHATS BAD ABOUT TRANSPUTERS.

The "raison d'etre" for Transputers

- More and more applications can benefit from using multiple processors
- Single processors are powerful and getting still more powerful but eventually their speed will plateau out.
- Cost of μPs means few cost constraints in using multiple processors. On paper you can achieve supercompute performance with quite a modest array of μPs. More later on this.
- Conventional μPs designed to be used singly.
- What is needed is a microprocessor that is designed from the start to be used as a building block in an array of processors
- Enter the Transputer designed by INMOS, introduced 1985.

What is a Transputer?

A family of micro-computers which have the following components packaged on a single chip:

* An integer processor.

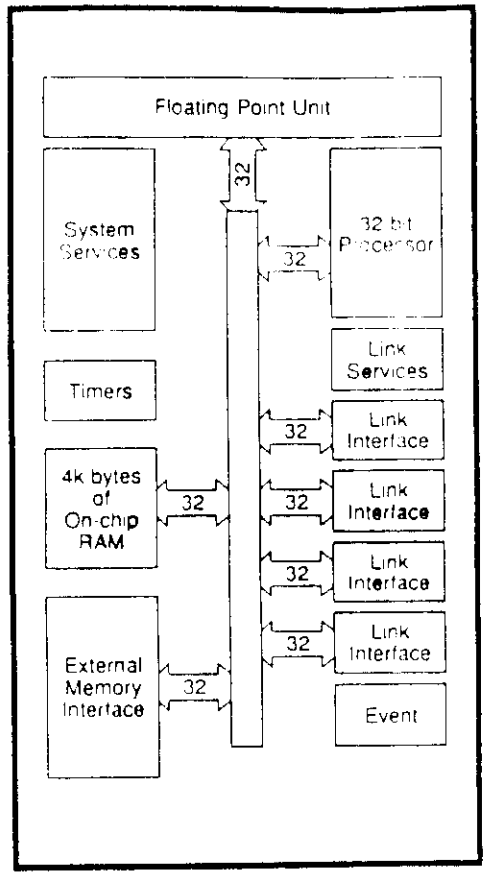
* 2 or 4kbytes of fast SRAM.

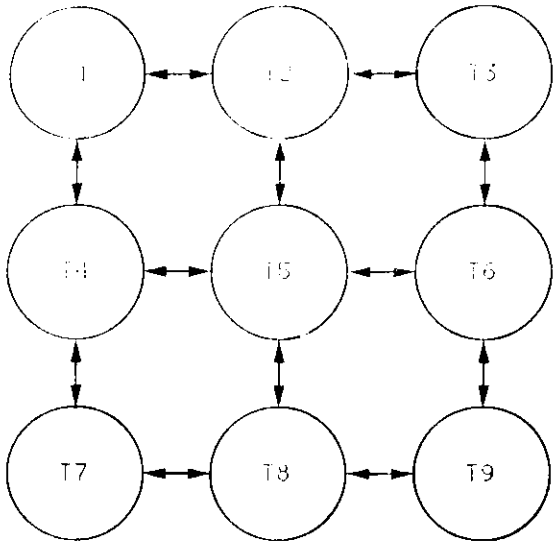
* Four serial links which allow easy connection to other Transputers.

* An interface to external memory.

* A real time kernel for process scheduling.

* Some Transputers also have an on chip floating point processor.





An array of Transputers communicating via their links. The Transputer hardware and the Occam language makes this easy to do!

Performance.

* The 20 MHz T800 chip you will be using has computational power of 1.5 to 3 Vax 11/780 equivalents.

* Low context switching over head, a few microseconds.

* Process to process link transfer rates of 1.7 Mbytes/s between two Transputers. Only a few microseconds setup time for a link transfer.

Some Simple Ideas About Processes

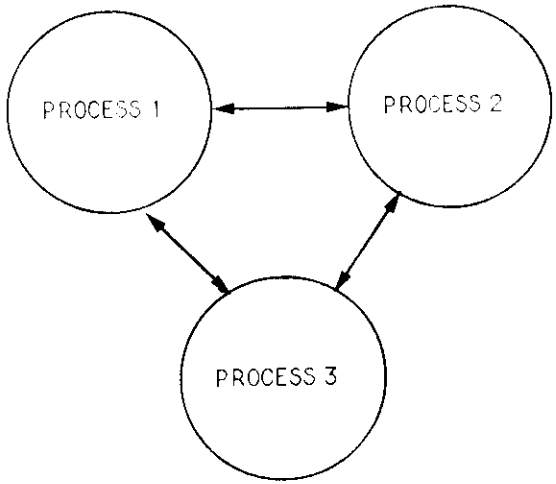
(more later)

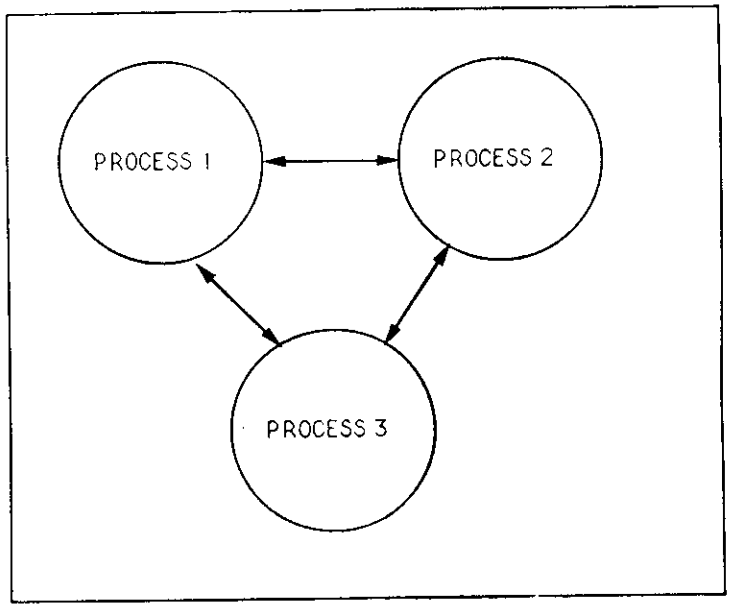
* An application can be made up of a number of communicating processes. For the moment we loosely use process to mean a part of the overall program.

*There are various different ways of mapping processes onto (one or more) processors. All processes could reside in a single processor or the program may be partitioned, most likely for performance reasons , over several processors.

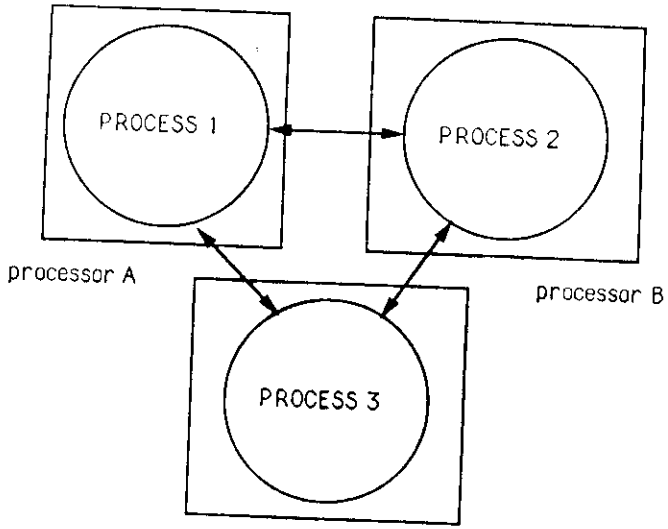
* We shall see that Transputers, their links and Occam make it relatively easy spread an application over multiple processors.

* You might like to consider how you would do this with orthodox microprocessor chips and languages!





processor 1



processor A

processor B

processor C

occam

A LANGUAGE FOR PARALLEL PROGRAMMING.

MODERN STRUCTURED LANGUAGE + PARALLELISM)

ALLOWS SPECIFICATION THAT PROCESSES

SHOULD RUN IN PARALLEL ON

A SINGLE TRANSPUTER

PAR

- ... process 1
- ... process 2
- ... process 3

IN THIS CASE THE TRANSPUTER

TIME SLICES BETWEEN THE 3

PROCESSES

- COMMUNICATION BETWEEN PROCESSES

  TAKES PLACE VIA CHANNELS

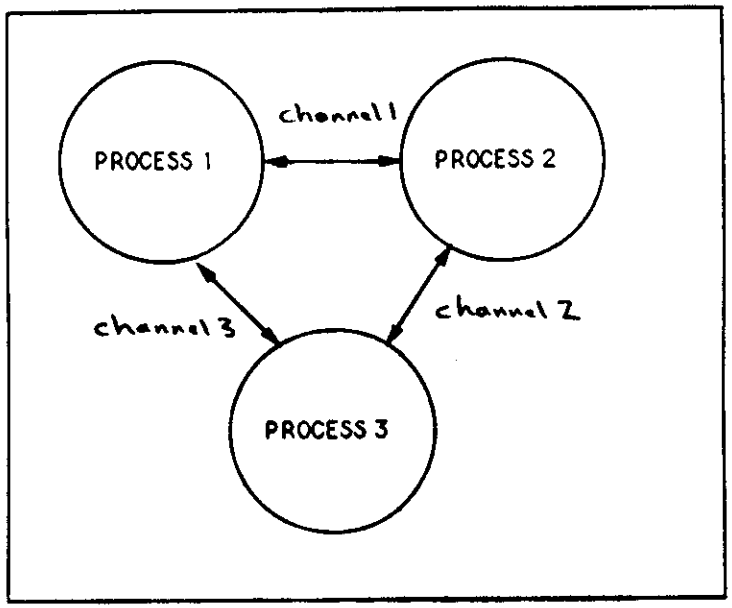
  AND MESSAGE PASSING

- SEND A VARIABLE DOWN A CHANNEL

  channel1 ! x

- RECEIVE A VARIABLE FROM A CHANNEL

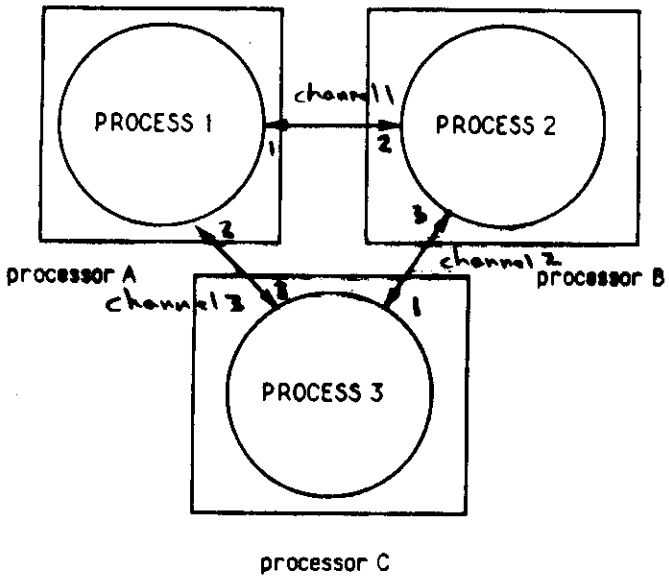
  channel1 ? x



processor 1

- OCCAM ALLOWS EXPANSION OF THE IDEA OF PROCESSES COMMUNICATING OVER CHANNELS IN A SINGLE PROCESSOR TO PROCESSES RUNNING TRULY IN PARALLEL IN DIFFERENT PROCESSORS

- OCCAM ALLOWS PROCESSES TO BE PLACED ON PROCESSORS AND CHANNELS TO BE ASSOCIATED WITH PHYSICAL TRANSPUTER LINKS



Link numbers shown in red.

USING TRANSPUTERS AT THE CHIP LEVEL

- TRANSPUTERS REALLY EASY TO BUILD WITH
  - CHEAP ~~#~~ £20 VERY LARGE QUANTITIES SOME VERSIONS
  - LOW COMPONENT COUNT

TYPICAL µP	TRANSPUTER
PROCESSOR CHIP	PROCESSOR CHIP
FP CHIP	
SRAM (FAST MEMORY)	DRAM
TIMER	
C/S IN RAM	GLUE (PALS, 7400 SERIES)
TRAM	
DRAM CONTROLLER	
DRAM	
SERIAL COMMS	
BUS BUFFERS	
GLUE (PALS, 7400 SERIES)	

- FLEXIBLE MEMORY INTERFACE, PROGRAMMABLE STROBES / TIMING + BUILT IN REFRESH NEEDS LITTLE OR NO GLUE.
- CAN PEAK HAN POKE INTO MEMORY VIA LINKS
- EASY LOADING OF PROGRAMS VIA LINKS
- TOOLS FOR EPROMming
- MUCH EASIER TO PROGRAM IN OCCAM THAN ASMB
- MULTI PROCESSOR DEBUGGER

- TRY IT !

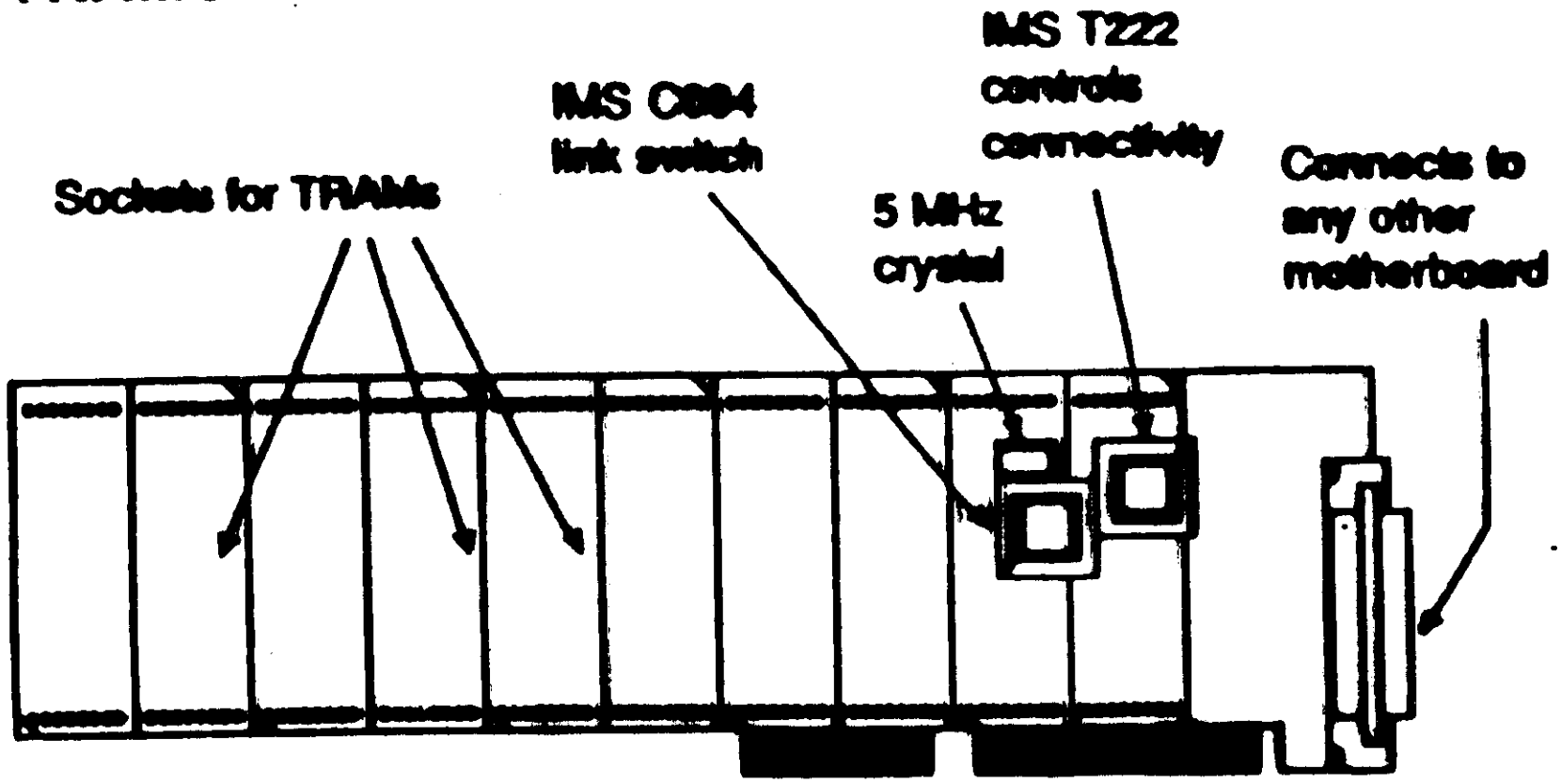
BOARD LEVEL PRODUCTS

- MODULAR SYSTEM OF TRAMS (TRANSPUTER MODULES) FROM INMOS.
- MOTHER BOARDS PLUGGING INTO VARIOUS HOSTS (IBM PC, UME etc) PLUS DAUGHTER BOARD PLUGGING INTO MOTHER BOARDS
- MANY TYPES OF DAUGHTER BOARDS

  PROCESSOR + 32K → 8M MEMORY
  SCSI
  ETHERNET
  GPIB
  LINK DRIVER
  GRAPHICS TRAM
- FLEXIBILITY TO CONFIGURE ACCORDING TO YOUR NEEDS.

Inmos

TRAMS - motherboards



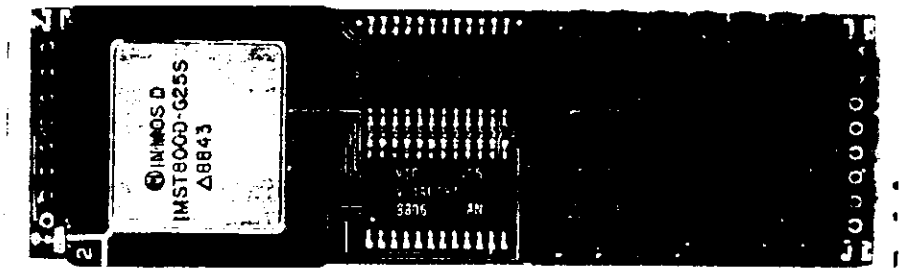
TTM

Transtech TRAMs
TTM16

TTM

Features

- IMST800, IMST425 or IMST414 transputer options
- 4 MBytes of dynamic RAM
- Zero wait state memory option
- 20, 25 or 30 MHz transputer speed option
- Four serial transputer links
- Only 16 active pins
- Industry standard size 1 TRAM
- Compatible with Transtech range of TRAM motherboards



Introduction

The Transtech TTM16 TRAM (TRAnsputer Module) is a small industry standard daughterboard for the Transtech range of TRAM motherboards. It has 4 MBytes of dynamic RAM and is capable of supporting the IMST800, IMST425 and IMST414 transputers.

TRAM Standard

Measuring only 1.05" by 3.66" (2.67mm by 9.30mm) the TTM16 conforms to the published TRAM standard, allowing them to be plugged easily onto a wide range of motherboards for many different host machines. Up to 10 TRAMs can be accommodated on a Transtech TMB08 board for IBM PC XT or AT's and compatibles, 4 on the Transtech TMB04 and TMB05, 16 on a TMB12 double extended eurocard and 32 on the MCP1000 Multi Computing Platform for Sun workstations, allowing rapid prototyping of transputer systems. Transtech TRAMs are also compatible with motherboards from other manufacturers. Further details on the TRAM standard and TRAM Module Motherboard Architecture are published by Prentice Hall in 'Transputer Technical Notes' ISBN 0-130929126-1.

TTM

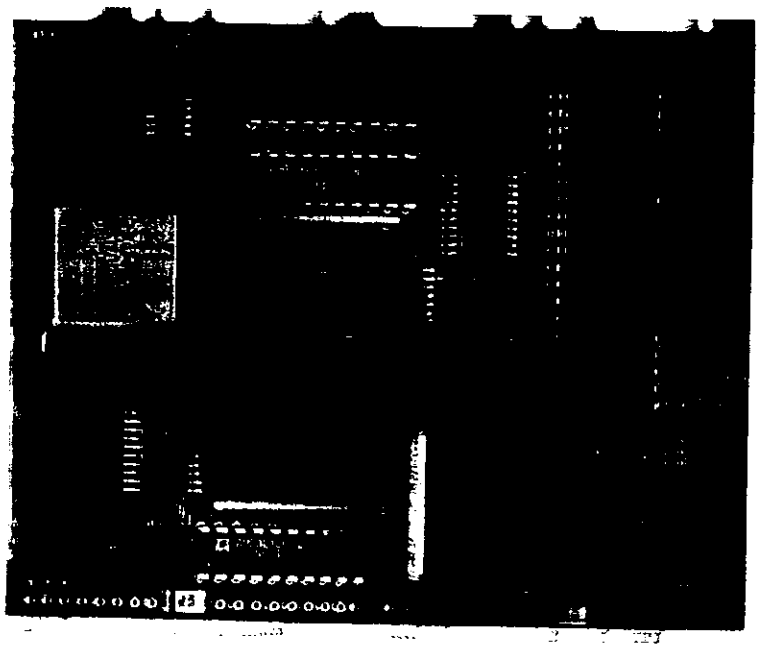
Transtech TRAMs
TTM11

TTM

A SCSI INTERFACE TRANSPUTER MODULE

Features

- IMST222 16-bit transputer
- 1.8 MBytes/sec data rate over SCSI bus
- Extendable to multi master, multi slave system
- Software support with TBIOS disk filing system
- Industry standard size 4 TRAM
- Compatible with Transtech range of TRAM motherboards



Introduction

The Transtech TTM11 is a small daughterboard for the Transtech range of TRAM (TRAnsputer Module) motherboards. It comprises an IMST222 16-bit transputer with 64K of fast static RAM interfaced to a Logic Devices SCSI controller. Data throughput is determined by a single Inmos link bandwidth, typically of the order of 1.2 MBytes/sec, although the SCSI bus side of the module will transfer at data rates of upto 1.8 MBytes/sec.

TRAM Standard

Measuring only 4.20" by 3.66" (10.67mm x 9.30mm) the TTM11 conforms to the published TRAM standard, allowing it to be plugged easily onto a wide range of motherboards for many different host machines. Up to 10 TRAMs can be accommodated on a Transtech TMB08 board for IBM PC XT or AT's and compatibles, 4 on the Transtech TMB04 and TMB05, 16 on a TMB12 double extended eurocard and 32 on the MCP1000 Multi Computing Platform for Sun workstations, allowing rapid prototyping of transputer systems. The TTM11 is compatible with TRAM motherboards from Transtech and also those from other manufacturers. Further details on the TRAM standard and TRAM motherboard architecture are published by Prentice Hall in 'Transputer Technical Notes' ISBN 0-130929126-1.

SOFTWARE FOR CHIPS AND BOARDS

- EXISTS PRIMARILY ON IBM PCs THOUGH RECENTLY AVAILABLE ON VAX, SUN / APOLLO
- EARLY EMPHASIS ON OCCAM BUT NOW HLLs LIKE FTN, C AND PASCAL INCREASINGLY AVAILABE
- MOST WIDELY USED SYSTEM IS TDS . TRANSPUTER DEVELOPMENT SYSTEM

The Transputer Development System is Used as the Basis for the Practical Sessions.

*** An integrated development system for:**

writing and compiling Occam program

running programs on one or several Transputers.

*** Provides the following features:**

A novel "folding" editor.

Occam compiler.

Linker and loader.

Run time support for Occam programs.

Debugger.

Various other utilities.

*** The hardware on which TDS and the user programs run:**

An IBM PC.

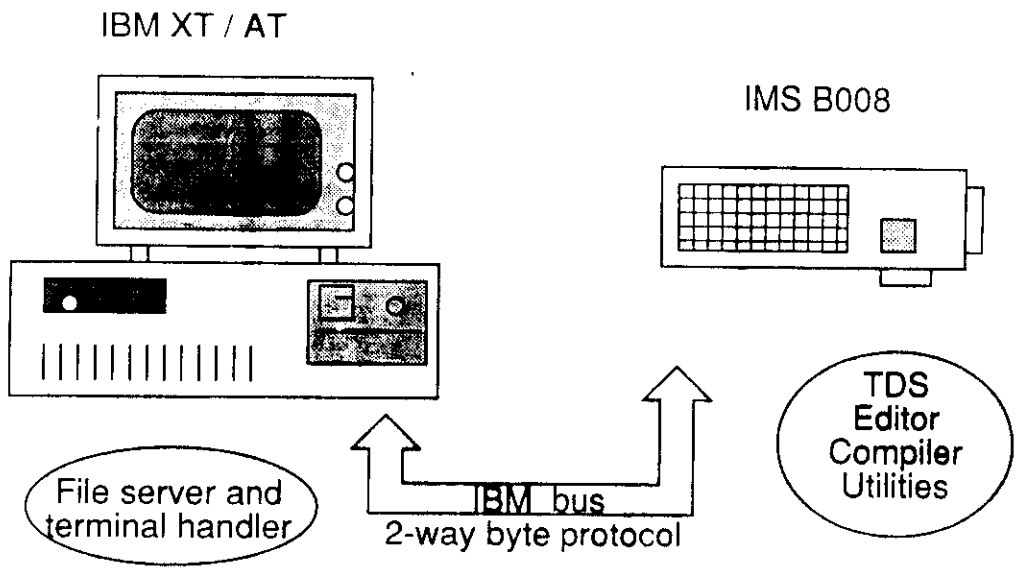
A plug in card for the PC housing several Transputers.

TDS system

* Most of the TDS system runs on the Transputer board.

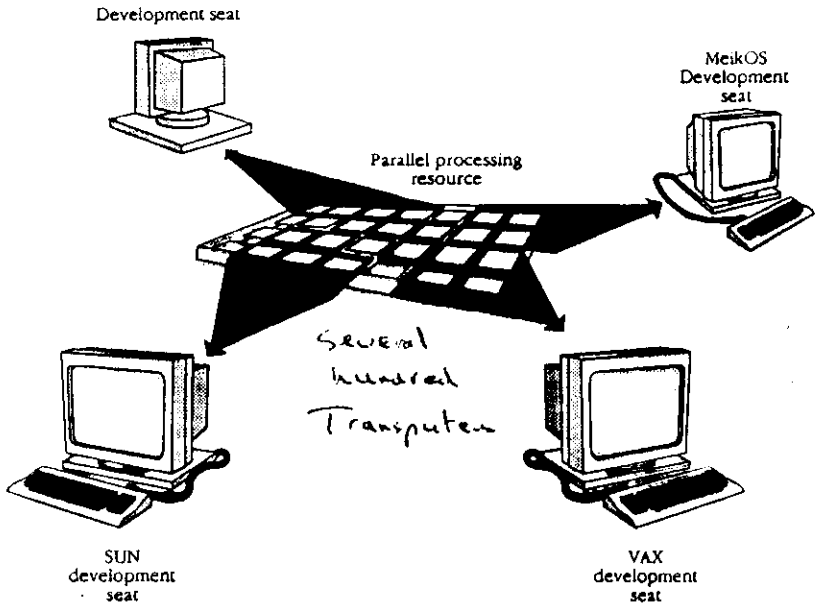
* The PC runs a server, under MS-DOS, which provides access from the Transputer board to its file system, screen and terminal.

* Users see very little of MS-DOS. Once TDS is started it provides a self contained environment. You would see little or no difference using TDS hosted from a PC, a VAX or a SUN workstation.



A TRANSPUTER SUPER - COMPUTER ?

FIG. 3 MULTI-USER PARALLEL PROCESSING RESOURCE



- EXAMPLE : MEIKO COMPUTING SURFACE
- MULTI USER - DIVIDE MACHINE INTO DOMAINS EACH WITH CERTAIN NUMBER OF TRANSPUTERS, USERS LOG INTO DOMAIN TO USE IT
- CAN BE VERY COST EFFECTIVE FOR CERTAIN TYPES OF PROBLEM
  - HEAVY FLOATING POINT
  - LITTLE I/O
- BENCH MARKS AT CERN SHOW FOR SCALER APPLICATIONS ARRAYS OF TRANSPUTERS CAN RIVAL SUPERCOMPUTERS IN POWER

WEAKNESSES OF COMPUTING SCIENCE

FOUND DURING EVALUATION AT CERN

- NOT VERY USER FRIENDLY!
- NEED TO BE AN EXPERT TO GET HIGH PERFORMANCE OUT OF PARALLEL MACHINE
- VERY POOR I/O RATES
- NO EASY WAY TO PORT EXISTING SEQUENTIAL PROGRAM TO PARALLEL MACHINE
- NOT A MAINFRAME REPLACEMENT CHEAP COMPUTE POWER, FEW IF ANY MAINFRAME SERVICES, SO FAR A COMPUTE SERVER FOR EXPERTS.

Table 2: DoDuc benchmark execution times

Static/dynamic refers to global saving/no saving of local variables.

System	Time
Cray XMP/48	48
IBM 3090/E	66
Apollo DN10000 (dynamic)	109
Apollo DN10000 (static)	168
DECstation 3100 (static)	189
3081/E	345
VAX 8800	390
NEC SX-2	882
Inmos B008 T800	971
IBM PC/RT	1360
Apollo 4000	1850
Micro Vax II	2420
VAXstation 2000	2440

1 CRAY = 20 Transputers

***Table 3*: GEXAM1 mean event execution time**

The CERN and Meiko MCS results differ because Meiko forced the most often called subroutine into on chip memory.

System	Time	T(8600)/T(System)
Cray XMP/48	3.05	8.52
IBM 3090/E	3.55	7.32
Apollo DN1000 (dynamic)	6.7	3.88
Apollo DN1000 (static)	9.9	2.63
DECstation 3100 (static)	11.6	2.24
VAX 8800	18.9	1.38
VAX 8600	26	1.0
MCS T800	36.3	0.72
Apollo 3500	90	0.45
Caplin T800	90	0.44
Apollo 3000	128	0.20

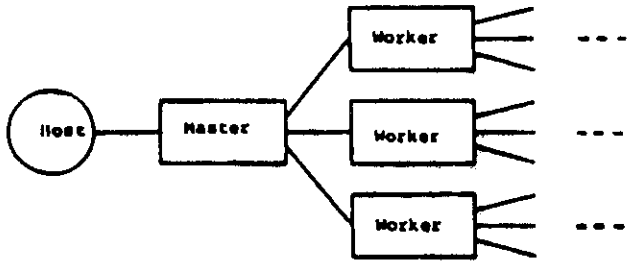
1 CRAY = 10 Transputers

BUT ALSO NOTE

1 CRAY = 2 HIGH END RISC.

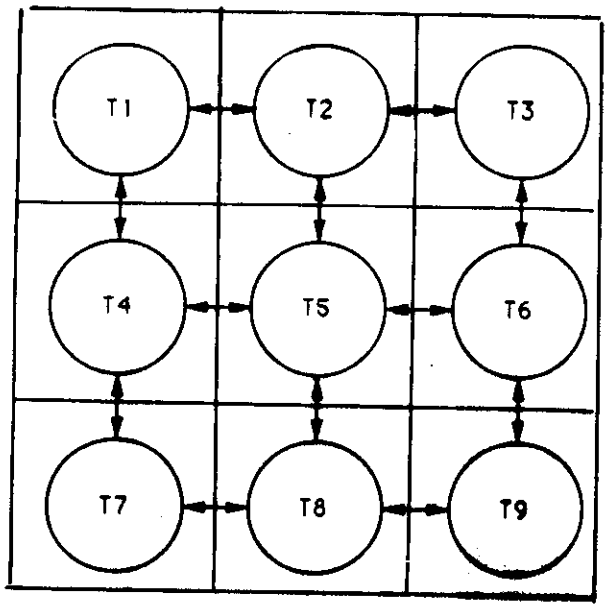
TYPES OF PARALLELISM THAT CAN BE EXPLOITED BY TRANSPUTERS

Processor farm or event parallelism



- REPEATED EXECUTION OF SAME PROGRAM WITH DIFFERENT DATA
- NO COMMUNICATION DURING COMPUTATION BETWEEN TRANSPUTERS
- WORK PACKETS SENT BY MASTER TO WORKER AND RESULTS RETURNED
- WORKS WELL WITH MONTE CARLO SIMULATION AND HEP DATA ANALYSIS

Geometric Parallelism



- MANY PHYSICAL PROBLEMS HAVE AN UNDERLYING GEOMETRIC STRUCTURE
- EG. TAKE AN IMAGE THAT NEEDS TO BE ANALYSED AND MAP IT ONTO TRANSPUTER ARRAY
- EACH PROCESSOR RESPONSIBLE FOR PARTICULAR SPATIAL AREA

PROCESSORS EXCHANGE INFORMATION OVER LINKS DURING COMPUTATION AT SUB AREA BOUNDARIES.

Algorithmic Parallelism

- FEATURES OF THE OVERALL PROCESSING ALGORITHM ARE SPREAD OVER THE PROCESSOR ARRAY

IN SUMMARY

EVERY PARALLELISM	SAME PROGRAM DIFFERENT INDEPENDANT DATA
GEOMETRIC PARALLELISM	GIVE SUBSET OF DEPENDANT DATA TO MULTIPLE PROCESSORS RUNNING "SAME PROGRAM"
ALGORITHMIC PARALLELISM	SPREAD ALGORITHM AND DATA OVER AN ARRAY OF PROCESSORS

PLUS HYBRIDS

TRANSPUTERS — A SUMMARY

- GREAT FOR REAL TIME AND DEDICATED APPLICATIONS
- PARTICULARLY POTENT AND COST EFFECTIVE FOR NUMBER CRUNCHING IF
  - LITTLE I/O
  - HEAVY FP
  - RELATIVELY SMALL AMOUNTS OF MEMORY PER PROCESSOR (1 MEGBYTE DRAM = 1 TRANSPUTER)
- PRESENT SYSTEMS CAN'T OFFER MAINFRAME SERVICES AND CONVENIENCE
- NOT YET VERY USER FRIENDLY TO VAX AND IBM PROGRAMMERS
- HLL TOO SLOW TO COME (OCCAM OVER EMPHASISED)
- MODERN RISC 5 TIMES FASTER FOR NUMBER CRUNCHING THAN T800 TRANSPUTERS. BUT WONT SCALE?

  HOW TO PUT MULTI RISC TOGETHER?

MORE INFORMATION ON TRANSPUTERS CONTACT

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