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FIFTH COLLEGE ON MICROPROCESSORS: TECHNOLOGY AND APPLICATIONS IN PHYSICS

2 - 27 October 1989

DSP Applications in High Energy Physics

D. CROSETTO
CERN, SPS Division, Geneva, Switzerland

MARKET APPLICATIONS

- Radar/Sonar
- Image Processing
- Communications
- Image/Data Compression
- Spectral Analysis
- Speech Processing

FUNCTIONAL APPLICATIONS

- 1-D and 2-D FFT
- 1-D and 2-D DCT
- Auto/Cross Correlation
- Convolution/Filtering
- Modulation/Demodulation
- Vector Multiply/Add

PERFORMANCE BENCHMARKS

Function	time (μsec)
1024-point block-floating complex FFT	
—Single VSP	3300
—Two parallel VSPs	1900
—Four parallel VSPs	1200
1024-point integer complex FFT	2600
128-point block-floating complex FFT	237
16 x 16 FCT	1100
8 x 8-point 2-D complex FFT	164
64 x 64-point 2-D block-floating complex FFT	18000
128-point x 128-point complex vector multiply	53
128-point magnitude-square/accumulate	26
128-point complex modulation or demodulation	52
4 x 4 matrix multiplication	33

DESCRIPTION

The ZR34161 Vector Signal Processor (VSP™) is a member of Zoran's family of high-performance Systems Processors™. The VSP is a 16-bit processor which introduces algorithm-level and vector-oriented instructions to digital signal processing (DSP) system design. It functions as the key element in high-performance DSP applications. In coordination with a host controller, the VSP performs computation-intensive tasks while making minimum demands on host resources and system I/O capacity.

The block diagram shown in Figure 1 illustrates a system which is useful in a number of different applications, such as doppler frequency estimation or "zoom" FFT spectral analysis. It also serves to illustrate the processing power of the VSP. This type of high-performance system is implemented very efficiently by the VSP; most of the blocks in the diagram can be implemented using a single instruction.

WHY THE VSP IS UNIQUE

The VSP achieves its high performance through a number of unique architectural features. Firstly, the VSP uses a "high-level", vector-oriented instruction set; for instance, "FFT" is a single instruction within the VSP. These types of instructions can greatly simplify the amount of programming effort required to implement signal processing algorithms. Secondly, the VSP provides a block floating-point arithmetic capability which will help retain the original dynamic range of an input signal when performing FFT operations. This typically provides dynamic-range performance significantly greater than that of 16-bit fixed-point integer machines. Finally, the nature of its architecture and instruction set allows additional VSPs to be paralleled on the same bus to increase the signal processing throughput well beyond that of a single VSP.

GENERAL FEATURES

- High-performance 16-bit digital signal processor
- Architecture optimized for DSP operations
- High-level Vector-oriented instructions
- Block floating-point arithmetic for FFT
- Concurrent I/O and arithmetic processing
- Easily paralleled for greater throughput
- Fabricated in two micron DLM CMOS
- <300mW power dissipation
- Powerful hardware and software development tools

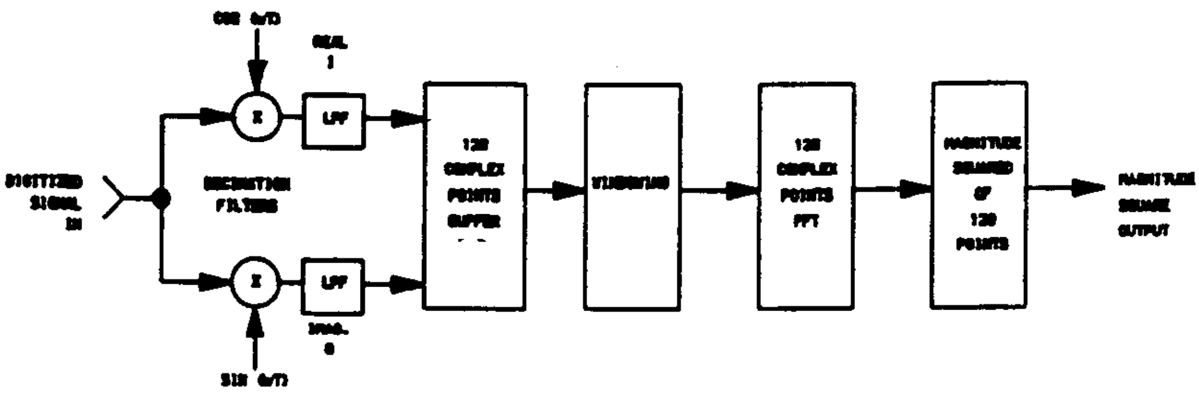


FIGURE 1. BLOCK DIAGRAM OF GENERAL COMPLEX DEMODULATION PROCESS IMPLEMENTED EFFICIENTLY BY THE VSP.

PHILIPS

PCB5010 and PCB5011 at a glance

The PCB5010 and PCB5011 are programmable digital signal processors (DSPs) belonging to our new CMOS SP 50 family of DSP ICs. With their highly parallel architecture and extensive I/O capabilities, they can provide all the processing power you could want. The PCB5010 has on-chip RAM, plus on-chip mask programmable ROM for data and program storage, giving a low chip-count by eliminating the need for external memories.

The PCB5011, a ROMless version, is available for small-scale production runs, and for special situations where a large program memory (up to 64 K) is required.

There are also PCF versions of these chips which are identical except for a higher operating temperature range.

Features of the PCB5010 and PCB5011

- Harvard architecture with two 16-bit data buses
- Up to 6 basic operations performed simultaneously during each instruction. The execution of a new instruction can begin every 125 ns.
- 16 × 16-bit multiplications in a 40-bit hardware multiplier/accumulator plus barrel-shifter/format adjuster
- 2-operand, 31-operation ALU
- Three-port scratchpad file containing fifteen 16-bit registers
- Two 128 × 16-bit static RAMs for data
- Three independent address computation units for the data memories
- Two independent externally-controlled serial input and output channels (up to 4 million bits/s)
- 16-bit bidirectional parallel data port (up to 8 million words/s)
- 16-bit address port including 4 page-bits (64 K × 16-bit external data memory address range)
- Maskable interrupt
- Pipelined mode (P) and non-pipelined mode (NP)
- CMOS technology
- Single 5 V power supply
- Operating temperature range:
  0 to 70 °C for PCB versions
  −40 to 85 °C for PCF versions

Specific features of the PCB5010

- 512 × 16-bit on-chip data ROM (mask programmable)
- 987 × 40-bit on-chip program ROM (mask programmable)
- 32 × 40-bit on-chip program RAM
- 5 × 40-bit on-chip ROM containing a 'load-RAM' program
- 68-pin PLCC package

Specific features of the PCB5011

- A second 16-bit bidirectional parallel data port with a 9-bit address port
- Direct access to 1024 × 40-bit external program memory (or 64 K × 40-bit when some external logic is added)
- 144-pin grid array package

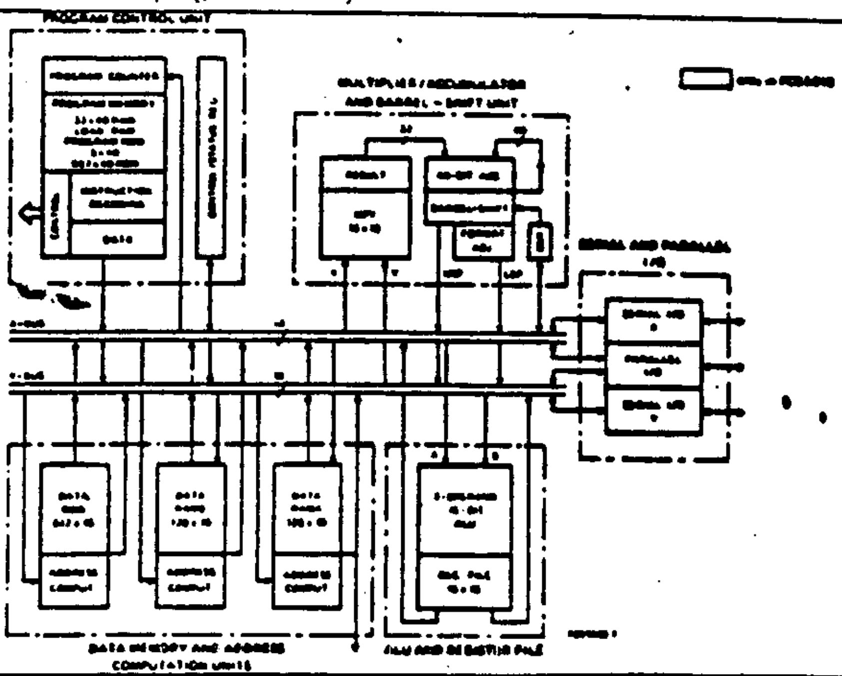


Fig. 1 Simplified block diagram of the PCB5010 and PCB5011 illustrating the double bus structure, powerful arithmetic units and on-board memory

NEC
NEC Electronics Inc.

μPD7723
ADVANCE
SIGNAL PROCESSO

Description

The μPD77230 Advanced Signal Processor (ASP) is the high-end member of a new third-generation family of 32-bit digital signal processors. This CMOS chip implements 32-bit full floating-point arithmetic, and is intended for digital signal processing and other applications requiring high speed and high precision.

All instructions execute in one instruction cycle. The μPD77230 executes a 32-bit by 32-bit floating point multiply with 55-bit product, sum of products, data move, and multiple data pointer manipulations—all in one 150-ns instruction cycle.

Features

- ☐ Fast instruction cycle: 150 ns using 13.3-MHz clock
- ☐ All instructions execute in one cycle
- ☐ 32- x 32-bit floating point arithmetic
- ☐ Large on-chip memory (32-bit words)
  - — 1K data RAM (two 512-word blocks)
  - — 1K data coefficient ROM
  - — 2K instruction ROM
- ☐ 8K- x 32-bit external memory; 4K may be instruction memory
- ☐ 1.5-μm CMOS technology
- ☐ 32-bit internal bus
- ☐ [illegible]-bit ALU bus
- ☐ Dedicated internal buses for RAM, multiplier, and ALU
- ☐ Eight accumulators/working registers (55 bits)
- ☐ 47-bit bidirectional barrel shifter
- ☐ Two independent data RAM pointers
- ☐ Modulo 2^n incrementing for circular RAM buffers
- ☐ Base and index addressing of internal RAM
- ☐ Data ROM capable of 2^n incrementing
- ☐ Loop counter for repetitive processing
- ☐ Eight-level stack accessible to internal bus
- ☐ Two interrupts: maskable and nonmaskable (NMI)
- ☐ Serial I/O (5 MHz)
- ☐ Master/slave mode operation
- ☐ Three-stage instruction pipeline
- ☐ Single +5-volt power supply
- ☐ Approximately 1.2 watts

Ordering Information

Part Number	Package Type
μPD77230R	68-pin PGA

Applications

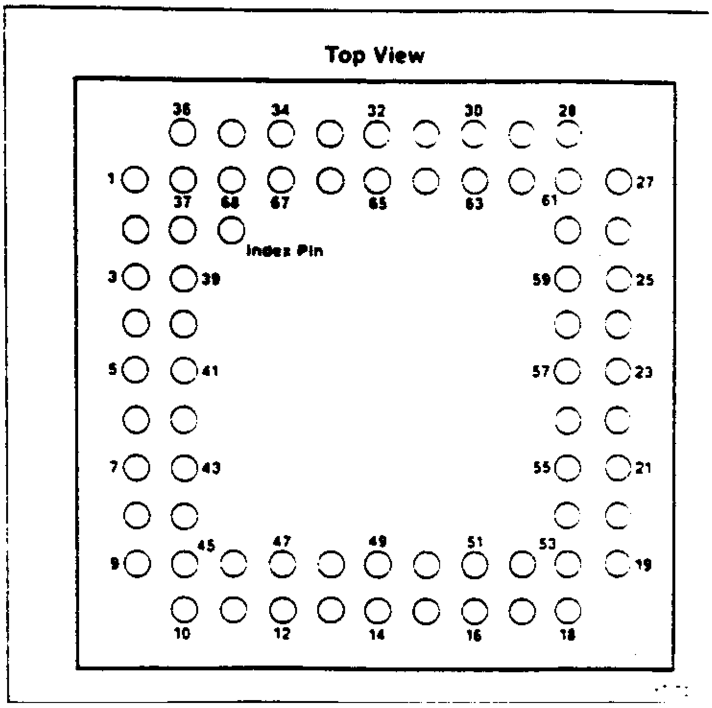
- ☐ General-purpose digital filtering (FIR, IIR, FFT)
- ☐ High-speed data modems
- ☐ Adaptive equalization (CCITT)
- ☐ Echo cancelling
- ☐ High-speed controls
- ☐ Image processing
- ☐ Graphic transformations
- ☐ Instrumentation electronics
- ☐ Numerical processing
- ☐ Speech processing
- ☐ Sonar/radar signal processing
- ☐ Waveform generation

Floating-Point Performance Benchmar

Second-order digital filter (biquad)	0.9
32-tap finite impulse response filter	5.25
Fast Fourier transform (FFT)	
32-point complex (radix 2)	0.15
512-point complex FFT	4.7
1024-point complex FFT	10.75
Square root	6.0

Pin Configuration

68-Pin PGA



FUJITSU (available)

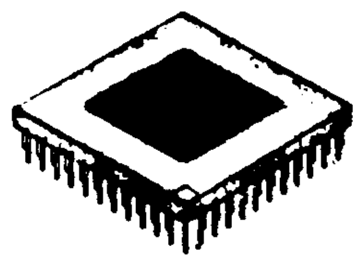
General Purpose Digital Signal Processor

MB 8764

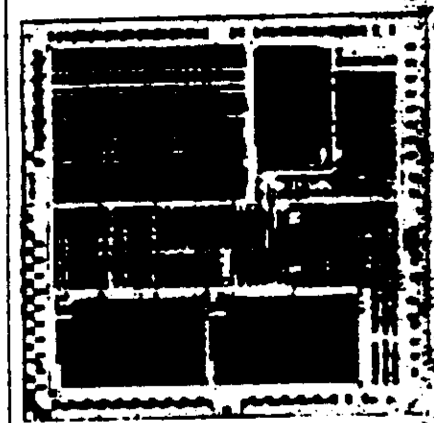
3a

The Fujitsu MB 8764 is a general purpose silicon-gate CMOS digital signal processor (DSP) integrated circuit. The MB 8764 features a high-speed pipelined multiplier, supports concurrent operations with compound instructions and multiple data paths, offers flexible and expandable memory options and has an on-chip DMA channel.
With its high-speed operation, the MB 8764 gives high throughput in various applications, such as telecommunications, signal processing and image processing.
Being packaged in the 88-pin pin grid array, the MB 8764 allows a complex system to be built with the external program ROM and data RAM accessed through dedicated address and data buses.

- General purpose high-speed digital signal processing
- High speed operation
  - 100 ns cycle time
- Parallel pipelined multiply function
  - 16 bits x 16 bits →26 bits
- Divide function
  - 26 bits ÷ 16 bits→16 bits
- Program ROM
  - 1024 words x 24 bits
  - Internal (mask-programmed) and external ROM selectable
- Part of the program ROM can be used for constant data storage
- Two built-in 128 x 16 bits RAMs
- Expansion RAM function
  - Expandable up to 1024 words x 16 bits
  - Two access speed rates can be selected
- Numerous I/O functions
  - 16-bit parallel interface
  - Three input modes and two output modes including DMA
- Powerful instruction set using compound instructions
  - One level of subroutine nesting (multi-level nesting can be programmed)
  - Two levels of loop nesting (multi-level nesting can be programmed)
  - Compound instructions (for example, an arithmetic/logic instruction combined with a move instruction) enable concurrent processing
  - 15 arithmetic/logic instructions
- Addressing
  - Direct addressing
  - Indexed addressing
  - Immediate addressing
  - Virtual shift addressing
- Silicon-gate CMOS process
- Single 5 volt power supply, TTL I/O interface (except pins for clock signals)
- 88-pin space-saving pin grid array package
- Support tool, including cross-assembly software and evaluation board for IBM-PC and VAX



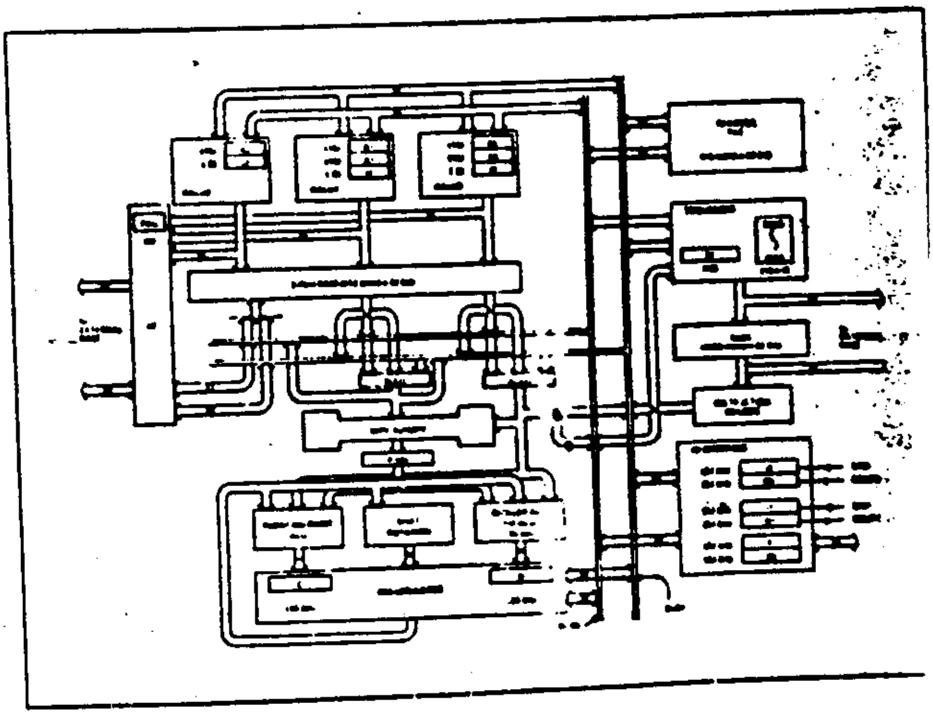
CERAMIC PACKAGE
RIT-88C-A01



This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields. However, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to this high impedance circuit.

F³-DSP (Fastest Fujitsu Floating-point DSP)

Features	
Cycle time	55 ns
Mult/Acc time	55 ns
Multiplier (Input 2x32 bit = result 48 bit)	FIX/FLOAT
ALU (Input 32 bit/36 bit = result 36 bit)	FIX/FLOAT
M-ROM internal prog. mem.	4 K words x 32
E-ROM external prog. mem.	64 K words x 32
RAM on-Chip-3-port	512 words x 32
RAM external DATA-RAM	1 MEGA words x 32
Register file	16 words x 32
Ext RAM I/O controller	
2 internal DATA BUSES	
Ext. RAM DATA BUS and common I/O BUS are seperated	
I/O controller for common I/O operations	
3 independent Addressing Units for DATA-RAM	
2 Serial Input and 2 Serial Output lines	
3-Stage PIPELINE operation	
4 subroutine levels	
16 interrupts	



FEATURES
Separate Program and Data Buses, Extended Off-Chip
Single-Cycle Direct Access to 16K × 16 of Data Memory
Single-Cycle Direct Access to 16K × 24 (Expandable to 32K × 24) of Program Memory
Dual Purpose Program Memory for Both Instruction and Data Storage
Three Independent Computational Units: ALU, Multiplier/Accumulator and Barrel Shifter
Two Independent Data Address Generators
Powerful Program Sequencer
Internal Instruction Cache
Provisions for Multiprecision Computation and Saturation Logic
Single-Cycle Instruction Execution
Multifunction Instructions
Four External Interrupts
125ns Cycle Time
600mW Maximum Power Dissipation with CMOS Technology
100-Pin Grid Array

APPLICATIONS
Optimized for DSP Algorithms Including
Digital Filtering
Fast Fourier Transforms
Applications Include
Image Processing
Radar, Sonar
Speech Processing
Telecommunications

GENERAL DESCRIPTION
The ADSP-2100 is a single-chip microprocessor optimized for digital signal processing (DSP) and other high-speed numeric processing applications. It integrates computational units, data address generators and a program sequencer in a single device.

The ADSP-2100 makes efficient use of external memories for ogram and data storage, freeing silicon area for increased processor performance. The resulting architecture combines the functions and performance of a bit-slice/building block system with the ease of design and development of a general-purpose microprocessor. The ADSP-2100 (K Grade) operates at 8.192MHz. Every instruction executes in a single 125ns cycle. Fabricated in a high-speed 1.5 micron double-layer metal CMOS process, the ADSP-2100 dissipates less than 600mW.

The ADSP-2100's flexible architecture and comprehensive instruction set support a high degree of operational parallelism. one cycle the ADSP-2100 can:

- generate the next program address
- fetch the next instruction
- perform one or two data moves
- update one or two data address pointers
- perform a computational operation.

DEVELOPMENT SYSTEM
The ADSP-2100 is supported by a complete set of tools for software and hardware system development. The Cross-Software System provides a System Builder for defining the architecture of systems under development, an Assembler, a Linker and a Simulator. The Simulator provides an interactive instruction-level simulation. A PROM Splitter generates PROM burner compatible files. An Emulator is available for hardware debugging of ADSP-2100 systems.

ADDITIONAL INFORMATION
For additional information on the architecture and instruction set of the processor, refer to the *ADSP-2100 User's Manual*. For more information about the Development System, refer to the *ADSP-2100 Cross-Software Manual* and the *ADSP-2100 Emulator Manual*. For examples of a variety of ADSP-2100 applications routines, refer to the *ADSP-2100 Applications Handbook, Volume 1*. Manuals are available from your local Analog Devices sales office. See ordering information.

inmos

Cascadable Signal Processor

Preliminary

FEATURES

- Full 16 bit, 32 stage, transversal filter
- Fully cascadable with no speed degradation or reduction in dynamic range.
- Coefficients selectable as 4, 8, 12, or 16 bits wide
- Data throughput to 10 MHz
- High speed microprocessor compatible interface.
- Data input and output through dedicated ports or via the microprocessor interface
- Fully static high speed CMOS implementation
- TTL compatible
- Single +5V ±10 % power supply
- Power dissipation < 1.5 Watts
- Standard 84-pin ceramic PGA

APPLICATIONS

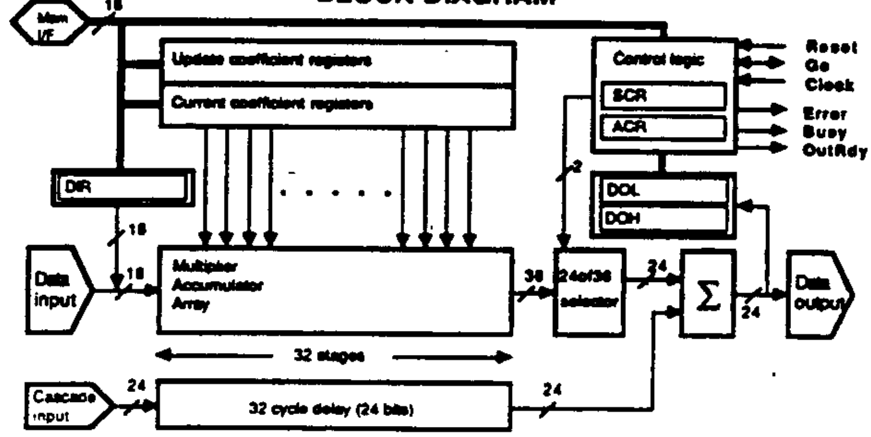
- Digital FIR filtering
- High speed adaptive filtering
- Correlation and Convolution
- Discrete Fourier Transform
- Speech processing using Linear Predictive Coding
- Image processing
- Waveform synthesis
- Adaptive and fixed equalizers and echo cancellers
- Spread spectrum communication
- Beamforming and beamscanning in sonar and radar
- Pulse compression
- High speed fixed point matrix multiplication

DESCRIPTION

The IMS A100 is a high speed, high accuracy 32 stage digital transversal filter. It's flexible architecture allows it to be used as a "building block" in a wide range of Digital Signal Processing (DSP) applications. The part is capable of performing high speed DFTs, convolution, and correlation, as well as many filtering functions.

The input data word length is 16 bits, and coefficients are programmable to be 4, 8, 12, or 16 bits wide; two's complement numerical formats are used for both data and coefficients. The coefficients can be updated asynchronously to the system clock during normal operation, allowing the chip to be used in a variety of adaptive systems. The IMS A100 can also be cascaded to construct longer transversal filters with no additional logic or degradation in speed, whilst preserving a high degree of accuracy. The device is controlled through a standard memory interface, allowing use with any general purpose microprocessor. Data communications can be either through the memory interface, or through dedicated data ports.

BLOCK DIAGRAM



APRIL 1987

2.1.1 Harvard Architecture

The TMS32010 utilizes a modified Harvard architecture in which program memory and data memory lie in two separate spaces. This permits a full overlap of instruction fetch and execution.

Program memory can lie both on-chip (in the form of the 1536 X 16-word ROM) and off-chip. The maximum amount of program memory that can be directly addressed is 4K X 16-bit words.

Instructions in off-chip program memory are executed at full speed. Fast memories with access times of under 100 ns are required.

Data memory is the 144 X 16-bit on-chip data RAM. Instruction operands are fetched from this RAM; no instruction operands can be directly fetched from off-chip. However, data can be read into the data RAM from a peripheral by using the IN instruction or read from program memory by using the TBLR (table read) instruction. The OUT instruction will write a word from the data RAM to a peripheral, while a TBLW instruction will write a data RAM word to program memory (presumably, off-chip).

Figure 2-2 outlines the overlap of the instruction prefetch and execution. On the falling edge of CLKOUT, the program counter (PC) is loaded with the instruction (load PC2) to be prefetched while the current instruction (execute 1) is decoded and is started to be executed. The next instruction is then fetched (fetch 2) while the current instruction continues to execute (execute 1). Even as another prefetch occurs (fetch 3), both the current instruction (execute 2) and the previous instruction are both still executing. This is possible because of a highly pipelined internal operation.

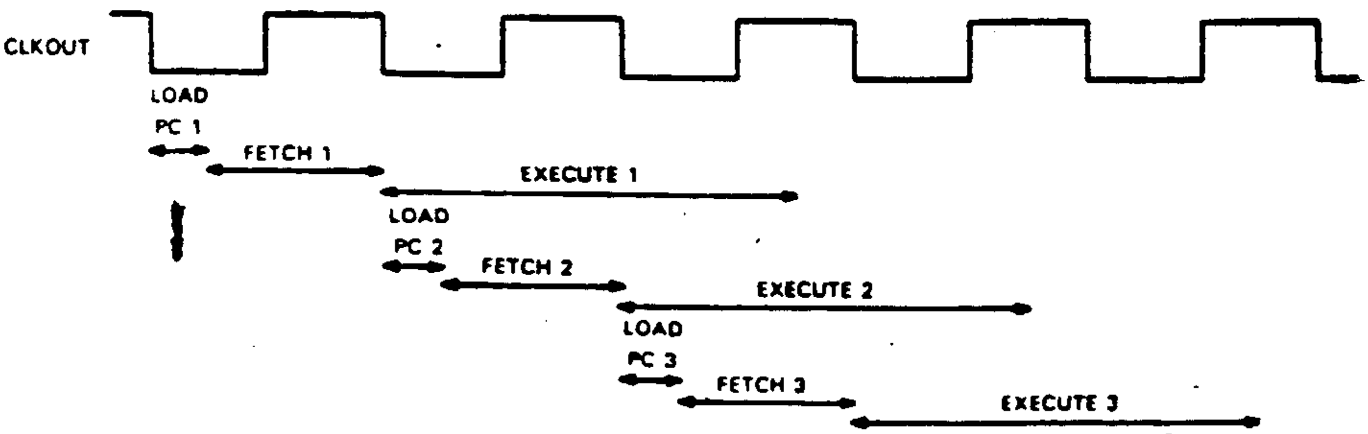


FIGURE 2-2 - HARVARD ARCHITECTURE

KEY FEATURES

- 16-bit instruction/data word
- 32-bit ALU/accumulator
- 16 x 16-bit multiply in 200 ns
- 0 to 15-bit barrel shifter
- Eight input and eight output channels
- 160ns or 200-ns instruction cycle
- 288-byte on-chip data RAM
- ROMless version – TMS32010
- 2.7-micron NMOS technology or CMOS
- Single 5-V supply
- 40-pin DIP
- 16-bit bidirectional data bus with 40-megabits-per-second transfer rate
- Interrupt with full context save
- Signed two's complement fixed-point arithmetic

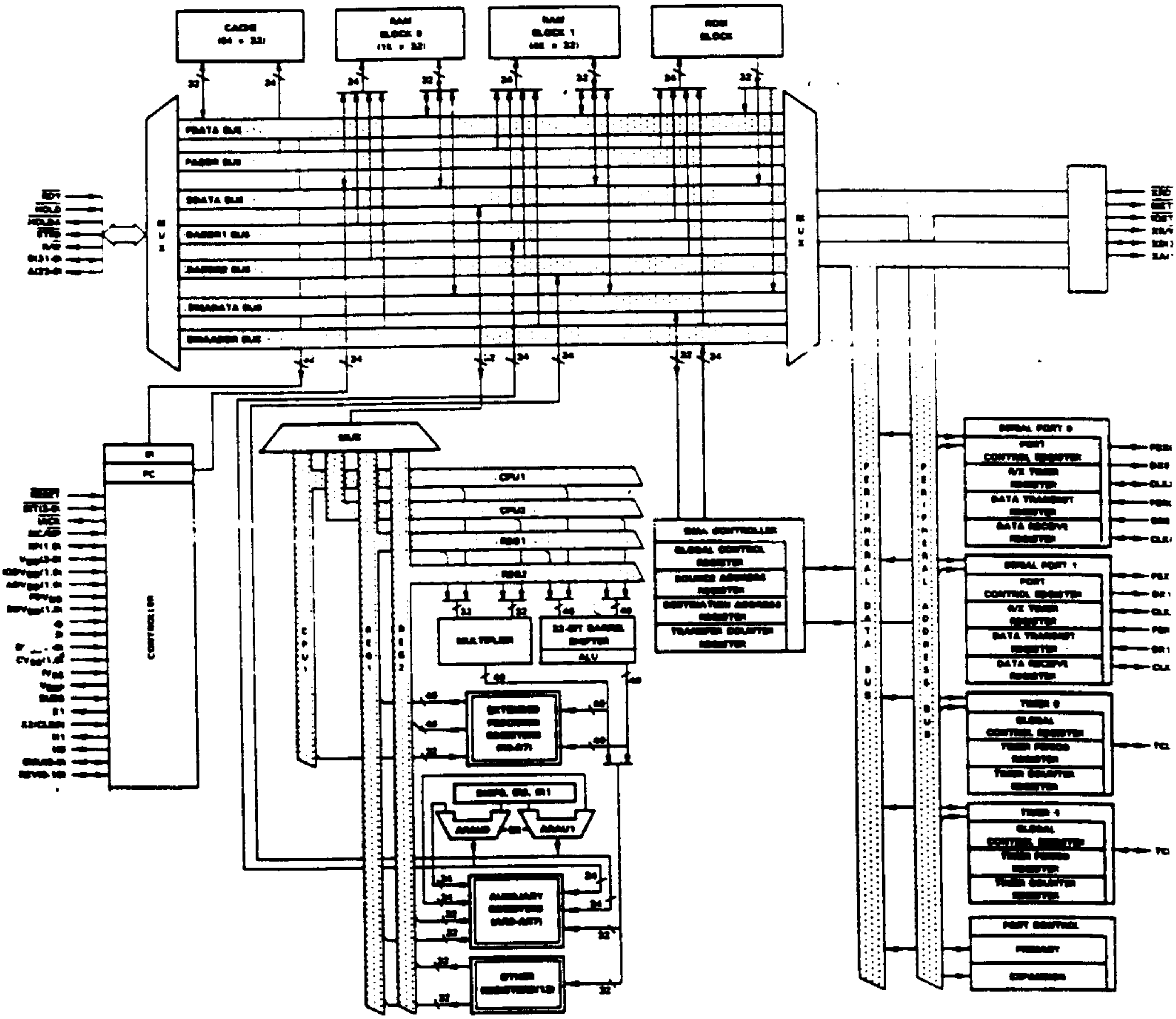


Figure 3-1. TMS320C30 Block Diagram

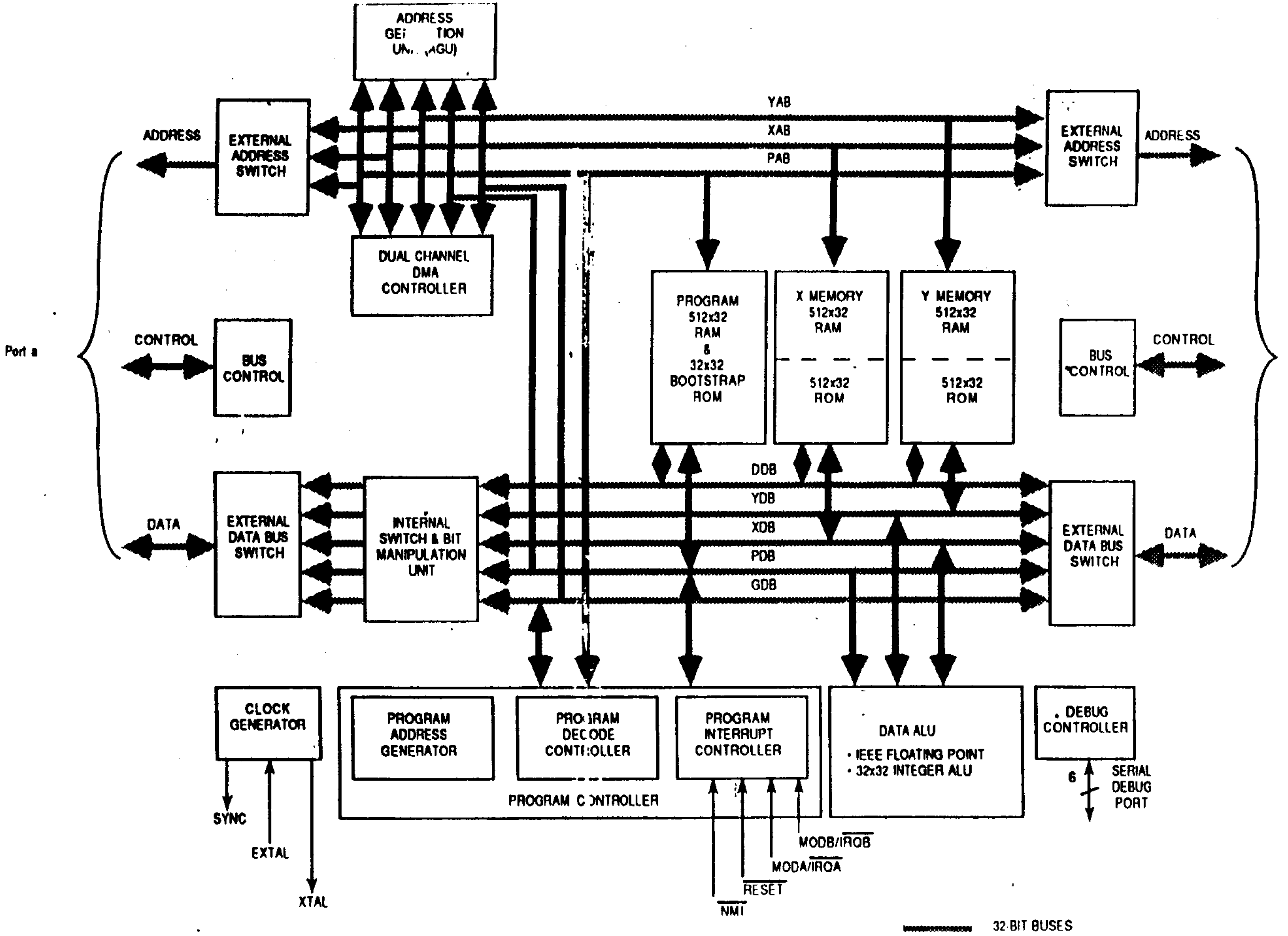
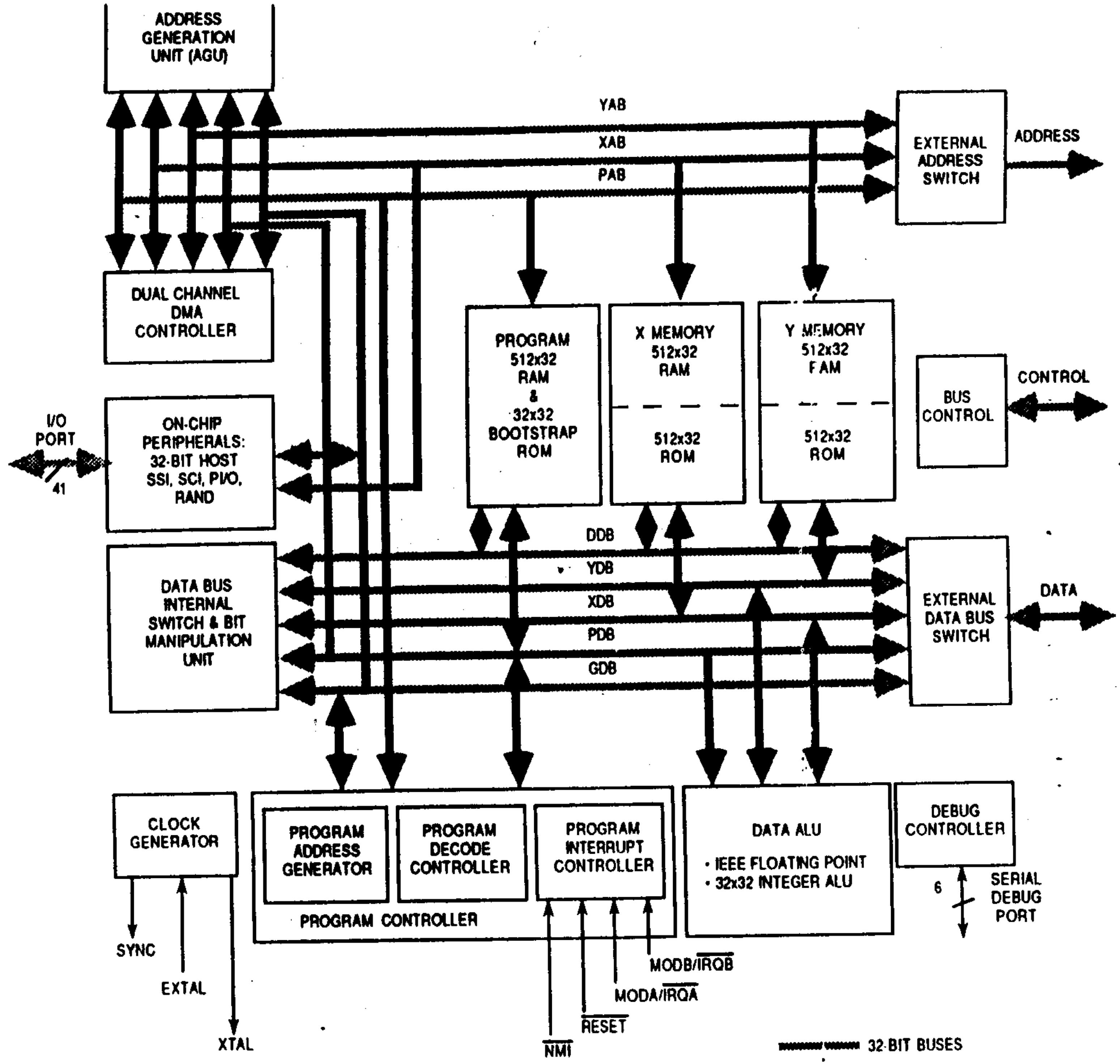
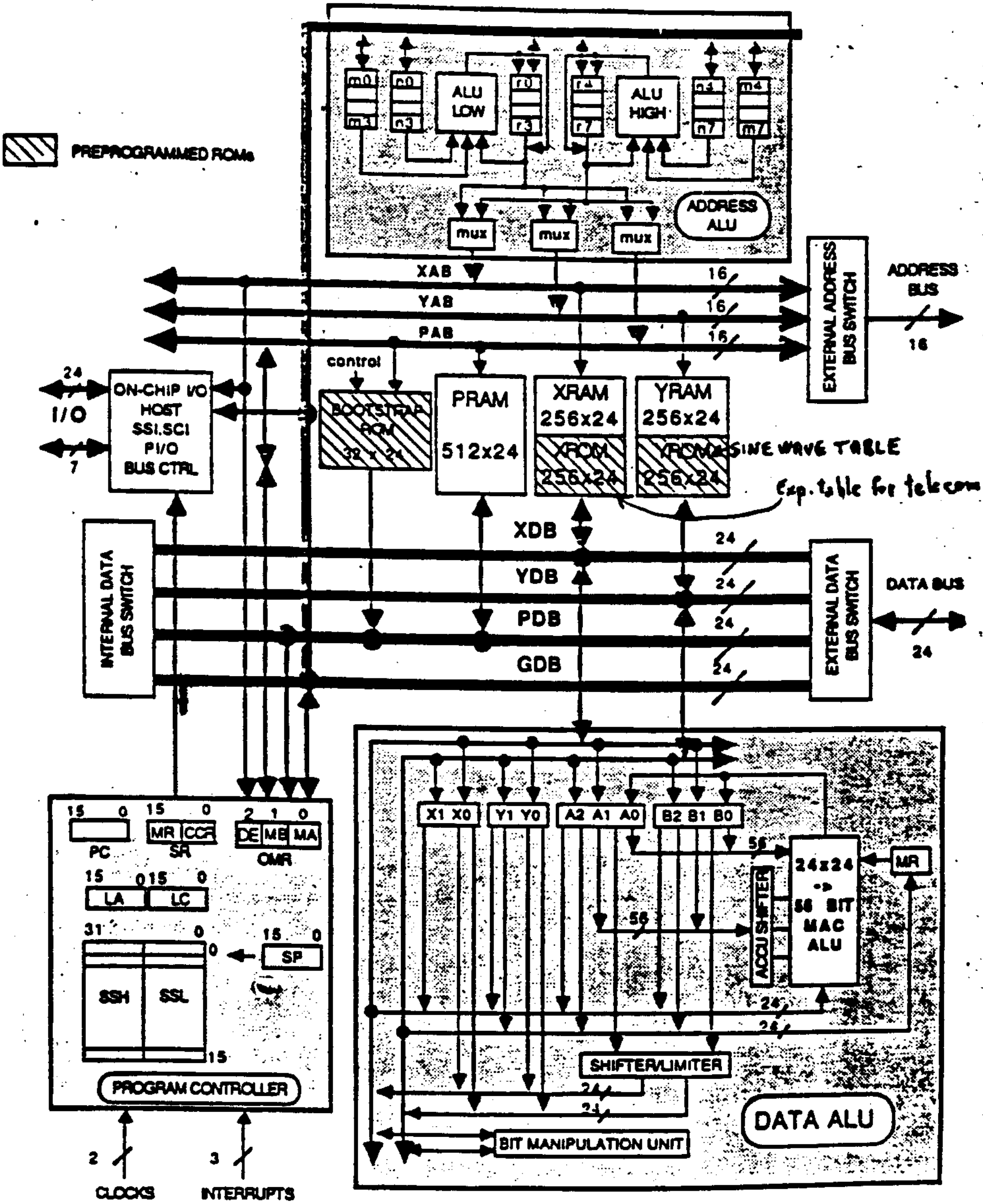


Figure 2. DSP96002 Block Diagram


ADDRESS GENERATION UNIT (AGU)
YAB
XAB
PAB
EXTERNAL ADDRESS SWITCH
ADDRESS
DUAL CHANNEL DMA CONTROLLER
PROGRAM 512x32 RAM & 32x32 BOOTSTRAP ROM
X MEMORY 512x32 RAM
512x32 ROM
Y MEMORY 512x32 RAM
512x32 ROM
BUS CONTROL
CONTROL
I/O PORT
41
ON-CHIP PERIPHERALS: 32-BIT HOST SSI, SCI, PI/O, RAND
DDB
YDB
XDB
PDB
GDB
DATA BUS INTERNAL SWITCH & BIT MANIPULATION UNIT
EXTERNAL DATA BUS SWITCH
DATA
CLOCK GENERATOR
SYNC
EXTAL
XTAL
PROGRAM ADDRESS GENERATOR
PROGRAM DECODE CONTROLLER
PROGRAM INTERRUPT CONTROLLER
PROGRAM CONTROLLER
NMI
RESET
MODA/IRQA
MODB/IRQB
DATA ALU
• IEEE FLOATING POINT
• 32x32 INTEGER ALU
DEBUG CONTROLLER
6
SERIAL DEBUG PORT
32-BIT BUSES

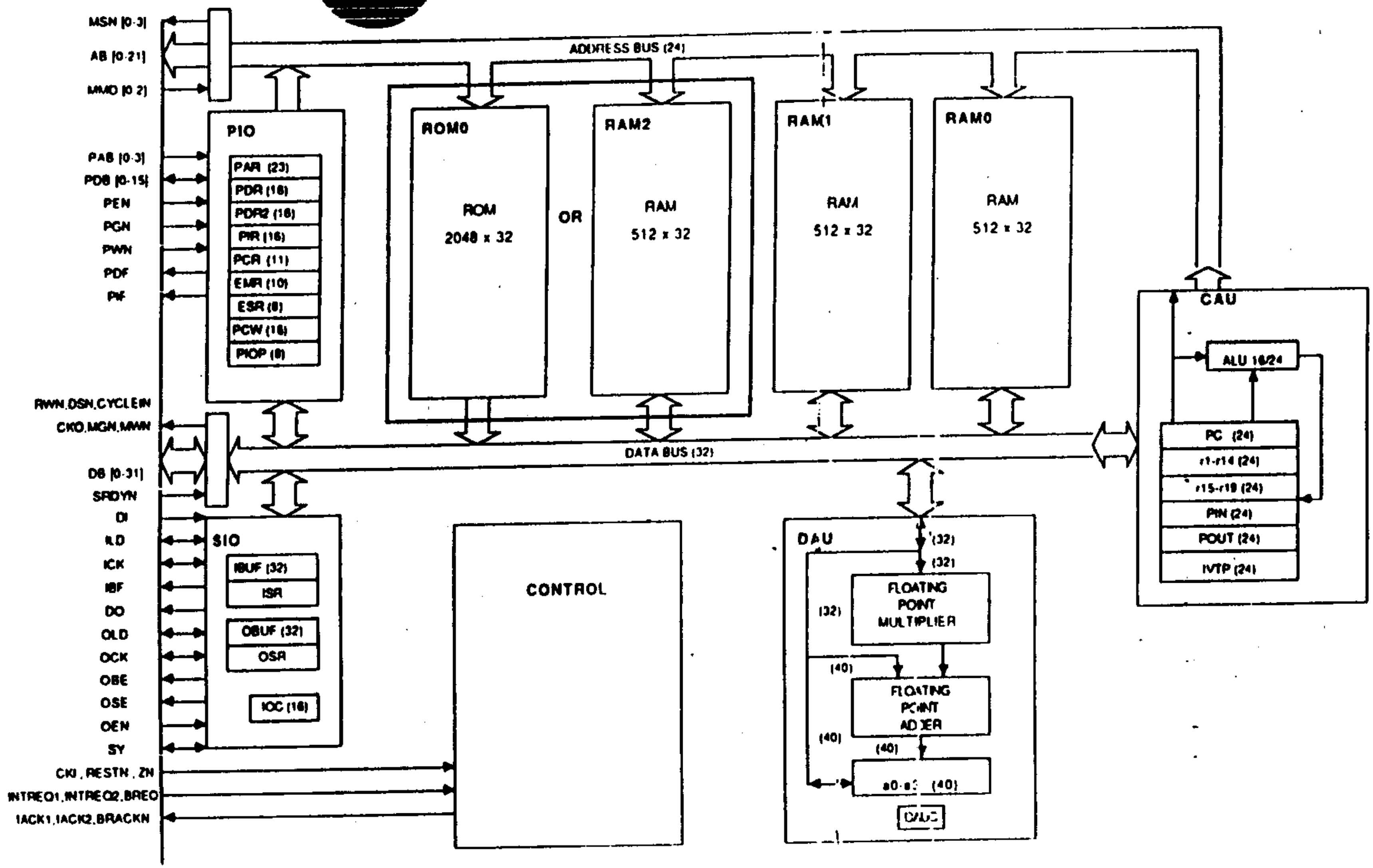
DSP56001 GENERAL BLOCK DIAGRAM



ADD X0,A B,X1 Y0,y: $3F80

ADD X0,A X1,X:(R3)+ Y:(R6)-,B

DSP32C Block Diagram



LEGEND

a0—a3	Accumulators 0 - 3
ALU	Arithmetic Logic Unit
CAU	Control Arithmetic Uni
DAU	Data Arithmetic Unit
DAUC	DAU Control Register
EMR	Error Mask Register
ESR	Error Source Register
FPA	Floating-Point Adder
FPM	Floating Point Multiplie
IBUF	Input Buffer
IOC	Input/Output ControlRegist
ISR	Input Shift Register
IVTP	Interrupt Vector Table Point
OBUF	Output Buffer
OSR	Output Shift Register
PAR	PIO Address Register
PC	Program Counter
PCR	PIO Control Register
PCW	Processor Control Word
PDR	PIO Data Register
PDR2	PIO Data Register 2
PIN	Parallel Input Register
PIO	Parallel I/O Unit
PIOP	Parallel I/O Ports
PIR	PIO Interrupt Register
POUT	Parallel Output Register
r1—r19	Registers 1—19
RAM	Read/Write Memory
ROM	Read-Only Memory
SIO	Serial I/O Unit

Features

- 50 MHz (80 ns) or 40 MHz (100 ns) operation
- All instructions are single cycle
- Twenty-two 24-bit general-purpose
- 32-bit floating-point arithmetic
- Full C compiler
- Data addressable as 8-, 16-, or 32-bit words
- Bit reversal for FFTs
- 133-pin PGA package
- Powerful single-cycle data format conversions:
  - IEEE 754 floating point
  - 24-bit and 16-bit integer
  - 8-bit linear byte
  - 8-bit μ-law and A-law
- Serial and parallel ports with DMA
- Low overhead looping

D.S.P. Performance Comparisoi

Firm	type	Technology	Cycle (nsec)	Architecture	Size-Instrec bit	Program Memory	Data Memory	N. Bus	ALU	Others
JALOG DEVICES,	ADSP 2100	CMOS	125	Hardward	24	16/32K	16 K	1	16-bit Fix	cash memora on chip
T &T	DSP 32	NMOS	250		32	2K	56K Ext 4K Int	2	32-bit Flo 16-bit Int	Serial I/o Parall I/o WE DSP32 SLib. $175
JJITSU	8764	CMOS	100		24	1K	1Kx16 Ext 256x16 Int	1	26-bit Fix	Edt-Ass-Debug CP/M-86 Hand. Emul.
IMOS	IMS A100	CMOS	100		16	Input 2.5 to 10 million samples/sec Processing rate 80-320 million instr./sec				Av. 1 Oct. 86 $ 500
~~ITEL~~	~~2920/21~~		~~400~~		~~24~~	~~192x24~~	~~40x25 bit~~			~~A/D 4 inputs D/A 8 outputs~~
TOROLA	DSP 56000	HCMOS	97.5	3 exec Un. Data ALU Addr. ALU Prog Contr.	24	64K Ext 2K Int.	256 RAM int 256 RAM 128K Ext	4 Data Bus 3 Add Bus	24-bit Fix	24 GP I/o 8 bit port DMA RS232C Codec Sync IBI 200
TIONAL	LM 32900	CMOS	100	Hardward	28	64K	2X (16 bit-64K)	7	32-bit Fix	IBM VAX NATIONAL NS32-VR
EC	μPD 77230	CMOS	150	Hardward	32	2 K	1K RAM 1K ROM	2	55-bit Float	VAX (Unix-VMS) Evakit 77230
ILIPS	DSP	CMOS	125	Hardward	40	64K	2x RAM (128x16) 512x16 RAM	2	16-Fix	
EXAS	TMS320 10 TMS320 20 TMS320C25	NMOS NMOS CMOS	200 (160) 100	Hardward Hardward	16-bit 16-bit	4K 64K 4K Int	144x16 64K 544 Int	1 1	32 bit Fix 32 bit Fix	8-I/o $ 30 ... $ 240

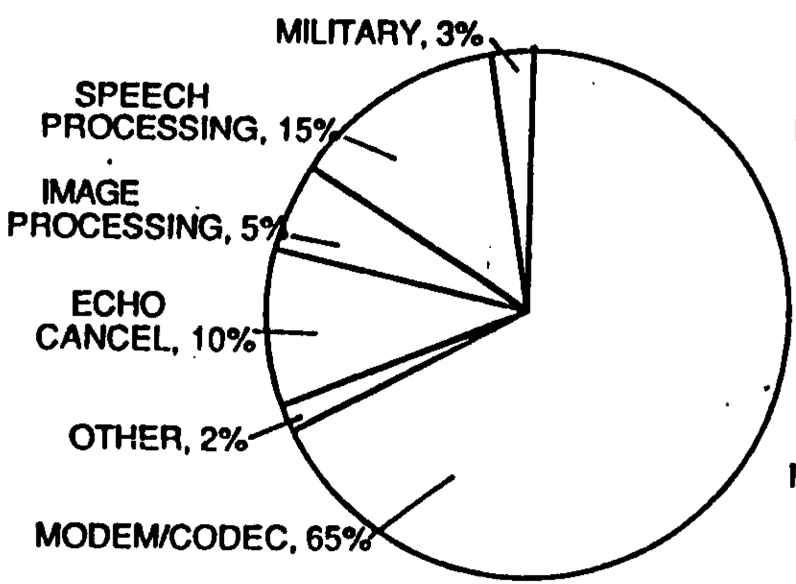
Thomson, ~~Philips~~ IBM

Others from: Advanced Micro Devices, American Microsystem Inc,

Fairchild General Instrument e Gigabit IDT International Microcircuit,

DSP APPLICATION AREAS

(BY UNIT VOLUME)



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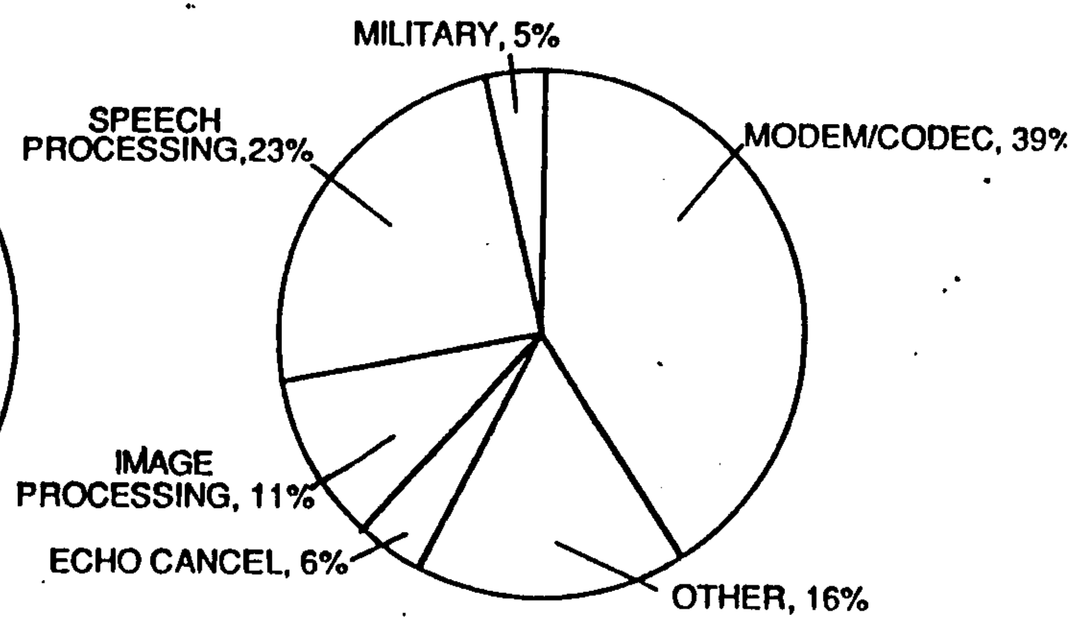
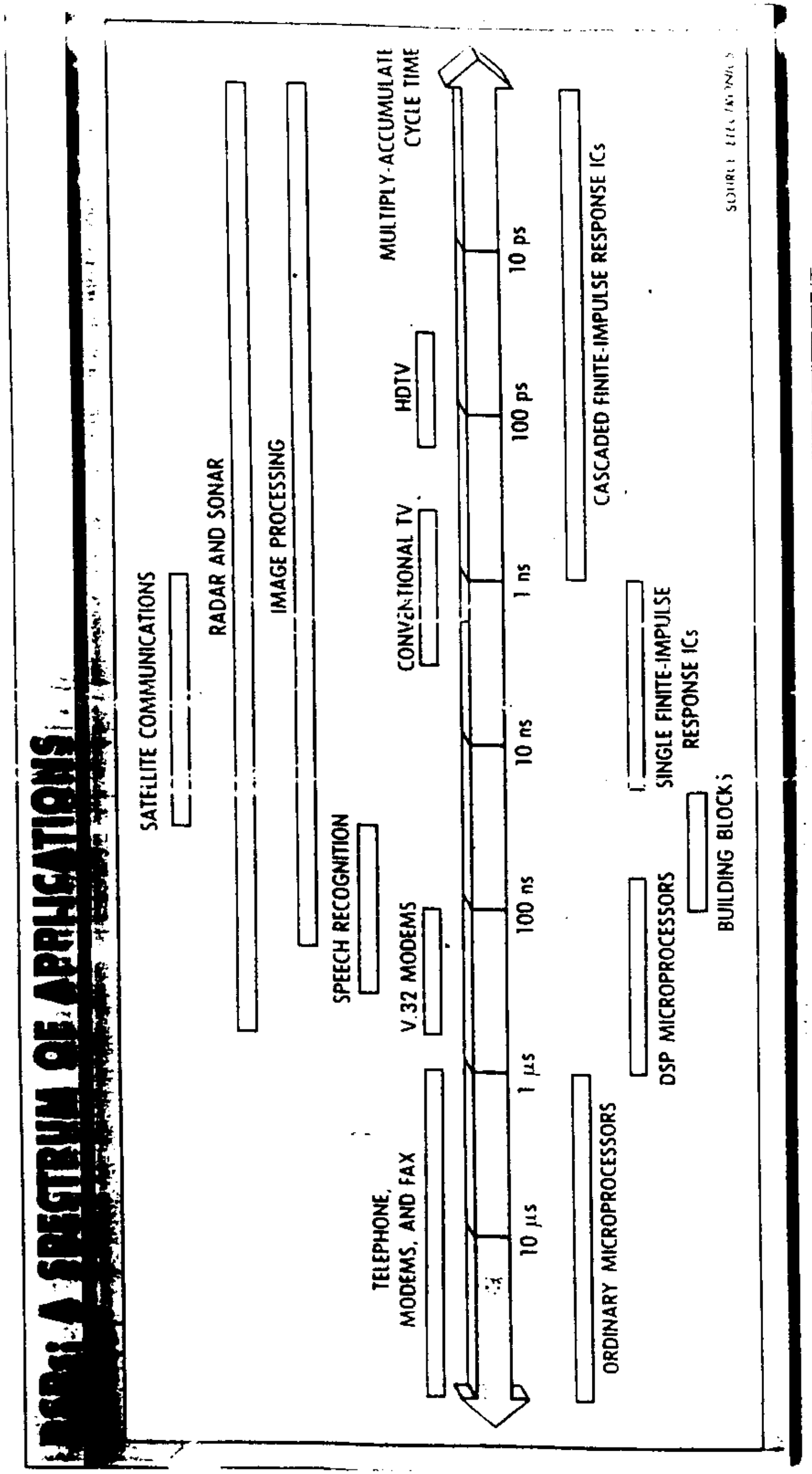


1989

Low-cost and high-speed favors the use of DSP' in these applications.

- telecommunication (high speed modems)
- image processing and pattern recognition
- speech recognition, musical synthesizer
- direction finding in radar,
- target tracking (closed loop systems)
- ultrasound medical imaging
- automobiles: antiskidid braking systems, adaptive suspension, engine control and instrumentation
- disk drives, tape drives
- printers, plotters and consumer products
- digital filters
- digital HIFI, digital AM/FM radio
- workstations (?)
- robotics
- spectrum analysis



DSP
worldwide third party support

FRANCE

- EIA
- OROS
- SYMINEX
- TEXAS INSTRUMENTS
- XCOM

GERMANY

- DSPACE
- ELECTRONIC TOOLS
- DISTEC
- FUCHS MESSETECHNIK
- KONTRON ELECTRONICS

ITALY

- PRACTICA SRL

UNITED KINGDOM

- BEDFORD RESEARCH
- COMPUTER SOLUTIONS LTD
- ENSIGMA
- JOYCE-LOEBL
- LOUGHBOROUGH SOUND IMAGES
- RACAL MICRO-ELECTRONICS SYS
- THORN EMI
- ULTRA DIG. SYST.

USA

- ADVANCED DIGITAL SYS
- AI WARE INC.
- ALLEN ASHLEY
- APPLIED BUSINESS
- ARIEL CORP
- ATHENA GROUP, THE
- ATLANTA SIG. PROCESSORS
- AVOCET SYSTEMS
- BURR BROWN
- CALCOMP
- CASUAL SYSTEM INC.
- Comm. Autom. and Control
- COMPUTALKER
- CYBERNETIC MICRO SYS
- 3D SYSTEMS INC.
- DAISY SYSTEM CORP
- DALANCO SPRY
- DIGITAL AUDIO CORP.
- DIGITAL SIGNAL PROC SOF.
- DIGITAL SOUND CORP
- DSP APPLICATIONS
- DSP TECHNOLOGY CORP
- EIGHTEEN EIGHT LAB.
- ELECTRO RENT CORP
- EMONA ENTERPRISES LTD
- FACS INC
- FORTH INC
- GAS LIGHT SOTWARE
- HEWLETT-PACKARD
- HYPERCEPTION
- JOHN WILEY & SONS
- KAY ELEMETRICS CORP
- MEMOCOM DEVELOP. TOOLS
- METME CORP
- MICRO K SYSTEMS
- MICROCRAFT CORP
- MICROWORKSHOP
- MOMENTUM DATA SYSTEMS
- NAVTROL COMPANY INC
- PC ELECTRONICS
- PH ASSOCIATES
- PRENCTICE-HALL INC
- RAPID SYSTEMS INC
- SARIN
- SENTRY
- SENTRY TEST SYSTEMS
- SIGNAL TECHNOLOGY INC
- SIGNIX CORP
- SIGNUM SYSTEMS
- SKY COMPUTERS
- SONITECH
- SPECTRON
- SPECTRUM SIGNAL PROC
- SPECTRAL INNOVATION
- SYMMETRIC RESEARCH
- TEKTRONICX INC
- TELEPHOTO COMMUNICATION
- TELERIC
- TELEVIC
- TIAC
- WADIA
- VALID LOGIC SYSTEMS
- VOTAN
- WHITMAN ENGINEERING

- SPECTRUM offers DSP~LINK letting you match analog or digital interface boards with DSP chip of your choice from Texas, Motorola and Analog Devices.

THE SPS GROUP HAS PURCHASED TWO SOFTWARE PACKAGES TO DESIGN DIGITAL FILTERS:

- Hyperception HYPERSIGNAL

- Atlanta Signal Processors, Inc.

Sometimes though these software packages are not suitable for solving high performance Real-Time applications. In that case it is necessary to use a particular type of DSPs more specific solving filtering problems, or in other cases, communication.

- **The leading firms in designing and manufacturing DSP's are:**

  Texas Instruments,
  NEC,
  Motorola,
  Philips,
  Zoran,
  Analog Devices,
  AT & T,
  Honeywell Inc.,
  Thomson,
  Inmos,
  Fujitsu.
  Intel
  National Semiconductor

- **The software development support is given by the firms themselves and also by:**

- TEKTRONIX that offers the Signal Processor Workstation (SPW) that runs on VAX or Apollo Computer Domain.

- DATACUBE offers Euclid Tools and DSP-1000

- DSP Development introduced DADiSP which is a menu driven software for displaying and analyzing digital waveforms.

- STEP Engineering offers Step-4 SDT running on IBM PC AT

THE SPS GROUP HAS PURCHASED:

MOTOROLA DSP96000

- SIMULATOR PROGRAM
-MACRO CROSS ASSEMBLER
- LINKER/LIBRARIAN

```
MOTOROLA DSP96002 SIMULATOR:  VERSION 1.0 3-27-89
load TEST
loading file:TEST.lod
disassemble
p:$00000000 01b003f4 00000005 = do #<$1f4,$6
p:$00000002 e9480b2a          = fmpy d6,d8,d2 fadd.s d3,d0 x:(r0),d4.s d2.s,y:(
r5)+
p:$00000003 eae66c2f          = fmpy d7,d8,d3 faddsub.s d4.d0 x:(r1)+,d6.s d5.s
,y:(r4)+
p:$00000004 00000000          = nop
p:$00000005 00000000          = nop
p:$00000006 00000000          = nop
0>

asm    break    change    copy    disassemble    display    <space>=more
```

```
  m7=  $ffffffff   n6=  $00000000   r6=  $00000000
  m5=  $ffffffff   n5=  $00000000   r5=  $00000006
  m4=  $ffffffff   n4=  $00000000   r4=  $00000000
  m3=  $ffffffff   n3=  $00000000   r3=  $00000000
  m2=  $ffffffff   n2=  $00000000   r2=  $00000000
  m1=  $ffffffff   n1=  $00000000   r1=  $00000000
  m0=  $ffffffff   n0=  $00000000   r0=  $00000000
d9.h=  $00000000 d9.m=  $00000000 d9.l=  $00000000 d9=0.000000000000000e+00
d8.h=  $40000380 d8.m=  $00000800 d8.l=  $00000000 d8=1.121038771459854e-44
d7.h=  $40000380 d7.m=  $00000700 d7.l=  $00000000 d7=9.809089250273719e-45
d6.h=  $40000380 d6.m=  $00000600 d6.l=  $00000000 d6=8.407790785948902e-45
d5.h=  $40000380 d5.m=  $00000500 d5.l=  $00000000 d5=7.006492321624085e-45
d4.h=  $40000380 d4.m=  $00000500 d4.l=  $00000000 d4=7.006492321624085e-45
d3.h=  $40000380 d3.m=  $00000400 d3.l=  $00000000 d3=5.605193857299268e-45
d2.h=  $40000380 d2.m=  $00000200 d2.l=  $00000000 d2=2.802596928649634e-45
d1.h=  $40000380 d1.m=  $00000200 d1.l=  $00000000 d1=2.802596928649634e-45
d0.h=  $40000380 d0.m=  $00000200 d0.l=  $00000000 d0=2.802596928649634e-45
  pc=  $00000000   sr=  $70000000   la=  $00000000   lc=  $00000000
 ssh=  $00000000  ssl=  $00000000   sp=  $00000000  omr=  $00000001
 cyc= 00000000000 ictr= 00000000000 cnt1= 00000000000 cnt2= 00000000000
p:$00000000 01b003f4 00000005 = do #<$1f4,$6
0>

asm    break    change    copy    disassemble    display    <space>=more
```

- Some of the characteristics that make the DSP particularly suitable to treat discrete signals are found in its instruction set.

  - Several presently available DSP's can: perform a simple operation $y = ax + b$ in one cycle (75 nsec) while at the same time performing some operations on addresses by updating pointers.

  - can have hardware "DO LOOP" instructions.

  - can have compare magnitude instructions

- Assembler language may be convenient to optimize a fast algorithm, but is a limitation for large programs. The principle firms: AT & T, Motorola, Philips and Texas Instruments are already providing "C" compilers for their DSP's.

- In recent years instead we see that the characteristics of the DSP's are improving very rapidly. No one features of the past was dropped (hardware multiplier, special instructions, etc.) but in addition we see that address capability has increased very much and some powerful one cycle instructions has been added (floating point).

- The DSP96002 from Motorola is capable of addressing 12 Gigabyte of memory: 4 gigabyte for Program memory, and 4 gigabyte each for the two Data memories banks.

- This DSP has also a high degree of parallelism and pipelining. One can write in a single line of assembly code the following operations that will be executed in one cycle

```
FMPY D9,D7,D1 FADDSUB.S D5,D2 D4.S,X:(R5) Y:(R1),D7.S
```

- The typical specifications that was distinguished a DSP with respect to other microprocessors, has changed since 1982. As a consequence, also the field of applications is increasing.

- At the beginning most DSP's had in common the characteristics of:

- Harward architecture (separation between Program and Data memories)
- very small Program and Data memory area
- small instruction set and most of them executed in one cycle (for this reasons similar to RISC)
- special instructions for treatment digitalized analog signals (such as: parallel multiply, barrel shifting, auxiliary registers for single cycle manipulation of data tables, etc.)

- From these characteristics, the user could see the best application of DSP in the area where a short but very efficient algorithm should be used in order to replace a function that was previously done with analog components; such as filters, fast Fourier transforms.

- Assembly language was sufficient because the code needed be optimized and not be longer than a few pages.

- With the advent of Fast A/D converters and new processors oriented towards signal processing (DSP), arose the tendency to treat analog signals in digital form, thus using discrete algorithms instead of analog functions. The advantage of the digital circuitry over the analog components is: high density, precision, programmability, stability and testability.

- Digital Signal Processor are special purpose microprocessors optimized for the processing of digitalized analog signals, which are discrete in both amplitude and time

- In 1982 there appear on the market a new externally programmable DSP family of processors, the TMS320XX of Texas Instruments.

  - 1st DSP 1978 AMI S2811
  - 1979 INTEL 2920/21 (Telecommunication)
  - 1980 NEC 7720
  - 1982 Texas 32010 First with the option of having the program memory on RAM. Ideal for low volume applications.

- High Energy Physics experiments now use huge detectors to track elementary particles and it is extremely important to be able to make decisions, based on the information of thousands of signals in real time as fast as possible.

- In 1985, the Torino group: D. Crosetto, E. Menichetti, G. Rinaudo and A. Werbrouck decided to use such a component as the basic element in an intelligent programmable trigger decision parallel processing system in the FEMC Delphi detector for satisfying the requirements of II level trigger decision within 44 usec and for having more refined informations on clusters in the detector within 200 usec for the III level trigger.

- A prototype of the parallel system made of six DSP working in parallel has been designed and build in VMEbus boards in 1986.

- The first test on beam H6 at CERN was made in the summer 1987. The performance was as expected and now the same system is foreseen to be used in other applications.

References: "FDDP" CERN-EP/87-151 25 August 1987
or 2nd Edition North-Holland, poster session
VMEbus in Research 11,12,13 Oct. 1988

- Looking towards a more general application of DSP in High Energy Physics Experiments, the use could be extended not only for triggering but also to treat analog signals in a data acquisition system to perform zero suppression.

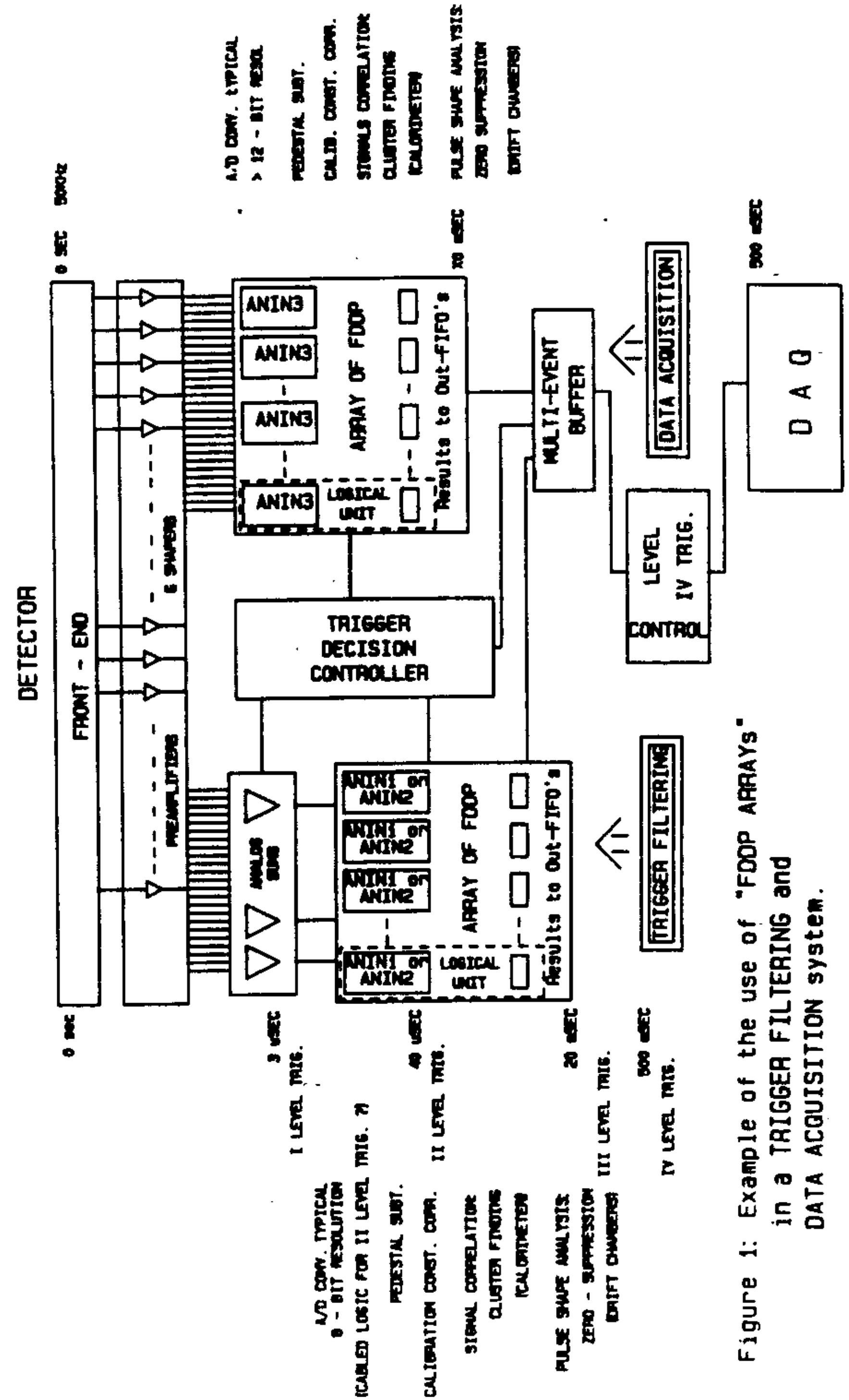
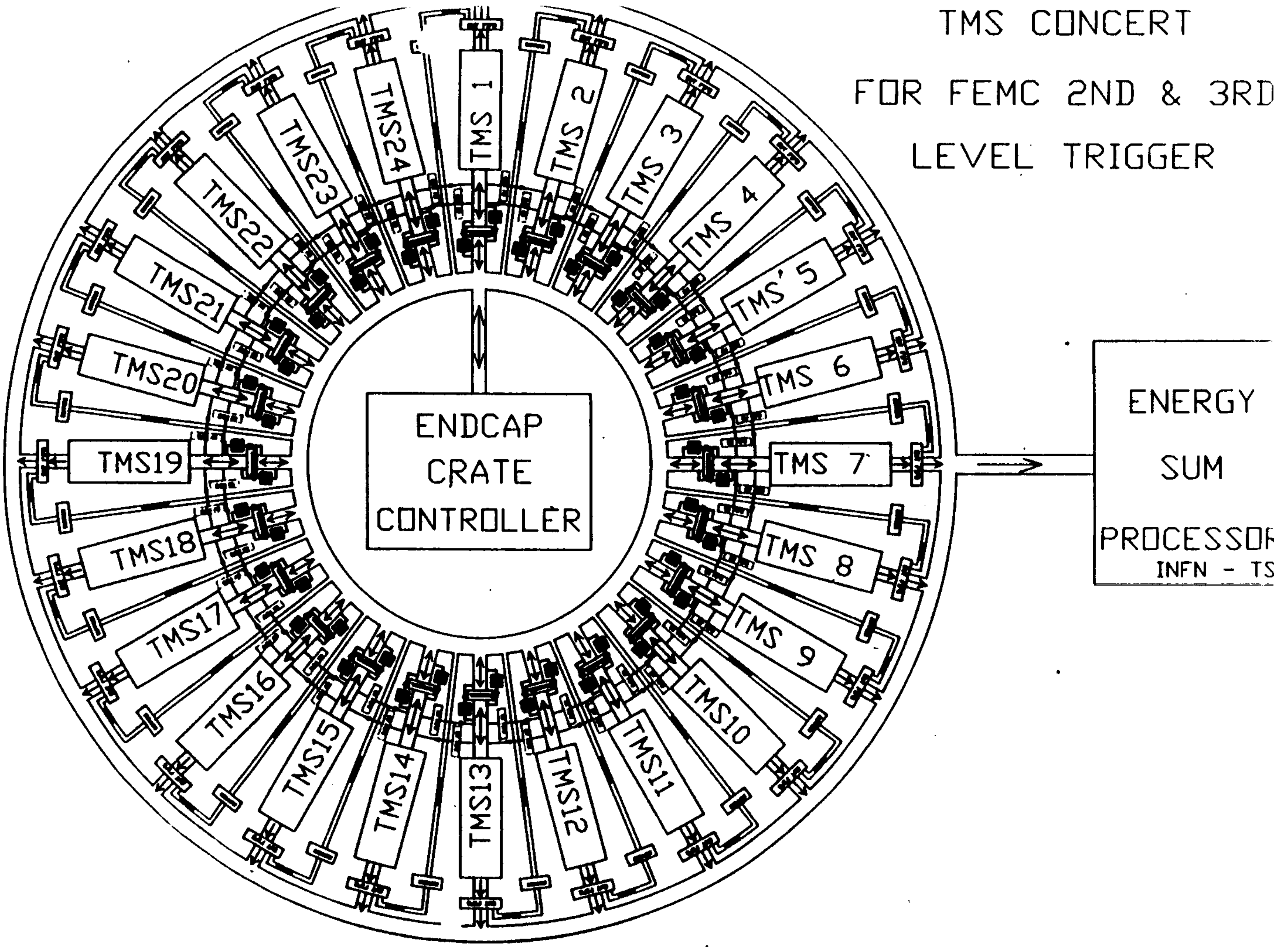


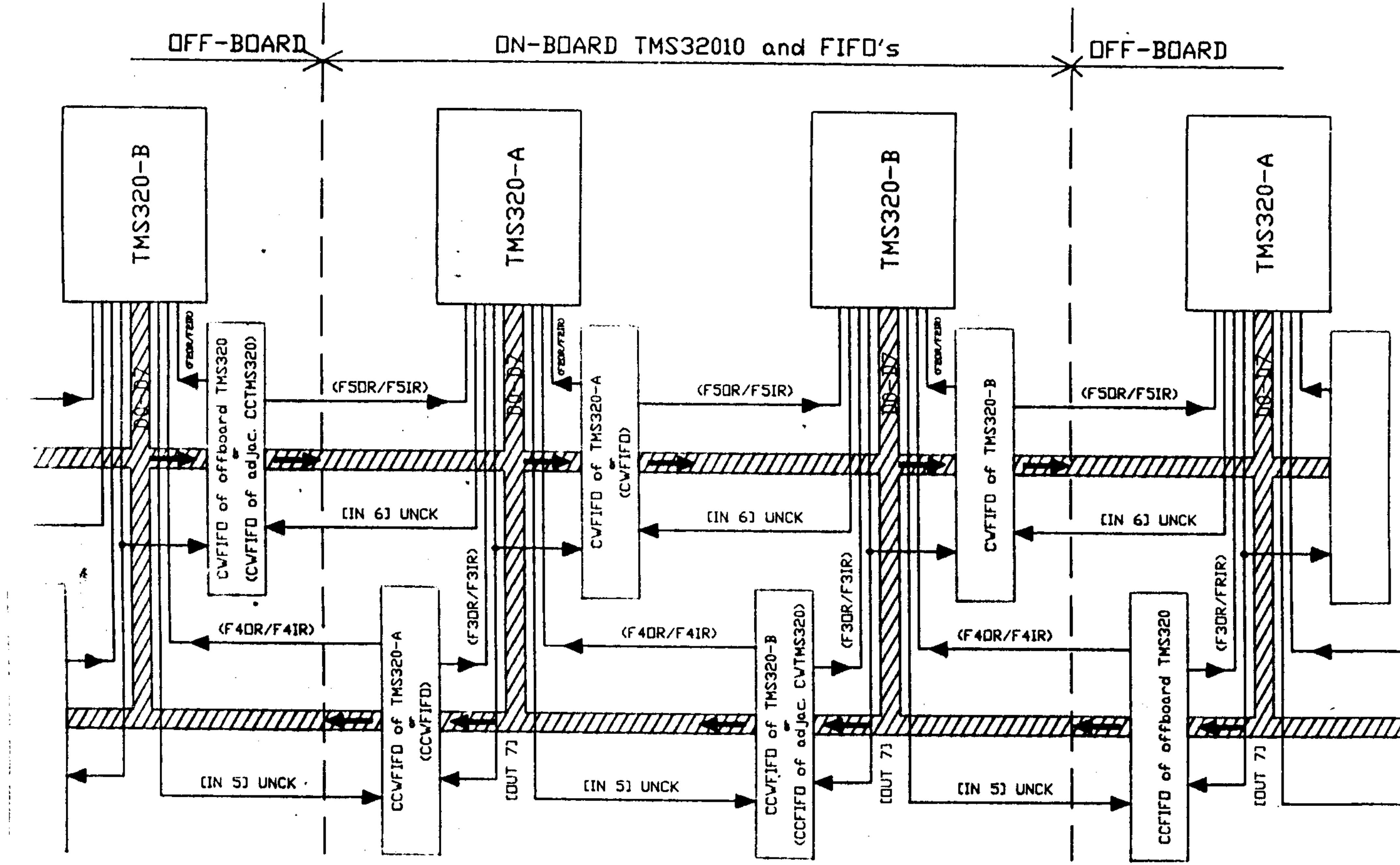
Figure 1: Example of the use of "FDOP ARRAYS" in a TRIGGER FILTERING and DATA ACQUISITION system.

TMS CONCERT

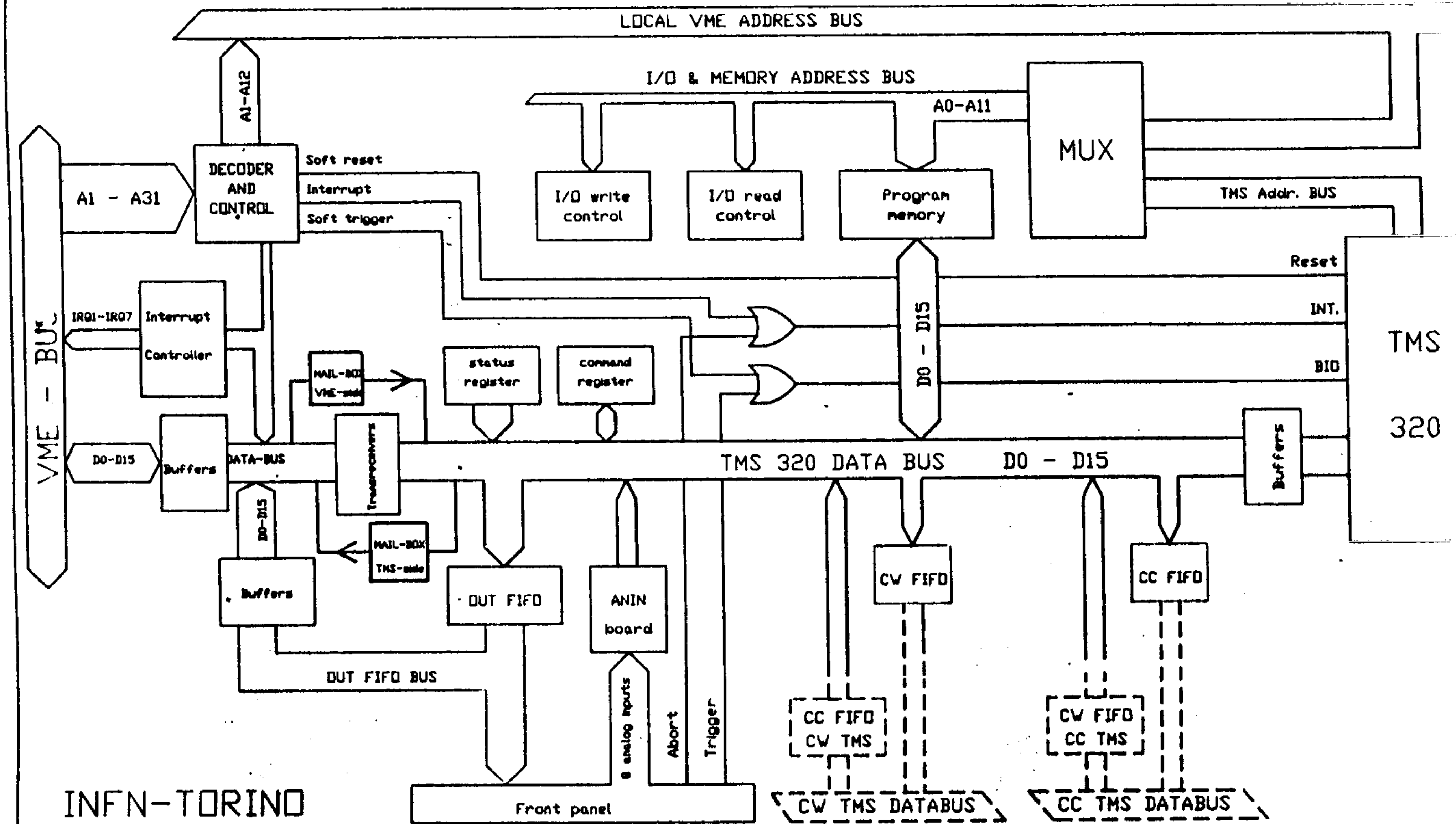
FOR FEMC 2ND & 3RD

LEVEL TRIGGER





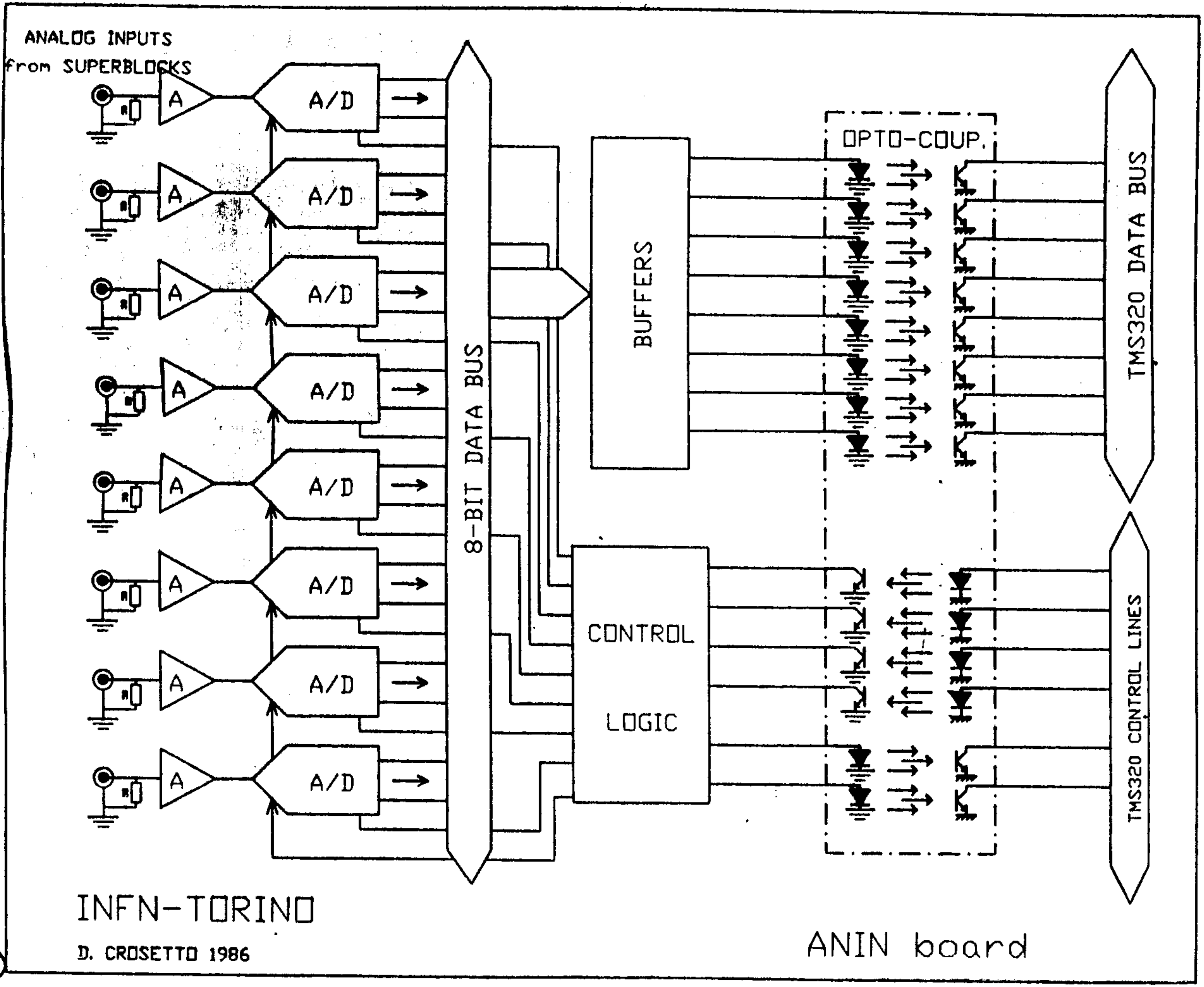
OFF-BOARD
ON-BOARD TMS32010 and FIFO's
OFF-BOARD
TMS320-B
TMS320-A
TMS320-B
TMS320-A
D0-D7
CWFIFO of offboard TMS320
or
(CWFIFO of adjac. CCTMS320)
CWFIFO of TMS320-A
or
(CWFIFO)
CWFIFO of TMS320-B
(F5OR/F5IR)
[IN 6] UNCK
(F4OR/F4IR)
(F3OR/F3IR)
(F3OR/FRIR)
CCWFIFO of TMS320-A
or
(CCWFIFO)
CCWFIFO of TMS320-B
or
(CCFIFO of adjac. CWTMS320)
CCFIFO of offboard TMS320
[IN 5] UNCK
[OUT 7]

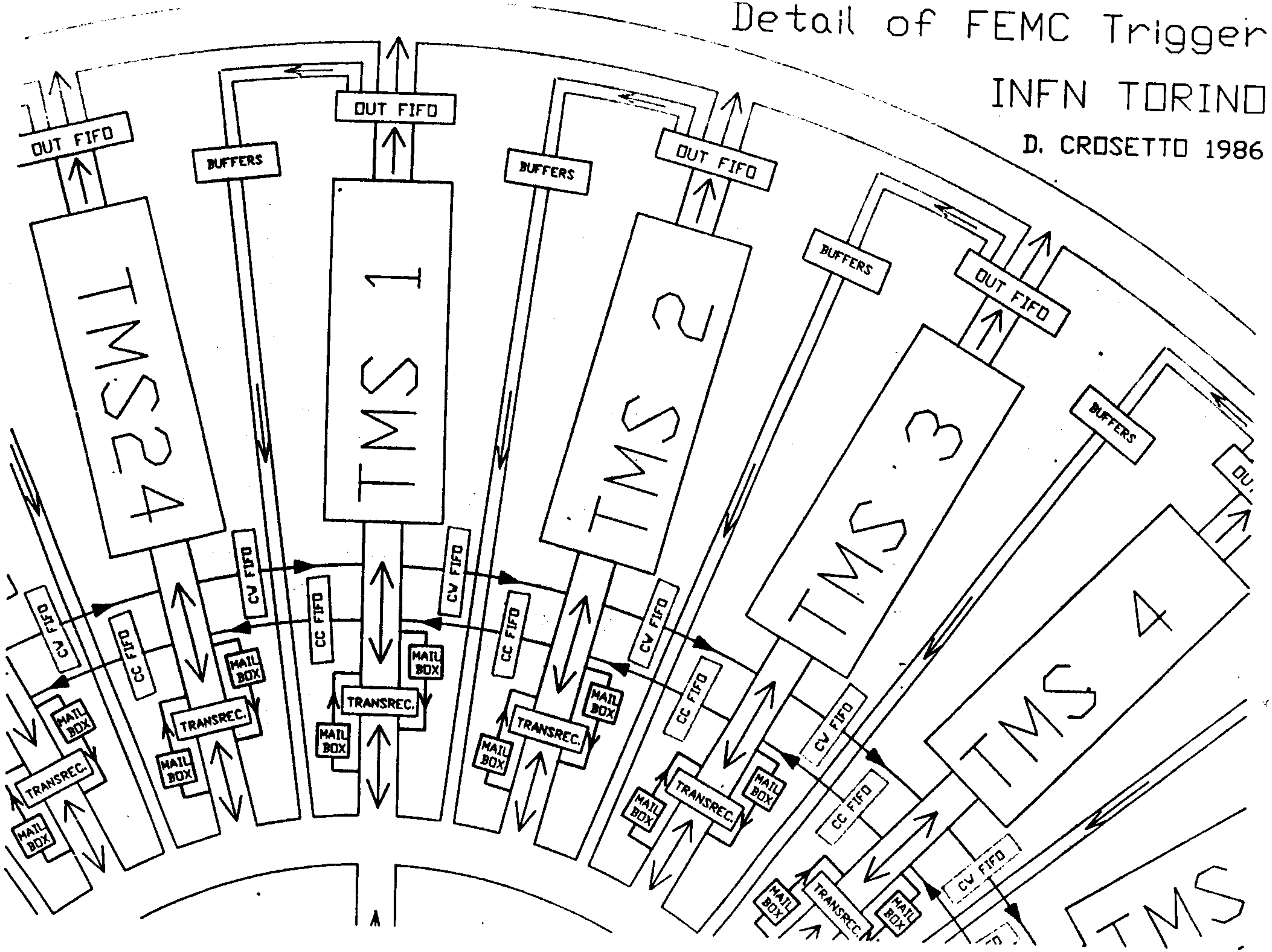


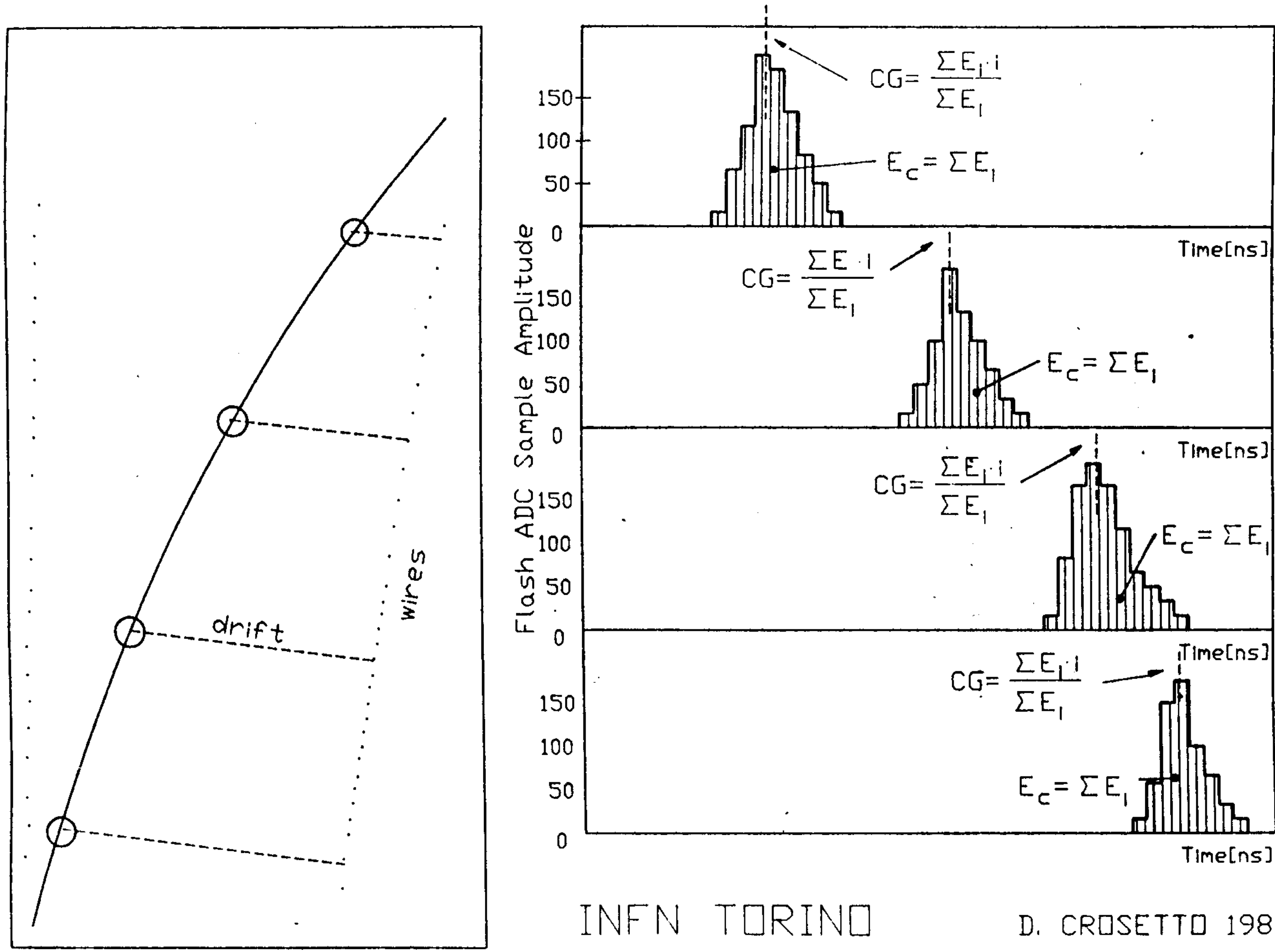
INFN-TORINO

D. CROSETTO 1986

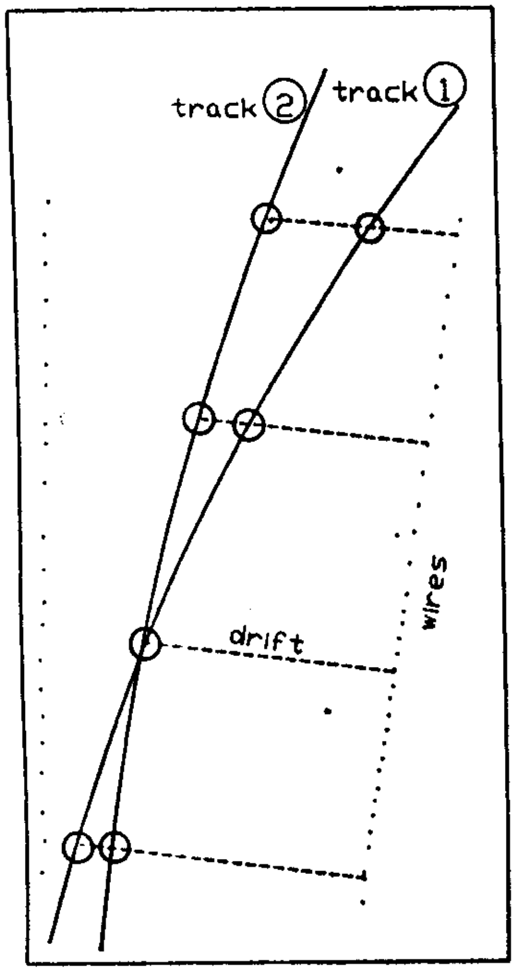
LOGICAL UNIT

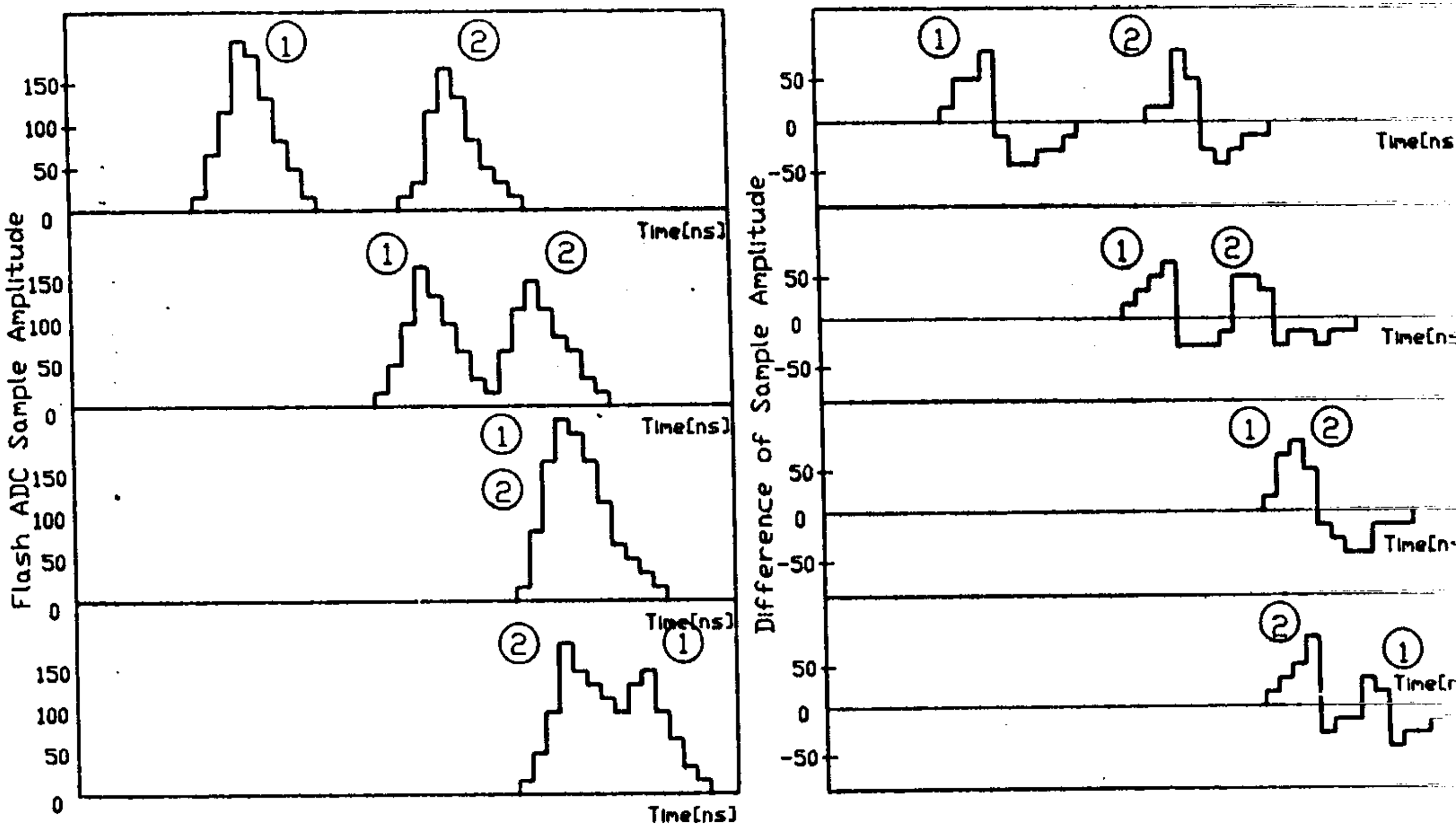

ANALOG INPUTS
from SUPERBLOCKS
A
A/D
8-BIT DATA BUS
BUFFERS
CONTROL
LOGIC
OPTO-COUP.
TMS320 DATA BUS
TMS320 CONTROL LINES
INFN-TORINO
D. CROSETTO 1986
ANIN board


Detail of FEMC Trigger
INFN TORINO
D. CROSETTO 1986
TMS24
TMS 1
TMS 2
TMS 3
TMS 4
TMS
OUT FIFO
BUFFERS
CV FIFO
CC FIFO
MAIL BOX
TRANSREC.



INFN TORINO D. CROSETTO 1987





INFN TORINO

D. CROSETTO 1987

DSP IN ACCELERATOR CONTROL

Diagnostic and corrections on operating parameters of an Accelerator require the analysis and processing of analog signals.

Sophisticated signal processing functions can be implemented using digital techniques

Digital systems are inherently more reliable, more compact, programmable and less sensitive to enviromental conditions and component ageing than analog systems.

Depending on whether the parameter to control has or does not have a correlation with other signals, then we may see requirements to inplement a Real-Time Control Function for:

- **a stand alone signal filtering or frequency analysis, or**

- **a linked DSP system that monitors and corrects parameters that have some degree of interdependence.**

Present hardware and software standardization in the Accelerator Control.

- OS-9 VME
- SCO XENIX for IBM PC AT

HOW DOES THE DSP FIT IN WITH THE ACCELERATOR CONTROL SYSTEM ?

STAND ALONE SYSTEM

NETWORK SYS.

Transp.-DSP

RISC-DSP

Is there an aperture to the following hard-ware and software systems in the future ?

- VME - VXI
- UNIX
- ORKID (Open Real-Time Kernel Interface Definition)
- (Occam, Heliös ??)

slots is 1.2 inches (as opposed to 0.8 inches for normal VMEbus) to provide enough room for the modules to be completely enclosed with a metal case for shielding. LEDs, switches, and test points are provided on front panels to aid system diagnosis and operator interaction. Input/output connections are made via front panel connectors.

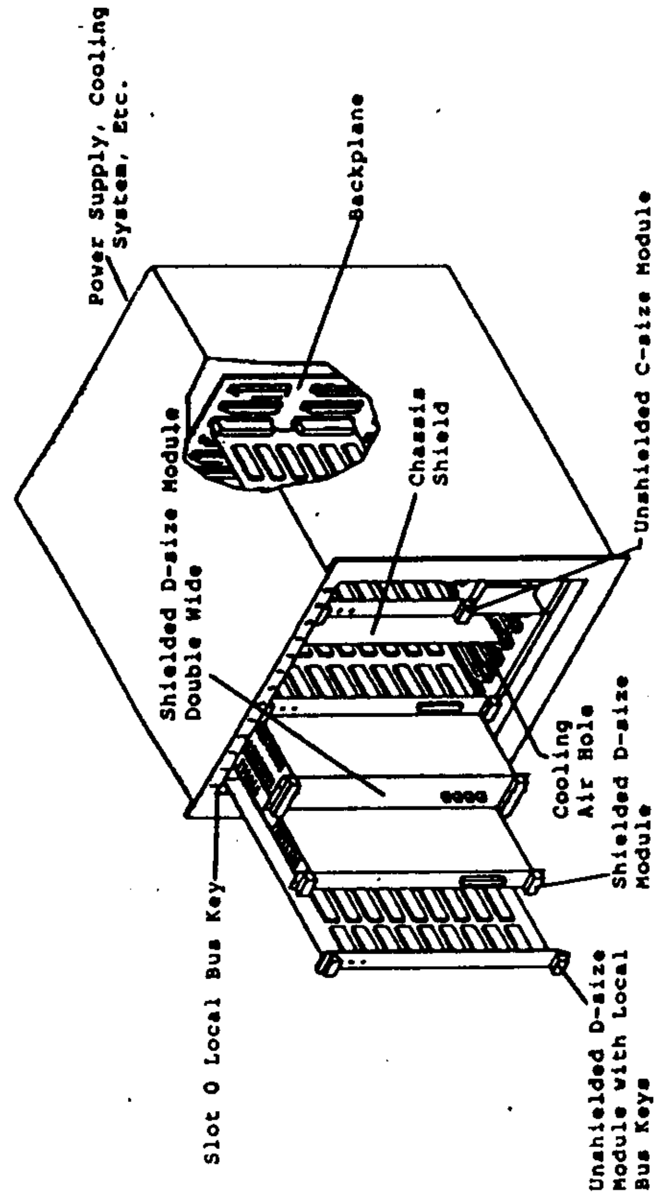


FIGURE 1
A VXIbus system consists of a backplane chassis into which plug-in modules are installed.

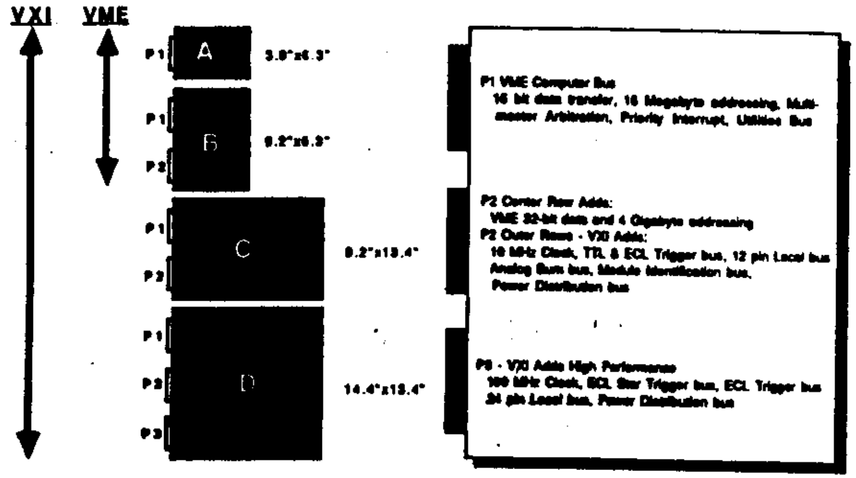


FIGURE 2
The VXIbus Specification uses the VMEbus specification as a base and adds two board sizes and backplane instrumentation signals.

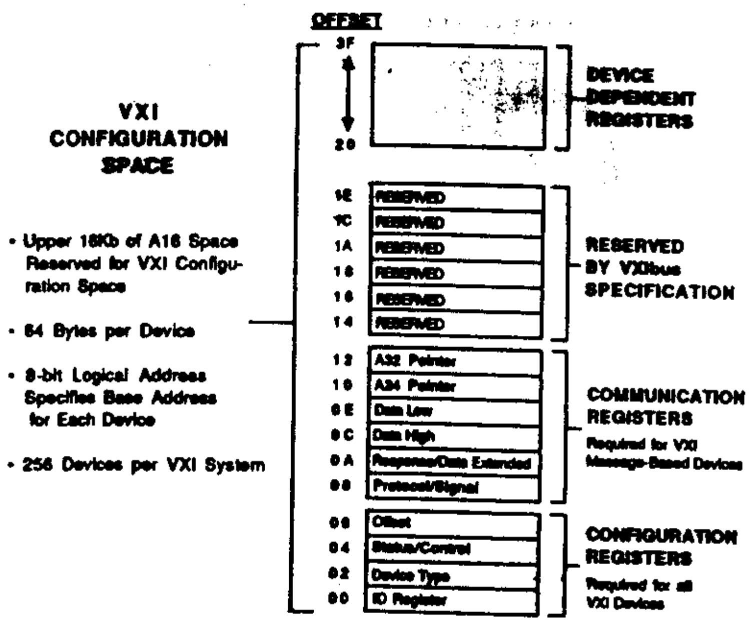


FIGURE 3
VXIbus modules must have a minimum set of registers located at specific addresses A module with only configuration registers is called a Register Based Device while a module that also has communication registers is called a Message Based Device.

ORKID History

- why, who, how?

- why?
  - growing impact of software on market
  - many similar, incompatible products
  - incredible waste of effort
  - availability, quality, support suffer

- who?
  - triggered by VMEbus manufacturers
  - who are suffering heavily
  - experienced the success of a standard
  - had an organisation to handle it
  - VITA

- how?
  - VITA TC created the SWSC (Feb. '88)
  - SWSC created ORKID WG (April '88)
  - members: CERN, Force, Motorola, Philips, SCG, Wind River (chair H. Maaskant)
  - corr. members: Eyring, Microware, Radstone
  - Z. Hunor (VITA Europe) as secretary

ORKID Guidelines

- The "O" in ORKID stands for:
  - non-proprietary
  - processor and bus independent
  - open to future developments
  - private extensions allowed

- defines a kernel interface, not a real-time system

- ORKID is state-of-the-art
  - but based on proven, implemented, concepts
  - supports portable AND robust programming
  - no "bells and whistles"
  - simple adaptation of existing kernels

- defined interface, different implementations
  - still wide range of products and aims
  - no end to competition

- no interoperability between different implementations

Some ORKID Details

- single and multiple node systems
  - local and global visibility
  - shared memory and network coupling

- MMU support will be defined later
  - is seen as very important
  - too little experience available now

- ORKID objects:
  - are named by the user
  - and accessed via kernel assigned IDs
  - IDs are unique over the system

- ORKID operations handle:
  - tasks
  - memory regions with variable size segments
  - memory partitions with fixed size blocks
  - counting semaphores
  - queues for fixed (but definable) length messages
  - synchronous event flags attached to tasks
  - asynchronous exception flags attached to tasks
  - timers and calendar
  - interrupts

The State of ORKID

- consensus reached, framework available
- full time professional hired by VITA
    - to finish writing by end May
- next ORKID meeting in June
- draft should be public after that
- WORKERS are still welcome
    - representing VITA corporate members
    - supporting the ORKID goals
    - ready to invest sufficient time

How to Get a Copy of the Draft

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- or contact VITA
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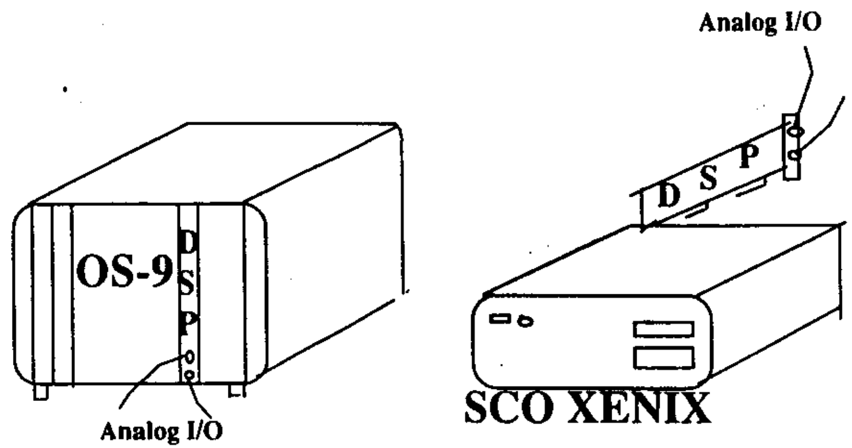
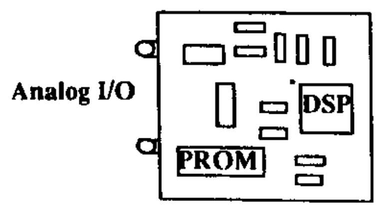
DSP

STAND-ALONE SOLUTIONS

IN THE ACCELERATOR CONTROL SYSTEM





Does a board always exist (VME or IBM PC AT) on the market having has basic element the DSP that we have selected and that satisfy our requirements ?

How do we initialize the board ? How do we program the DSP with the algoritm performing the necessary filtering function ?

Are there any functions already implemented callable by:

- Unix drivers or OS-9 drivers for the VME boards
- MS-DOS drivers or SCO Xenix drivers for the IBM PC AT boards ?

Or, is there a stand alone DSP board with the software algoritm burned in a PROM ?

SIMULATE

THE DIGITAL FILTER ALGORITHM

BEFORE TO BUY ANY

BOARD OR
HARDWARE SYSTEM

What then could be the reality for the future in the short term ?

STAND ALONE SYSTEM

(for a short-term solution)

for very high performance Real-Time applications

- **Based on VME**
- **DSP: INMOS A-100 or**
  Motorola DSP56000+DSP56200
- **Interfaced to VAX, uVAX (DRQ11)**
  or to IBM-PC
  or UNIX drivers for the Loughborough VME56k board.

MCF-256 FUNCTIONAL SPECIFICATIONS

The following highlights the functional specifications of the MCF-256 system

NO. OF INPUTS (NC)	1-512
NO. OF TAPS/CHANNEL (NT)	4-4096
NO. OF DECIMATION (ND)	1-1024
CHANNEL SAMPLING RATE (fs)	see table 2
INPUT DATA WORD LENGTH	16-Bit
COEF. DATA WORD LENGTH	16-Bit
OUTPUT DATA WORD LENGTH	16-bit Mantissa and 4-bit Exponent
HOST PROGRAMMABLE PARAMETERS	NC,NT,ND, Filter Taps Output Exponents, Coef. Memory Bank
HOST COMMUNICATION DATA RATE	125 K words/sec.
DYNAMIC RANGE	>90dB

Note that because of the internal memory size limitation, the following restrictions apply;

$NCxNT \leq 65536$

$NCxND \leq 16384$

Table 2
MCF-256 Channel Sampling Rate
(No Decimation: ND=1)

No. of INPUTS (NC)	No. of TAPS/CHAN (NT)	MAX. SAMPLE RATE (MAX. fs)
1-16	4-4096	12.5/(NT)MHZ
17-32	4-2048	12.5/(2xNT)MHz
33-64	4-1024	12.5/(4xNT)MHz
65-128	4-512	12.5/(8xNT)MHz
129-256	4-256	12.5/(16xNT)MHz

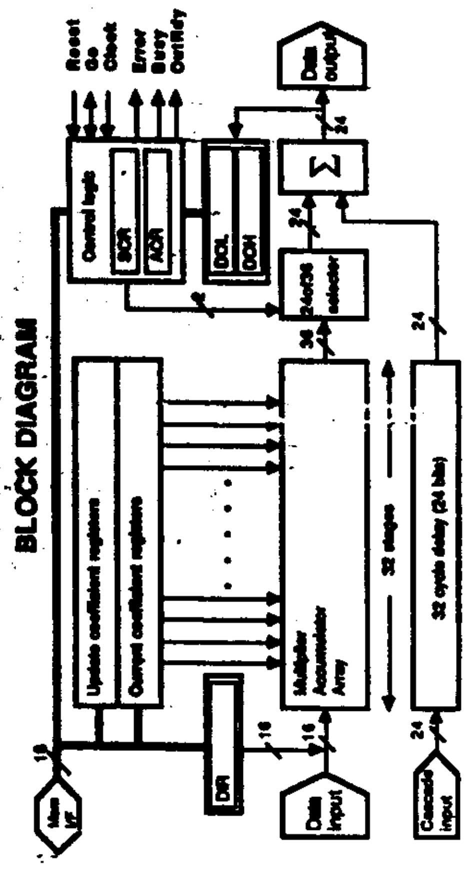
Note: For ND > 1, the input sample rate is ND x fs. For example, with decimatio 256 channels and 256 taps per channel the maximum sample rate is 6KHz.

DESCRIPTION

The IMS A100 is a high speed, high accuracy 32 stage digital transversal filter. It's flexible architecture allows it to be used as a "building block" in a wide range of Digital Signal Processing (DSP) applications. The part is capable of performing high speed DFTs, convolution, and correlation, as well as many filtering functions.

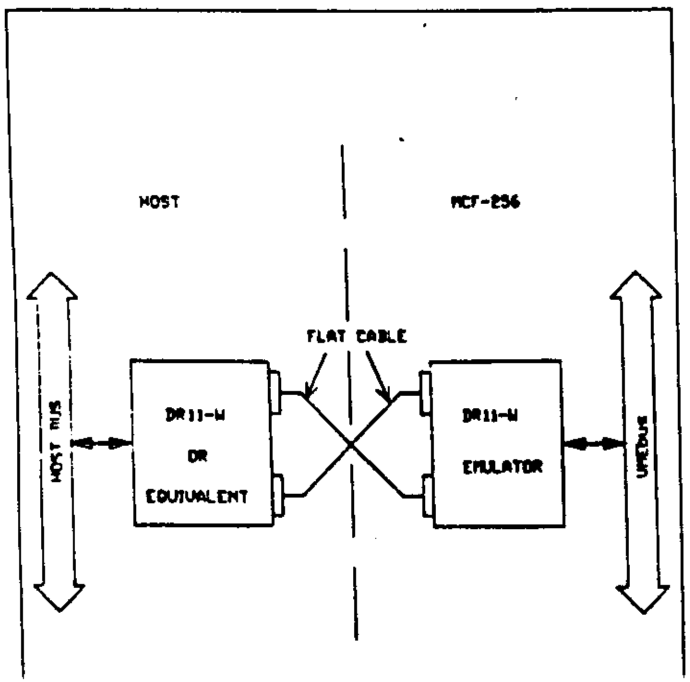
The input data word length is 16 bits, and coefficients are programmable to be 4, 8, 12, or 16 bits wide; two's complement numerical formats are used for both data and coefficients. The coefficients can be updated asynchronously to the system clock during normal operation, allowing the chip to be used in a variety of adaptive systems. The IMS A100 can also be cascaded to construct longer transversal filters with no additional logic or degradation in speed, whilst preserving a high degree of accuracy. The device is controlled through a standard memory interface, allowing use with any general purpose microprocessor. Data communications can be either through the memory interface, or through dedicated data ports.

BLOCK DIAGRAM



The MCF-256 system includes a VMEbus DR-11 emulator board for interfacing to a host computer (MICROVAX, VAX, or PC AT). The host sends commands and data to the MCF-256, and also receives data from the MCF-256 via a 16-bit parallel link. The link is terminated at both ends by a DR-11 or equivalent card as shown in Fig. 8. All communication is initiated by the host computer. The MCF-256 system only responds to the host requests. All transfers over the link are DMA transfers for high speed communication. Each transfer is initiated and terminated by interrupting the receiving device. All communications are controlled by a link driver software: A library of user callable Fortran subroutines have been developed for the VAX and PC AT host computer in order to communicate with the MCF-256 system.

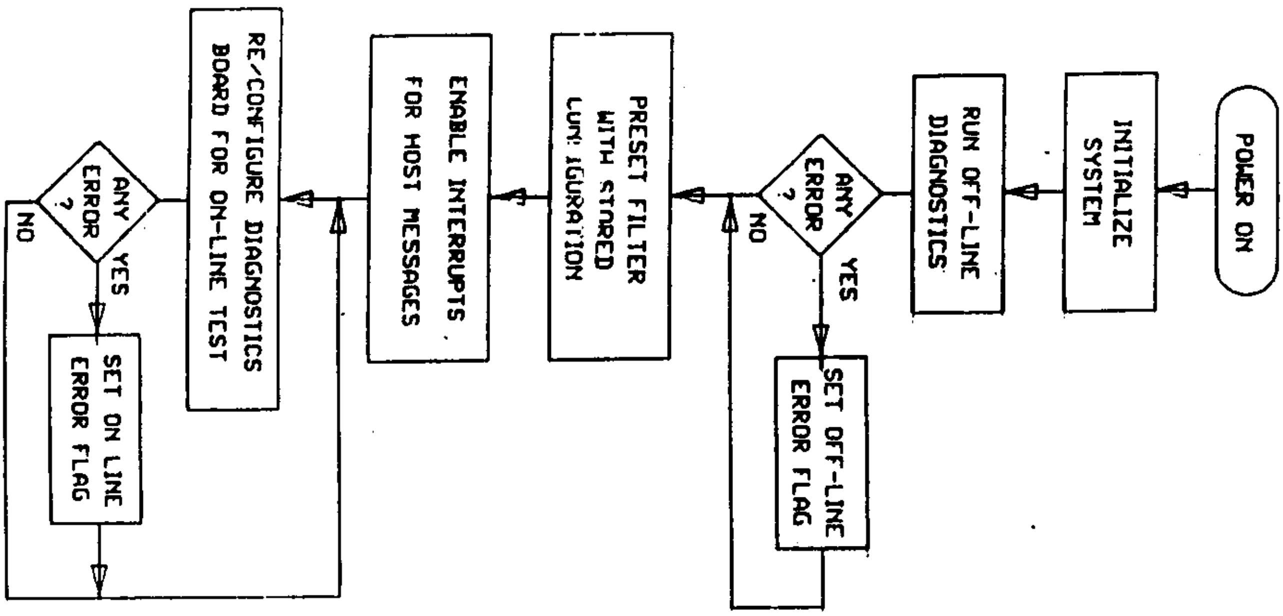
All parameters downloaded from the host are stored in the battery backed memory board. These parameters are then entered in the filter and the I/O boards. The CPU board holds the entire system software in PROMs. Fig. 9 shows a simple flow chart of the system firmware which shows the sequence of important operations following a power up.



HOST COMMANDS

The host software developed for the MCF-256 system allows the host to download an upload all system parameters, run off-line diagnostics and read system status by usin set of simple commands. A list of important commands are given below:

#	COMMAND	ACTION
1	MCF_SET_CONFIG	configure the MCF-256 system in terms of No. of Inputs, No. of Taps, No. of Decimation a Sampling Frequency
2	MCF_SET_TAPS	download filter taps
3	MCF_SET_BANK	select the active coefficient bank
4	MCF_SET_EXPONENT	set the filter output exponents
5	MCF_SET_ANALOG	set analog outputs and the cut-off frequency o the reconstruction filters
6	MCF_SET_DIAGNOSTICS	run off-line diagnostics
7	MCF_GET_CONFIG	return current configuration
8	MCF_GET_TAPS	upload filter taps
9	MCF_GET_BANK	return active coefficient bank number
10	MCF_GET_EXPONENT	upload filter output exponent values
11	MCF_GET_ANALOG	upload analog channel numbers and the cut-of frequency of the reconstruction filters
12	MCF_GET_STATUS	return the system status register
13	MCF_GET_OFF_ERR	return off-line diagnostics error codes
14	MCF_GET_ON_ERR	return on-line diagnostics error codes



Features

Real-Time Applications

SPECIFICATIONS (Typical at 25° C)

INPUT SECTION:

No. of Analog Inputs	4 (Simultaneous Sampling)
Input Resolution	12-bit (2's Complement)
Max. Sampling Rate	500 KHz, Single Channel 125 KHz, Four Channel
Input Impedance	>5MΩ
Input Range	± 5V Full Scale

OUTPUT SECTION:

No. of Analog Outputs	4 (Simultaneous Updating)

DIGITAL FILTER SECTION:

No. of Digital Filter Channels	4 for Real Data 2 for Complex Data
Input Data Word Length	16-bit (2's Complement)
Tap Data Word Length	16-bit (2's Complement)
Output Data Word Length	16-bit (2's Complement)
No. of Taps/Channel	4 to 255
Throughput Rate (N Taps, M Channel)	10/ [M (N+2)] MHz for Real Data 10/ [M (4N+4)] MHz for Complex Data
Decimation Interval (DI)	Max. 16 Filter Cycles or Sampling Periods

1 VME board = 3800 MIPS

Video Bandwidth FIR Filter

1 MIPS INMOS A-100 is not comparable to 1 MIPS Motorola 56000 or ATE

FEATURES

- Up to 5MHz Throughput Rate
- 128, 256 or 348 Taps for the L, M or H Version [illegible]
- 16 bit Input, 16 bit coefficient and 24 bit output
- Dual Banked Coefficient Memory
- Direct Data Input from an External Source or the VMEbus Host
- 1K Word Output FIFO or [illegible] Host
- P2 Connector for External Data I/O
- Programmable Output Decimation Interval
- Programmable Output Scaling
- Front Panel Overflow [illegible]
- Programmable Interrupt Interval
- Full VMI bus Compatibility

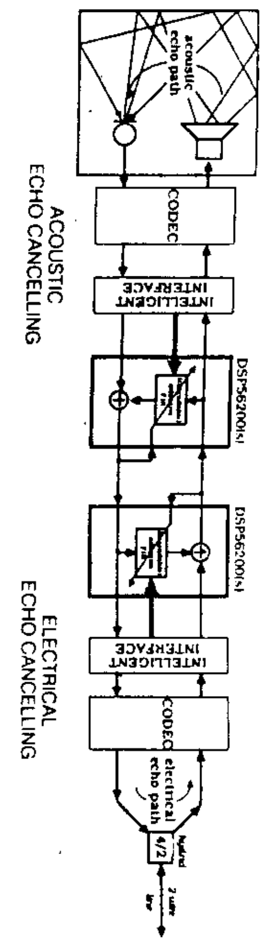
REAL-TIME APPLICATIONS

- Operation with Single or Two channel Input Data
- Direct Processing of a Complex (I & Q) Input with either Real or Complex Taps
- [illegible] Video [illegible]
- Correlation, Convolution and [illegible]
- High-speed Adaptive Filtering
- Hilbert Transformation
- Waveform Synthesis
- Bandwidth Reduction
- Harmonic Analysis
- Pulse Compression

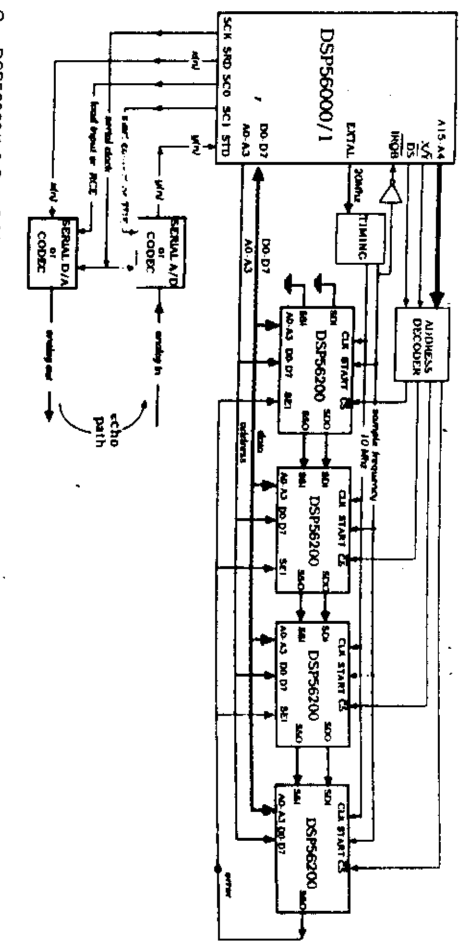
SPECIFICATIONS

Input Data Word Length	16-bit
Coef. Data Word Length	8, 12 or 16-bit
Output Data Word Length	24-bit (User Scaled)
Max. Throughput Rate	5, 3.3 or 2.5 MHz for 8, 12 or 16-bit Coefficients
Max. No. of Taps	128, 256 or 384 for the L, M or H Version
Decimation Interval (DI)	1-128 Sample Perious
Interrupt Interval	Up to 256xDI sample periods in steps of 2xDI
Power Input	+5V ±5% at 3.5A (H) 3.0A (M) 2.5A (L)
Operating temp.	Commercial Range
Board Size	233mm(W)x160mm(L)

ACOUSTIC/TELEPHONE ECHO CANCELLER (A/TEC)



FOUR-CHIP ADAPTIVE FILTER SYSTEM



One DSP56000/1 & Four DSP56200s implement a 1024 tap echo-canceller up to 19 khz or a 128 tap echo-canceller up to 120 khz

DSP56200 PERFORMANCES

Maximum sampling frequency is a function of the number of taps and of the number of DSP56200's used

MODE	TOTAL NUMBER OF TAPS 32	64	128	256	512	1024
FIR FILTER • Standalone • 4 chip in cascade	227khz	132khz	71khz 222khz	37khz 132khz	71khz	37khz
ADAPTIVE FIR • Standalone • 4 chip in cascade	123khz	69khz	37khz 120khz	19khz 69khz	37khz	19khz
DUAL FIR FILTER • Standalone • 4 chip in cascade	122khz	68khz	36khz no cascade in dual mode	-		

DSP56200 ... digital signal processing peripheral designed to perform computationally intensive tasks associated with digital filtering. A flexible chip-cascading scheme enables the user to build filters with extended tap lengths and/or increased speed. Its performance, features and simple interface make the DSP56200 a natural solution for problems such as echo cancelling, telephone line equalization, noise cancelling, conventional filtering and many other DSP applications.

The high performance 10.25 MHz internal operation of the DSP56200 allows many DSP algorithms to be implemented in one chip.

The core of the chip consists of a 16 x 24 → 40-Bit multiply accumulation unit, 256 x 16-Bit data RAM and 256 x 24-Bit coefficient RAM. The interface is extremely versatile providing an 8-Bit I/O port with 4 address pins and 3 control pins, and 5 serial I/O pins to allow true cascadability.

The operating modes, set by the user, determine how the DSP56200 will operate. The key features of the mode-select are:

- single channel
- dual channel (non-cascadable, non-adaptive)
- stand alone/cascadable
- fixed coefficients/LMS coefficient update

With a programmable tap-length of up to 256 taps in single channel mode and 128 taps in dual channel mode the DSP56200 offers a very high degree of user flexibility. Features such as programmable gain and leakage, as well as a DC tap option further highlight the chip's capability. The adaption algorithm can be disabled during "double-talk" situations allowing the coefficients to remain constant, and indeed unused coefficient and data memory is available as "scratch-pad" memory. The DSP56200 utilizes an ultra-low power stand-by mode to reduce power consumption.

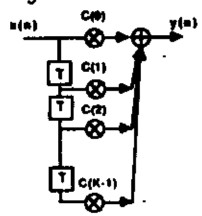
FINITE IMPULSE

RESPONSE FILTERS

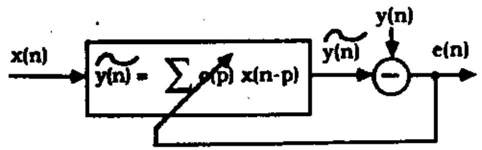
The filtered output signal y(n) is obtained by weighted summation of a finite set of input samples. Coefficients of the weighted sum constitute the impulse response of the filter.

FIR filters can be linear phase filters and this structure is generally chosen for adaptive filtering.

$$y(n)=\sum_{p=0}^{k-1} c(p)x(n-p)$$



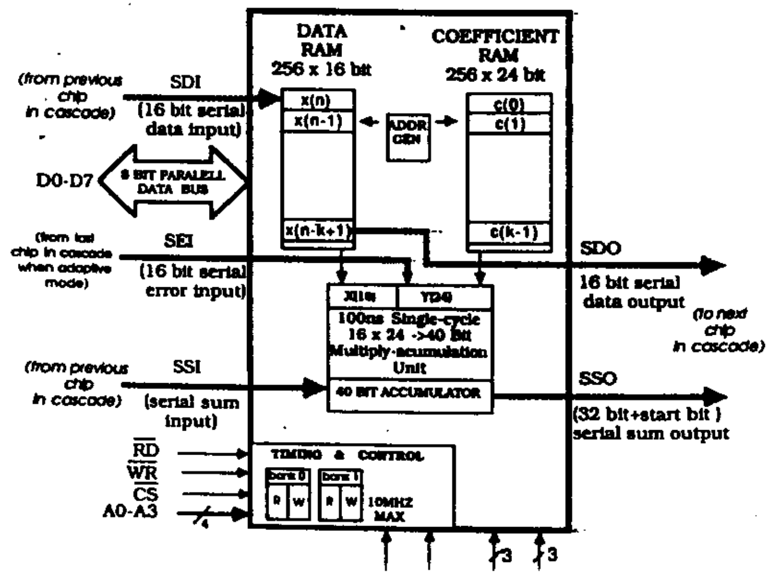
ADAPTIVE FILTERING



The filter approximates a signal y(n) with the input sequence x(n). Using the error e(n) between the filtered output $\tilde{y}(n)$ and the desired signal y(n), an adaptive algorithm adjusts the filter coefficients, altering its response in order to minimize a measure of the error. In the DSP56200, coefficients are adapted by the Least Mean Square (LMS) algorithm.

$$c_{n+1}(p) = c_n(p) + K\,e(n)\,x(n-p) + \mathrm{sgn}\,(c_n(p))L$$

DSP56200 GENERAL BLOCK DIAGRAM



Loughborough Sound Images Ltd

DSP56001 VME BOARD

User Manual

Preliminary January 1989

UNIX drivers for VME56K.

The UNIX drivers support the following features.

- Select memory space (P, X or Y)
- Set memory address
- Read memory
- Write memory
- Start program running
- Stop program running
- Set handshake flag in interface
- Clear handshake flag in interface
- Read handshake flag in interface

These routines are all implemented via the host interface of the DSP56001 wh is mapped as a slave port onto the VME bus. All transfers take place over the bus as byte transfers.

These drivers support the 'open', 'close', 'IOCTL', 'read' and 'write' funtions, which can be called from programs running under UNIX and SUN workstation

2.5 DSP56200 Configuration

The board is supplied with two DSP56200 FIR filter devices. The DSP56200 can be configured as an FIR filter or as an adaptive filter. More than one DSP56200 can be cascaded to form a filter of more taps, at a given sample rate, than would be possible using just one device. The two devices supplied are mapped into the on board I/O peripheral space. The first device (A) occupies locations from Y:$FFD0 to Y:$FFDF and the other device (B) is at Y:$FFE0 to Y:$FFEF. Link LK19 can be used to select the type and length of the filters required (figure 2.10). In the single/cascaded FIR or single/cascaded adaptive mode device A has the first half of the coefficients and device B the second half. The START signal is produced from the on board sample rate generator.

1.6 Software

A monitor program is supplied that runs on an IBM-PC or compatible. Full details are in section 3. It controls the VMEbus based board via the RS232 link provided. It supports accesses to all available memory, including on-chip memory, and to on-chip registers. Programs can be run at full speed, up to breakpoints, or be single stepped. An option is available to time user code via the on-board interval timer. Further details in Section 3.
The monitor reserves for its use one address register set (R7,N7,M7), and program memory addresses $40 to $7F and $E000 to $E100.

If the Motorola software has been purchased, it includes their DSP56000 Macro Cross Assembler and DSP56000 Cross Linker. These provide the facility to process source program code and generate an object code file for use with the DSP56001. The simulator program is provided as a software tool to develop programs and algorithms for the DSP56001. The Motorola DSP56000 'C' Compiler software is available, and can be purchased as a separate item.

1.7 Additional Documentation

2.9.2 Sample Rates for Analog I/O

An on board sample rate generator or an external trigger source may generate the sample rate for the ADCs and DACs. The source for this trigger is selected with link LK13. If link Lk13a is inserted, and link LK13b removed the external trigger is selected. Otherwise, if link LK13b is inserted and link LK13a removed the on board sample rate generator is selected. On shipping the on-board sample rate generator is selected.

NETWORK SYSTEM

(for a short-term solution)

The ideal is to find an existing expandable parallel processing system with standard software and hardware support with which to interface DSP-Peripherals.

1. A parallel reconfigurable processing system based on Transputers.
(serial transfer rate: 20 Mbit/sec)
- each Transputer having as a cooprocessor a DSP (Motorola, or AT & T, or Texas) as a front-end to the peripherals: A/D, D/A, Serial I/O, Parallel I/O. (acquisition time up to 50 Mbyte/sec). See Fig. 3

2. A parallel reconfigurable processing system based on RISC processors.

DSP SELECTION

Selection of a general purpose DSP to be used in the network system for general application.

Among existing DSPs, I will take the following into consideration for their performance and their diffusion (consequently hardware and software support):

- AT & T DSP32C
- Motorola DSP96001
- TEXAS INSTRUMENT TMS320Cxx

- Full standard C language compiler for the *WE* DSP32 Digital Signal Processor
- Complete development environment, with symbolic debugging and assembly-language interface
- Standard *UNIX*® System library support, including libm and a subset of libc
- Includes *WE* DSP32-AL Application Software Library of signal processing functions

The DSP32-CC package provides a complete development environment for writing, debugging, and testing programs. In addition to the C compiler, an enchanced version of the *WE* DSP32-SL Support Software Library, a symbolic debugger, and other utilities are included.

AT&

WE® DSP32C Development System

Clockwise from top: DSP32C software development card, dynamic RAM expansion card, multiple in-circuit emulation interface, in-circuit emulation card (and cable), and PCbus interface card.

Features

- Software development card for IBM PC/XT/AT* (and compatib personal computers, featuring:
  - Full-speed operation of DSP32C (50 MHz)
  - 16 Kwords of static RAM (0 wait states)
  - Optional 48 Kwords of additional static RAM (1 wait state)
  - Optional expansion card w 1 Mword of dynamic RAM
  - Serial I/O through an AT& T7520 High-Precision Co
- In-circuit emulation card with high-speed PC interface
- Multiple in-circuit emulation interface allows up to four emulation cards to be controll through one PCbus interface
- Software development and in-circuit emulation cards are controlled by the DSP32C software simulator

Description

The DSP32C Development System is actually a family of products. This modular desig allows you to purchase only t components you need to assemble the exact developm environment your application requires. The two major uses the system are real-time softw development and in-circuit emulation of the target hardw

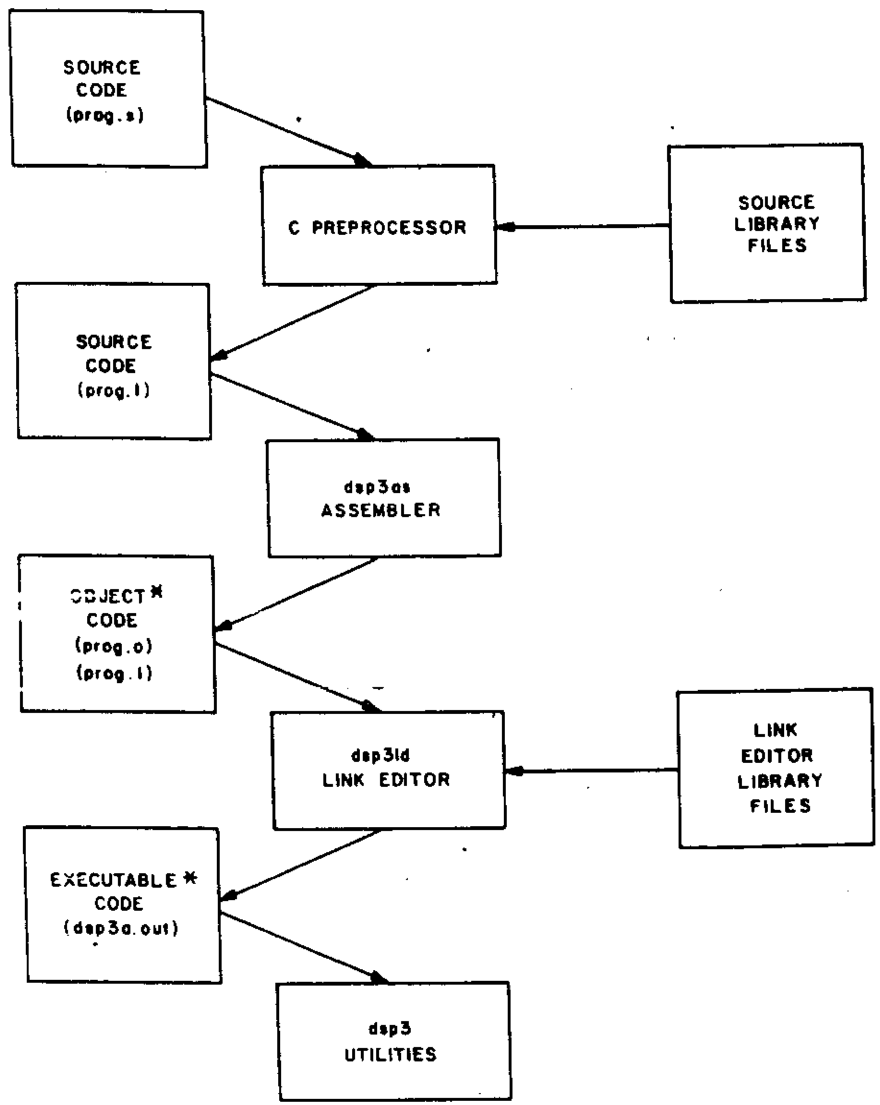


Figure 1. Software Generation Process

dsp3sim	Simulator	**dsp3init**	Development System Initializer
dsp3as	Assembler	**dsp3size**	Object File Code Size Reporter
dsp3ld	Link Editor	**dsp3strp**	Symbol Table and Line Stripper
dsp3make	Make Utility	**dsp3nm**	Symbol Table Lister
dsp3ar	Archive Utility	**dsp3dump**	Object File Dumper
dsp3msk	Mask ROM Formatter		

Software Summary

DSP56KCCx
DSP56000/1 Family C Language Compiler

DSP56KCCx is a full Kernighan and Ritchie C implementation supporting development of DSP56000 Family applications.

Features include support of:

- Structures/Unions
- Floating Point
- Pointer Variables
- In-Line Assembly Language Code Compatibility
- Full Function Pre-processor supports:
  - Macro Definition/Expansion
  - File Inclusion
  - Conditional Compilation
- Low Compiler Overhead (approximately 20%)
- Full Error Detection and Reporting

Ordering information:

Host Platform	Operating System	Order Number
IBM®-PC	DOS 2.X, 3.X	DSP56KCCA
Macintosh® II	MAC OS 4.1	DSP56KCCB
SUN-3®	UNIX® BSD 4.2	DSP56KCCC
VAX®	VMS 4.X	DSP56KCCD
VAX	UNIX BSD 4.2	DSP56KCCE

Each package consists of:

- Software
  - C Compiler (CC56000)
  - Macro Cross Assembler Program (ASM56000)
  - Linker/Librarian (LNK56000/LIB56000)
- Documentation
  - DSP56KCC Compiler User's Manual
  - C Pre-Processor User's Manual
  - Macro Cross Assembler Reference Manual
  - DSP56000/1 Data Sheets
  - DSP56000 User's Manual

MOTOROLA
SEMICONDUCTOR
TECHNICAL DATA

BR522/D

DSP320to56001

Software Summary

DSP320to56001 Translator Software

The DSP320to56001 translator software will convert any 32010 code into code for Motorola's powerful new digital signal processor chip, the DSP56001. The primary features of DSP320to56001 are:

- Translation of any 32010 applications software into DSP56001 source code
- Two modes of operation:
  - — Translates to 56001 source code for potential optimization and assembly with the DSP56000SASMA or DSP56000CLASA software
  - — Translates and runs 32010 Code "as is" directly and immediately on the DSP56000ADS, Motorola's DSP560001 Applications Development System
- Runs on IBM[1]-PC under MS[®]-DOS or PC-DOS
- C source code of DSP320to56001 program is provided on diskette
  - — User may modify for 32020 and 320C25 translation
  - — Third party vendors may contact Motorola for licensing details
- Registration card provided so users can obtain future optimized versions of DSP320to56001 software, hand-coded macro routines, etc.

MOTOROLA DSP DEVELOPMENT SOFTWARE 32010 TO 56000/1 CODE CONVERSION

HARDWARE REQUIREMENTS

The conversion programs are delivered on one double-sided, double-density 5 1/4 inch floppy disk and may be run from either a floppy disk or a hard disk. They require only enough disk space to hold the output of the converted source file.

The minimum hardware requirements for the conversion programs are:
IBM-PC, XT, AT, or compatible with 256K bytes of RAM and one 5 1/4 inch floppy disk drive.
PC-DOS/MS-DOS v2.0 or later.

The DSP56000 Application Development System (DSP56000ADS) is recommended as a development tool for designing real-time DSP56000/1 signal processing systems.

IBM is a registered trademark of International Business Machines Corporation.
MS-DOS is a trademark of Microsoft, Inc.

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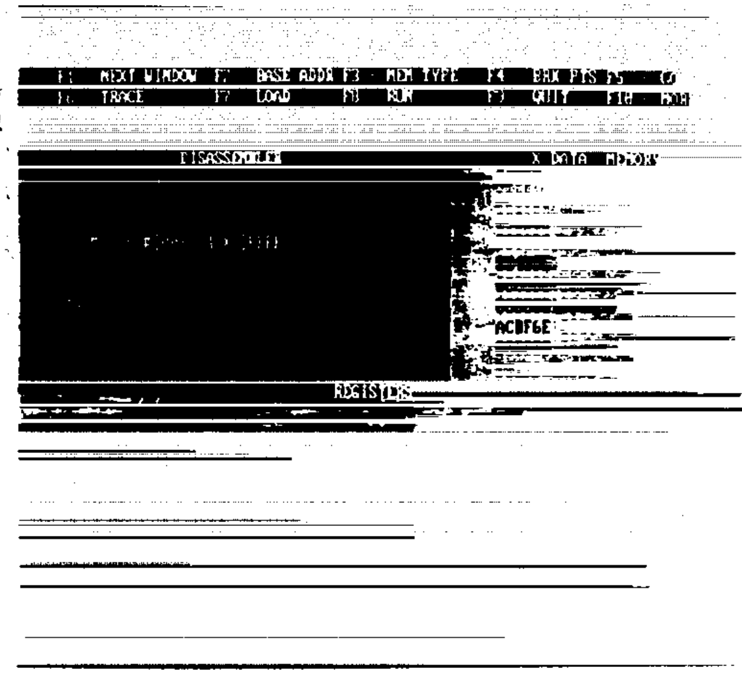
MOTOROLA DSP56001 Development and Applications



- *PC plug-in with 20 MHz Processor*
- *144 KBytes Fast SRAM Supplied User-expandable to 576 KBytes*
- *Window-based Debug Monitor*
- *Motorola Support Software included - Assembler, Linker and Simulator C Compiler also available*
- *Twin Channel 16 bit A/D and D/A*
- *Serial and Parallel I/O Expansion*

TMS320 Applications

TMS320C3X

320C30 32-Bit CPU
Virgule glissante
Super DSP

Work stations

Réglages complexes

TMS320C2X

32020 16-Bit CPU
320C25 100 ns Cycle
320E25 128 K' Mots adressage
320C26C 1,5 K Mots de RAM

Télécommunication

Industrie *Véhicules à moteur* *Domaine militaire*

TMS320C1X

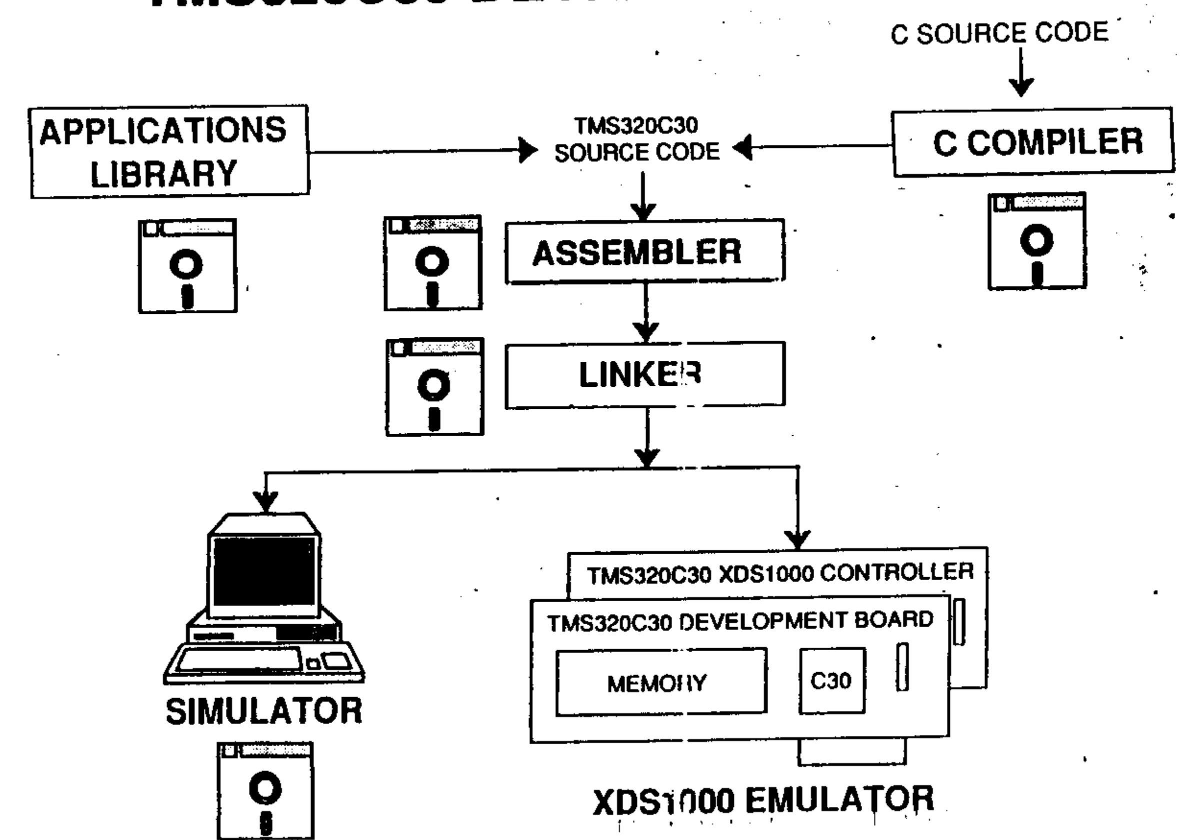
32010 Low Cost
320C10 16-Bit CPU
320C15/E15 ROM/EPROM
302C17/E17 160 ns Cycle
32014/E14 Fonctions contrôleurs

Modems *Bien de consommation*

Traitement de parole *Téléphonie* *Ordinateurs* *Saisie des valeurs de mesure*

TMS 320-DSP FAMILY OF CHOICE

TMS320C30 DEVELOPMENT TOOLS



TMS320 BENCHMARKS

BENCHMARK	TMS320C1x CYCLES	@ 160nS	TMS320C2x CYCLES	@ 80 nS	TMS320C3x CYCLES	@ 60 nS
FIR FILTER						
20 TAP	49	127.5 KHZ	29	431.03 KHZ	25	667 KHZ
64 TAP	133	47.0 KHZ	73	171.73 KHZ	73	228 KHZ
67 TAP	139	45.0 KHZ	76	164.47 KHZ	76	219 KHZ
IIR FILTER						
4 X BIQUAD	44	142.0 KHZ	36	347.22 KHZ	23	725 KHZ
5 X BIQUAD	56	111.6 KHZ	43	284.09 KHZ	27	617 KHZ
TRANSPOSE BIQUAD	69	90.6 KHZ	54	231.48 KHZ	37	450 KHZ
DOT PRODUCT	6	0.96 μS	6	.48 μS	4	.240 μS
MATRIX MULTIPLY						
2 X 2 TIMES 2 X 2	24	3.84 μS	21	1.7 μS	12	.720 μS
3 X 3 TIMES 3 X 1	24	3.84 μS	22	1.8 μS	13	.780 μS
MEMORY TO MEMORY FFT						
64 POINT RADIX 2	3687	590 μS	3088	247 μS	2603	156 μS
256 MOINT RADIX 2	41478	6.64 mS	17602	1.408 mS	12857	.771 mS
1024 POINT RADIX 2	331237	53.0 mS	109755	8.784 mS	61511	3.67 mS
PORT TO MEMORY FFT						
64 POINT RADIX 2	2954	473 μS	1621	130 μS	1370	82 μS
256 POINT RADIX 2	41418	6.64 mS	8520	.682 mS	6734	.404 mS
1024 POINT RADIX 2	331237	53.0 mS	56286	4.503 mS	32354	1.94 mS

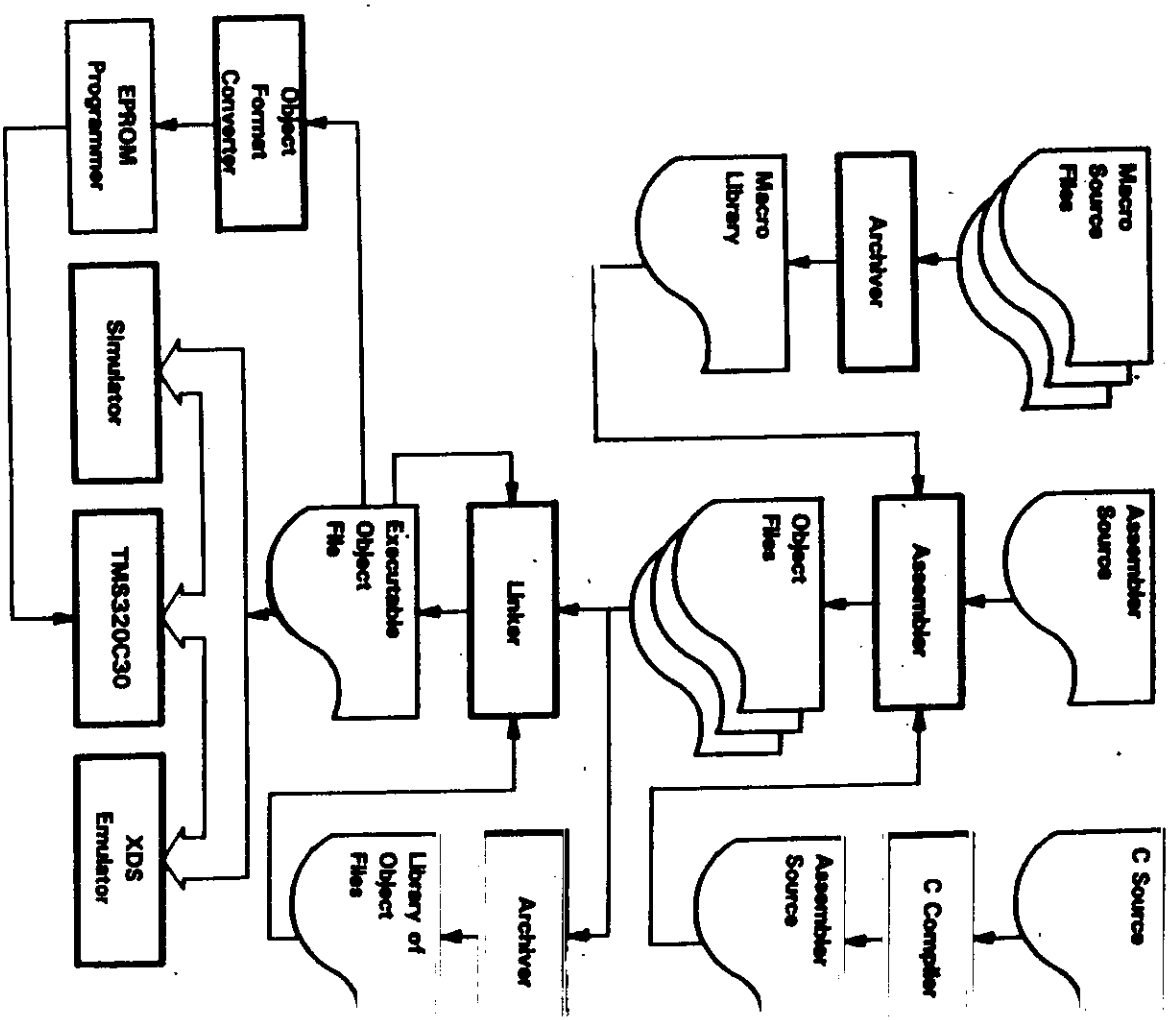


Figure B-1. TMS320C30 Development Environment

CONCLUSIONS

Trigger Systems as well as Accelerator Control Systems require exploiting the field of embedded processors and parallel processing.

- Embedded processors must usually be able to respond to events very quickly, must be very compact and must make code debugging easy, even during real-time operation. In the past these needs have been met by microcontrollers at the low end and bit-slice design at the high end.

- RISC, DSP, CISC and TRANSPUTERS can be used in embedded systems.

- Even if their throughput is different, the task in some applications can be well satisfied by more than one component.

- To better optimize a project or application, one should try to think how one component will fit better than another.

- An investigation must certainly include the component instruction set, speed and internal architecture that is best suitable for the application algorithms or for the needs of the more general project.

- More decisive in determining the overall throughput in a project, can be the harmonious interaction and inter-communication of the various components rather than the speed of any one single component.

- Thus the real effort in designing a specific application or project should be based on defining

"THE MULTIPROCESSING ARCHITECTURE"

for the best performance solution to the application or project.