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H4.SMR. 405/11

SECOND WORKSHOP ON TELEMATICS

6 - 24 November 1989

Switching System

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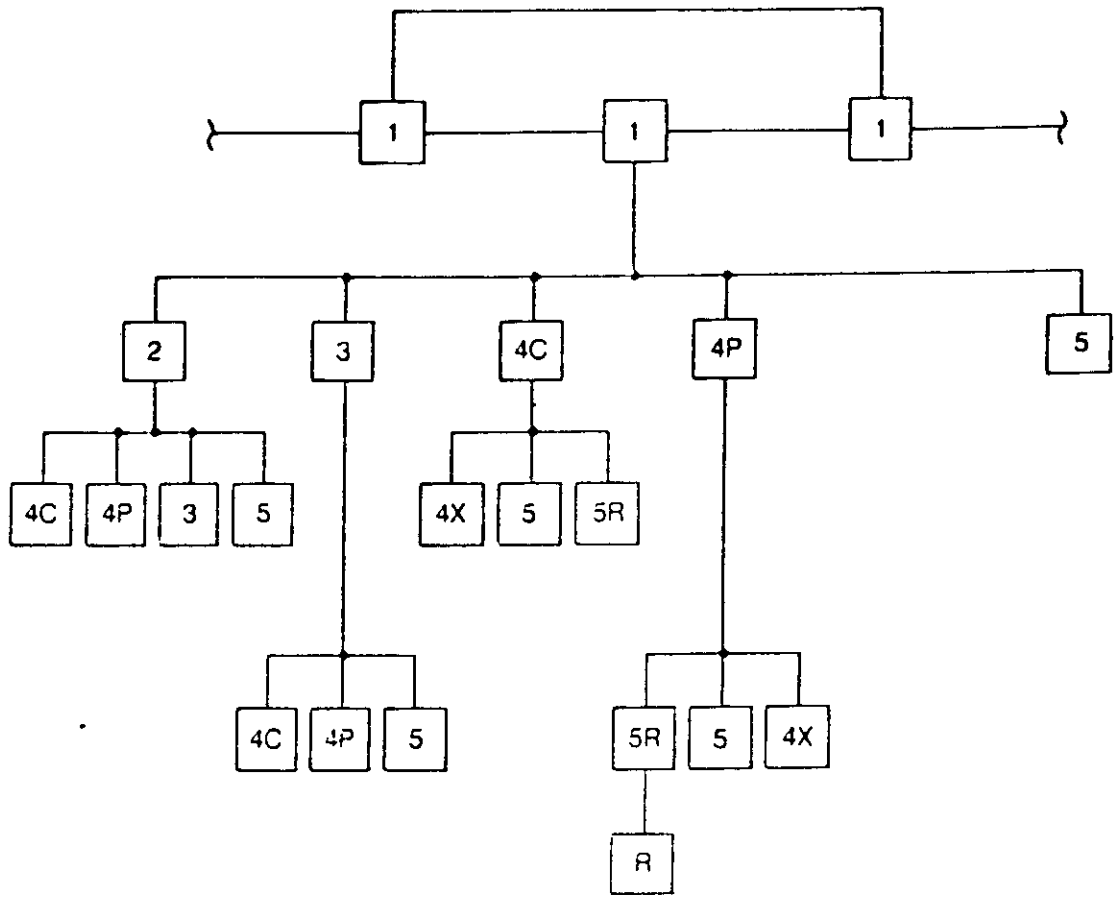


Key	Class	Name	Abbreviation
1	1	Regional Center*	RC
2	2	Sectional Center*	SC
3	3	Primary Center*	PC
4	4C	Toll Center	TC
4P	4P	Toll Point	TP
4X	4X	Intermediate Point	IP
5	5	End Office	EO
5R		End Office with Remote Switching Unit	
R		Remote Switching Unit	RSU

*May be a "point" rather than a "center". The abbreviation is then RP, SP, or PP.

Figure 1-4. *Network Heirarchy*

Figure 1-6. Example of Bell Telephone Network
(Courtesy of Bell Telephone Laboratories)

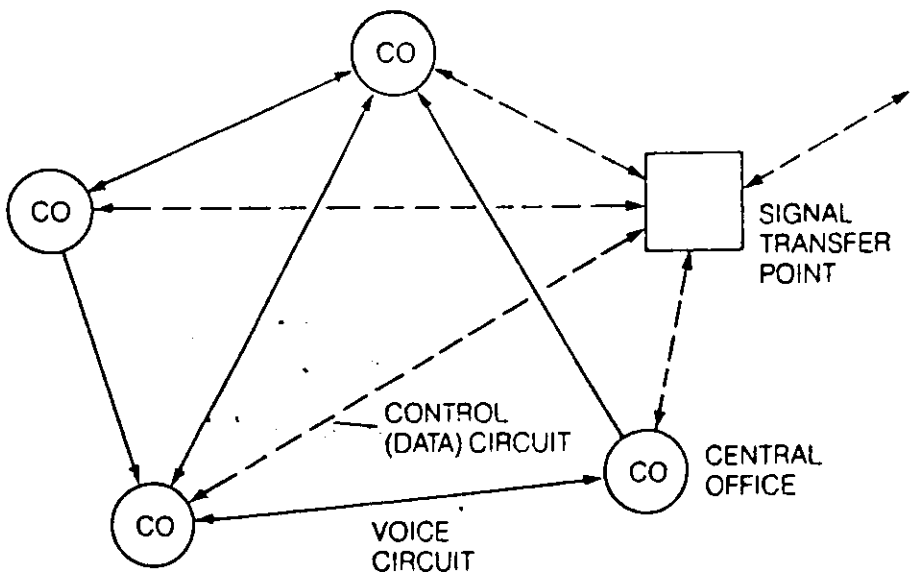


Figure 1-14. *Common Channel Interoffice Signaling (CCIS)*

Table 1-3. Network Call Progress Tones

Tone	Frequency (Hz)	On Time (Sec.)	Off Time (Sec.)
Dial	350 + 440	Continuous	
Busy	480 + 620	0.5	0.5
Ringback, Normal	440 + 480	2	4
Ringback, PBX	440 + 480	1	3
Congestion (Toll)	480 + 620	0.2	0.3
Reorder (Local)	480 + 620	0.3	0.2
Receiver Off-hook*	1400 + 2060 + 2450 + 2600	0.1	0.1
No Such Number	200 to 400	Continuous, Frequency modulated at 1 Hz Rate	

*Receiver off-hook is a very loud tone, 0 dBm per frequency.

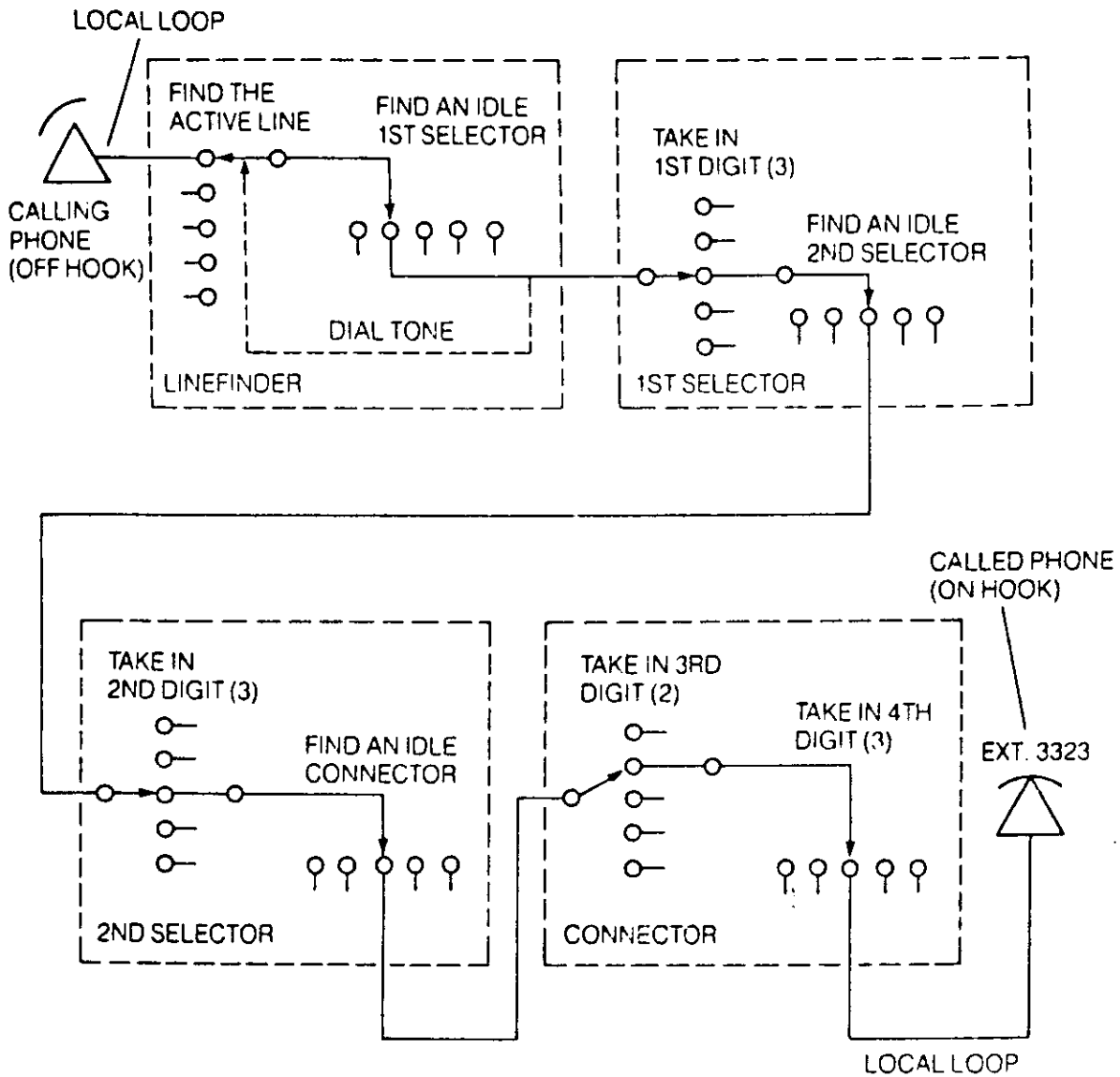


Figure 1-17. Strowger Step-by-Step Switching

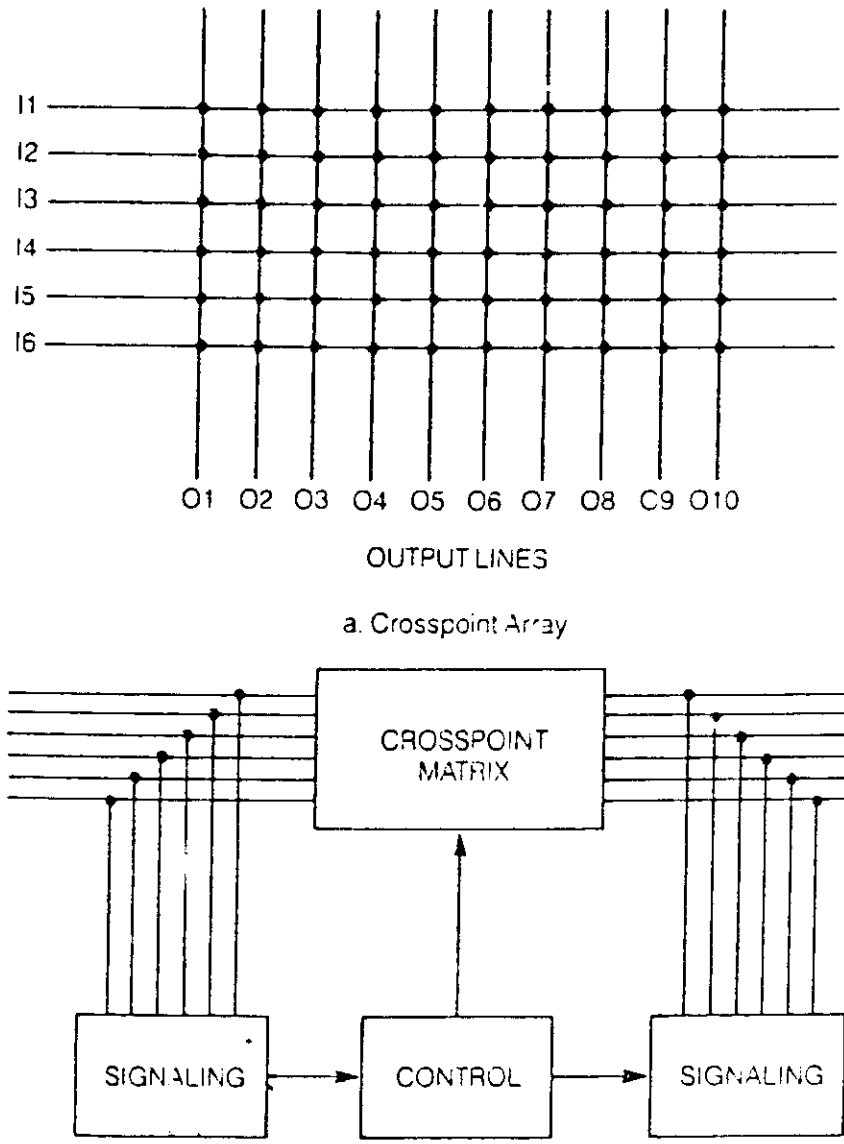


Figure 1-19. *Crossbar Switching*
(From J. Bellamy, Digital Telephony, *John Wiley & Sons, Inc., 1982, Copyright © 1982 by John Wiley & Sons, Inc., Reprinted by permission of John Wiley & Sons, Inc.)*

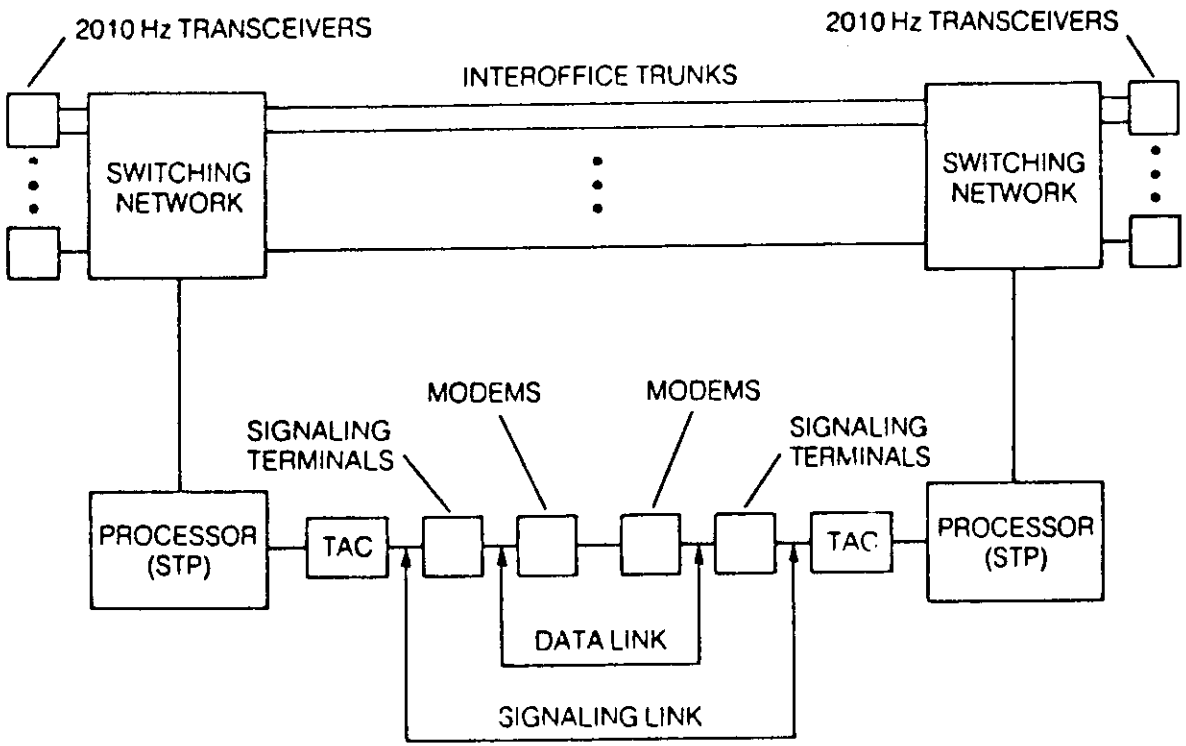


Figure 1-22. *CCIS Signaling Facilities*
(Copyright© 1980, American Telephone and Telegraph Co.)

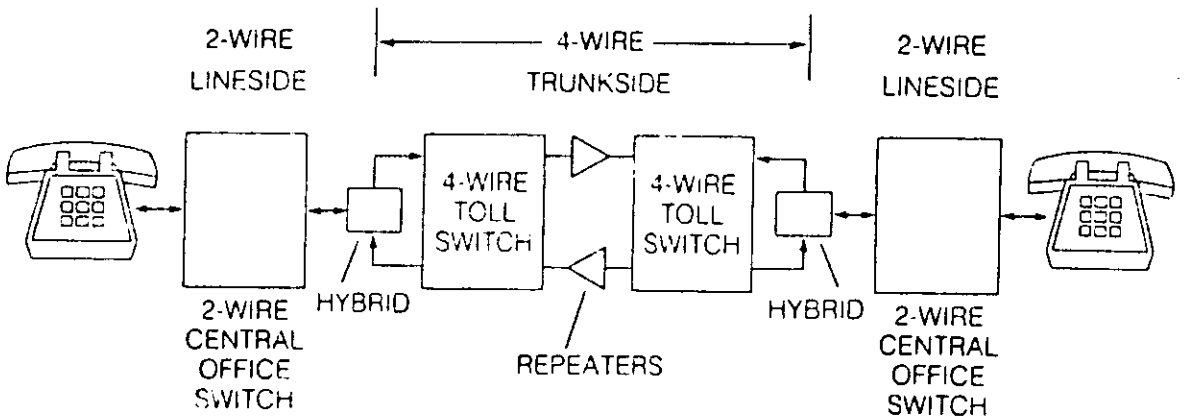
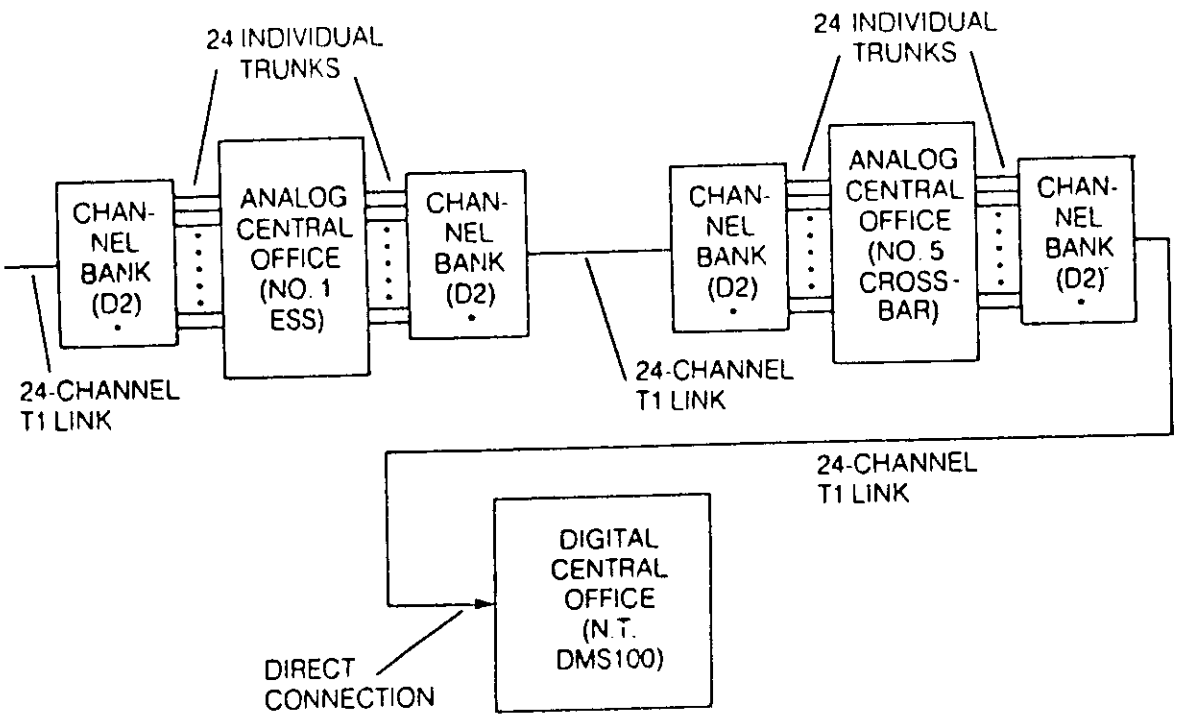


Figure 7-1. *Typical Analog Telephone Connection for a Long Distance Call*



*Each channel bank does a digital-to-analog and analog-to-digital conversion.

Figure 6-11. A/D and D/A Conversions

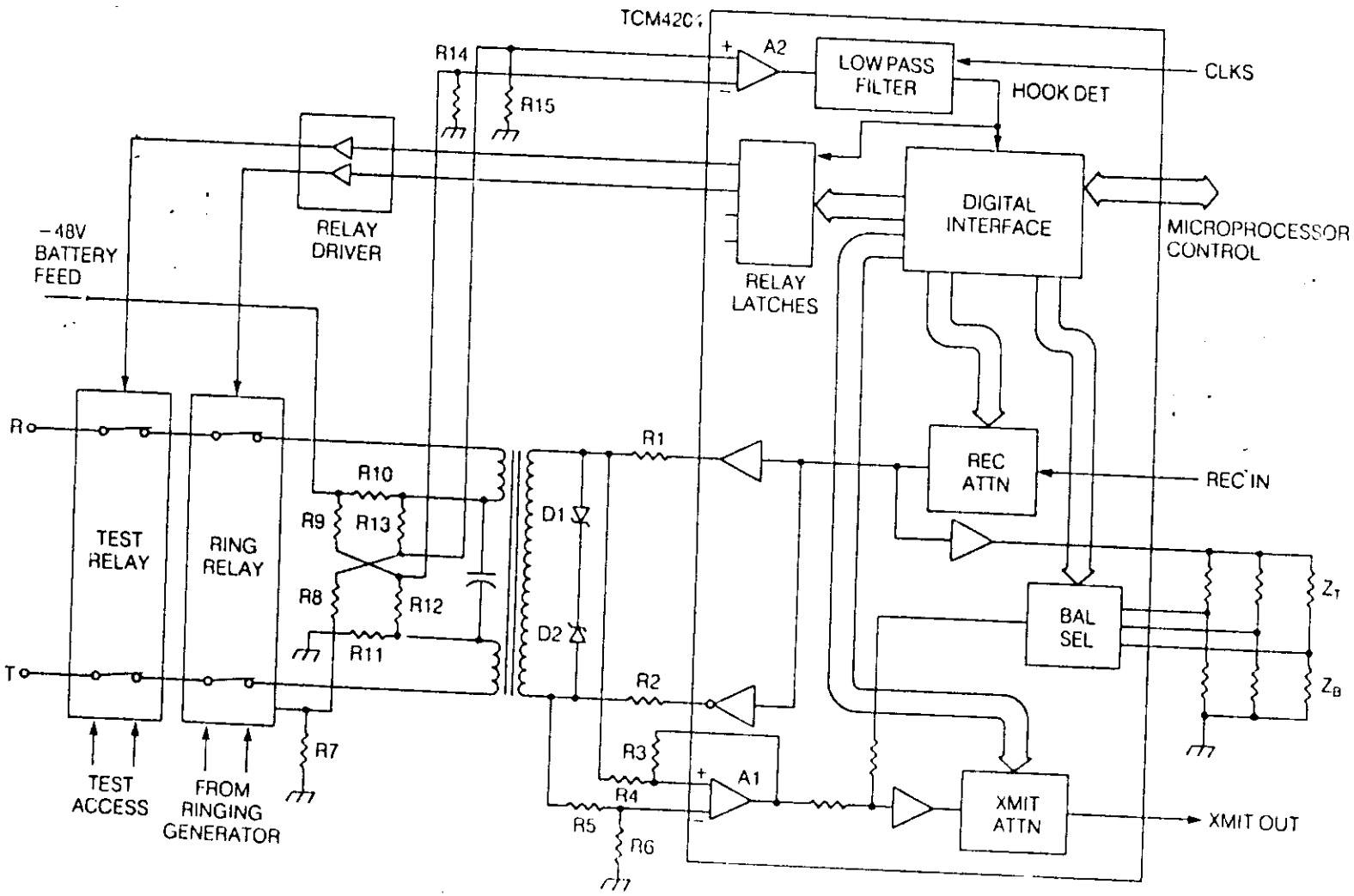


Figure 7-8. Subscriber Line Control Circuit

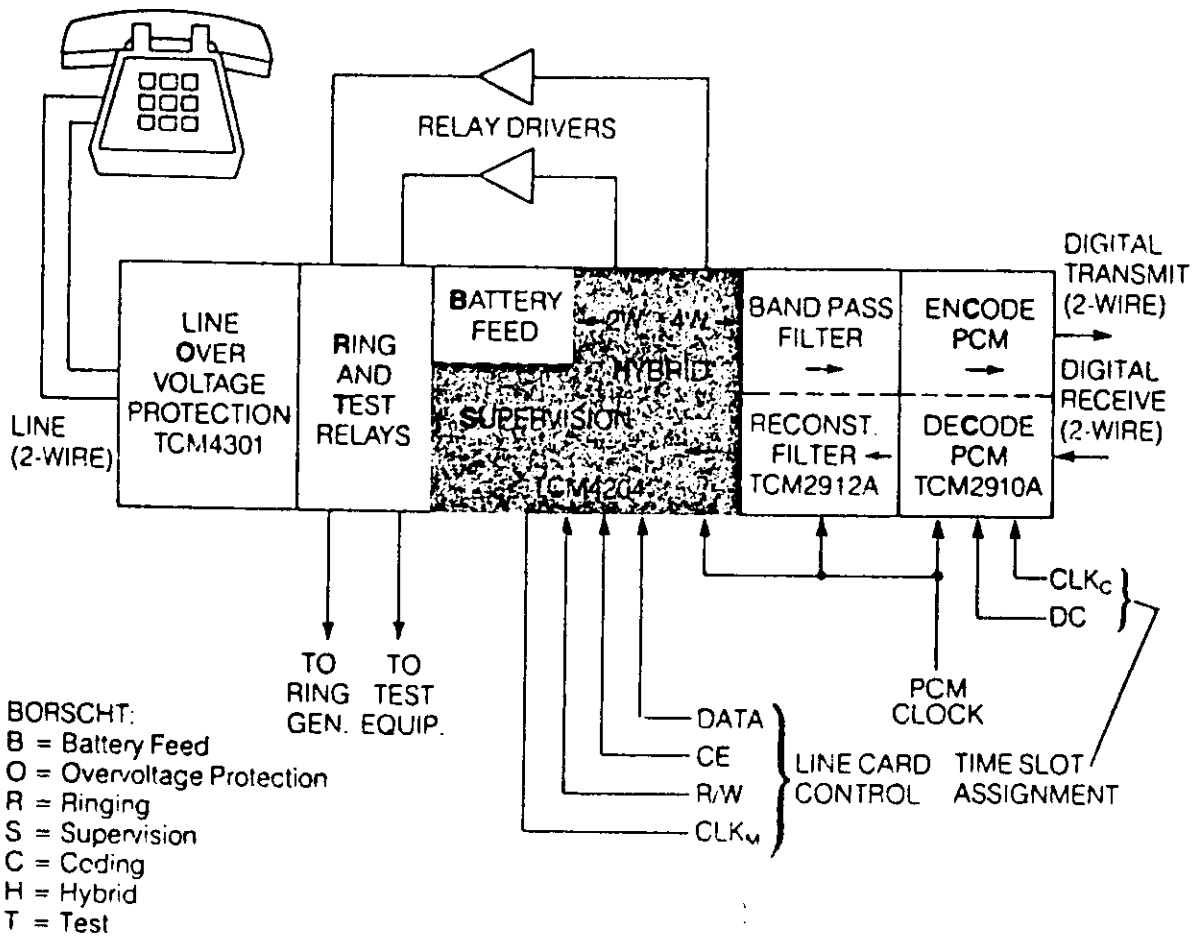


Figure 7-7. Digital Line Card Block Diagram

Operation

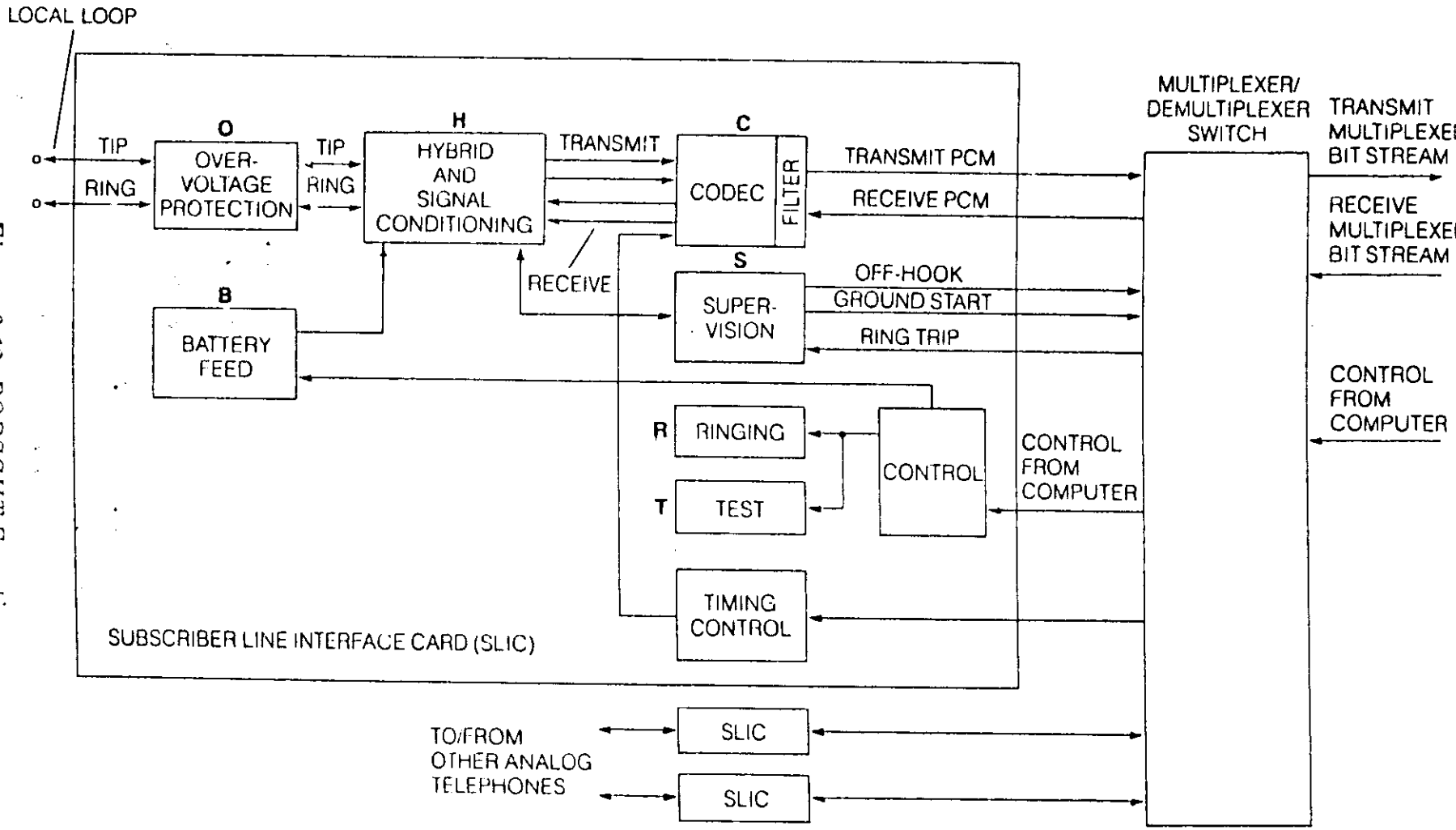


Figure 6-12. BORSCHT Functions

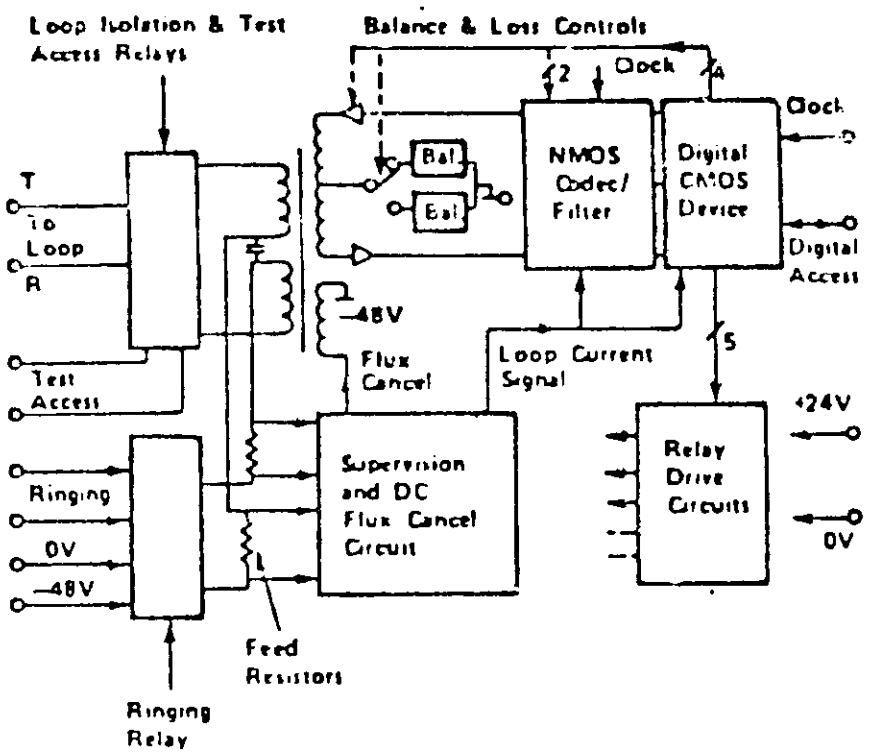


Fig. 11-2. DMS-100 line circuit block schematic. (From J. Terry, D. Younge, and R. Matsunaga, "A Subscriber Line Interface for the DMS-100 Digital Switch," *NTC* '79. © IEEE.)

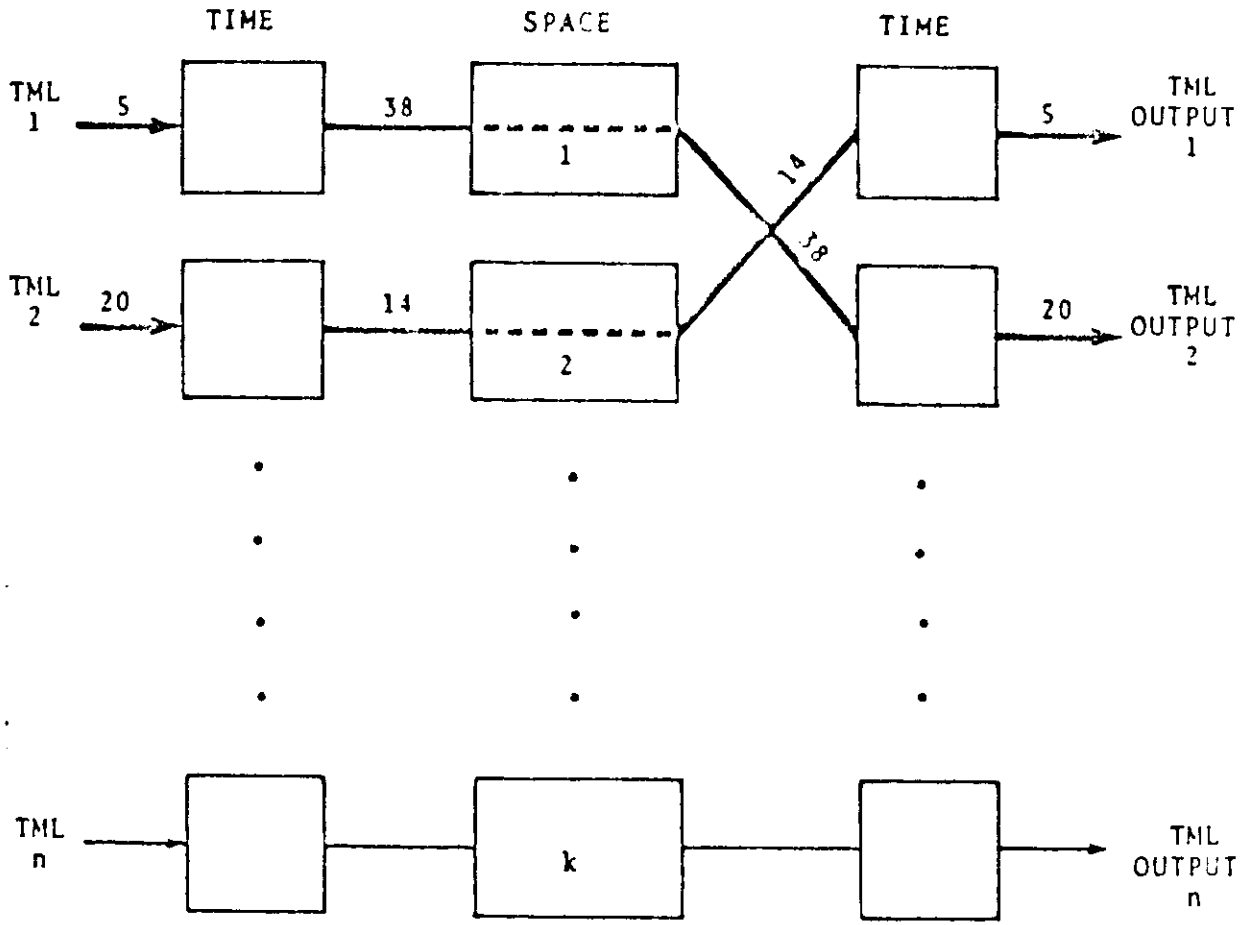


Fig. 11–4. Time-space-time (TST) switching network.

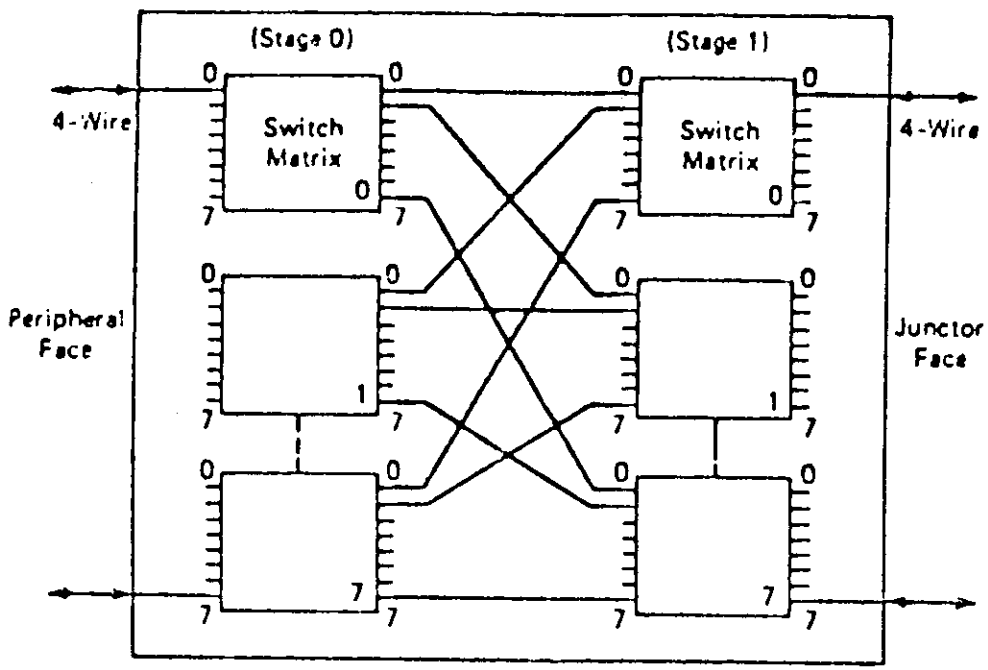


Fig. 12-8. DMS-100 network module switching matrix. (From J. Terry, H. Krausbar, and J. Hood, "DMS-200 Traffic Peripherals," *ICC '78*, © IEEE.)

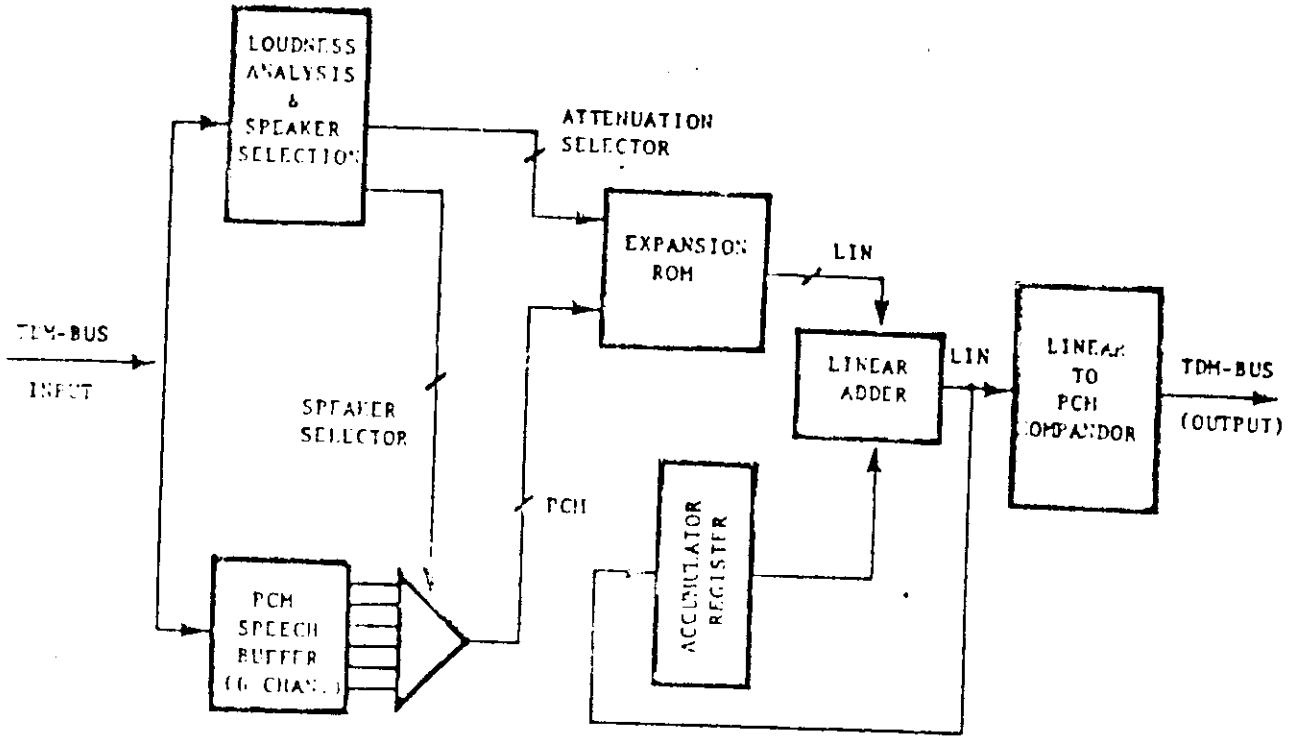


Fig. 11-6. Digital conference circuit. (From E. A. Munter, "Digital Switch Digitalks," *IEEE Communications Magazine*, Nov. 1982, © IEEE.)

Table 11-1. Provisioning of Service Circuits.

SERVICE CIRCUIT ELEMENT	TIME FRAME	PROBABILITY OF ALL CIRCUITS BUSY
DTMF receivers	HDBH[1]	<5%
Interoffice receivers	ABSBH[2]	<1%
Interoffice transmitters	THDBH[3]	<1%
Tone circuits	HDBH	<0.1%
Ringing circuits	HDBH	<0.1%
Dial tone delay	ABSBH	Max. 1.5% > 3 seconds
	THDBH	Max. 8% > 3 seconds
	HDBH	Max. 20% > 3 seconds
Conference circuits	ABSBH	<1% of 3 port attempts
Announcement circuits	ABSBH	<1% with overflow to tone trunks

[1] High Day Busy Hour
[2] Average Busy Season Busy Hour
[3] Ten High Day Busy Hour

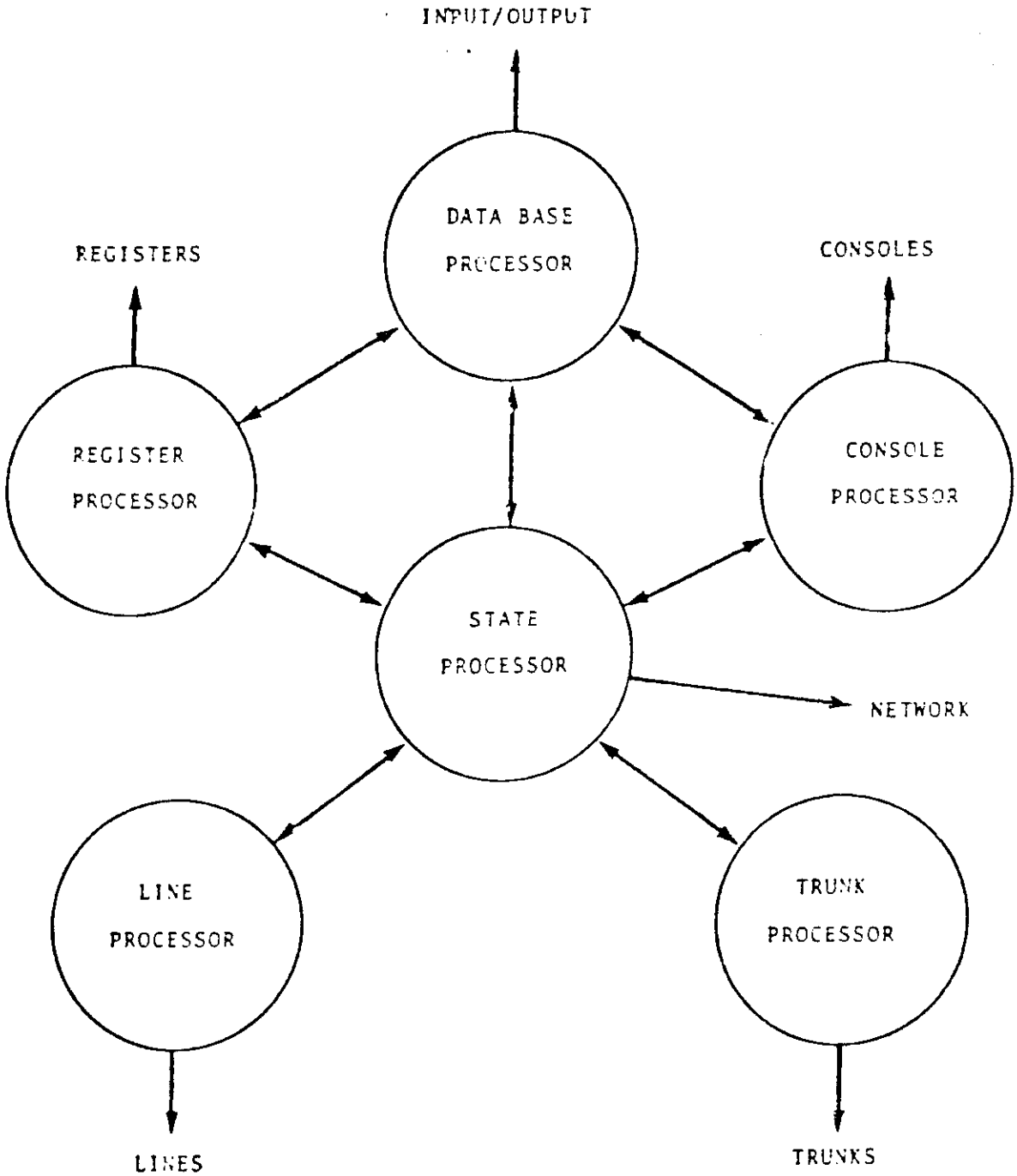
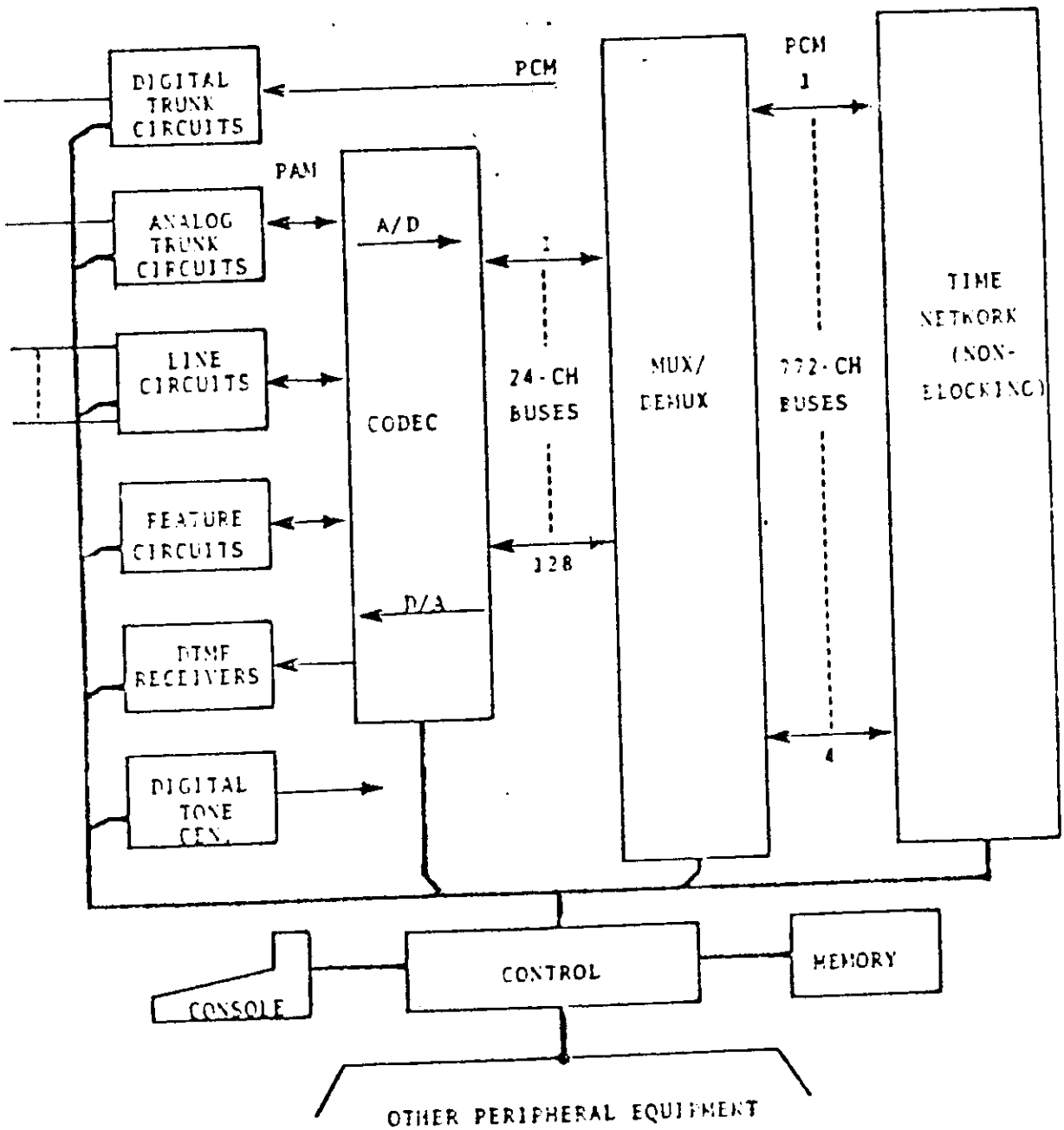


Fig. 12-2. Rockwell 580 DSS control complex.



MAXIMUM SIZE - 2400 LINES, 600 TRUNKS

Fig. 12-1. Rockwell 580 DSS block diagram.

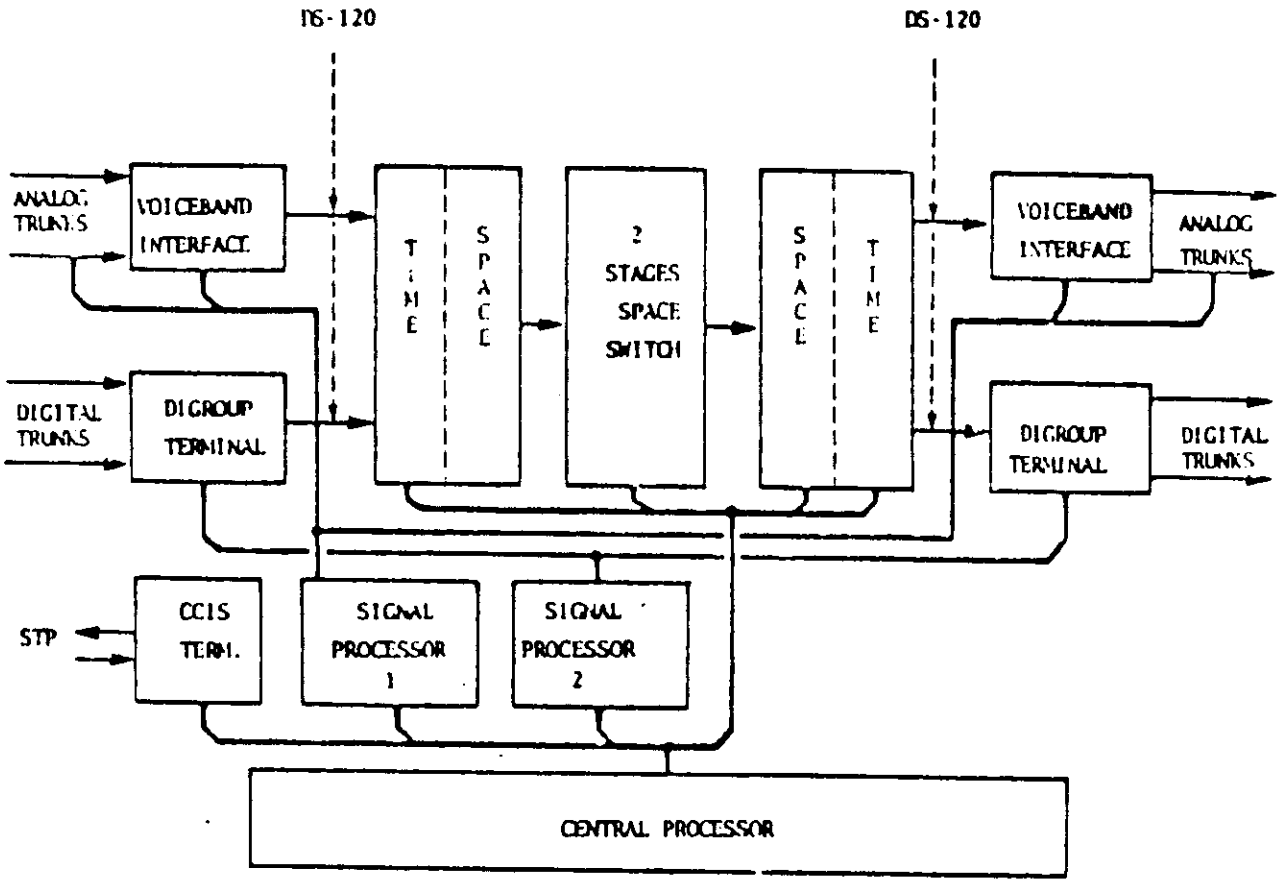


Fig. 12-15. AT&T No. 4 ESS switching system. (Based on Figs. 1 and 2, Bruce, Giloth, and Siegel, "No. 4 ESS—Evolution of a Digital Switching System," *IEEE Transactions on Communications*, July 1979, © 1979 IEEE.)

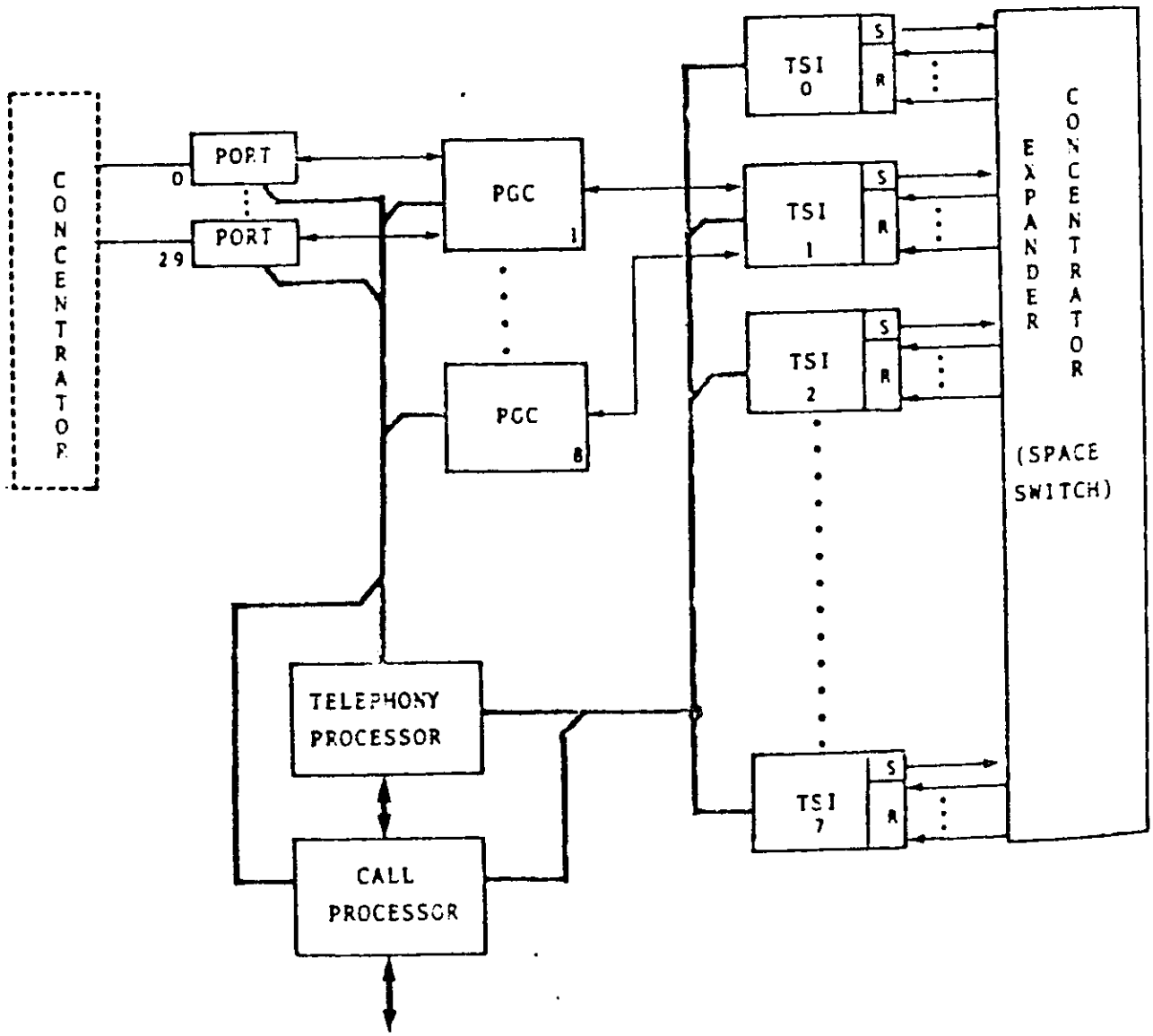


Fig. 12-3. Stromberg-Carlson System Century DCO, 1920-port system.

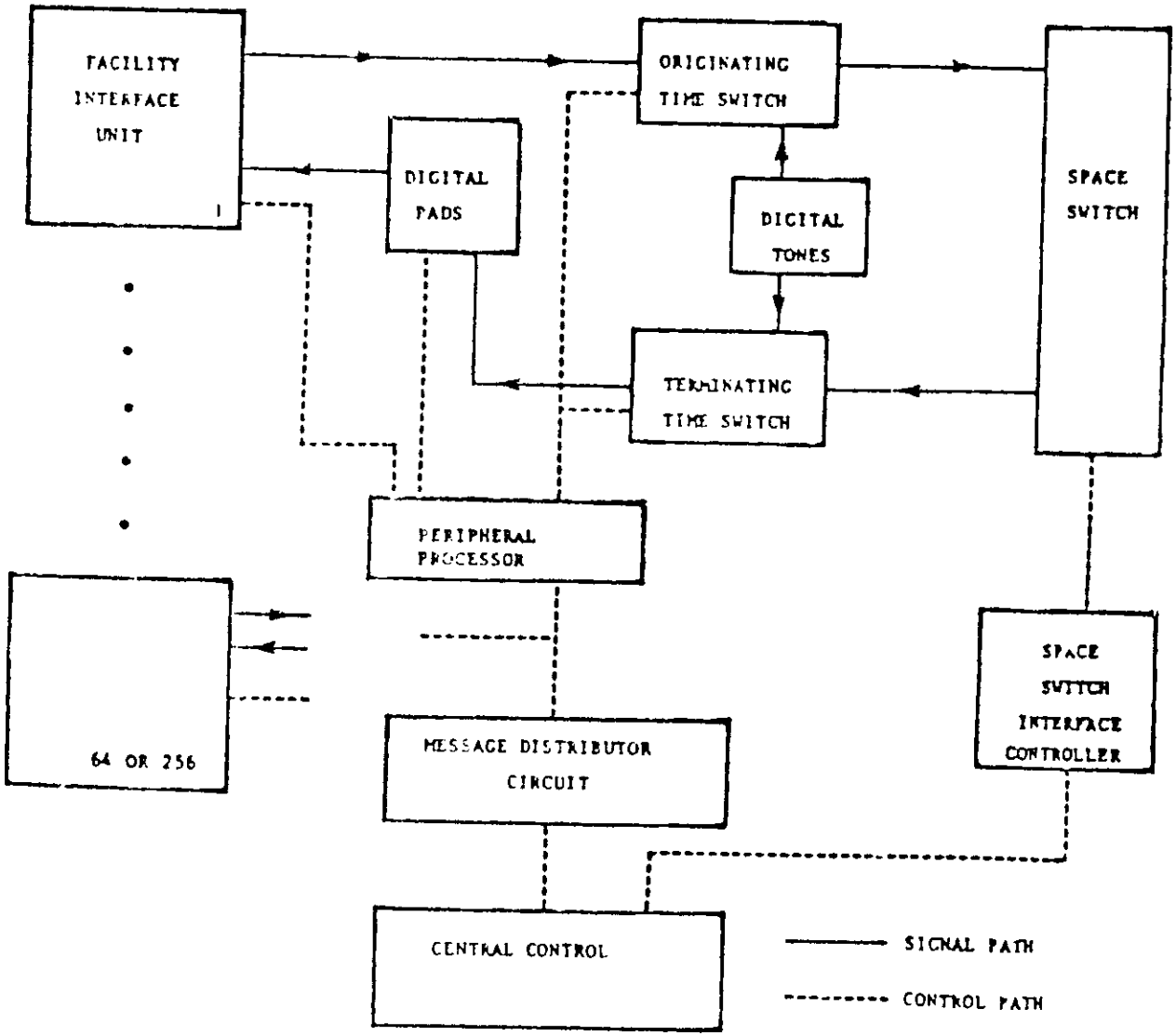


Fig. 12-9. GTE GTD-5 EAX simplified block diagram.

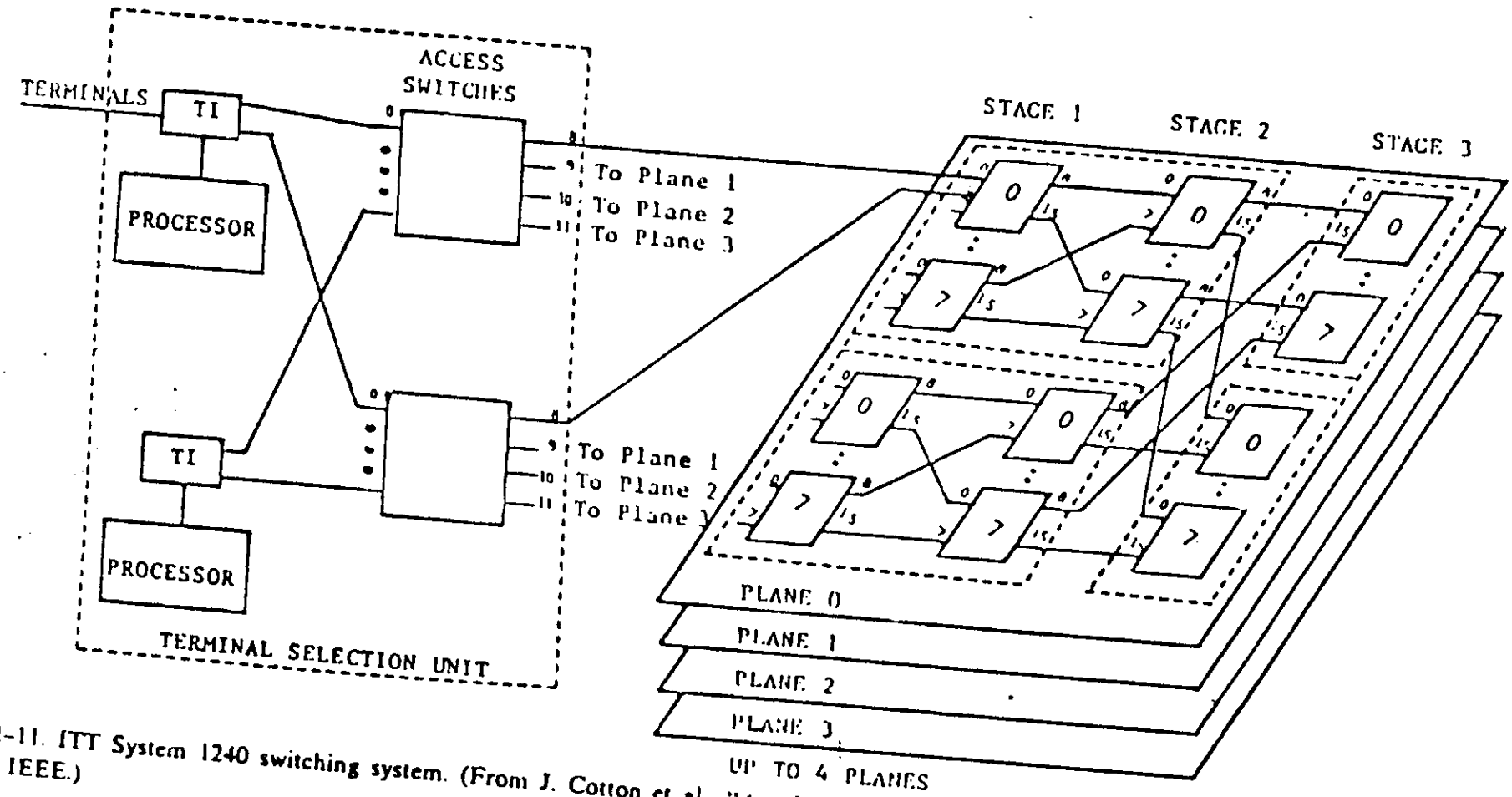


Fig. 12-11. ITT System 1240 switching system. (From J. Cotton et al., "An Expandable Distributed Control Digital Switching Network," '80. © IEEE.)

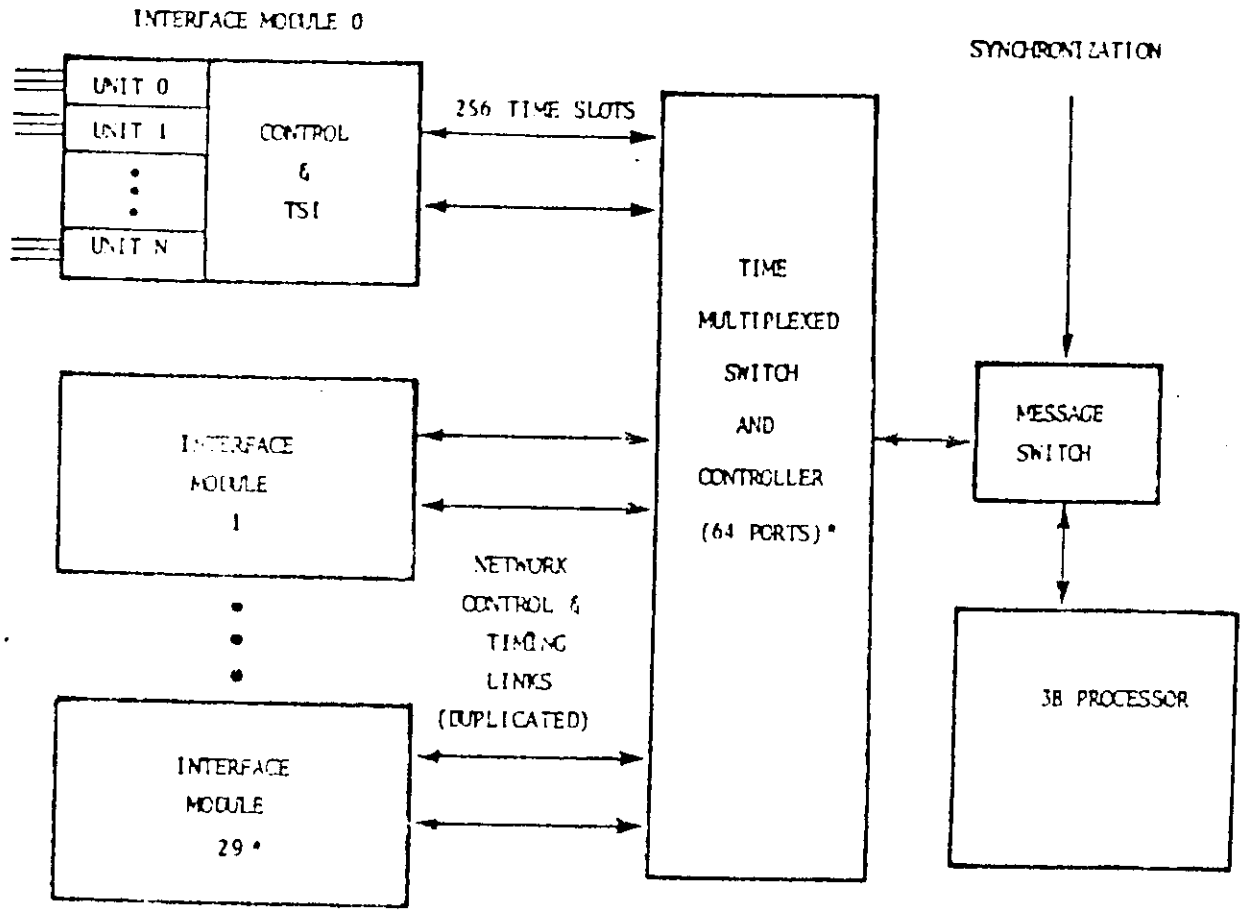
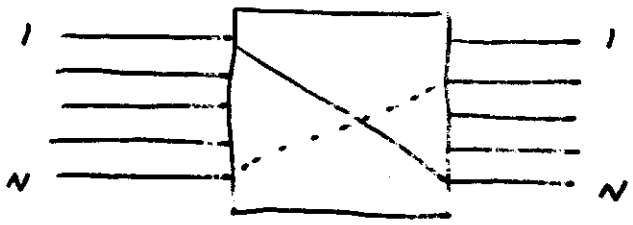


Fig. 12–10. AT&T No. 5 ESS switching system.

SWITCHING



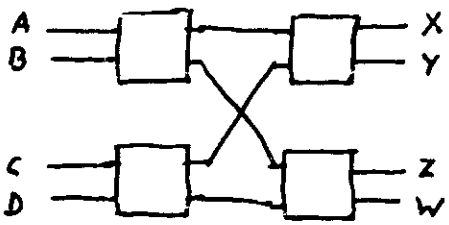
Interconnection in any random manner

$\frac{N}{2}$ to other $\frac{N}{2}$

$\frac{N}{2}$ Simultaneous connections without any restrictions

NON-BLOCKING SWITCHING

Electromechanical switching - Blocking inherent
∵ large switches are built from small modules



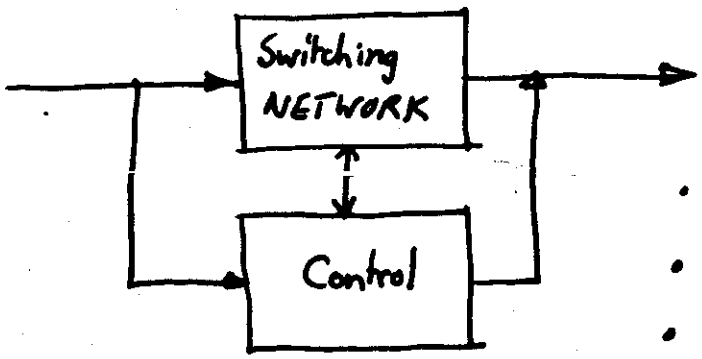
When B is connected to Z
A cannot be connected to W

For 1000 line switch $\sim 10^6$ relays would be needed to build a fully non blocking switch - highly impractical

Single stage and multistage switching
Telephony Traffic theory / Traffic engineering
Relays, Crossbars and semiconductor gates (analog, poor isolation)

Electromechanical Devices: Reliable but need constant maintenance
cleaner environment
Large Space, power
Most important Blocking
End to End path exist → SPACE SWITCHING

Basic Functions of a Switch



- Receive "Signals"
- Perform Interconnection
- Send "Signals"
- Supervision and Monitoring
- Charging, Administration, etc

- Signalling : (SERVICE CIRCUITS)
  - Receive Dialled Digits / Tones
  - Send Dialled Digits / Tones
  - Send / Receive signals to other exchanges

- Interconnection (NETWORK)
  - Connect the incoming line to the desired outgoing line

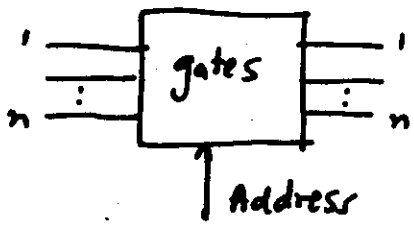
- CONTROL
  All the processing, Real Time and non RT fns.

Older systems : Strowger, step by step : distributed control and switching but v poor control. limited facilities
Crossbar : Centralized Control
- Highly optimized
- v poor overload handling

Electromechanical devices : Fully hardware oriented
optimization → saving hardware
Systems difficult to adapt to high traffic conditions

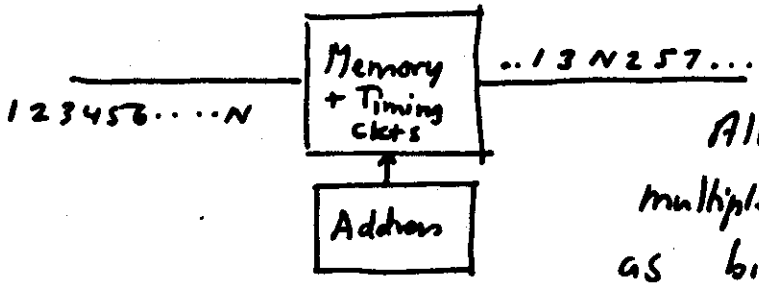
DIGITAL SWITCHING

- Here two modes are possible :
  - CONVENTIONAL SPACE SWITCHING USING GATES
  - TIME SWITCHING USING GATES AND MEMORIES



Space switch : ok for small n, number of gates too large for even reasonable n.

- Better, cost effective mode is TIME SWITCHING



All channels are time multiplexed and hence arrive as bit streams with channel numbered (addresses) by their time of arrival. Switching amounts to changing the bit sequence or performing a permutation operation. Implementation is simple :

- All incoming bits are stored in a sequence as they arrive in a memory called the buffer memory
- Bits from this memory are read out in a sequence as desired by the connection table (which provides the readout addresses to the memory)

IF CHANNEL 3 IS TO BE CONNECTED TO 5, THEN IN THE TIME SLOT OF 3 READ OUT CONTENTS OF 5 AND IN TIME SLOT OF 5 READ OUT THE CONTENTS OF 3.

ADVANTAGES OF DIGITAL SWITCHING

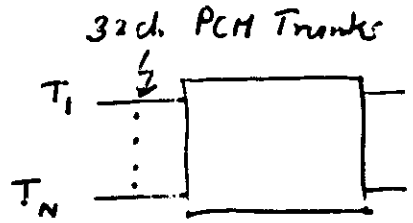
- COMMON TECHNOLOGY / MODULES
  100 CH ⟶ 100,000 CH SWITCHES
- FEWER PART / PCB TYPES
  EG. ONLY 30 PCB TYPES FOR AN ENTIRE FAMILY
- LOWER AND LOWER COST
- LOWER POWER. WITH CMOS TECHNOLOGY
  SYSTEMS NEED LESS AIRCONDITIONING
- VERY HIGH RELIABILITY
- LESS SPACE
- BETTER MAN MACHINE COMMUNICATION /
  FAULT DIAGNOSIS AND ISOLATION
- EASE OF DUPLICATION / REDUNDANCY
- EASY TO MAINTAIN, OPERATE AND MANUFACTURE
- COST EFFECTIVE RURAL COMMUNICATION
- REMOTE MAINTENANCE AND CONTROL
- IMPLEMENTATION OF MESSAGE BROADCASTING /
  VOICE MESSAGING IS EASIER
- SERVICE CIRCUITS, TONE GENERATORS,
  ANNOUNCEMENTS FAR EASIER TO IMPLEMENT

SWITCH ARCHITECTURE

- A 1000 channel switch requires only a few chips
- Memory oriented – Exploitation of VLSI technology
- Synchronization and timing ckts are important

Limiting factor: Memory cycle time

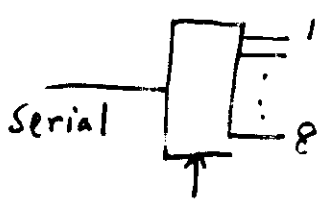
Basic idea of time switch: In a sampling time of 8 kHz i.e. 125 μs the switch must receive speech samples from all the subscribers connected to it and send out an equal number



For 1000 ch., N = 32

32 ch → 2.048 Mbps ~ 4 μs per channel
~ .5 μs per bit

In order to save time handle all 8 bits of a channel in parallel.



A number of tricks are done to overcome timing problem. In 4 μs one must read all 32 lines and also send out data on outgoing lines.

- 32 read and 32 write cycles
- Read all 32 in parallel but Read out in required manner 32 + 1 memory cycles.
- Duplication of hardware

- Using fastest chips "All Time Switches" upto 4 channel 8000 ch capacity have been built (CMOS – ECL – etc.)