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Brief Resume of Aspects of

VLSI FABRICATION TECHNOLOGY AND SOME TRENDS TO THE FUTURE

Lecture No. 1

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Brief Resume of Aspects of

VLSI FABRICATION TECHNOLOGY AND SOME TRENDS TO THE FUTURE

Mino Green

Lecture No. 4

This is the last lecture in this brief series and while I wish to continue talking about the elements of the VLSI fabrication process, I also wish to mention those topics in fabrication which are either just being used or are going to be used in the future. So this is even more of a mixture than you have had so far!

IV.1 TRENDS IN VLSI FABRICATION TECHNOLOGY

As stated earlier there is always the push to decrease feature size, increase speed, increase complexity. This is illustrated by the curve shown in Fig. IV.1; in which we see that the 10 Megagate memory is upon us. So what are the trends in silicon fabrication needed to satisfy future expectations? We should consider some of the following:

a) Scaling rules and FET design. At greater than 1μm S/D separation there has been a tendency to use constant-field scaling. However, with submicron devices there is some push towards other scaling rules, such as shown by McNelly (Vol 21 p3) in Table IV.1.

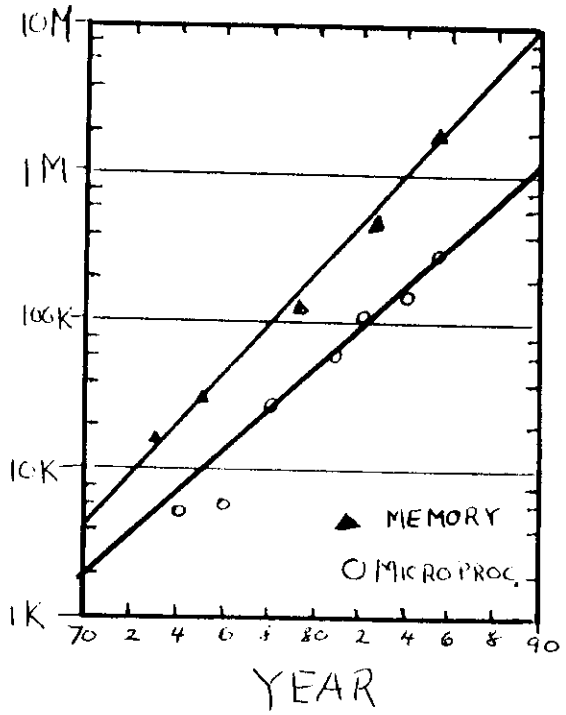


FIG IV. 1 INCREASING CHIP COMPLEXITY (© IEEE 1986, Vol 20 VLSI Electronics Microstructure Sci.)

Table IV.1 : Scaling MOSFETs

Parameter	Constant-field scaling[a]	Constant-voltage scaling[a]
Lateral dimensions	K	K
Vertical dimensions	K	K
Device area	K^2	K^2
Gate oxide thickness	K	K
Junction, well depths	K	K
Doping concentrations	1/K	$1/K^2$
Threshold voltages	K	1
Supply voltages	K	1
Resistivities	K	K^2
Resistances	1	K
Current/device	K	1/K
Power/device	K^2	1/K
Chip power density	1	$1/K^3$
Dielectric capacitances	K	K
Gate delay	K	K^2
Delay * power product	K^3	K

[a] K, device scaling factor

Keeping the voltage, V_{DS}, at a constant value has external advantages but does cause internal problems like hot electron effects.

FET designs to cope with small S/D values involve grading the pn junctions in the S/D regions. Thus the polycide process considered recently has been modified to give a graded pn junction to decrease field gradients. Using the polycide process in conjunction with both n^+ – and p^+ polysilicon is a coming process: to avoid work function differences which can make turning off FETs difficult.

b) Isolation. We have looked at LOCOS as a device isolation methodology. At submicron levels LOCOS is too rough.

c) Lithography. Here we have the position that while optics is not at the limit yet, the future looks as though either X-ray lithography or a mix-and-match of optics and direct e-beam writing will come in.

d) Ion implantation. We have not discussed ion-implantation yet it is an area under constant development as specialized doping requirements come, e.g. BICMOS.

e) Dielectrics. Low temperature processing and multilevel metallizations make dielectric development very important. Both organic - polyimides, and inorganic - spin on glasses, are being experimented with.

f) Interconnects. This is a large and complex problem involving multilevel metallization. Optical interconnects are being considered for chip-to-chip links and even intra-chip links.

g) Mounting and Packaging. As the number of input/output pins per chip increase, so the challenge of chip mounting increases. Tape automated bonding would appear to be the technology that will cope with the immediate needs of the industry. But this is an area of great importance - and cost - which is in a state of rapid change.

h) Semiconductor Material. This has been a course about silicon, but there are some advantages in other semiconductors, e.g. those based on III/V compounds, such as high electron mobility for high speed devices and OPTO-ELECTRONIC capability. This is an important and rapidly growing area.

Now let us consider several of these topics in a little more detail.

IV.2 ISOLATION

You have considered LOCOS as the isolation method of VLSI, but it is rough and does take up a lot of room by virtue of the bird's beak effect. A method which is more comparable with the submicron challenge is sidewall masked isolation (SWAMI). The LOCOS and SWAMI methods are compared in Figure IV.2, and Table IV.2.

Table IV.2 : SWAMI Process Steps

a)	1.	Grow stress relief oxide (SRO I)
	2.	Deposit silicon nitride (nitride I)
	3.	Pattern island regions (masking)
	4.	Plasma etch Si_3N_4 and SiO_2
	5.	Plasma etch silicon step
b)	6.	Grow stress relief oxide (SRO II)
	7.	Deposit Si_3N_4 (nitride II)
c)	8.	Plasma etch nitride II
d)	9.	Grow isolation field oxide
e)	10.	Strip Si_3N_4 (wet etch)
	11.	Deposit and densify LPCVD SiO_2
	12.	Etch back SiO_2

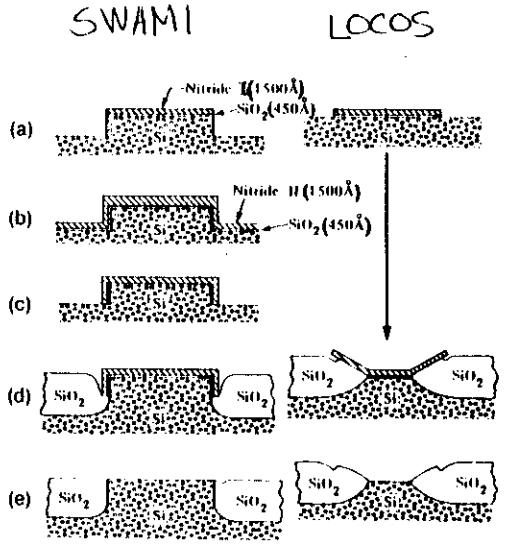


Fig. IV.2, Schematic sequence of the SWAMI process, compared to the conventional semi-recessed LOCOS process. (From Chiu *et al.* . Copyright © IEEE, VOL8 p500)

Even greater isolation is obtained by etching deep narrow trenches in the silicon, e.g. 5-6μm deep 1μm wide and filling the trenches with CVD silicon dioxide.

IV.3 LITHOGRAPHY

Mask and light as used in lithography is a parallel process which makes for fast wafer processing, essential if the price is to be kept low. Decreasing wavelength, e.g. excimer lasers, will allow submicron feature sizes to be fabricated, but the decreasing depth of focus of the optical system places severe constraints on the opto/mechanical system. Two strategies are considered. Firstly, mixed optical and e-beam lithography and then X-rays.

Typically a submicron gate might cover an area of .3μm^2 while the gate density might result in a figure of about 100μm per gate, so that only a few percent of the wafer needs to be processed at submicron feature size. If this is true and we can align the e-beam writing in step-and-repeat to an optical stepper, then it should be possible to achieve submicron gates, by e-beam writing, at reasonable throughputs, e.g. 5 minutes.

An extreme example of a small gate FET is shown in Fig. IV.3

X-ray lithography is being pursued vigorously in both Germany and the United States since it is a solution to the problem of diffraction limited optics. The wavelengths of easily generated X-rays vary over the range 4-50Å so that lithography down to very small sizes might be contemplated. X-ray lithography uses proximity printing, in which the mask is held a short distance above the plane containing the x-ray photo-resist. This is a near-field pattern situation. Since we are dealing with s-rays, no lenses, mirrors etc. can be used. We are thus dependent on either parallel light or a "point-source" in order to limit penumbral distortion.

X-ray sources come in three kinds. There is the well known electron beam striking a metal target. Typical source power dissipation is 4kW with poor conversion efficiency of 4.8×10^{-4} and spot size 3mm. There is synchrotron radiation which gives nearly collimated radiation of high energy (10-50Å). The disadvantage at this moment being cost. Finally there are plasma sources, created by high power lasers or electric discharges, in which the electron temperature is raised to very high values (40 million Kelvin!)

The mask material, material of support and wavelength of radiation are intimately interlinked. Fig. IV.4 shows some important curves. It should be noted that the most absorbing materials have an adsorption coefficient that is only fifty times larger than the most transparent materials. This then determines the constraint on the support material that will be used e.g. on its thickness, but does not determine the contrast. The support simply reduces the total intensity presented to the mask and the resist. The contrast is simply related to the (log) ratio of X-ray intensity at the masked and unmasked regions. A window of resonable compromise, amongst all the process restrictions, seems to lie somewhere between 5Å to 20Å in wavelength.

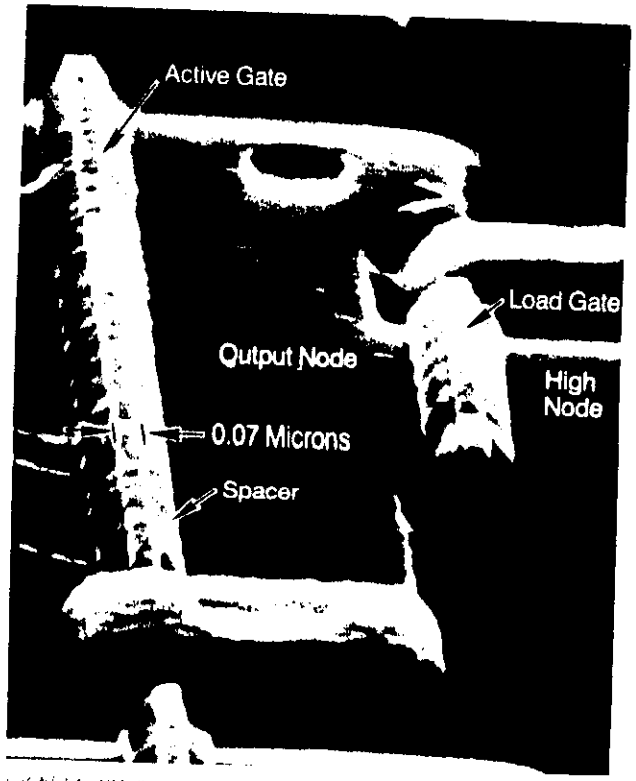


Fig. IV-3 An NMOS inverter with effective gate length of 700 Å for cryogenic operation at 4 V. Fabricated at IBM Watson Research Center by direct write electron beam lithography. (Courtesy of Dr. George Sai Halasz.)

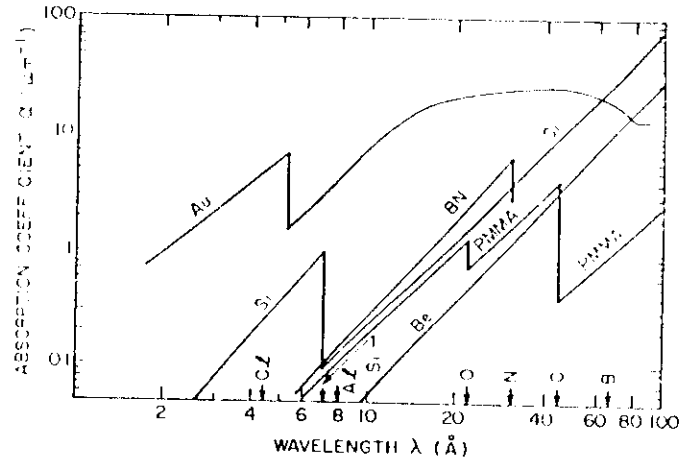


Fig. IV-4 Absorption coefficient versus wavelength for materials common to x-ray processing. Specific atomic absorption lines are indicated.

IV.5 ION IMPLANTATION AND ION BEAMS

Ion implantation (I-I) is the prevailing technique used to introduce desired impurities into the AEG region of silicon in a uniform, predetermined and reproducible way. The method consists in directing a broad beam of a selected high energy positively charged ionic species at the patterned wafer. The ions are implanted in the exposed areas of the wafer, be it in silicon or the poly, masking is done by photo resist, or in self aligned schemes by poly. Typical energies lie in the range 30 to 200KeV and beam currents of high current machines start at about 10ma.

The implantation process has been well modelled and a number of simulation packages are available. The most versatile tool is the computer programme TRIM (IBM). This is a Monte Carlo programme developed by Ziegler et al. It can predict range, longitudinal and lateral straggle, atom displacements and sputtering for all elements and for multilayer substrates.

There is a tendency now to use ion implanters for specialized tasks. On a practical basis low and medium energy implants are done on one machine (say up to 300KeV), while high energy implants MeV range require a more specialized machine. The BICMOS process requires high energy implants in the buried N^+ regions, cf Fig. IV.5.

Local doping can also be carried out with ion beam machines. These machines are also capable of ion sputtering of dielectric overlayers, of lithography of mask repair, etc. Fig. IV.6 shows in schematic form the essentials of a micro-ion beam system. A vital feature is the high brightness liquid metal (LM) field emission ion source. The trick is to find a liquid metal alloy eutetic which contains the ion-to-be-used but which is molten at a sufficiently low temperature so that the overall vapour pressure is compatible with high vacuum (say 10^{-6} mm Hg). Thus an alloy Au(82) Si(18) emits about 14% of its total flux as $^{28}Si^{++}$ and is used for doping GaAs. The melting point is 370°C. The other part of the trick is to have a submicron field-emitting tip of this molten alloy. Fortunately, the balance of electrostatic and surface tension forces on the meniscus of LM protruding from the end of a small nozzle results in a stable cone-shaped structure. Application of an electric field (positive tip) results in field evaporation of positive metal ions. In practice, a tungsten tube with a loose fitting tungsten needle is used; the liquid metal wets the tungsten needle and forms a cone over the needle tip which locates the ion source.

Slow but steady progress is being made with this field. It is, however, expensive and specialized, and implantation damage (which must be annealed out) must always be considered in any process methodology. Ions made using liquid metal ion sources are listed in Table IV.3.

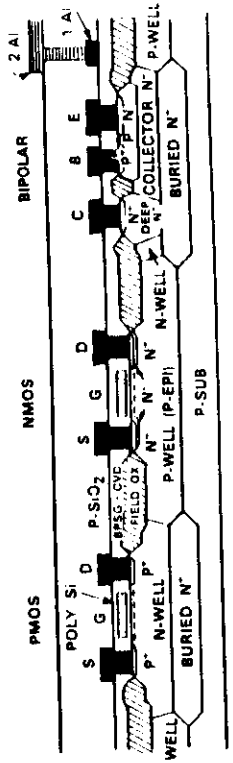


FIG IV.5 Cross section of devices formed by Toshiba BiCMOS process. Three additional masks (buried n^+, deep n^+ shinker, and p^- base) have been added to a CMOS process to optimize n-p-n transistor performance. (VLSI 81 p.[illegible])

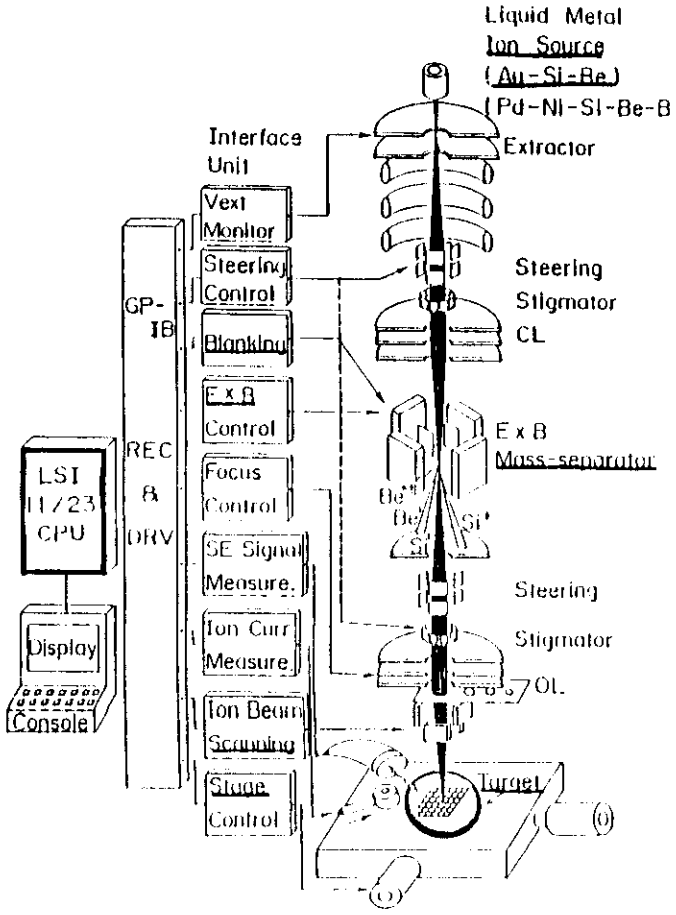


Fig. IV.11B system with computer control

Table IV.3 : Ions from Liquid Systems

Ion	Element or alloy
Be	Au-Be, Au-Si-Be, Ga-Si-Be, Pd-Si-Be
B	Pt-B, Pd-Ni-B
Al	Al
Si	Au-Si, Ga-Si-Be, Pd-Si-Be
P	Pd-As-B-P
Ni	Pd-Ne-B
Cu	Cu
Zu	Zn
Ga	Ga
Ge	B-Pt-Au-Ge
As	Pd-Ni-B-As-As-Sn-Pb, As-Pt
Pd	Pd-Ni-B
In	In
Sn	Sn, As-Sn-Pb
Sb	Sb-Pb-Au
Cs	Cs
Pt	Pt-B
Au	Au
Pb	Pb-Sb-Pb-Au
Bi	Bi

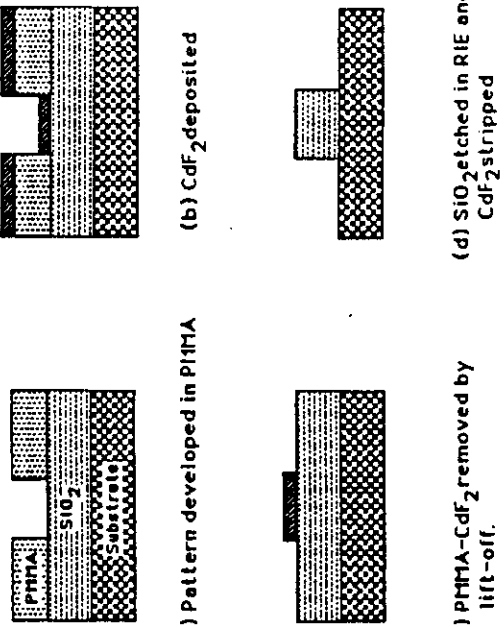
IV.6 MISCELLANEOUS TOPICS

As feature sizes get smaller, it is necessary, as we have seen, to revise a large number of process techniques. We end by mentioning two topics.

a) Pattern reversal with inorganic resists: Thin layers (ca 2000Å) of e-beam resist have now to be used. Unfortunately these materials do not have the selectivity in RIE that is needed. In order to overcome this difficulty, the highly resistive inorganic halides such as CaF_2, BaF_2, SrF_2, CdF_2 have been employed in the pattern reversal scheme depicted in Fig. IV.7. The CdF_2 is deposited by evaporation and the lift off is achieved using chloroform. The CdF_2 has a selectivity in RIE typically greater than 60, cf Table III.2. This technique has already, in my laboratory, given feature sizes of 1000Å.

There is a desire to achieve 100Å lithography, not for silicon, but for opto electronic devices employing the III/V compounds, and various "natural lithography"

FIG IV.7 Pattern Reversal using CdF_2



schemes have been suggested. Thus a single layer array of latex balls has been used to give triangular pillars of 300Å size. Surely very small features will soon be achieved.

b) Clean Rooms and in situ processing: In all that we have said it has been assumed that the fabrication is carried out in clean rooms by highly disciplined operatives. Clean conditions are the key to high yields. The size and number of allowable airborne particulates in the clean room is decreasing all the time. Class 100 is standard for 2–3μm feature size fabrication. The definition of class 100 is: 100 particles per cubic foot (28.3 litres) of $\frac{1}{2}\mu$m diameter or more. Class 10 and Class 1 were simply a reduction in particle count, not size. But Japanese manufacturers are now demanding (and, I suppose, getting) particle size of 0.1μm rather than $\frac{1}{2}\mu$m.

This concern with contamination has led to the idea of *in situ* processing. The principle underlying *in situ* processing is the replacement of current aligner based lithography by direct beam writing and local area beam induced layering, all done in one continuous ultra high vacuum system. An example of such a system, which has been built and operated, is shown in Fig. IV.8. This is certainly a topic which should generate much further discussion.

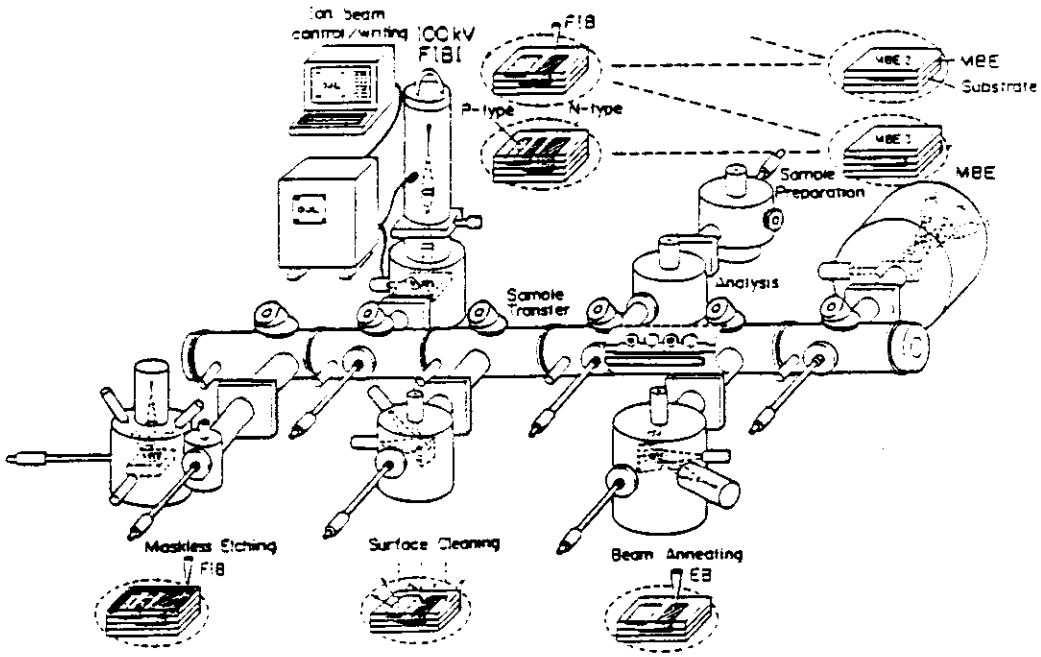


FIG.8 The ultra high vacuum in situ processing system composed of FIB doping MBE and etching.