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ICTP - INFN COURSE IN "BASIC VLSI DESIGN TECHNIQUES" 6 November - 1 December 1989

ADDITIONAL MATERIAL FOR LECTURES

by

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PROCESS FLOW
nMOS

1. Start with silicon wafer. (p-type)
2. Buffer oxide (ca. 200Å). } 1st layering
3. Si_3N_4 (oxidation mask, 800Å). }
4. Photo resist — FIRST MASK — <Active Area>
5. Boron I-I into exposed areas, p^+ doping.
6. Oxidation of p^+ areas to form FIELD OXIDE (0.5 - 0.9 μm thick) LOCOS (local oxidation process) } 2nd layer
7. Remove all buffer oxide and Si_3N_4 and thermally grow GATE OXIDE (250Å) → 3rd layer

8. Photo resist — SECOND MASK - <pulldown MOS>
9. Boron to delineated pulldown MOS. (II through gate oxide).

10. Photo resist. — THIRD MASK - <pullup MOS>
11. As or P to delineate pullup MOS.

12. Photo resist — FOURTH MASK - <buried contact>
13. [redacted] arsenic to make n^+ region.
14. Reuse of FOURTH MASK to make buried contact available (and oxide free).
15. LAYER IN n^+ POLY SILICON. (0.4 μm)

16. Photo-resist – FIFTH MASK – <gates, interconnections>.

17. The exposed Poly Si and gate oxide is removed. n^+ I-I carried out. The p^+ area under field oxide not doped only exposed active area doped in this self aligned step.

18. Exposed n^+ areas lightly re-oxidized.

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19. Layer with insulating oxide

20. Photo resist – SIXTH MASK – <vias>

Electrical contacts from buried contact layer and poly-Si to first metal layer.

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21. Layer with Aluminium.

22. Photo resist – SEVENTH MASK – <interconnects>

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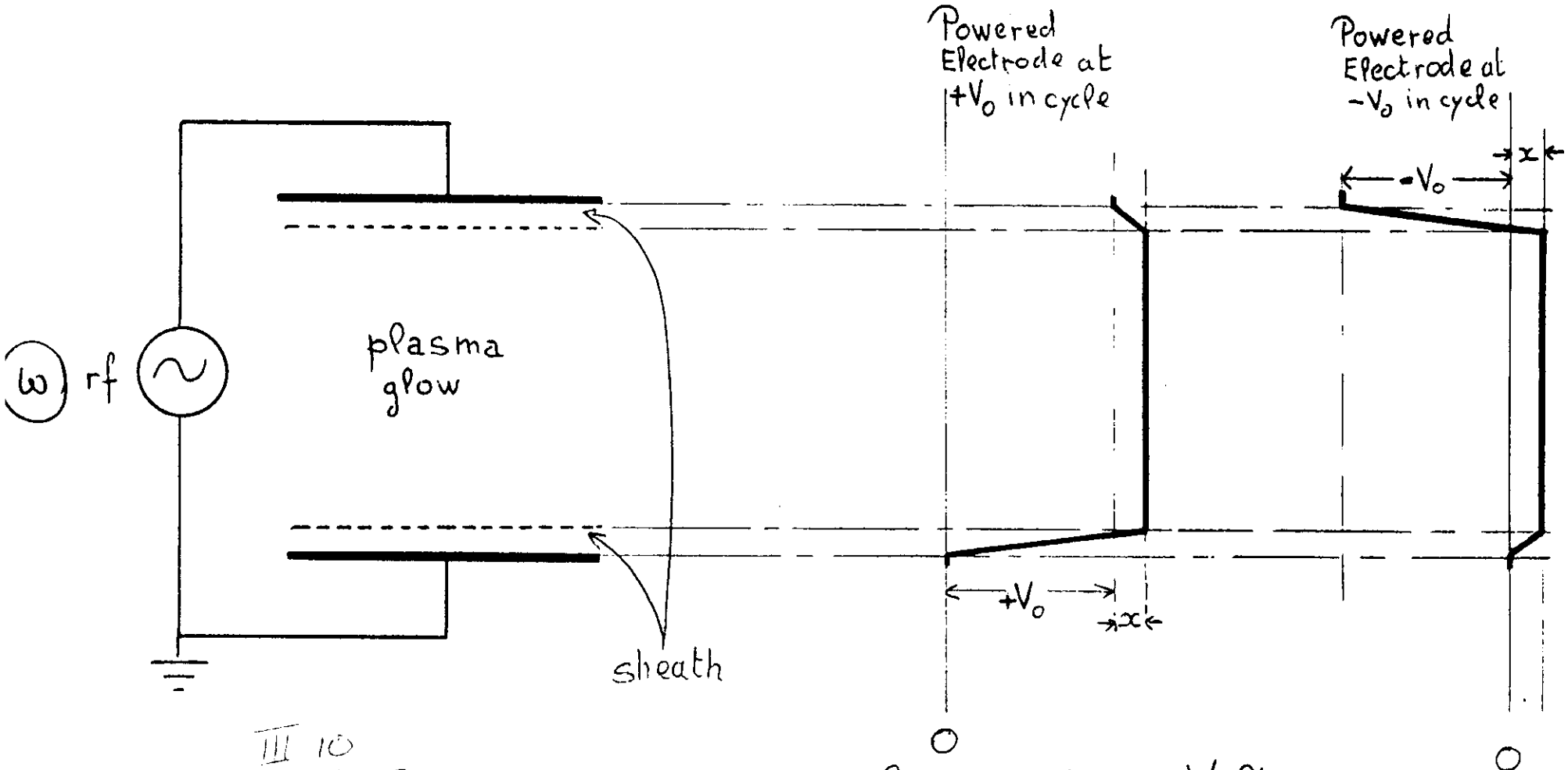
23. Layer with encapsulating over glass.

24. Photo resist. – EIGHTH MASK – <Pad areas>

Expose areas for wire bending.



III 10

FIG. ~~V~~ 2. Symmetrical parallel plate reactor. Voltage distribution shown for peaks in the a.c. excitation.