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COLLEGE ON
"THE DESIGN OF REAL-TIME CONTROL SYSTEMS"
1 - 26 October

DIGITAL SIGNAL PROCESSING

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1-26 October 1990

DIGITAL SIGNAL PROCESSORS

INTERNATIONAL CENTRE FOR THEORETHICAL PHYSICS

DIGITAL SIGNAL PROCESSORS

- **Digital Signal Processors are special purpose microprocessors optimized for the execution of digital signal algorithms. They are traditionally designed for performance, not extensive functionality nor programmer convenience.**

1. Historical evolution of DSP.

- 1stDSP	1978	AMI S2811
-	1979	INTEL 2920/21 (Telecom.)
-	1979	Bell Labs DSP1 (not mark.)
-	1980	NEC uPD7720
-	1980	Analog Devices ADSP-2100
-	1981	Hermes (not marketed)
-	1982	Hitachi 61810
-	1982	Texas 32010

The last line represents a great widening of the applicability spectrum due to external reprogrammability, ideal for low volume applications.

In the beginning most DSP's were distinguishable from other microprocessors due to their characteristics of:

1) Harvard architecture (separation between Program and Data memories)

2) internal and very small Program and Data memory area

3) small instruction sets, and mostly executable in one cycle (for this reasons similar to RISC)

4) special hardware units for treatment of digital signals (such as: parallel multiply, barrel shifting, auxiliary registers for single cycle manipulation of data tables, etc.)

Characteristics of different chips

2. Basic elements of a real-time processor.

- **ALU (one or more, for Addr and Data)**
- **(Floating Point Unit)**
- **Control Unit**
- **Program RAM or ROM**
- **Data RAM**
- **Parallel I/O Controller (DMA)**
- **Serial I/O Controller (DMA)**
- **(A/D and D/A Converters)**
- **Interrupt**

- **After performance comparison with other components it will become clearer why the DSP is more suitable for several types of applications.**

- **There are several ways to realize a concurrent system of many basic elements listed above, each one having a different throughput, privileging in one case one aspect respect to another**

- **The most important thing to do in selecting a component in a certain application is to know the characteristics of all the components that can solve the same problem in order to make balanced judgement.**

2.1. Characteristics of DSPs.

- **In recent years we see that the characteristics of the DSP's are improving very rapidly.**

- **no one features of the past was dropped** (hardware multiplier, special instructions, **etc.**)

- **in addition today's DSPs use** extensive pipelining, several independent memories with large address capability, parallel function units (one cycle floating point instruction), and hardwired design (**not microprogrammed).**

- **Applications in this field are increasing so rapidly that at present a classification among the hardware of the DSPs must be made (section 4).**

- **Among the several DSPs existing on the market today, I will describe one from the "General Purpose DSP family". Not with the intention to make any preferences, but just due to the fact that in the past I have used Texas and AT&T General Purpose DSPs, as example I will describe now the Motorola DSP96000.**

- **The best DSP for your application will certainly be the one that has the best rate performance/price.**

- Some of the characteristics that make DSP's particularly suitable to treat discrete signals are found in its instruction set.

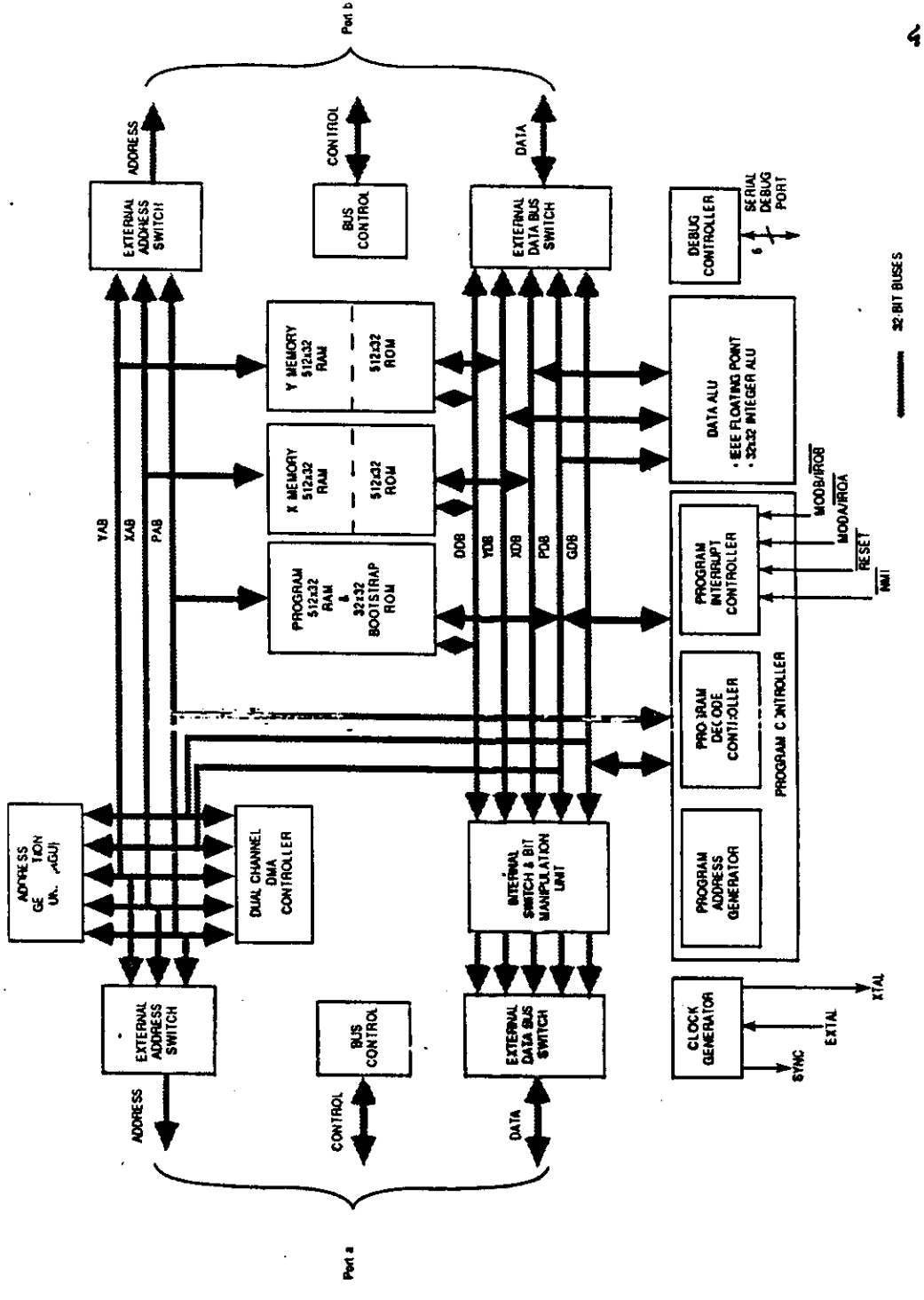
- Several presently available DSP's have hardware "DO LOOP" instructions,

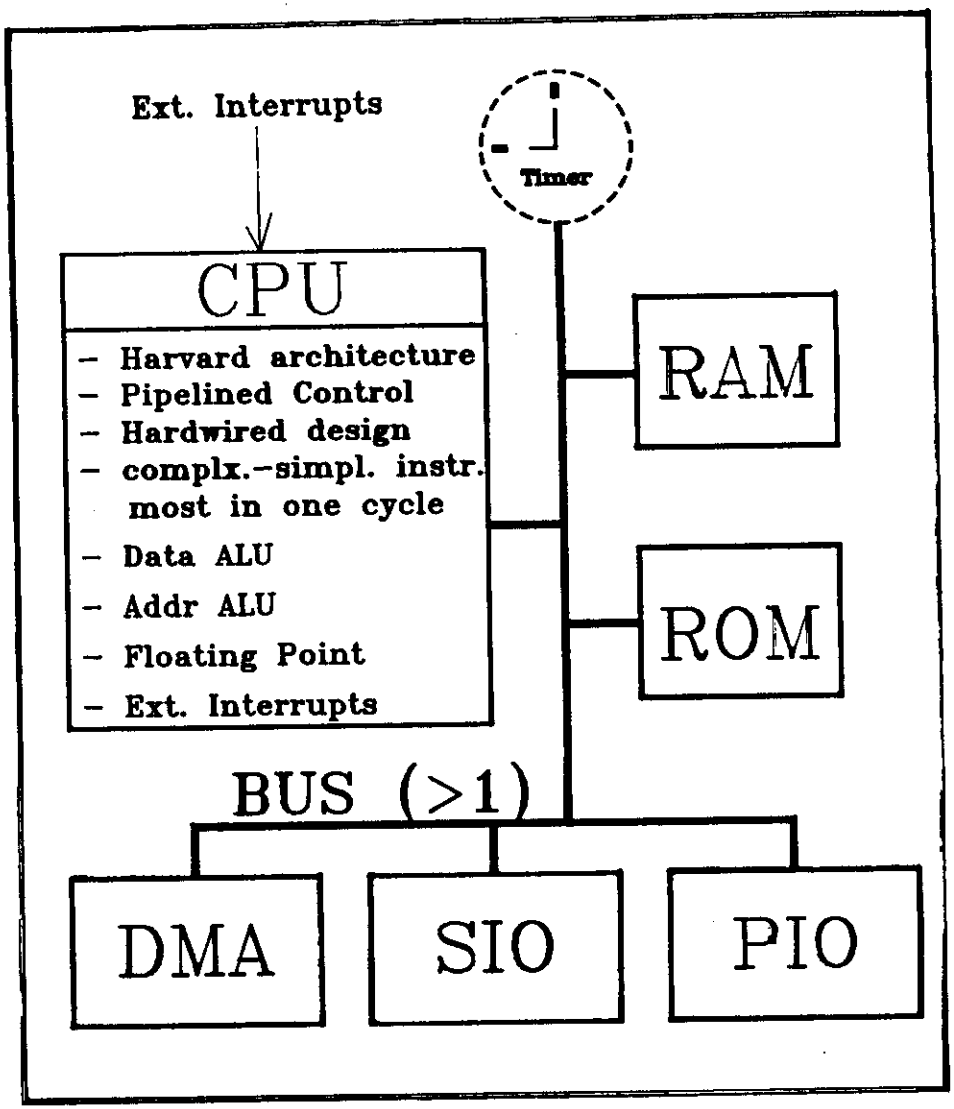
- have bit-reverse addressing

- can perform a simple operation y = ax+ b in one cycle (75 nsec) while at the same time performing some operations on addresses by updating pointers. E.g. a single line of assembly code of the Motorola DSP96000 (ideal for Butterfly FFT calculation),

FMPY D9,D7,D1 FADDSUB.S D5,D2 D4.S,X:(R5)+ Y:(R1)+,D7.S

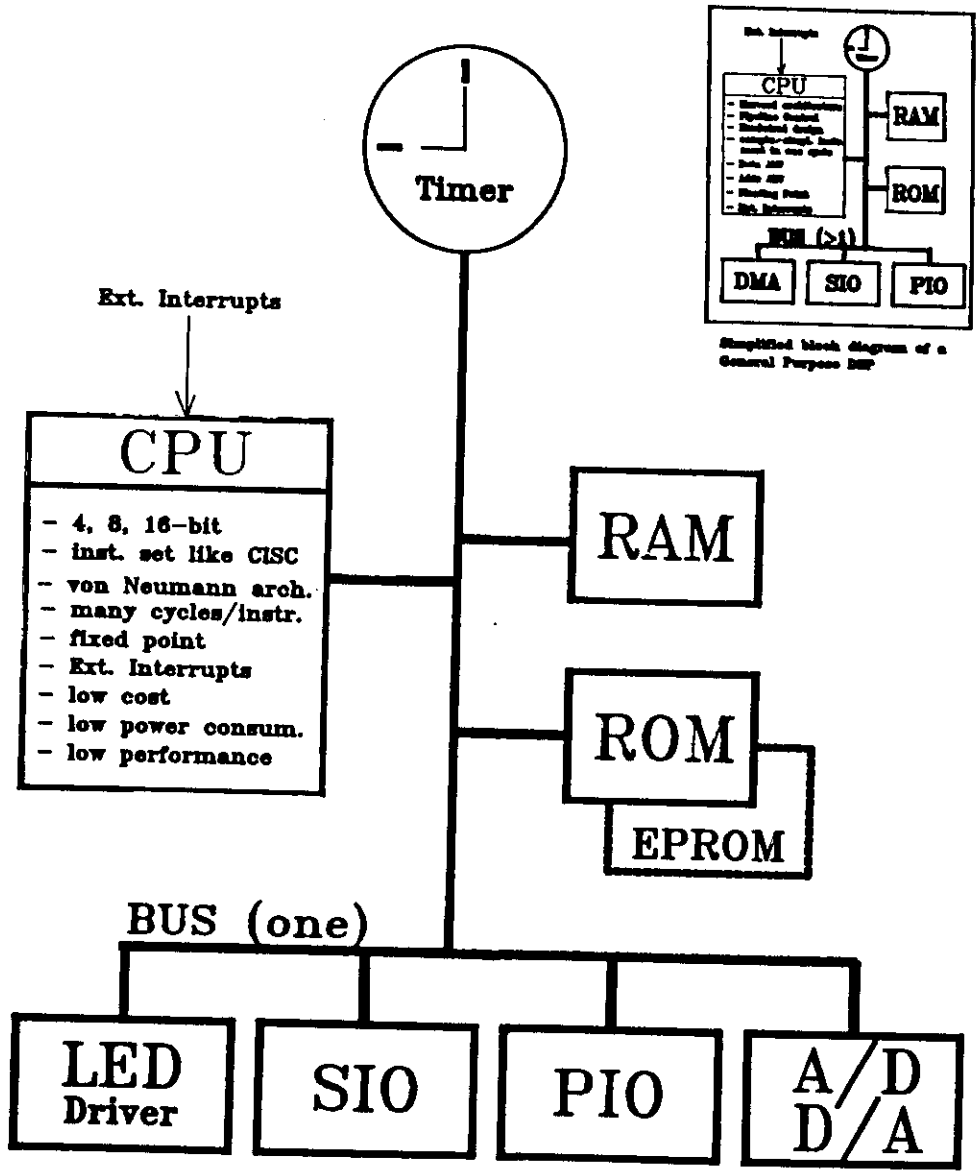
executed in one cycle, will generate the results of multiplication, addition, subtraction between two terms and will update the pointers to the data in the memory.





Simplified block diagram of a General Purpose DSP

MICROCONTROLLERS versus DSP



MICROCONTROLLER versus DSP

- A "microcontroller" contains all the necessary components of a complete system on one piece of silicon (E.g. Intel 8051, Motorola MC6804, MC6805, MC68HC11, etc.).

The microcontroller has less performance than a DSP, has 4, 8, 16-bit,

- has an instruction set more like CISC processor (using more then one cycle per instruction).

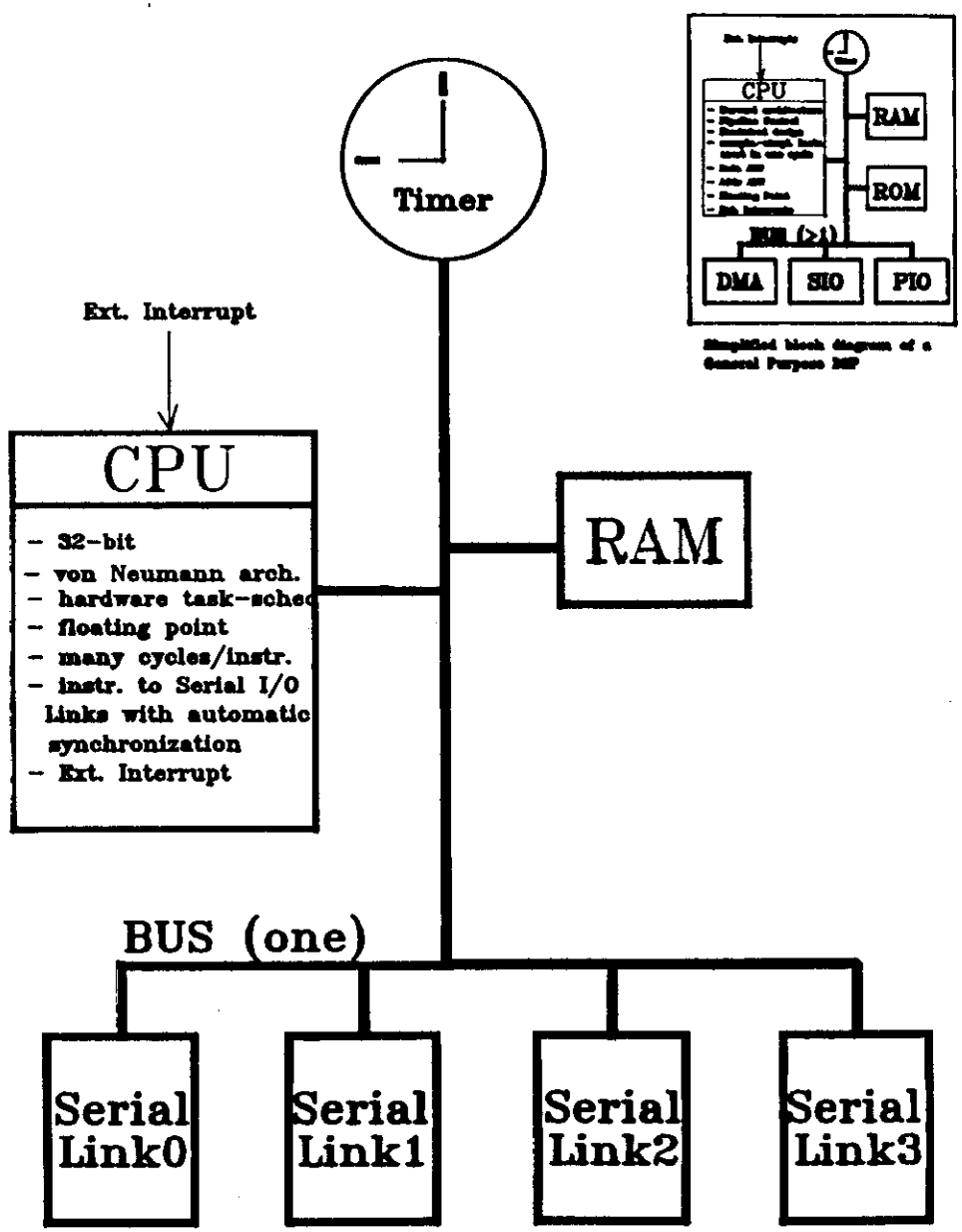
- has some extra programmable peripherals on chip, like A/D converters are not available on DSP.

- is not designed to build concurrent systems

- is intended to be used for economical applications in embedded systems where is necessary only to have the capability of one of the most common 8-bit or 16-bit microprocessor instruction sets.

Applications:
- industrial control, device controller (printers, plotters, etc.)

TRANSPUTER versus DSP



2.3. TRANSPUTER versus DSP.

- A Transputer contains in a single chip:
- an integer processor
- a Floating Point Unit
- 4 Kbyte of memory
- 4 high speed serial links (20 Mbit/sec)

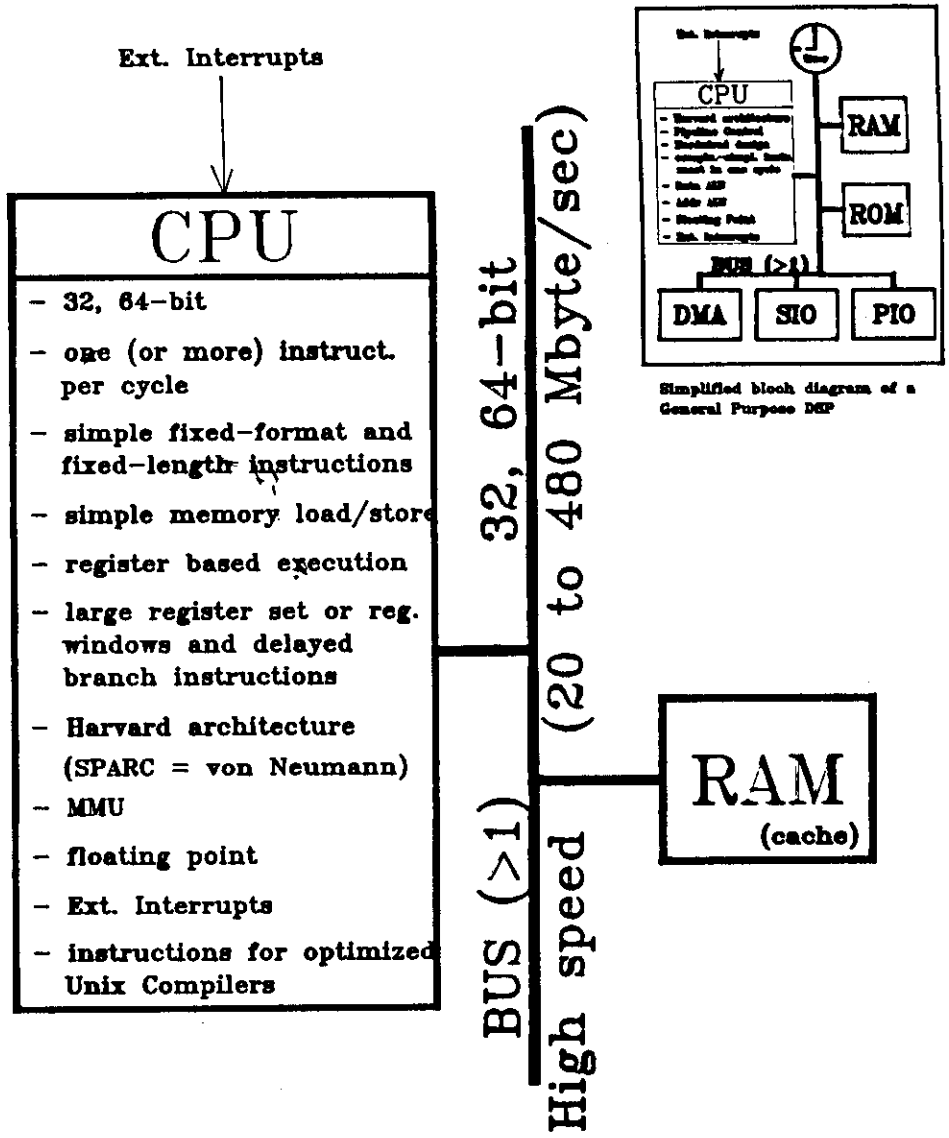
- Transputer is designed as a programmable component to implement a system with much higher degree of concurrency then is currently common.

The formal rules of Occam provide the design methodology for this family of concurrent systems. Special instructions divide the processor time between the concurrent processes, and perform interprocessor communication.

With the Transputer it is easier to build concurrent systems because of the good coordination between hardware and software (Occam), it is easy to transport software on different concurrent systems with different numbers of transputers.

DSPs have the performance of 20 to 40 Mflops, the T800 Transputer have 4.5 Mflop.

RISC versus DSP



Simplified block diagram of a General Purpose DSP

2.4. RISC versus DSP.

- Initial simple concepts of a register-intensive cpu design from Seymour Cray in 1960 for CDC 6600

- modern notion of RISC architectures emerged from John Cocke's project at IBM in 1970.

- Cocke's team goal was to design the best CPU architecture for an optimizing compiler,

1) the machine should be register-to-register with only load and store accessing the memory,
2) the architecture eliminated microcode and microsequencers in favor of simple, hardwired, pipelined, one-instruction-per cycle CPU design.

- RISC technology created an almost insatiable demand for memory speed.

1) The answer to this problem comes with high performance memory hierarchy, including general purpose registers and cache memories,
2) instruction set is regular and simple with few addressing modes: indexed and PC-relative.

- RISC variations from these common theme.

- IBM 1975 with 801 minicomputer
- BERKELEY 1980 with RISC I and RISC II
- STANFORD 1981 with MIPS
(Microprocessor Without Interlocked Pipeline Stages)

IBM and Stanford pushed the state of art in Compiler Technology to maximize the use of registers.

The BERKELEY team did not include compiler experts, so a hardware solution was implemented to keep operand in registers.

To optimize the task switching time they have defined many sets or windows of registers (global and local) so that registers would not have to be saved on every procedure call.

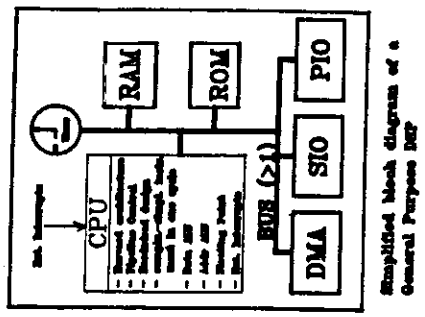
The disadvantage of register windows is that they use more chip area.

- Clipper recognize the growing memory bandwidth. Their solution was to separate instruction and data buses.

The MC88000 follows the dogma of simple, one-cycle, fixed-length instructions and load/store architecture.

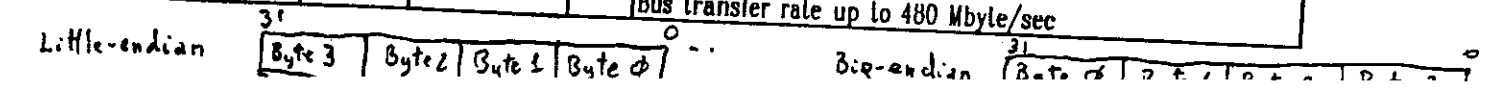
The MC88000 have the system's ability to incorporate new, specialized execution units.

CISC (CRISP) versus DSP



Other RISC's vendors: - MIPS and SPARC from Fujitsu, Bipolar Integrated Technology, Cypr LSI Performance Semiconductor, Device Technology. Acorn Sanyo for VL86C010. Hewlett-Packard with the Apollo Domain 10.000. AMD 29(family. HARRIS RTX2000 (highly integrated FORTH-executing microc troller).

Type	VLSI chips set	inst. per cycle	Clock rate	Architecture	Regs	Comments
CLIPPER	3	1	33 Mhz	Harvard	72	8k icache, 8k dcache Onchip 2 x 64 TLB
SPARC	6	1	33 Mhz	von Neumann	<520	Register windows and delayed branch instr. Need simpler compilers. Supports the Big-endian format
R3000	2	1	25 Mhz	Harvard	48	64k icache, 64k dcache. On chip 64 TLB. Clever Compilers.
29000	3	1	25 Mhz	Harvard	195	Microprocessor Without Interlocked Pipeline Stages. No Direct Cache support branch cache On chip 64 TLB
"8000	3	1	20 Mhz	Harvard	32	Special bit-field instructions. Division, SQRT op. Addr. 8 Gbyte for Oper. System, 4 Gbyte for user Supports Byte ordering formats: big-endian, little endian.
i860	1	3	30 Mhz	Harvard	64	Special instr. for graphic processing, 3D graphic Unit MMU (4Gbyte), FCU, FAU, FMU, 4Kb icache, 8k dcache Supports Byte ordering formats: big-endian, little endian
IBM RISC	7	5	30 Mhz	Harvard		CPU = 3 processors (ICU, FXU, FPU) Bus transfer rate up to 480 Mbyte/sec



2.5. CISC (CRISP) versus DSP

- CISC (Complex Instruction Set Computer) use a large amount of hardware complexity to provide high degree of instruction set capability.

-large instruction set (some very complex instructions)

- different length and execution time of instruction

- Instructions can manipulate bit, byte, word and long word.

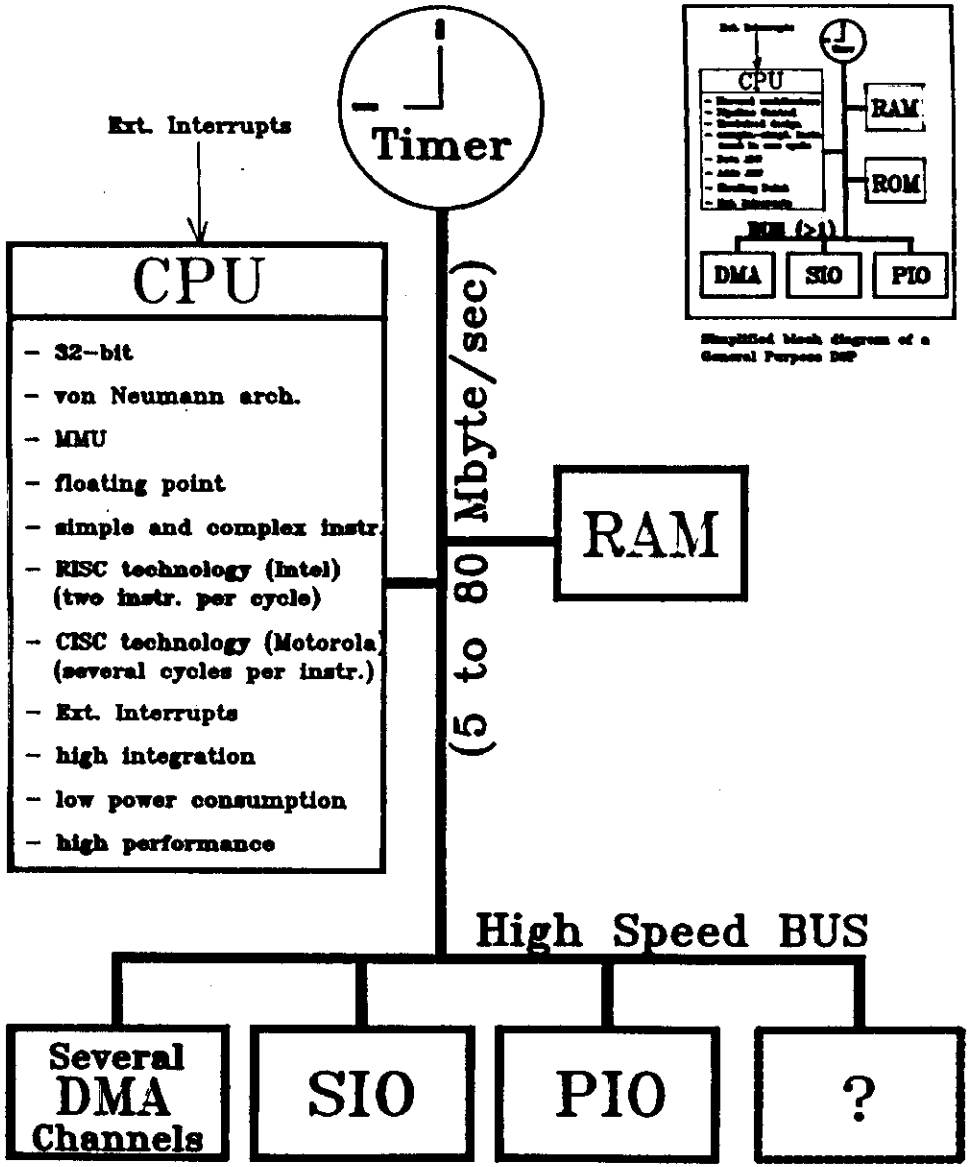
- The dynamic bus interface allows for simple, highly efficient access to devices of different data bus width.

- support, directly via BUS Monitoring, Multimaster and Multiprocessor applications.

- RISC and CISC may become more alike in the future. RISC is a technology, a philosophy of design, not a product. Some design techniques that have been applied to RISC machine can be applied to CISC architecture to improve performance.

- Processors like the 32532 with Intel 80486 and Motorola 68040, incorporate more RISC-like features to push the number of cycles for most of the instructions below 2. These new features will probably characterize the new type of processor as CRISP (Complexity-Reduced Instruction Set Processor)

High Performance
EMBEDDED CONTROLLERS versus DSP



High performance EMBEDDED CONTROLLERS versus DSP.

This architecture has been designed to meet the need of embedded applications (machine control, robotics, process control, avionics, and instrumentation).

- These type of applications require high integration, low power consumption, quick interrupt response time and high performance.

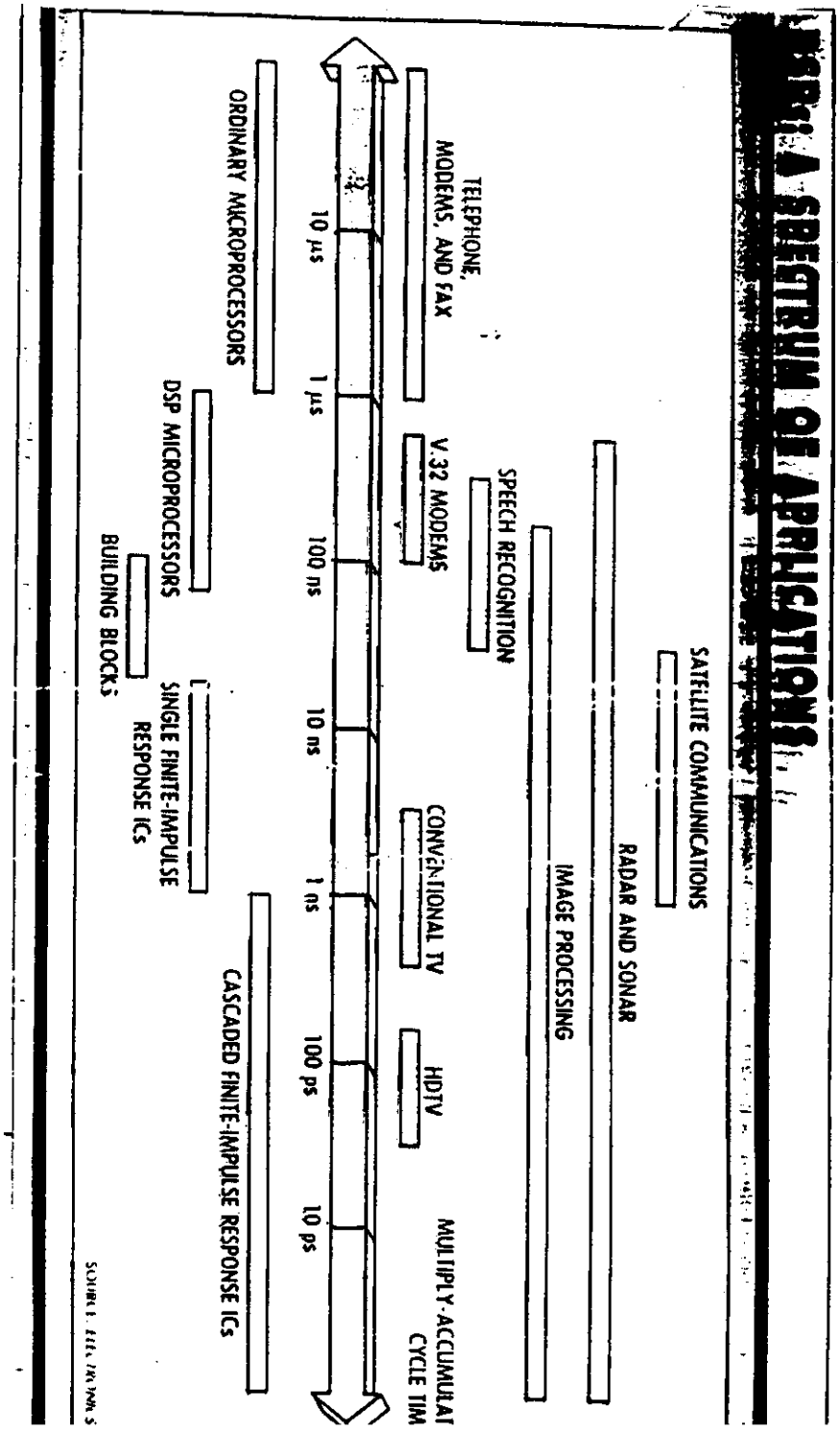
- Intel chips (80960) are based on a RISC core architecture. Each processor in the series will add its own special set of functions to the core to satisfy the need of a specific application or range of applications in the embedded market. For example, future processors may include DMA controllers, timers, or an A/D converter.

- other characteristics are: large register set, Fast instruction execution, load/store architecture, simple instruction format, overlapped instruction execution, integer execution optimization.

- The Motorola MC683xx family combines the high performance of M68000 family microprocessor with intelligent data-handling peripherals on a single chip.

- In one chip (32-bit) besides the CPU, there are: DMA controller, a timer module, a serial I/O module, a system interface module, and a 16-bit data port. Instructions are similar to the M68000 Family and need several cycles per instruction.

3 Future trends in microprocessors.



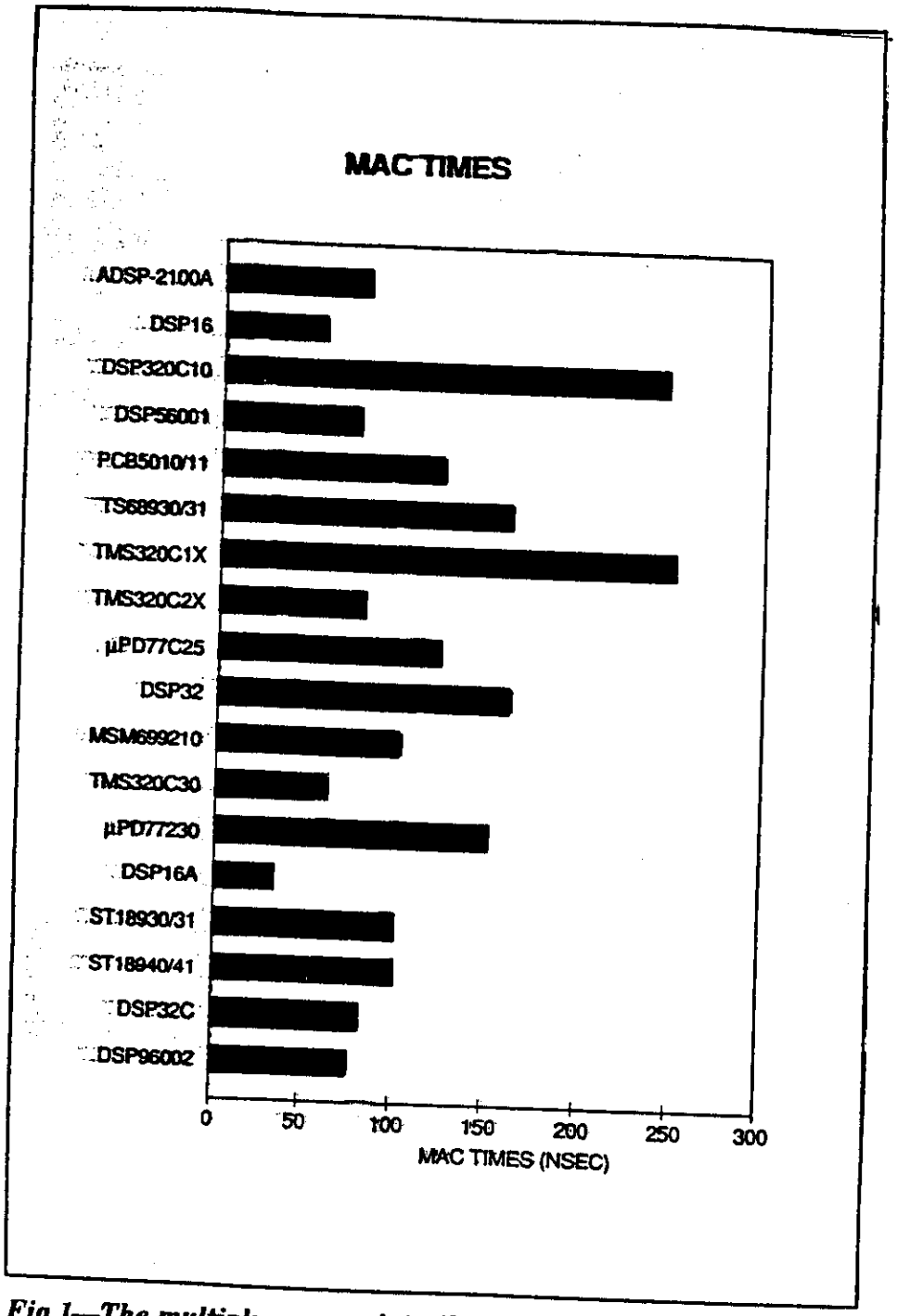


***Fig 1—The multiply-accumulate (MAC) times** for the DSPs match the execution times for the filters. Filters*

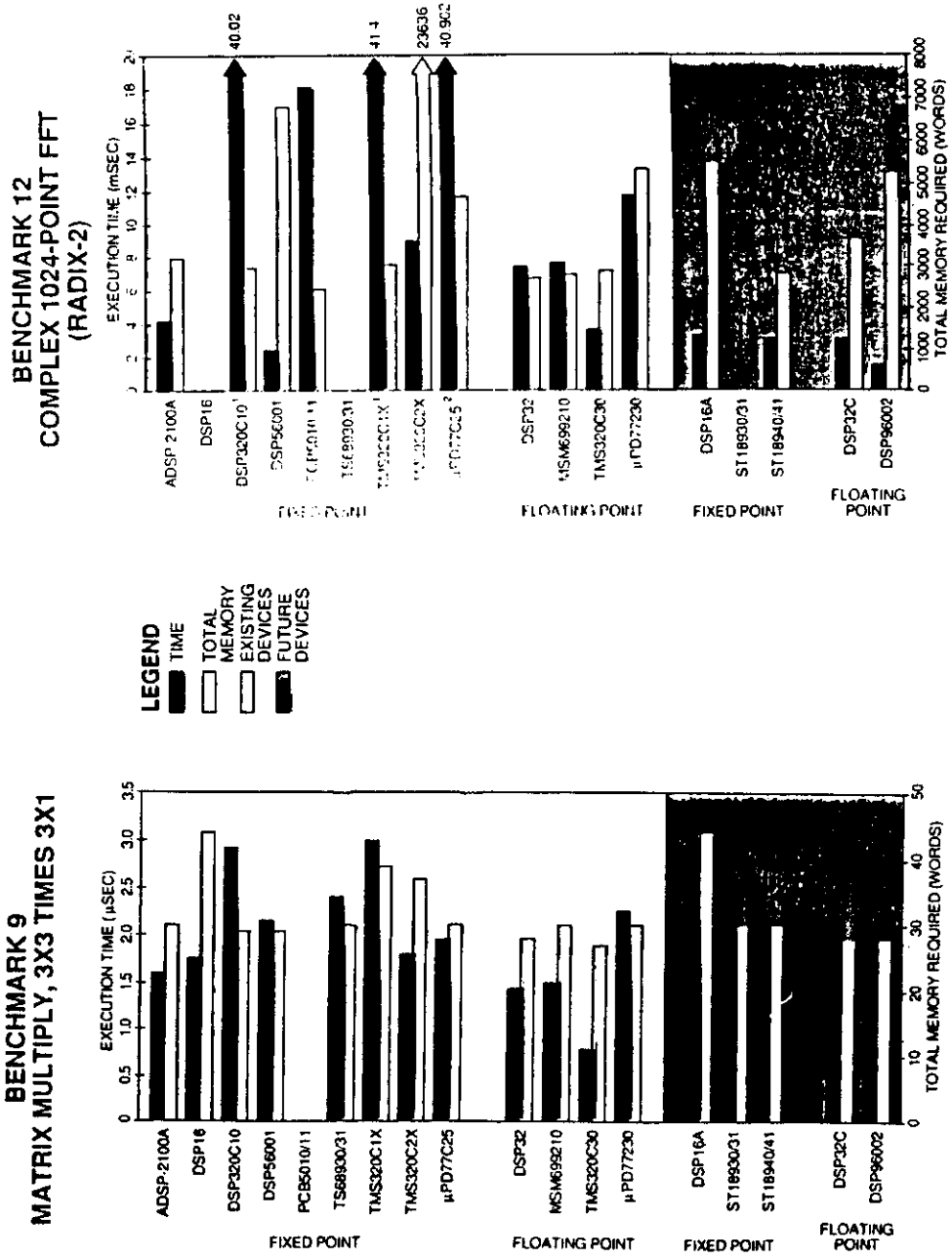


Table 2. Firm	Type	Tec. Cyc	I-s	P-m	D-m	Nbus	ALU	Other feat.
Analog Devices	ADSP2100A ADSP210x	CMOS 80 CMOS	24	32K	16K	1	16-Fix	
AT&T	DSP16 DSP16A DSP32 DSP32C	CMOS CMOS 15 CMOS 40 CMOS 20	 16 32 32	 2k	 4k	 2	 16-Fix 32-Flo 32-Flo	 SIO, PIO, DMA
Fujitsu	MB8764 MB87064	CMOS 100 CMOS	24	1k	1k	1	26-Fix	Like 8764 fewer-p
Hitachi	61810 DSPi	CMOS 250 CMOS 50	16 16				16-Flo	Fast I/O
Inmos	IMS-A100	CMOS 100	16				16-Fix	Filters
Motorol	DSP5600x DSP56200 DSP9600x	HCMOS 75 HCMOS 97 HCMOS 75	24 8 32	256 256 512	256 256 2k	7 1 8	24-Fix 16-Fix 32-Flo	Filters
Nation	LM32900	CMOS 100	28			7	32-Fix	
NEC	uPD7281 uPD77230 uPD77220	CMOS CMOS 150 CMOS 100	 32 24	 2k	 2k	 2	 55-Flo 24-Fix	Data Flow subset of 77230
Oki	6992	CMOS 100	22				22-Flo	
Philips	5010	CMOS 125	16			2	16-Fix	
Thomson	68931	CMOS 360	32				32-Fix	
Toshiba	6386/7	250	16				16-Fix	
Texas Inst.	TMS320C10 TMS320C25 TMS320C30	160 100	16 16 32	144		1	32-Fix 32-Fix 32-Flo	
TRW	TMC2310	50	16			1	16-Fix	
Zoran	34161 34322 35325	100 100 100	16 32 32			1	16-Flo 32-Flo 32-Flo	 IEEE-Flo

4. Classification of DSP hardware.

Among all the DSP chips available on the market there are four main classification of the hardware:

4.1. High performance general purpose DSP.

These processors have an architecture similar t an MPU/MCU, but in addition may include on chi multiplier, RAM, ROM, DMA, peripherals I/O hardware Do-loop, pipelining and several interna and external busses.

Some examples of these DSP types are:

- AT&T DSP16, DSP16A, DSP32, DSP32C
- Motorola DSP5600x, DSP9600x
- Texas TMS320Cxx
- Analog Devices 2100.

4.2. Algorithm specific DSP.

The architecture is configured for the optimum processing of a specific algorithm.

Among the DSP types designed for executing digital filter algorithms (FIR, IIR) there are: INMOS A100, LSI64240, Motorola DSP56200

Among the DSP types designed for executing FFT there are: TRW2310, HDSP66110, UT69532, Zoran.

4.3 Application specific DSP.

This type of DSP's are designed to implement specific applications such as a modem or voice encoder/decoder.

4.4. Building blocks

Multiplier, adder, registers, RAM, ROM, I/O peripherals, etc. can be used as building block components to configure a complete DSP system with very high performance but with higher costs. (E.g. MaxVideo)

6. DSP software support.

- Assembler language may be convenient to optimize a fast algorithm, but is a limitation for large programs. The principle firms: AT & T, Motorola, Philips and Texas Instruments are already providing "C" compilers for their DSP's.

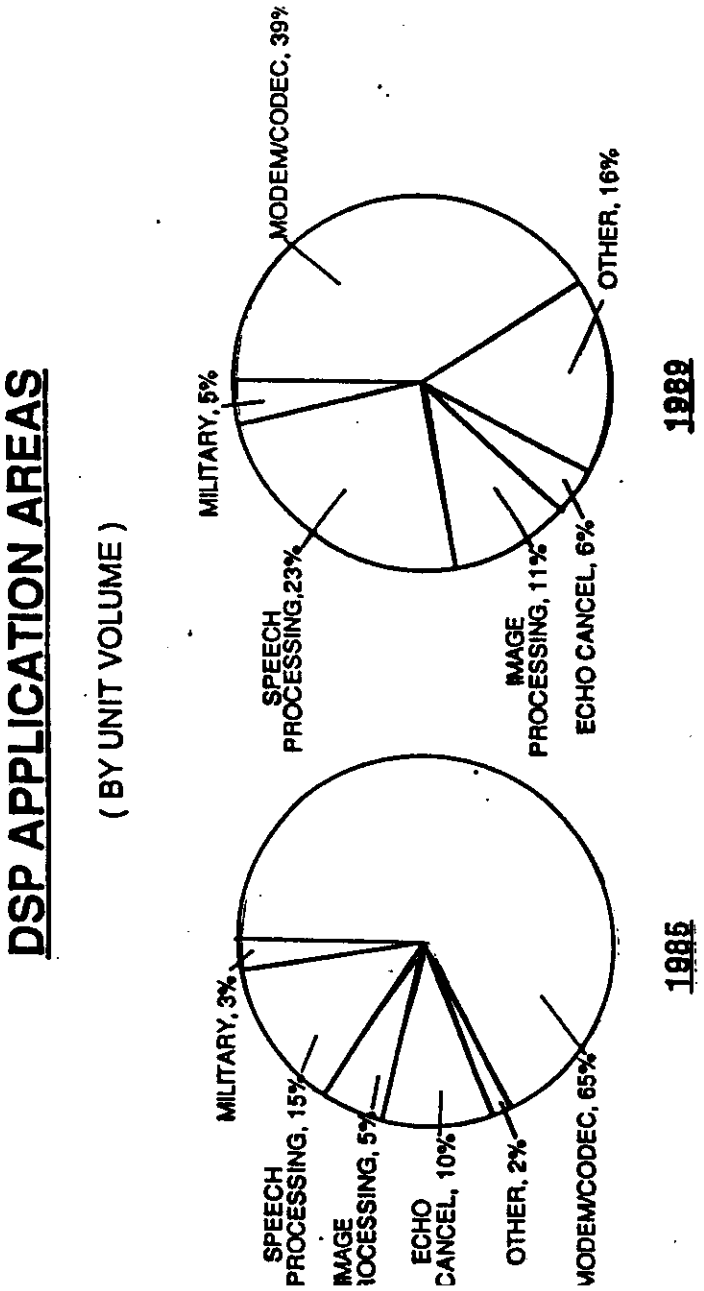
- Software development support is given by the firms themselves and also by:

- TEKTRONIX that offers the Signal Processor Workstation (SPW) that runs on VAX or Apollo Computer Domain.

- DATACUBE offers Euclid Tools and DSP-1000

- DSP Development introduced DADiSP which is a menu driven software for displaying and analyzing digital waveforms.

- STEP Engineering offers Step-4 SDT running on IBM PC AT
- BURR-BROWN



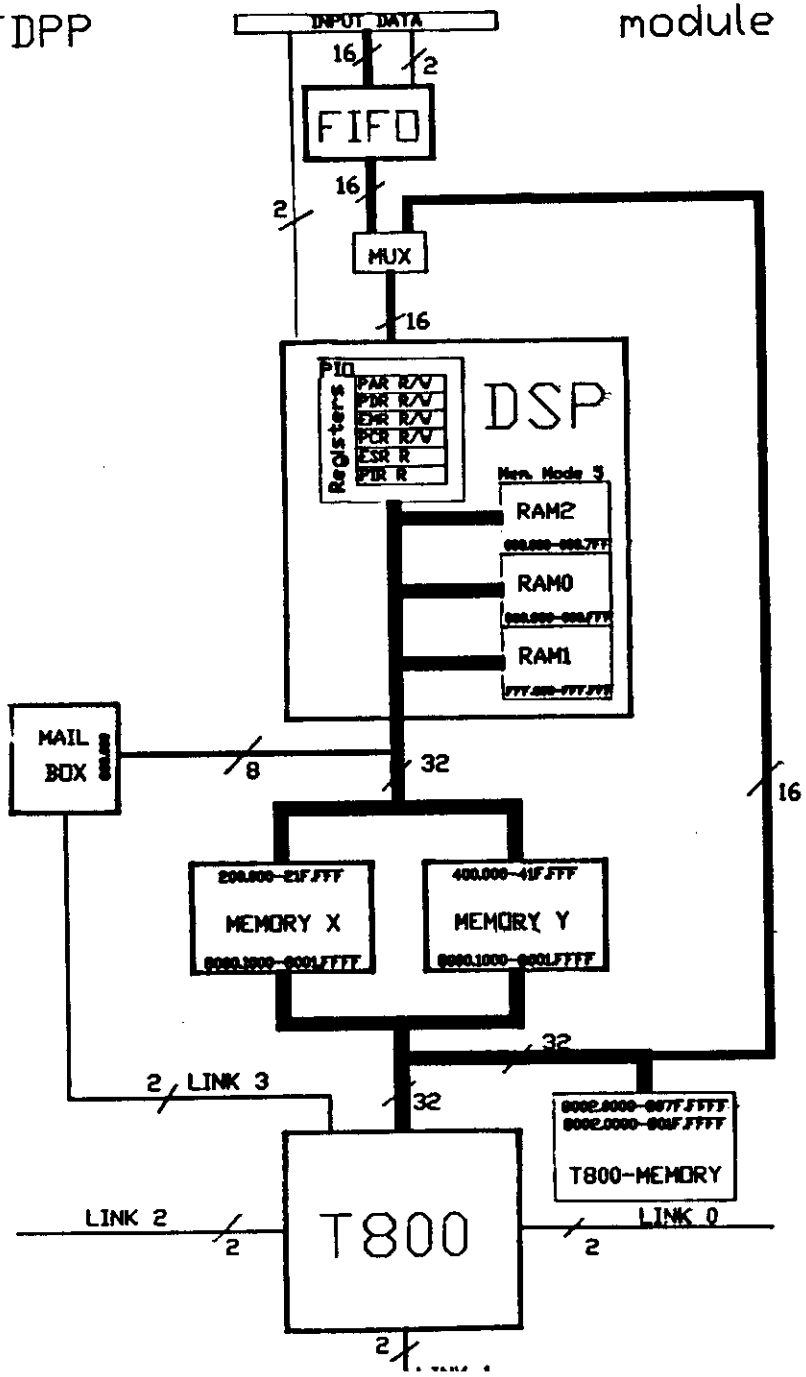
3.7. Applications overview

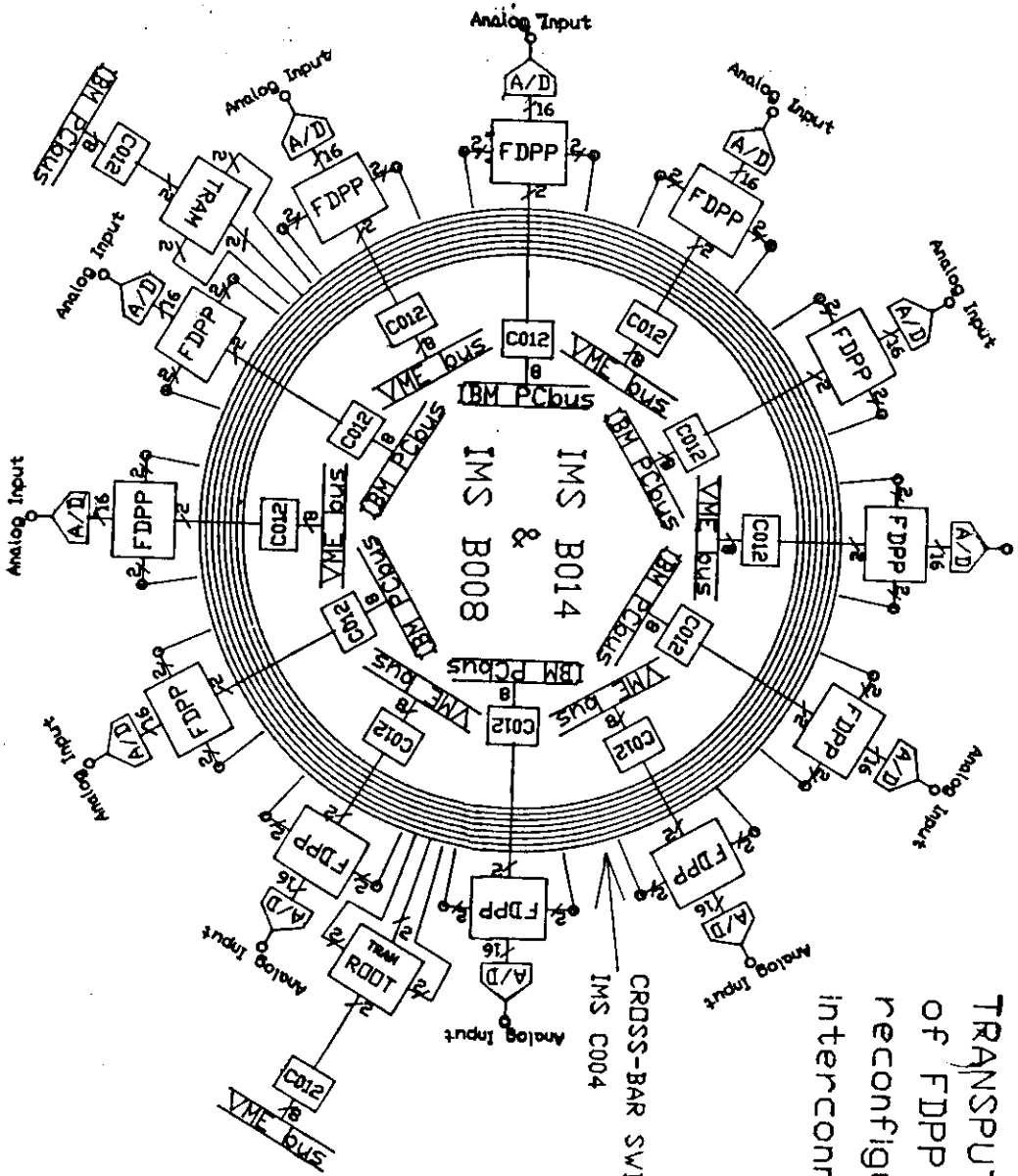
Low-cost and high-speed, favors the use of DPS in these applications.

- **instrumentation**
- **telecommunication (high speed modems)**
- **image processing and pattern recognition**
- **speech recognition, musical synthesizer**
- **direction finding in radar,**
- **target tracking (closed loop systems)**
- **ultrasound medical imaging, image processing**
- **automobiles: antiskid braking systems, adaptive suspension, engine control and instrumentation**
- **vibration analysis**
- **medical electronics**
- **digital video**
- **disk drives, tape drives**
- **printers, plotters and consumer products**
- **digital filters**
- **digital HIFI, digital AM/FM radio**
- **workstations**
- **robotics**
- **spectrum analysis**

Fast Digital Parallel Processing

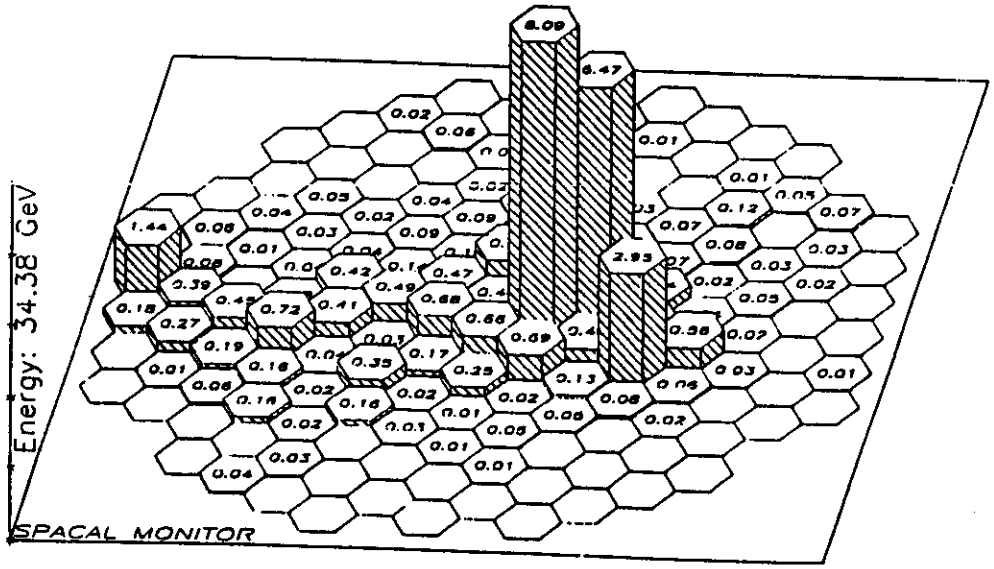
FDPP module





TRANSPUTER CLUSTER of FDPP with reconfigurable interconnection

70 GeV π^- Interacting in upstream Target



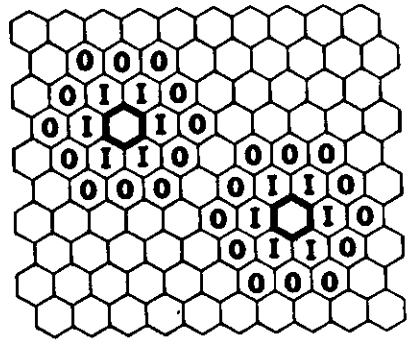
Algorithm 1

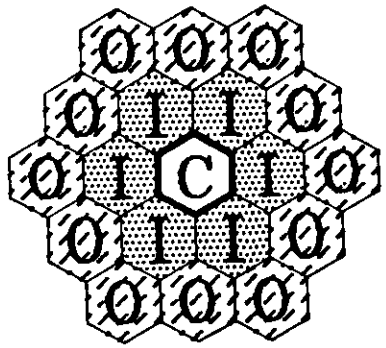
each FDPP

- scans 100 channels
- finds local maximum
- calculate E, I/C, O/C

in 58 μsec

(electron events)

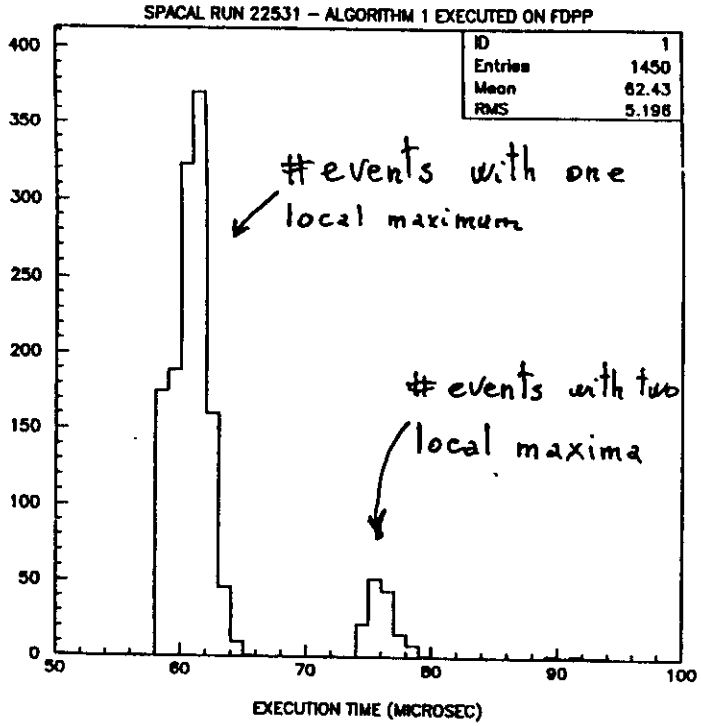


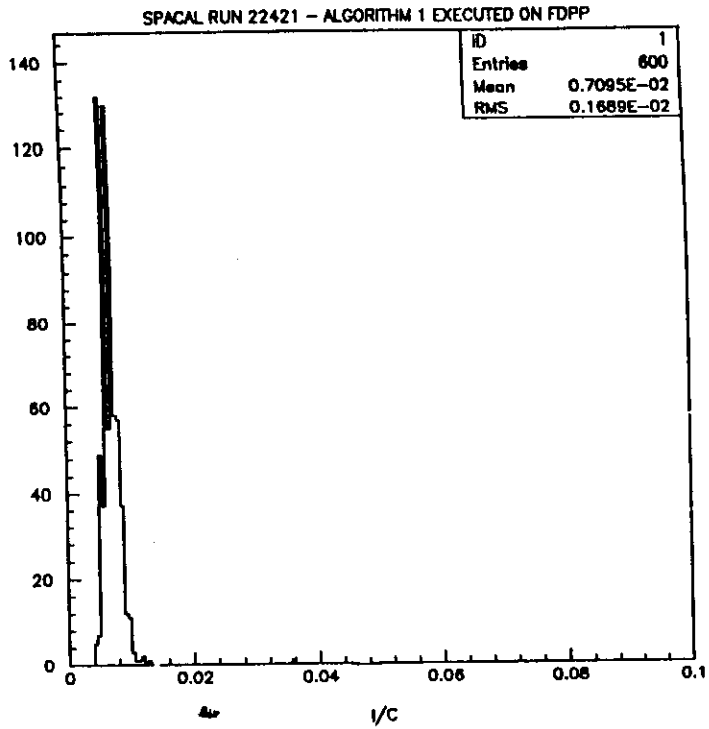


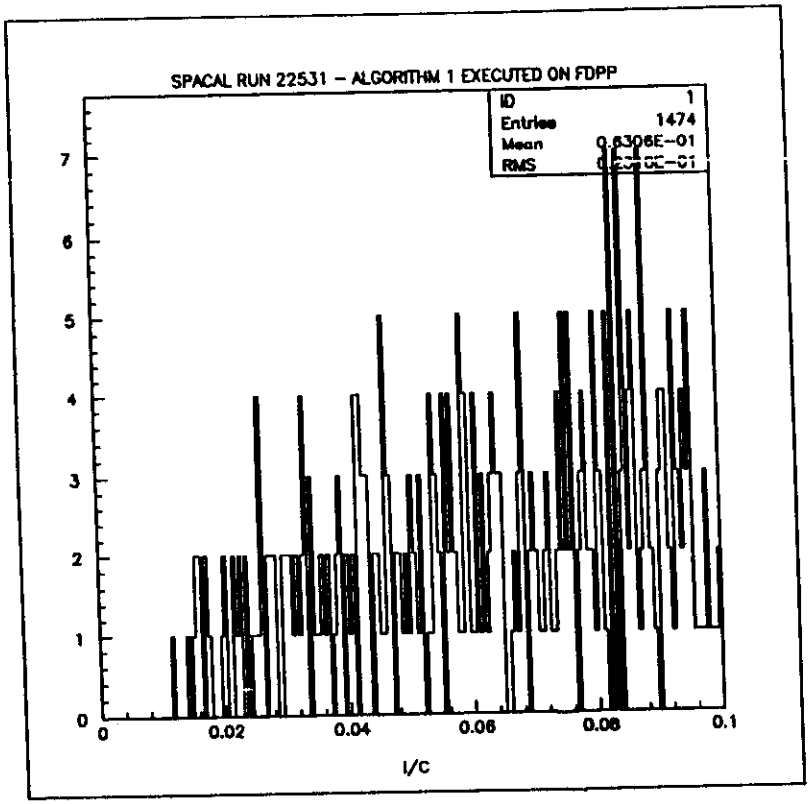
$$E = C + \sum_{i=1}^{6} I + \sum_{i=1}^{12} O$$

$$I/C = (1/6 \sum_{i=1}^{6} I)/C$$

$$O/C = (1/12 \sum_{i=1}^{12} O)/C$$


SPACAL RUN 22531 – ALGORITHM 1 EXECUTED ON FDPP
ID 1
Entries 1450
Mean 62.43
RMS 5.196
#events with one local maximum
#events with two local maxima
EXECUTION TIME (MICROSEC)


SPACAL RUN 22421 – ALGORITHM 1 EXECUTED ON FDPP
ID 1
Entries 600
Mean 0.7095E-02
RMS 0.1689E-02
1/C



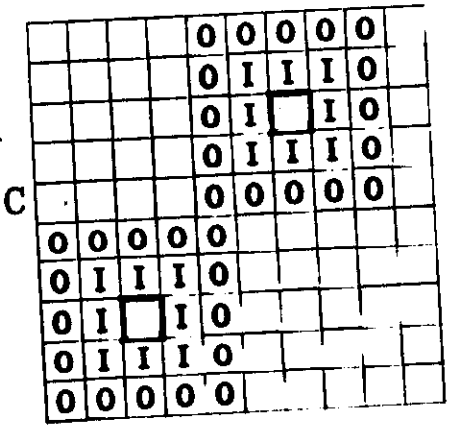
Algorithm 2

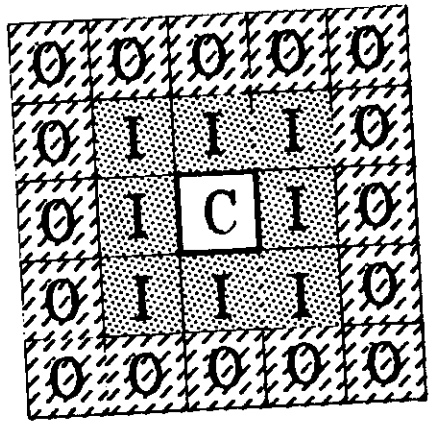
each FDPP

- scans 100 channels
- finds local maximum
- calculates E, I/C, O/C

in 59 μsec

(electron events)





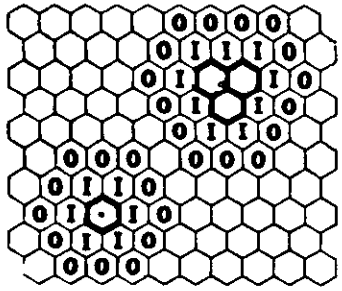
$$E = C + \sum_{i=1}^{8} I + \sum_{i=1}^{16} O$$

$$I/C = (1/8 \sum_{i=1}^{8} I)/C$$

$$O/C = (1/16 \sum_{i=1}^{16} O)/C$$

Algorithm 3

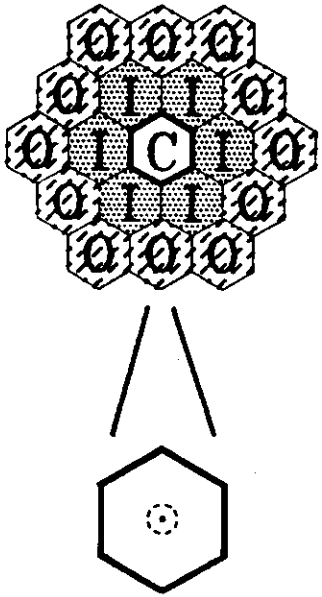
each FDPP



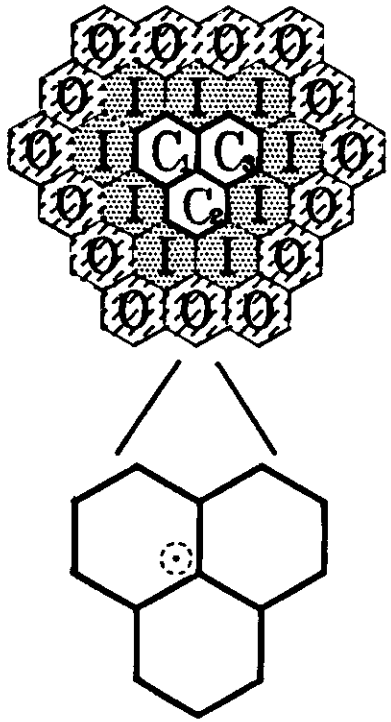
- scans 100 channels
- finds type of hit
- finds local maximum
- calculate E, I/C, O/C for different type of hit

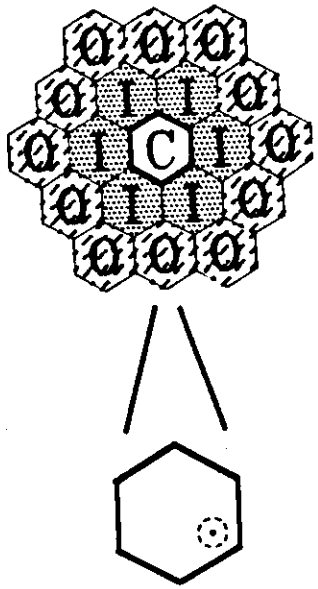
in 62 μsec

(electron events)

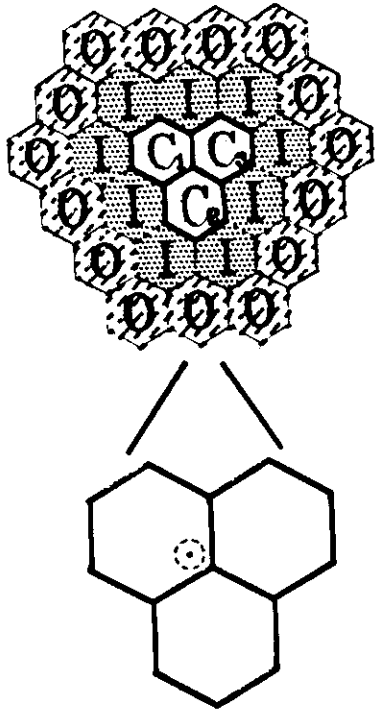


OR





OR



$$E_1 = C + \sum_{i=1}^{6} I + \sum_{i=1}^{12} O \qquad C = C_1 + C_2 + C_3$$

$$E_2 = C_1 + C_2 + C_3 + \sum_{i=1}^{9} I + \sum_{i=1}^{15} O$$

$$(I/C)_1 = (1/6 \sum_{i=1}^{6} I)/C \qquad (I/C)_2 = (1/9 \sum_{i=1}^{9} I)/C$$

$$(O/C)_1 = (1/12 \sum_{i=1}^{12} O)/C \qquad (O/C)_2 = (1/15 \sum_{i=1}^{15} O)/C$$

The same event N.32 from RUN 22531 on SPACAL (1990)

$E_1 = 27.25$ Gev	$E_2 = 28.25$ Gev
$(I/C)_1 = 0.1667$	$(I/C)_2 = 0.2874$
$(O/C)_1 = 0.1544$	$(O/C)_2 = 0.0977$

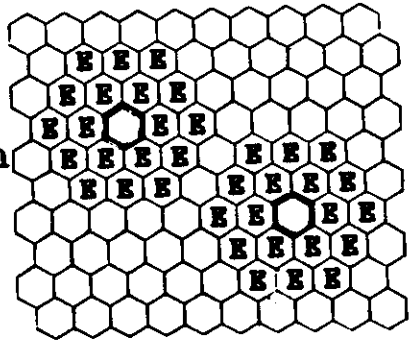
Algorithm 4

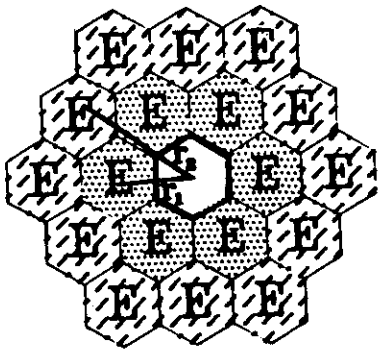
each FDPP

- scans 100 channels
- finds local maximum
- calculate R_p

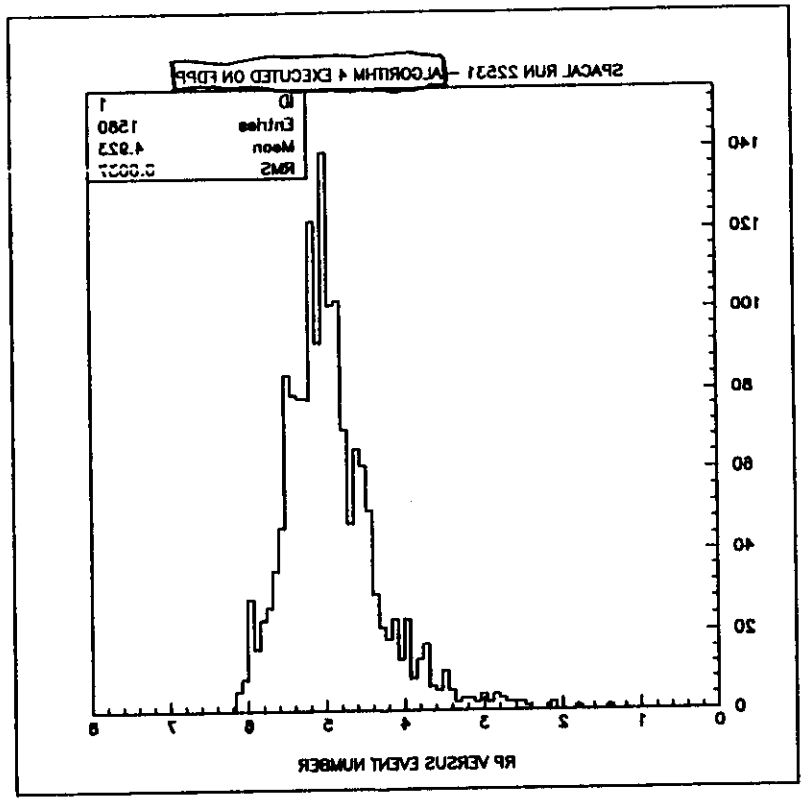
in 58 μsec

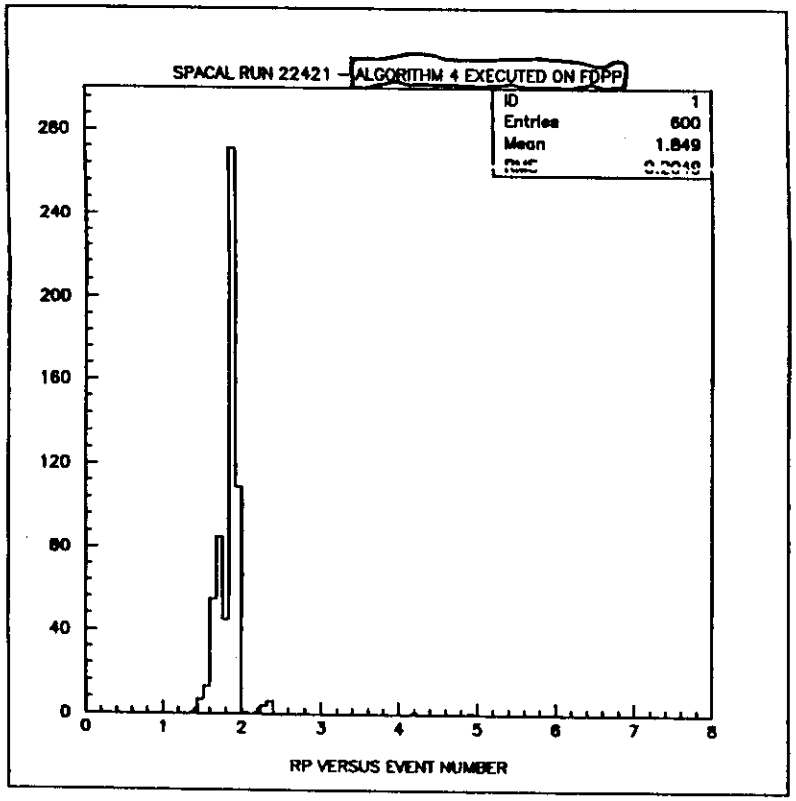
(electron events)





$$R_p = \frac{\sum_{i=1}^{18} r_i \, E_i^{0.4}}{\sum_{i=1}^{18} E_i^{0.4}}$$





256 x FDPP modules
for HEP real time algorithms

FDPP architecture for an
array of 100x100 channels

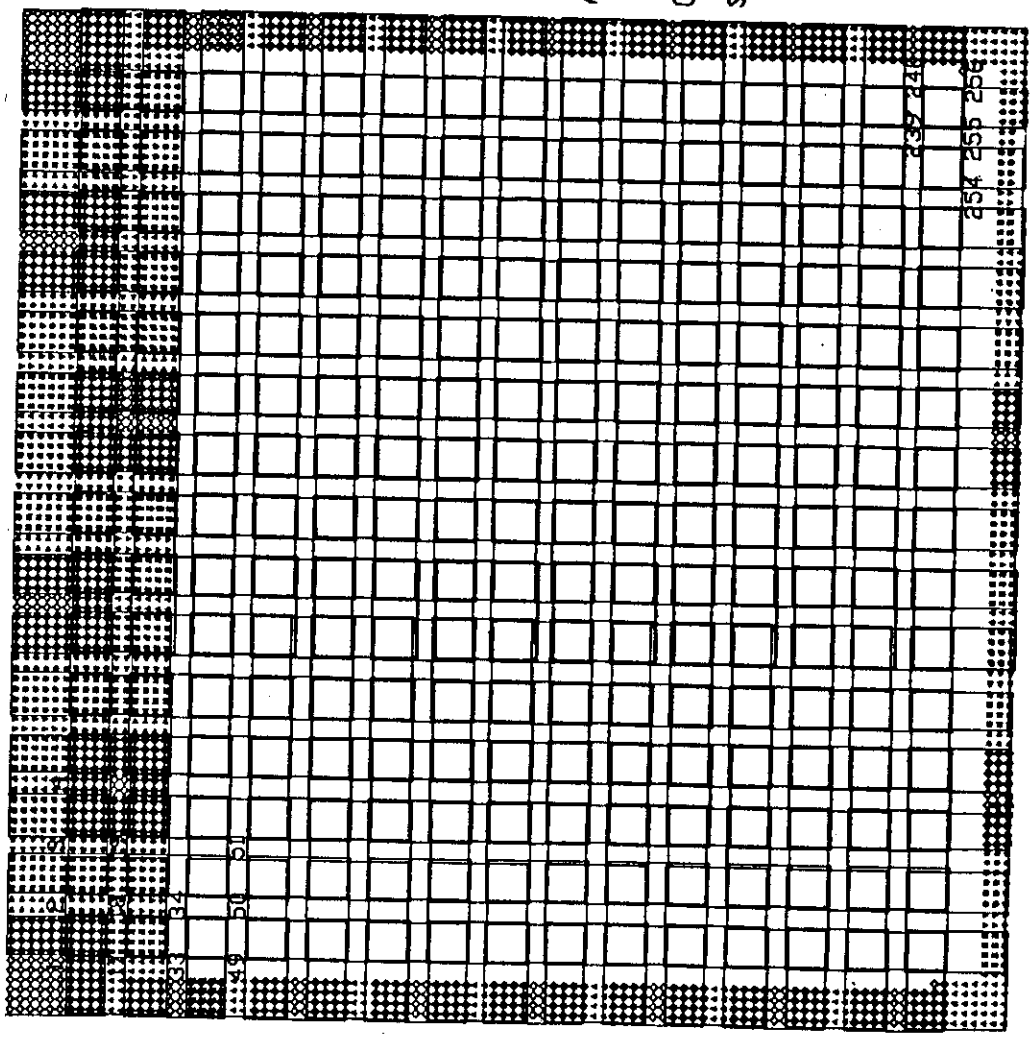
Each FDPP module analyse 36
channels out of 100 data-in

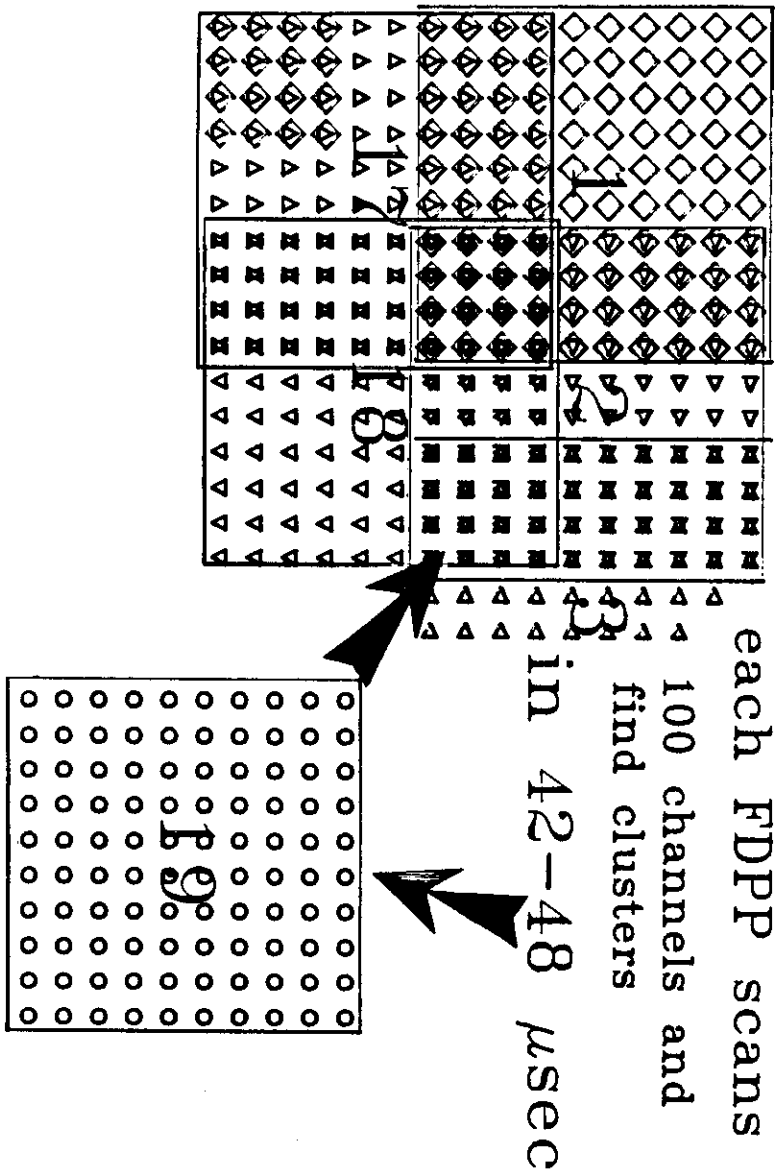
GENERIC PEAKFINDING

All peaks are found in μsec ~5

CLUSTER-ANALYSIS

SIMPLE JET/ELECTRON FINDER





SUMMARY

CALORIMETER 100 x 100 channels

(with square or hexagonal elements)

- A 256 FDPP parallel architecture

(with a granularity of 100 channels/FDPP)

finds CLUSTER in the WHOLE DETECTOR

(calculates energy and cluster shape factors)

within 60 μsec

Detailed timing for a granularity of 100 channels/FDPP:

- **scans channels** **42 - 48 μsec**
- **E, I/C, O/C or Rp** **15 - 17 μsec (in floating point)**

Detailed timing for a granularity of 49 channels/FDPP:

- **scans channels** **21 - 24 μsec**
- **E, I/C, O/C or Rp** **15 - 17 μsec (in floating point)**

Lowest cost per Mflop available in the market (AT&T DSP32C = 7 US $ per Mflop)