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COLLEGE ON
"THE DESIGN OF REAL-TIME CONTROL SYSTEMS"
1 - 26 October

RECALL OF THE M6809 SYSTEM and THE ROSY JUNIOR

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These are preliminary lecture notes, intended only for distribution to participants.

Recall of the M6809 System
and
The ROSY Junior

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Cambridge University Computer Laboratory

Outline of Lectures

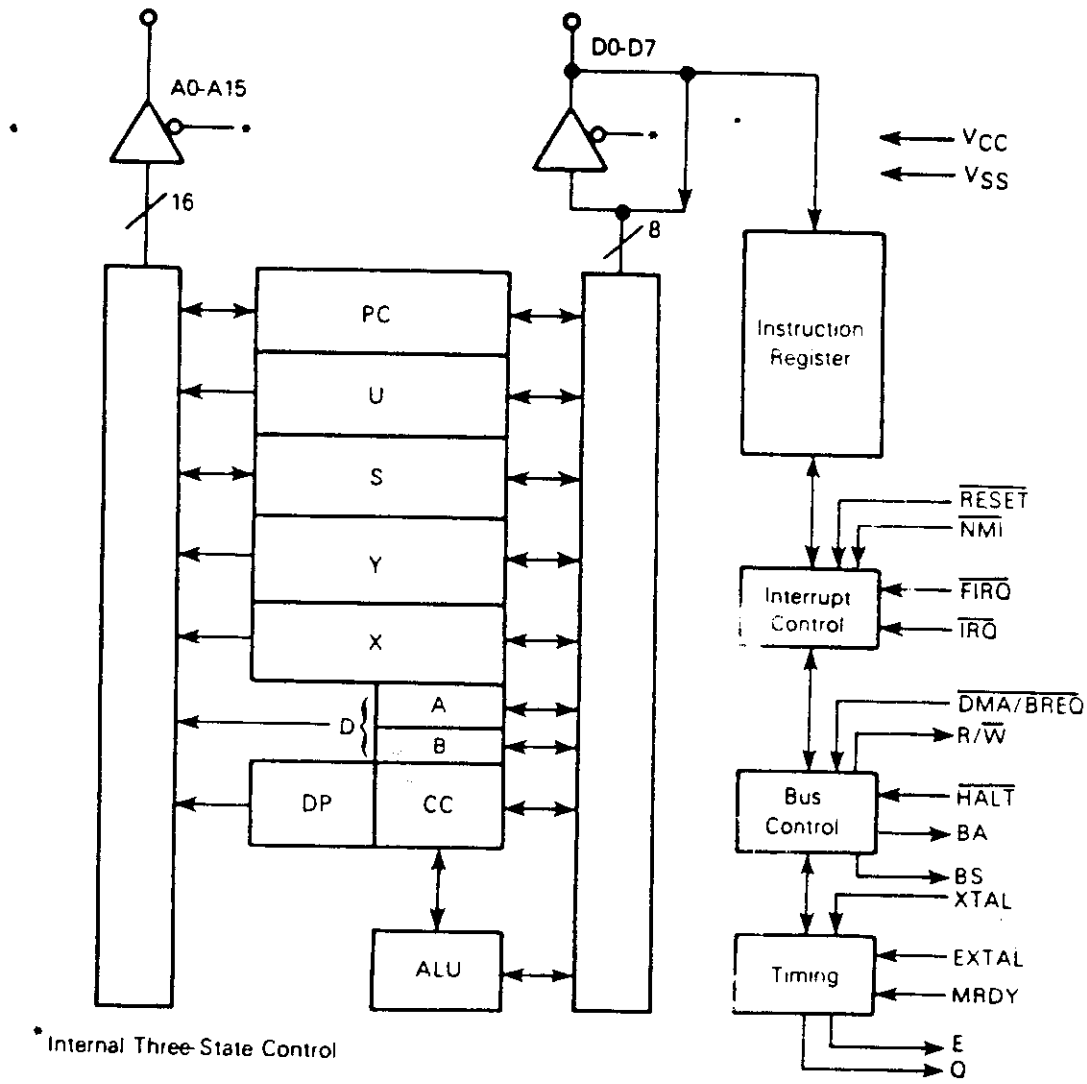
- Characteristics and functions of hardware components used in the ROSY Junior.
- Mircroprocessor (MC6809)
- Parallel Interface Adapter (MC6821)
- Asynchronous Communications Interface Adapter (MC6850)
- Programmable Timer Module (MC6840)
- Memory Devices (EPROM & RAM)
- Floppy Disk & Controller (WD2793)
- Direct Memory Access Controller (MC6844)
- ROSY Junior
  - System Overview
  - Memory Subsystem
  - Peripheral Subsystem
  - Disk Subsystem

Highlights of M6809

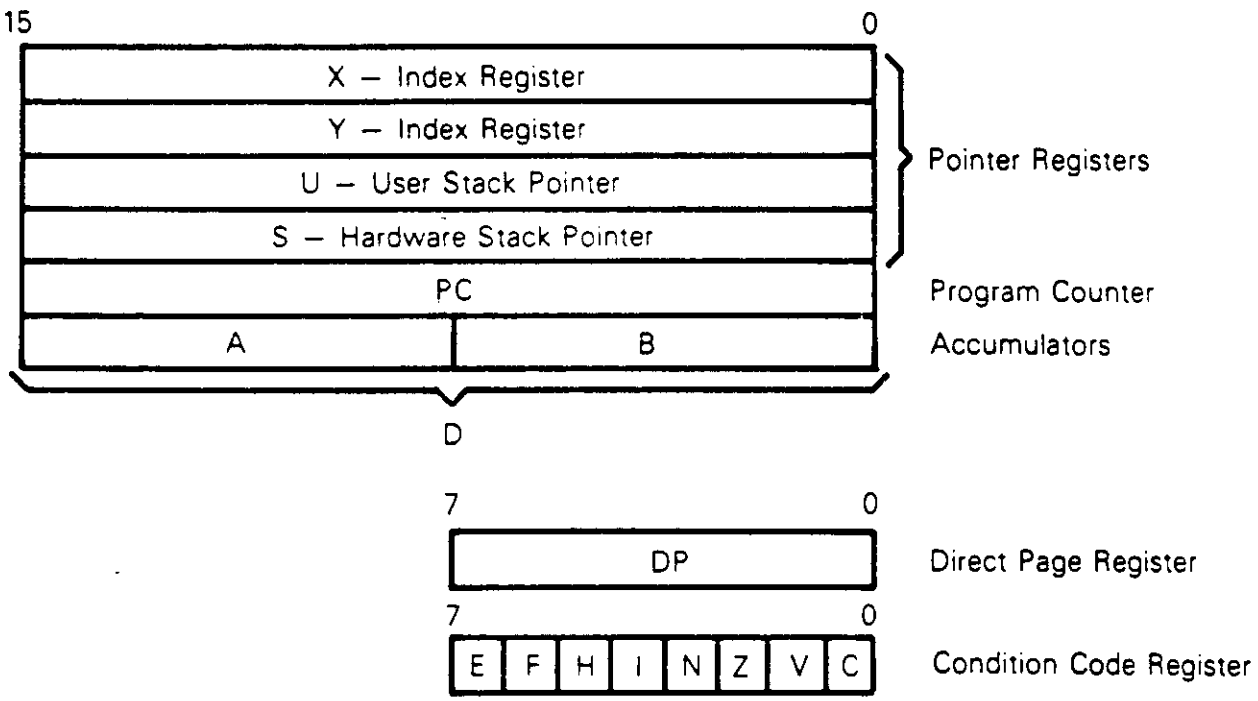
- **Hardware**
  - Clock: 1, 1.5 or 2 MHz (on-chip oscillator or external)
  - Address bus: 16 lines; data bus: 8 lines
  - Interrupts: NMI, FIRQ, IRQ
  - Features for DMA & slow memory access
  - Synchronization to external event
  - M6800 family compatible

- **Software**
  - 10 addressing modes
  - 59 opcodes, 1464 instructions
  - 16-bit arithmetic, 8×8 unsigned multiplication
  - Good stack manipulation
  - Load effective address

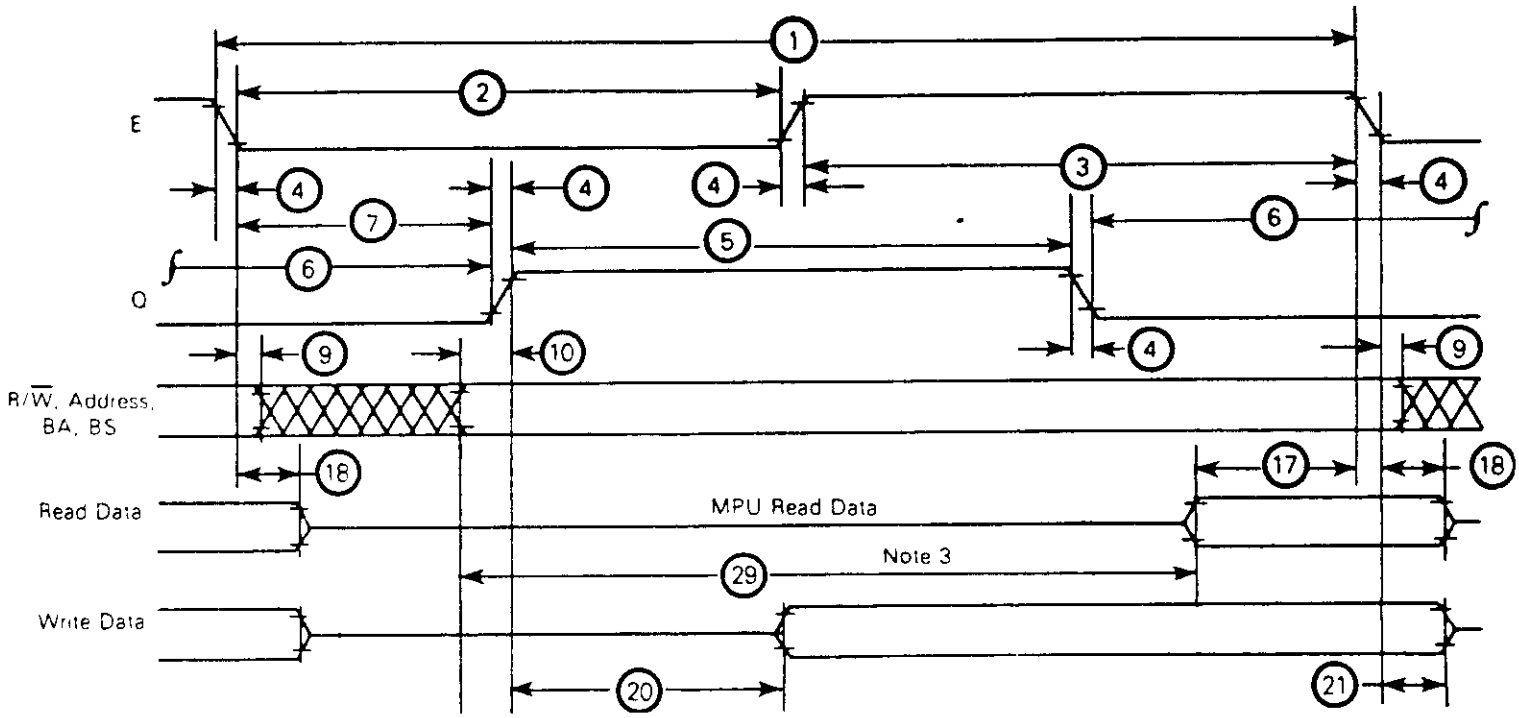
MC6809 Block Diagram



M6809 Programming Model



M6809 Bus Timing



BUS TIMING CHARACTERISTICS (See Notes 1 and 2)

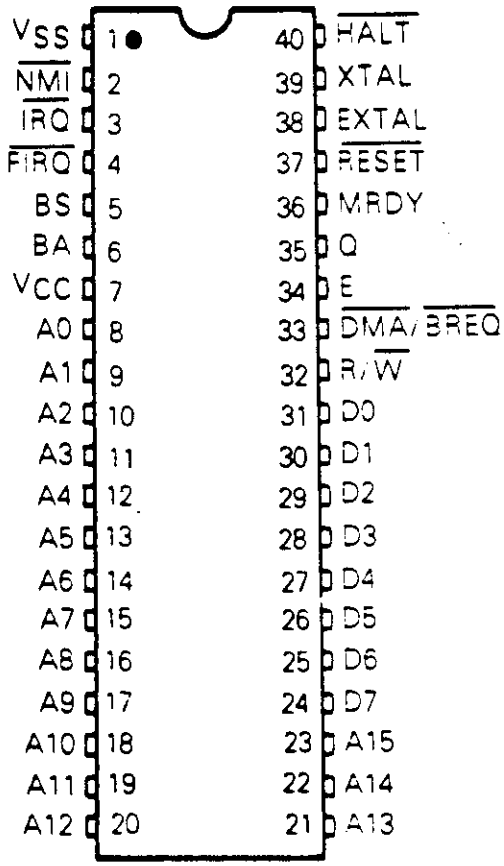
Ident. Number	Characteristics	Symbol	MC6809		MC68A09		MC68B09		Unit
			Min	Max	Min	Max	Min	Max	
1	Cycle Time (See Note 5)	t_{cyc}	1.0	10	0.667	10	0.5	10	µs
2	Pulse Width, E Low	PW_{EL}	430	5000	280	5000	210	5000	ns
3	Pulse Width, E High	PW_{EH}	450	15500	280	15700	220	15700	ns
4	Clock Rise and Fall Time	t_r, t_f	–	25	–	25	–	20	ns
5	Pulse Width, Q High	PW_{QH}	430	5000	280	5000	210	5000	ns
6	Pulse Width, Q Low	PW_{QL}	450	15500	280	15700	220	15700	ns
7	Delay Time, E to Q Rise	t_{AVS}	200	250	130	165	80	125	ns
9	Address Hold Time* (See Note 4)	t_{AH}	20	–	20	–	20	–	ns
10	BA, BS, R/W, and Address Valid Time to Q Rise	t_{AQ}	50	–	25	–	15	–	ns
17	Read Data Setup Time	t_{DSR}	80	–	60	–	40	–	ns
18	Read Data Hold Time*	t_{DHR}	10	–	10	–	10	–	ns
20	Data Delay Time from Q	t_{DDQ}	–	200	–	140	–	110	ns
21	Write Data Hold Time*	t_{DHW}	30	–	30	–	30	–	ns
29	Usable Access Time (See Note 3)	t_{ACC}	695	–	440	–	330	–	ns
	Processor Control Setup Time (MRDY, Interrupts, DMA/BREQ, HALT, RESET) (Figures 6, 8, 9, 10, 12, and 13)	t_{PCS}	200	–	140	–	110	–	ns
	Crystal Oscillator Start Time (Figures 6 and 7)	t_{RC}	–	100	–	100	–	100	ms
	Processor Control Rise and Fall Time (Figures 6 and 8)	t_{PCr}, t_{PCf}	–	100	–	100	–	100	ns

ess and data hold times are periodically tested rather than 100% tested

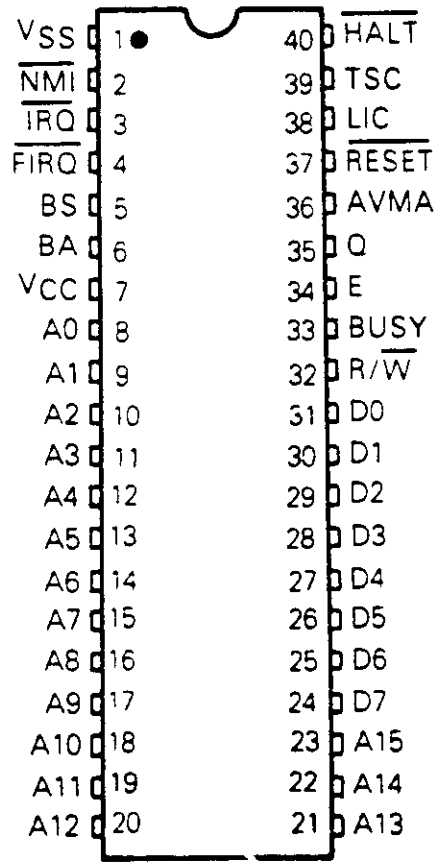
evels shown are V_L 0.4 V, V_H 2.4 V, unless otherwise specified.
ent points shown are 0.8 V and 2.0 V, unless otherwise specified.
s time is computed by: 1 4 7 max · 10 17
) for BA and BS is not specified.
uring MRDY or DMA BREQ is 16 µs.
MC68A09 1.5 MHz, MC68B09 2.0 MHz.

Differences between MC6809 & MC6809E

MC6809



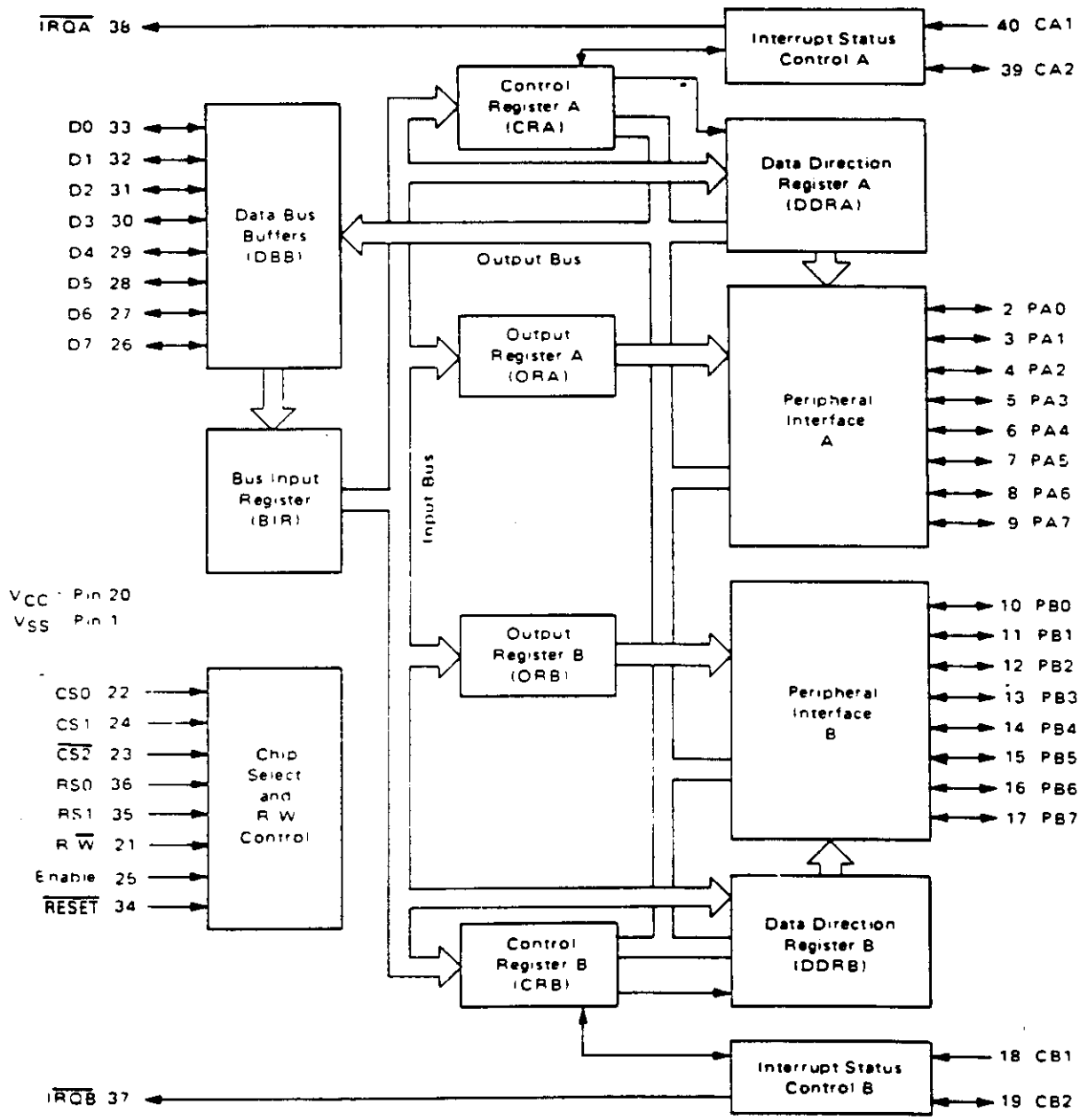
MC6809E



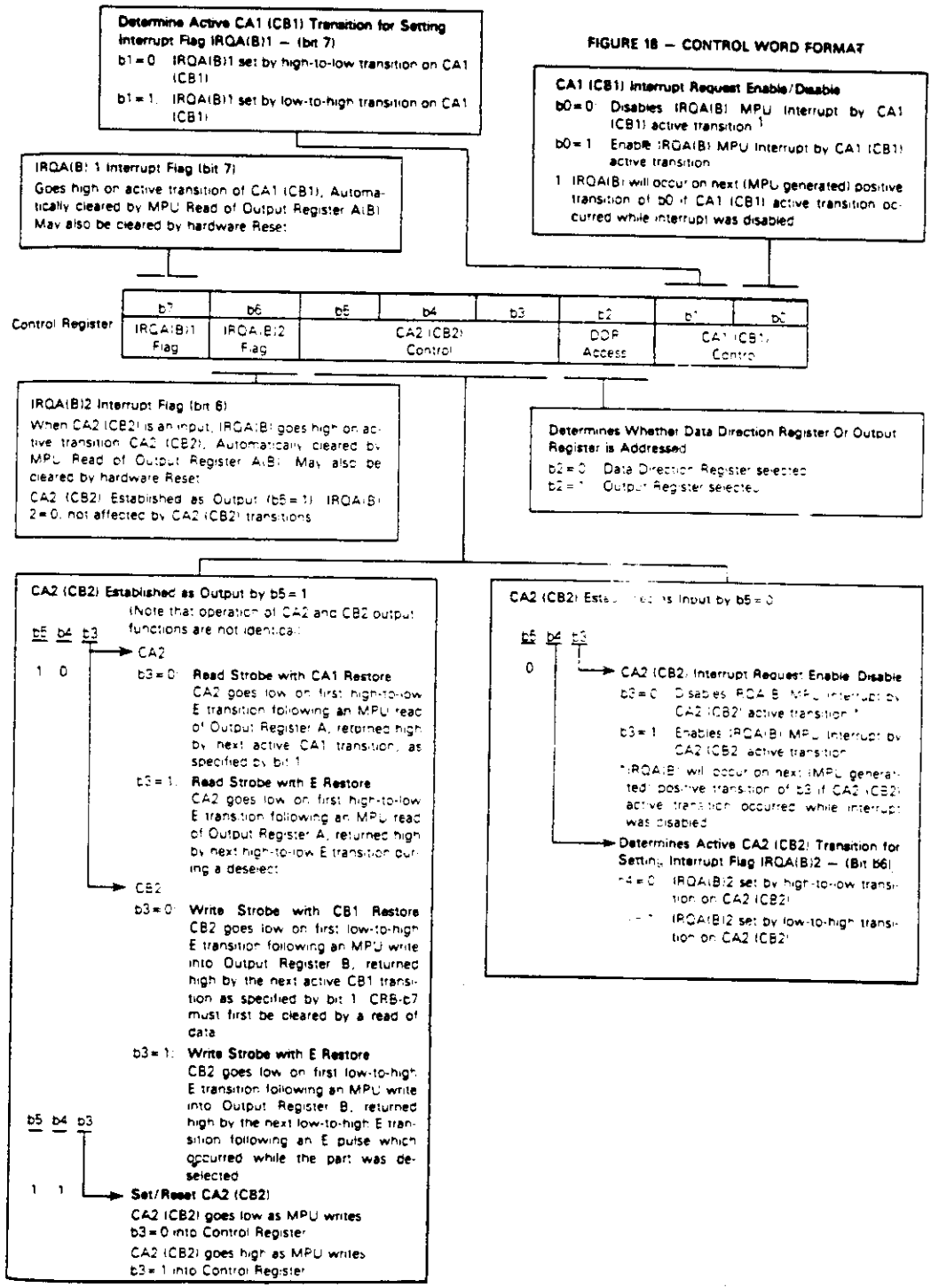
Highlights of MC6821 PIA

- Peripheral Interface Adapter that provides *universal* means of interfacing with a high degree of flexibility
- 8-bit data bus for communicating with MPU
- Two 8-bit I/O ports with handshake control logic
- Two programmable control registers
- Two programmable data direction registers
- Four individually controlled interrupt input lines, two usable as peripheral control outputs
- Handshake control logic for input and output peripheral operation
- Program controlled interrupt and interrupt disable capability
- high impedance tri-state and direct transistor drive peripheral lines

MC6821 PIA Block Diagram



MC6821 PIA Control Registers



PIA Programming Exercise

Write a subroutine to initialize port A of a PIA as inputs and port B as outputs. Assume that the PIA is at $EC10 – $EC13, conventional configuration.

Write an endless loop program to read the status of port A and send it to port B.

Asynchronous Communications Interface Adapte

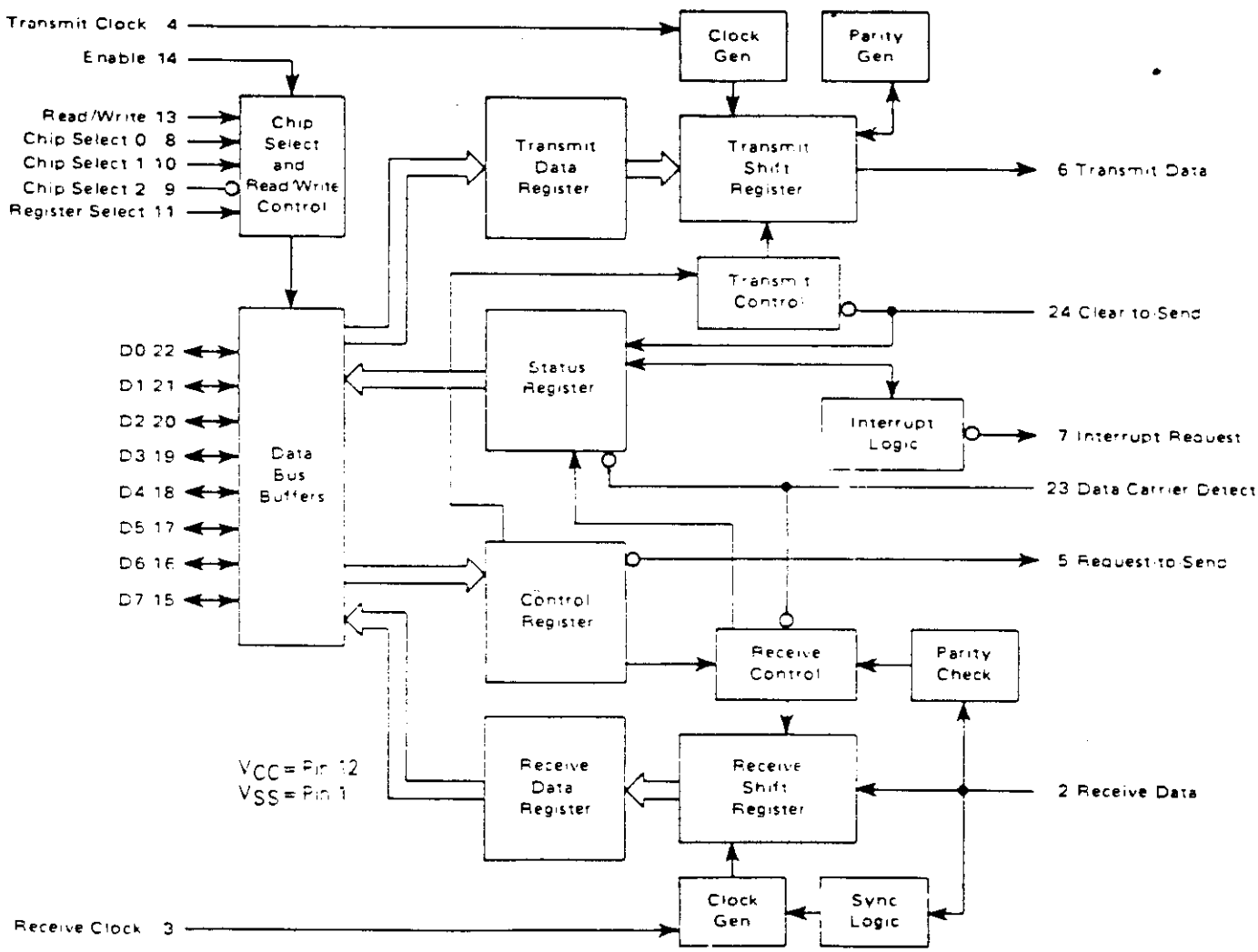
- **Serial Communications**
  - Synchronous, BSC or *bisync*, HDLC
  - Asynchronous, RS232C or CCITT V.24

- **RS232C**
  - Serial data timing format
  - Data Terminal Equipment (DTE)
  - Data Communications Equipment (DCE)
  - Signal lines: TxD, RxD, RTS, CTS, DSR, DCD, DTR

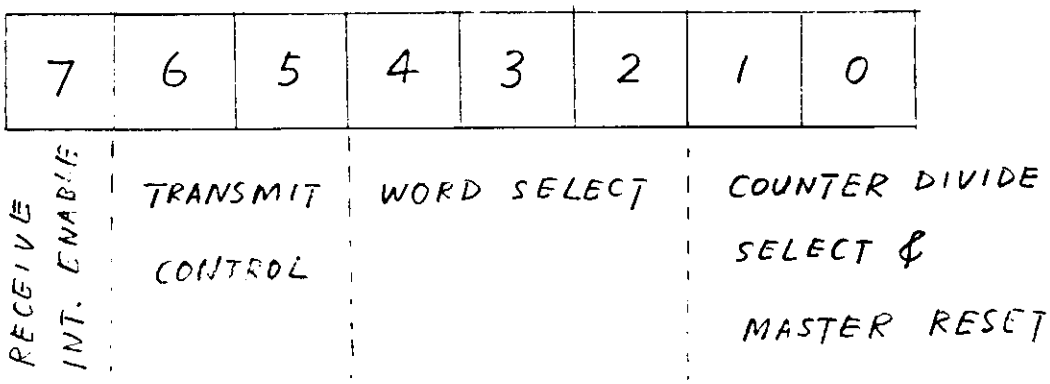
Highlights of MC6840 ACIA

- Asynchronous Communications Interface Adapter that provides data formatting and control to interface serial asynchronous data communications information to bus organized systems.
- The parallel data of the bus system is serially transmitted and received by ACIA with proper formatting and error checking.
- A programmable control register provides variable word lengths, clock division ratios, transmit control, receive control, and interrupt control.
- Control lines are provided for peripheral or modem operation.
- 8- or 9-bit transmission.
- Optional odd or even parity.
- Parity, overrun and framing error checking.
- Optional $\div 1$, $\div 16$, and $\div 64$ clock modes.

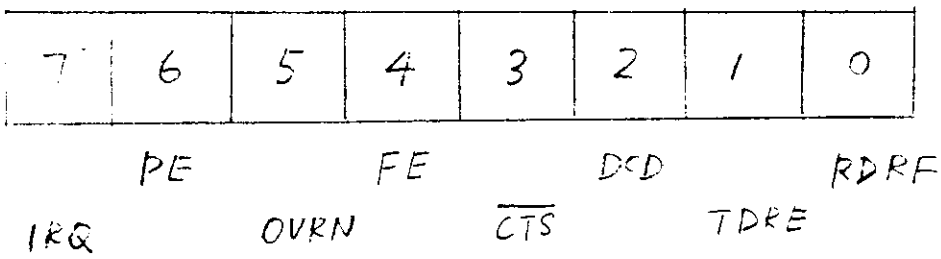
MC6850 ACIA Block Diagram



MC6850 ACIA Control Register



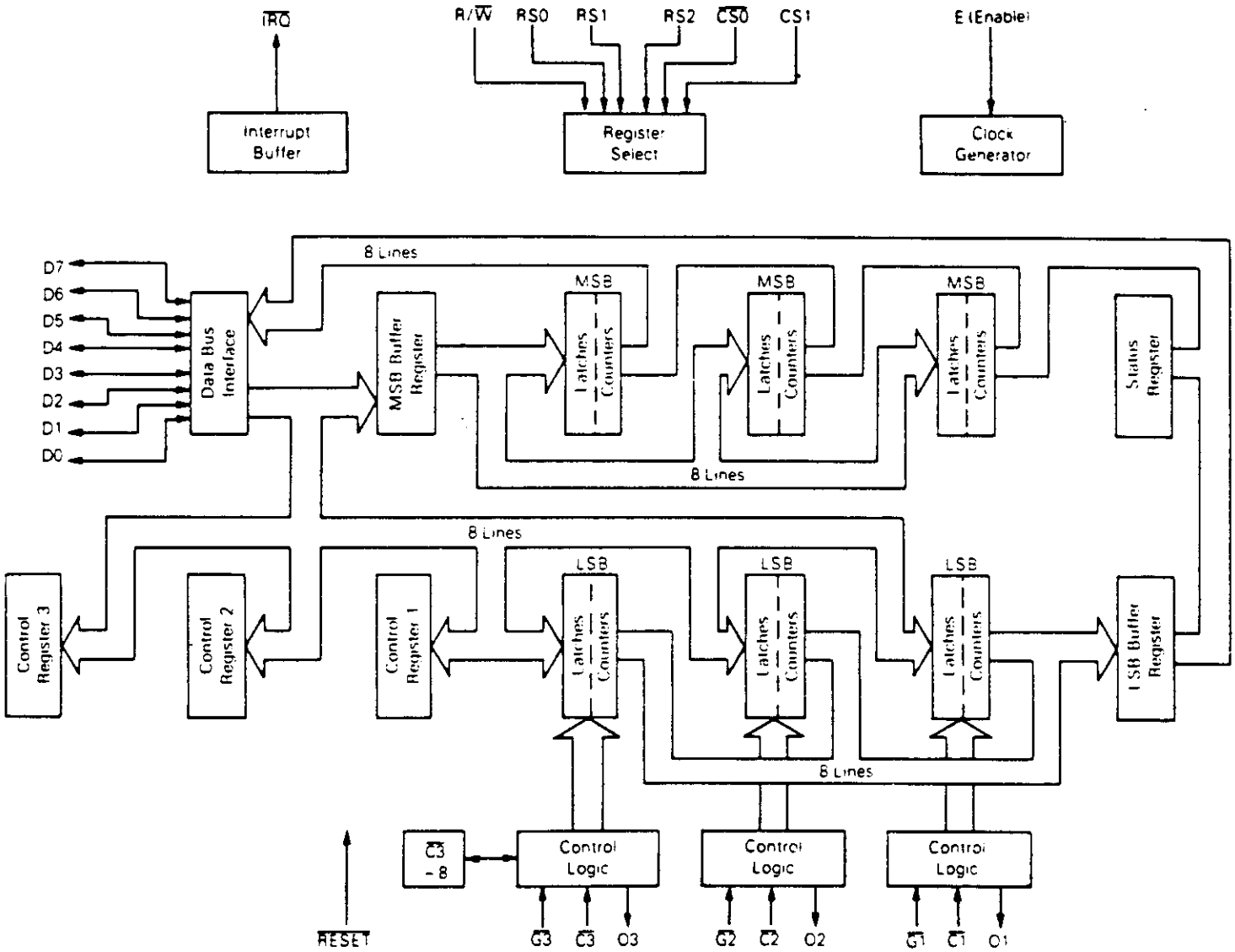
MC6850 ACIA Status Register



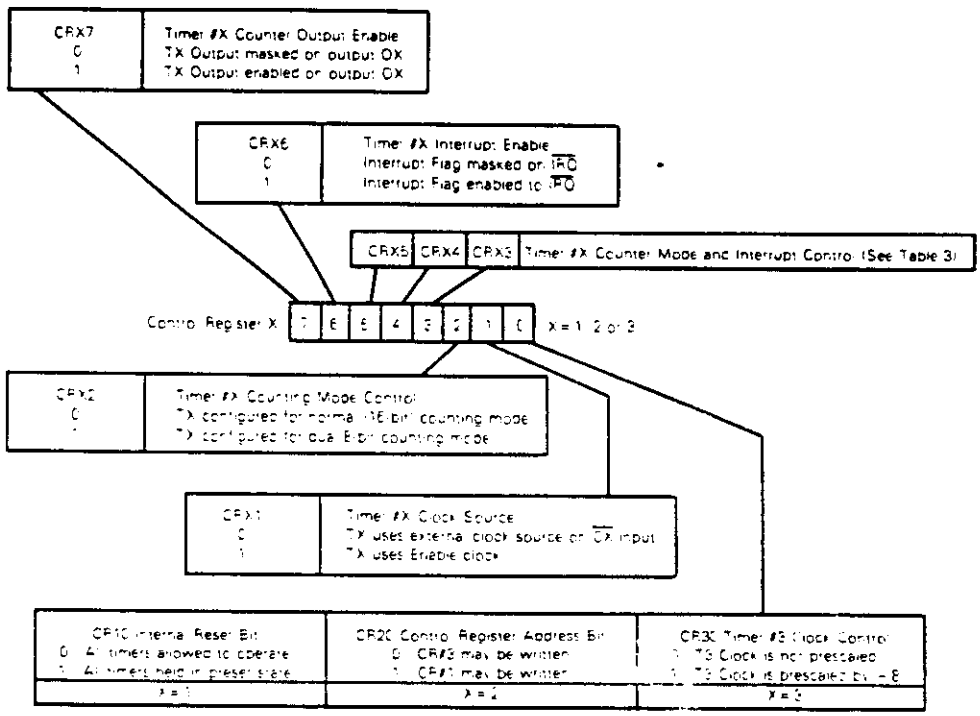
Highlights of MC6850 PTM

- Programmable Timer Module that provides timing and counting facility.
- Three 16-bit binary counters, three corresponding control registers, and a status register.
- Used for tasks such as frequency measurement, event counting, interval measuring, pulse generation and square wave generation.

MC6840 PTM Block Diagram



MC6840 PTM Control Register



MC6840 PTM Status Register

Bits 0, 1, and 2 are individual flag bits for Timers 1, 2, and 3 respectively. Bit 7 is a Composite Interrupt Flag.

MC6840 PTM Timer Operating Modes

- **Wave synthesis modes**
  - Continuous operating mode
  - Single-shot
- **Wave measurement modes**
  - Frequency comparison or period measurement mode
  - Pulse width comparison mode

Read Only Memories

- Two types of high density EPROMs
- TMM27512, 64 Kbytes
- μPD27C1001D, 128 Kbytes

Random Access Memories

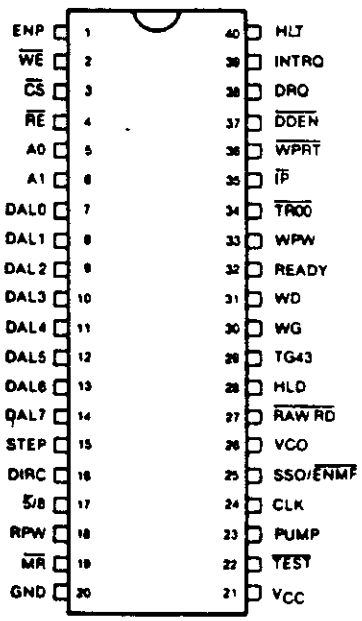
- TC55257, 32 Kbytes

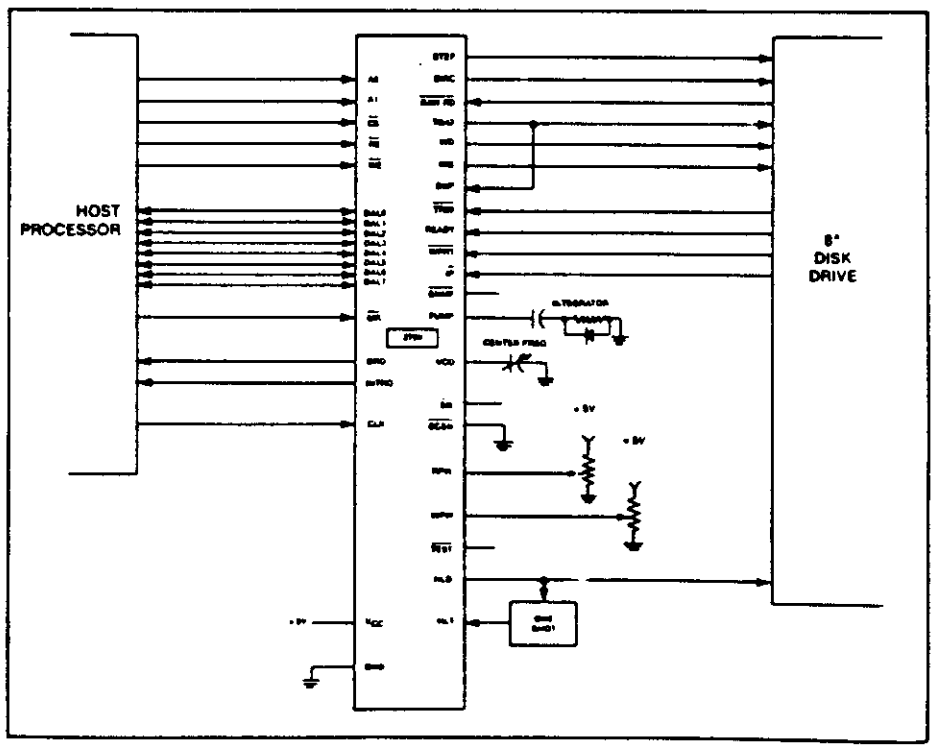
Floppy Disk Storage

- Bulk long-term storage
- Secondary storage
- Medium for programs/data transfer
- 3.5 inch microfloppy disks (1980s)
  - Capacity: 0.5 Mbytes/side, 80 tracks at 8000 bits/in
  - Track density: 48 tracks/in or 96 tracks/in
  - Data transfer rates: 125 Kbits/s or 250 Kbits/s
- Principle of recording: frequency modulation (FM) & modified frequency modulation (MFM)
- Floppy disk controller & direct memory access
- New development: perpendicular recording

WD2793 Floppy Disk Controller

- Performs the function of controller and formatter for floppy, mini-floppy and microfloppy disks.
- Accommodates single and double density formats (FM & MFM).
- Phase-lock-loop data separator.
- 8-bit bidirectional bus for data, status and control word transfer.

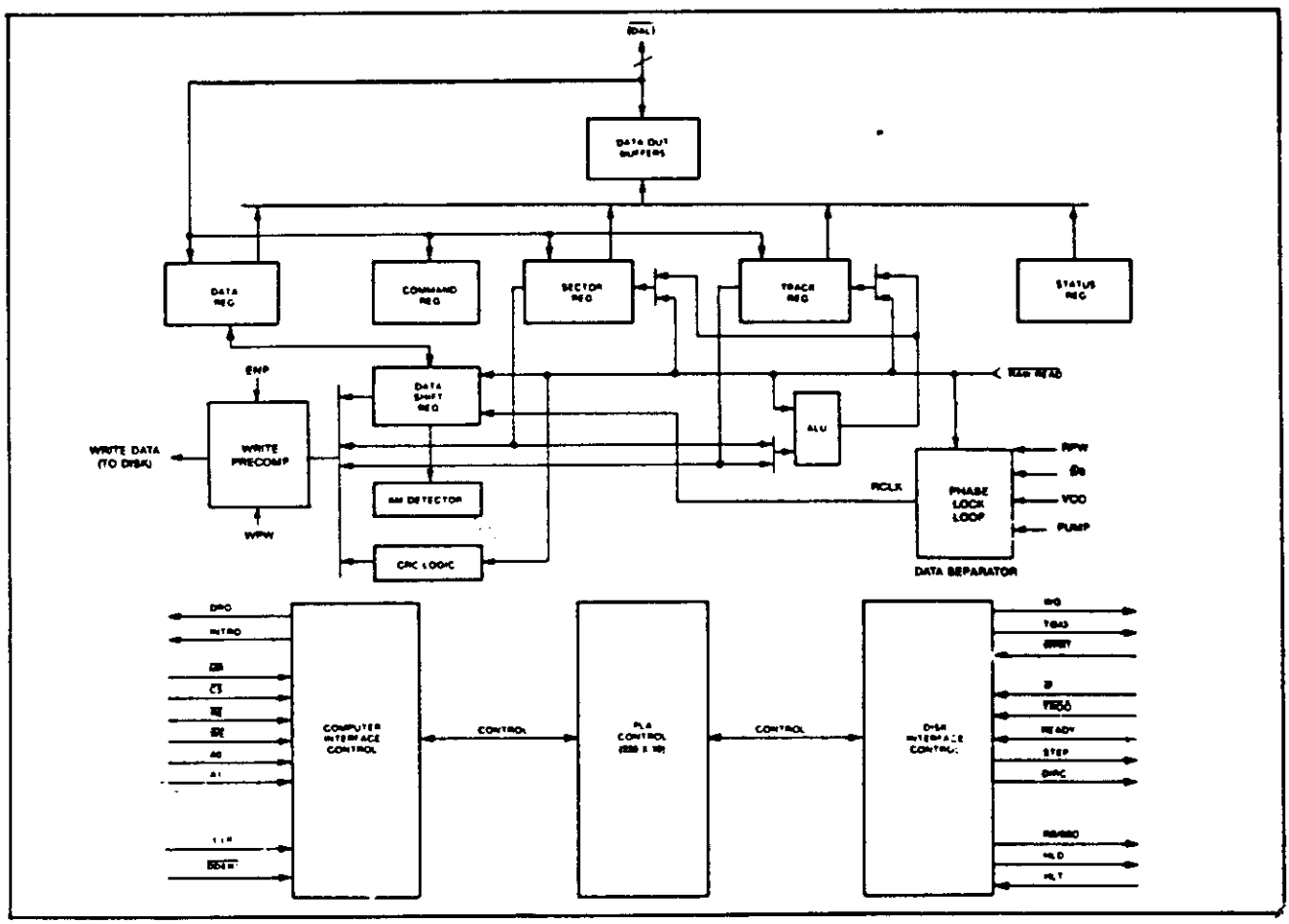




Floppy Disk Controller Interfacing

- Interfaces to processor via eight data access lines and associated control signals.
- Usual access of registers by Chip Select, Read Enable, Write Enable and two address lines.
- Interfaces to disk drive via 11 control and sensing lines.

FDC Block Diagram



Functions of FDC

- Test function.
- Sector lengths: 128, 256, 512 or 1024 bytes.
- Cyclic redundancy check (V.41): $G(x) = x^{16} + x^{12} + x^5 + 1$
- Commands: Restore, seek, step, step-in, step-out, read sector, write sector, read address, read track, write track, force interrupt.
- IBM standards. IBM3740: 128 bytes, 26 sectors/track. System 34: 256 bytes, 26 sectors/track.

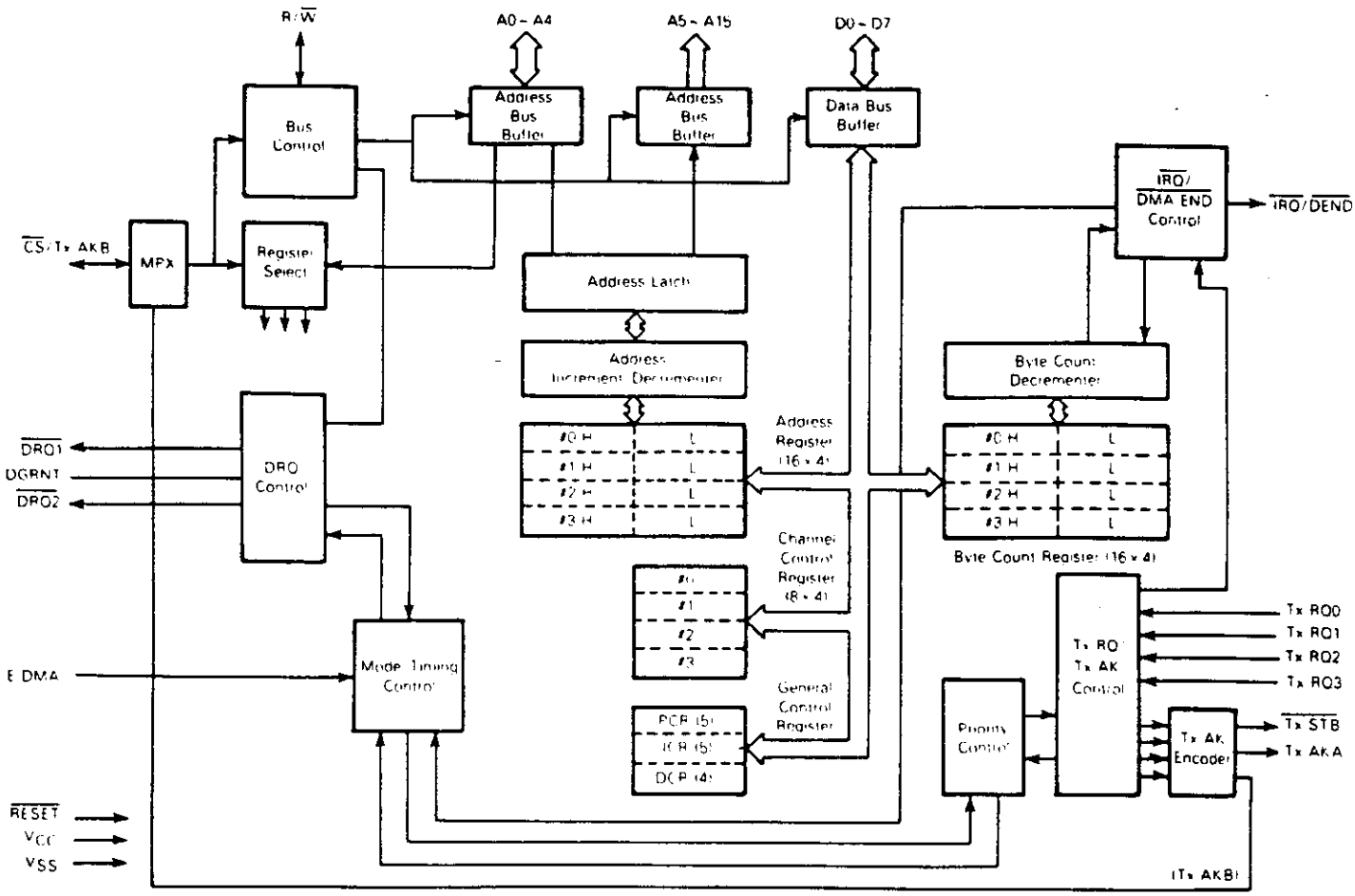
Direct Memory Access

- Necessity of DMA.
- Direct Memory Access Controller (DMAC) transfers data directly between memory and peripheral device controller such as the FDC by taking over the control of address and data bus of MPU.
- In ROSY Junior the data rate is 125 Kbits/s or 250 Kbits/s.

Highlights of MC6844 DMAC

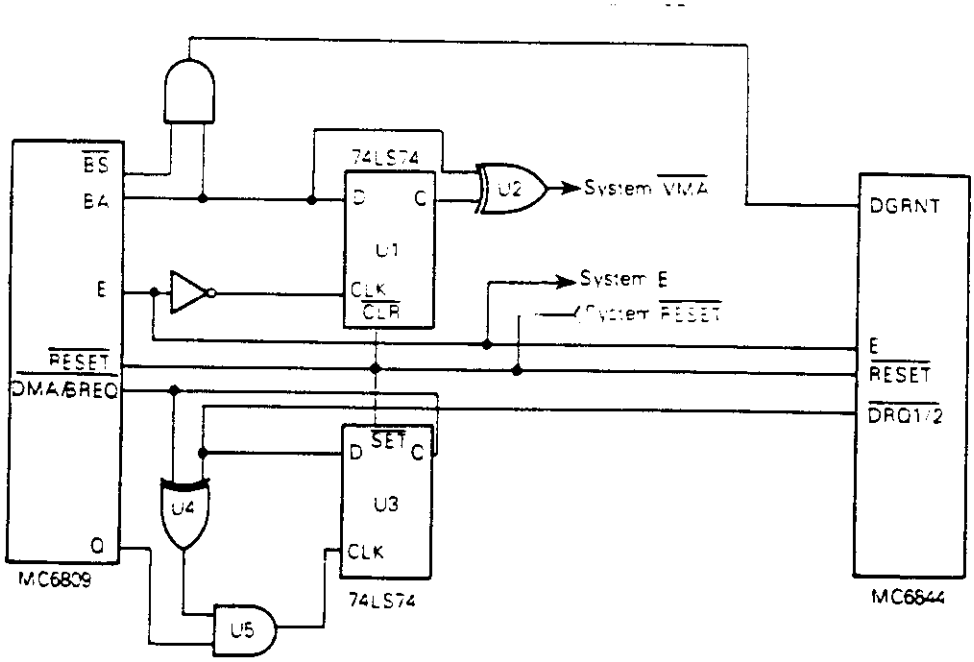
- A direct memory access controller for the M6800 family.
- Four DMA channels, each can be independently configured.
- Each channel: 16-bit address register and 16-bit byte counter register.
- 2 Mbytes/s maximum data transfer.
- Fixed or rotating priority service control.
- Data chain function for large burst of da

MC6844 DMAC Block Diagram



MC6844 DMAC Functions

- Software initialization
- Hardware initialization
- Bus control
- Transfer modes
- MC6844/MC6809 bus arbitration



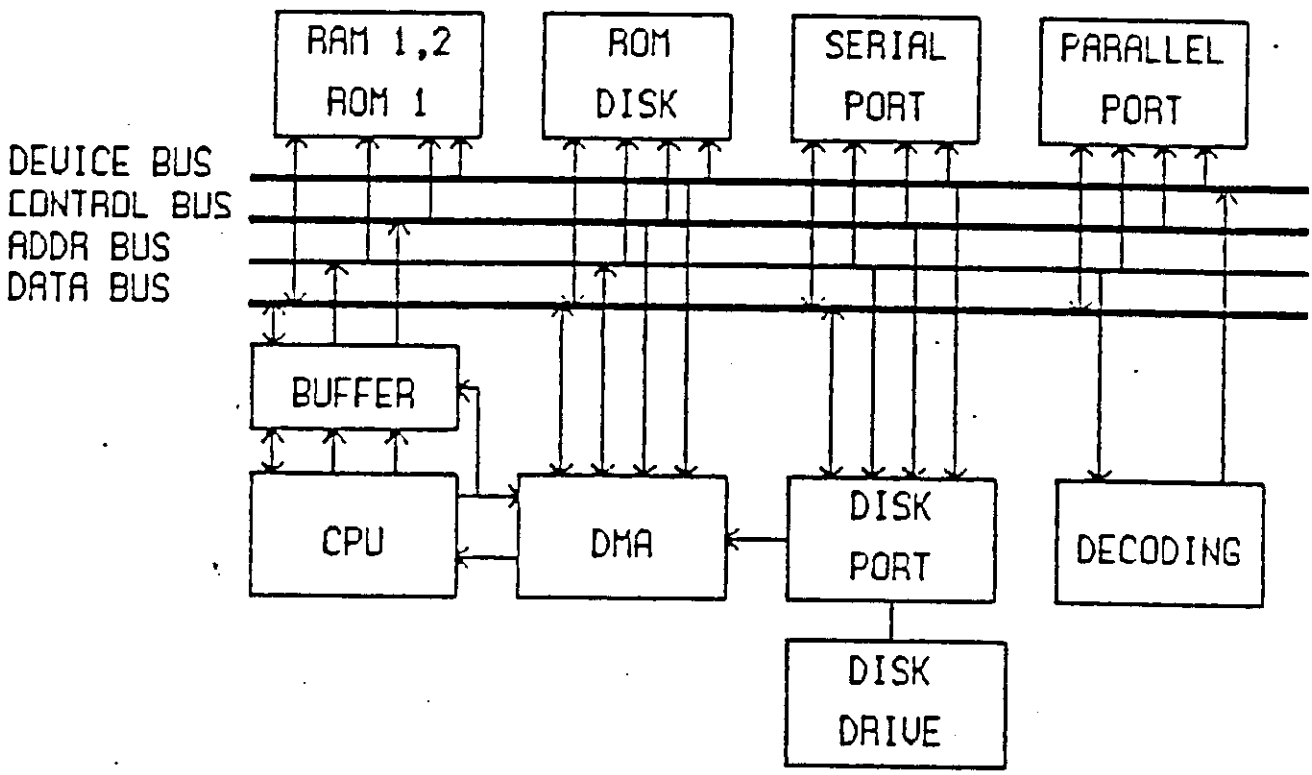
ROSY Junior Overview

- A bit of history
- A 6809 development system featuring
  - Dual microfloppy disks
  - Virtual disks
  - Resident OS – ROSY
  - DOS — FLEX & OS-9
  - Two-page memory
  - Compact design
  - Compatible with ROSY

ROSY Junior Hardware Features

- MC68B09 2 MHz MPU
- 128 Kbytes EPROM (2 pages)
- 64 Kbytes RAM (2 pages)
- Two 3.5 in floppy disks (single & double density)
- Three serial links for terminal, host & printer
- One parallel interface for general use
- Extension bus
- Plugged-on memory unit with 640 Kbytes EPROM & 160 Kbytes RAM
- DMA for floppy disk transfer
- PALs as glue chips

ROSY Junior Hardware Layout



ROSY Junior Memory Maps

Address	Rosy/Flex	OS-9
F000-FFFF	Rosy monitor	OS-9 kerne
EC00-EFFF	Io device	devic
E800-EBFF	Floppy driver	Floppy driver
C000-E7FF	RAM2	RAM2
A000-BFFF	Rosy monitor	RAM2
8000-9FFF	RAM2	RAM2
0000-7FFF	RAM1	RAM1

ED00-EDFF Bus conector CSD

Address	Device	use
EF40-EF7F	I/O BUS	LOGIDULES
EF30-EF38	Bus connector	User port C(CSC)
EF28-EF2F	Bus connector	User port B(CSB)
EF20-EF28	Bus connector	User port A(CSA)
EF18-EF18	74LS273(U12)	RMSK(Logical sector number)
EF00-EF03	SY6551A(U20)	ACIA2(serial printer)
EE00-EEFF	ROM2	Romdisk window
ECC0-ECDF	MC68B44(U24)	DMA channel
EC84-EC87	WD2793	WD(floppy controller)
EC82-EC82	74LS74(U29)	DIC(disk interrupt control)
EC81-EC81	74LS245(U30)	PIR(Polling interrupt)
EC80-EC80	74LS273(U32)	DRS(drive select)
EC54-EC55	MC68B50(U18)	ACIA1(host communication)
EC18-EC1F	MC68B40(U13)	PTM(trace timer)
EC14-EC15	MC68B50(U19)	ACIA0(terminal)
EC10-EC13	MC68B21(U23)	PIA0(parallel port)

ROSY Junior Memory Subsystem

- Supports two operating systems by page swapping.
- One 64-Kbyte EPROM (U08) is split into two pages by a select signal (OS9); lower half for ROSY monitor and upper half for OS-9 kernel.
- Another 64-Kbyte EPROM (U09) is used as ROMDISK.
- One 32-Kbyte RAM (U10) provides contiguous memory block $0000–$7FFF.
- Another 32-Kbyte RAM (U11) is used partly for ROSY/FLEX (18 Kbytes) and partly for OS-9 (26 Kbytes).
- Page or OS select signal (OS9) is at $EF10. Writing a 1 selects OS-9 operating system; a 0 selects ROSY/FLEX operating system. On power-up, ROSY/FLEX is selected.

Peripheral Subsystem

- **Serial Interface**
  - MC68B50 ACIA (U18) for TERMINAL
  - MC68B50 ACIA (U19) for HOST
  - SY6551A ACIA (U20) for PRINTER
  - MAX232 (U21, U22) as RS232C interface (single 5V supply)
  - Interrupts of U18, U19: NMI in ROSY/FLEX mode, IRQ in OS-9 mode.
  - Interrupts of U20: no interrupt in ROSY/FLEX mode, IRQ in OS-9 mode.

Peripheral Subsystem

- **Parallel Interface**
  - MC68B21 (U23) provides parallel interface for general use
  - Jumper selectable IRQ/FIRQ

- **Programmable Timers**
  - MC68B40 PTM provides programmable timers
  - One channel provides 100-Hz signal for real-time clock
  - Interrupts: NMI in ROSY/FLEX mode, IRQ in OS-9 mode.

Floppy Disk Subsystem

- Two 3.5 inch microfloppy disks
  - Data rate: 125 Kbits/s or 250 Kbits/s
  - Single or double sided
  - 48 or 96 tracks/inch
- WD2793 (U28) floppy disk controller
- A 74LS273 octal D flip-flop (U32) as disk select register at $EC80
  - Bit 0–3 select drive
  - Bit 5 selects density
  - Bit 7 selects side
- MC68B44 DMAC (U24) for data transfer
  - Uses Mode 2 (single byte transfer) so that system regains bus control after each byte transfer to support multitasking.
  - Bus arbitration problem
  - Interrupt technique