UNITED NATIONS EDUCATIONAL, SCIENTIFIC AND CULTURAL ORGANIZATION
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I.C.T.P., P.O. BOX 586, 34100 TRIESTE, ITALY, CABLE: CENTRATOM TRIESTE

UNITED NATIONS INDUSTRIAL DEVELOPMENT ORGANIZATION

INTERNATIONAL CENTRE FOR SCIENCE AND HIGH TECHNOLOGY
c/o INTERNATIONAL CENTRE FOR THEORETICAL PHYSICS 34100 TRIESTE (ITALY) VIA GRIGNANO, 9 (ADRIATICO PALACE) P.O. BOX 586 TELEPHONE 040-224572 TELEFAX 040-224575 TELEX 460449 APH I

SMR/474 - 7

**COLLEGE ON**
**"THE DESIGN OF REAL-TIME CONTROL SYSTEMS"**
**1 - 26 October**

# *D-A, A-D CONVERSION*

**Dario CROSETTO**
**C.E.R.N.**
**S.P.S. Division**
**CH-1211 Geneva 23**
**Switzerland**

# 1. SIGNAL ANALYSIS.

## 1.1. Signal Classification.

Signal analysis in its widest application simply means the extraction of useful information from input data.

Input data can be, by nature, either continuouse) or discrete as a function of some indcpendent either continuous or discrete variable.

According to the methods of analysis chosen, transitions to/from discrete (quantization) are frequently effected.

The transition from continuous to discrete will be called analog-to-digital conversion (ADC) and the inverse transition will be called digital-to-analog conversion (DAC). As well quantization of the input signal when done will be effected at regular intervals of the independent variables.

Signals can be classified as **continuous or discrete; deterministic or stochastic.**

In the whole picture of Data Analysis, the particular case of treatment of signal of our interest are stochastic with an independent variable (continuous or discrete) in the time or frequency domain and a dependent variable in continuous or discrete form.

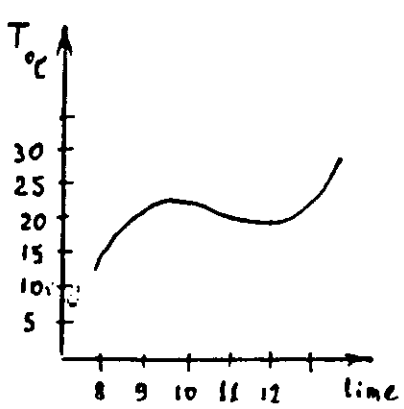


Figure 1a.

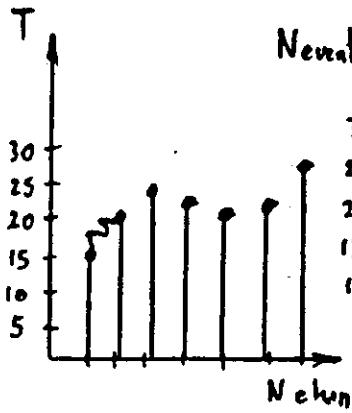


Figure 1b.

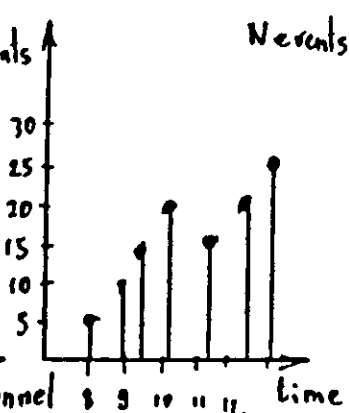


Figure 1c.

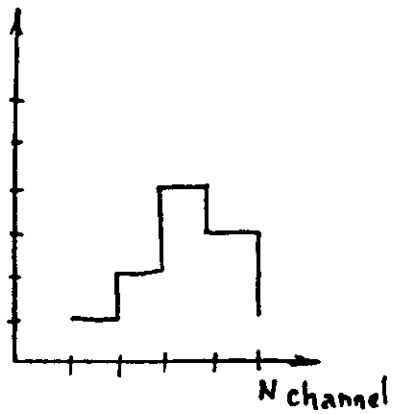


Figure 1d.

Figure 2b illustrates the transformation of a continuous time variable signal in the Digital Signal Processing phases.

- The continuous time variable input signal is first transformed into Pulsed Amplitude Modulation (PAM) by the Sampling and Hold (S/H) (independent variable = discrete, dependent variable = continuous),

- then is transformed to a Pulse Code Modulation (PCM) by the Analog-to-Digital converter (A/D) (independent variable = discrete, dependent variable = discrete),

- then the signal is processed digitally by the Digital Signal Processor (DSP), Discrete Results are then transformed by Digital-to-analog converter (DAC) in analog signals (independent variable = discrete, dependent variable = continuous),

- finally the analog signal is filtered (independent variable = continuous, dependent variable = continuous).

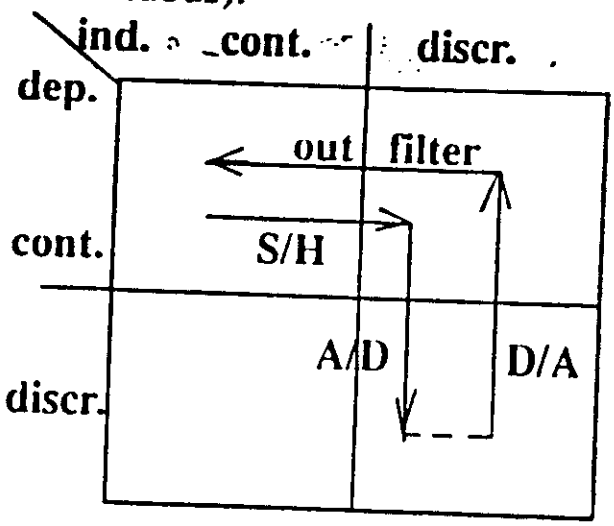



Figure 2a. Transformations of the independent and dependent variables in the Digital Signal Processing phases.

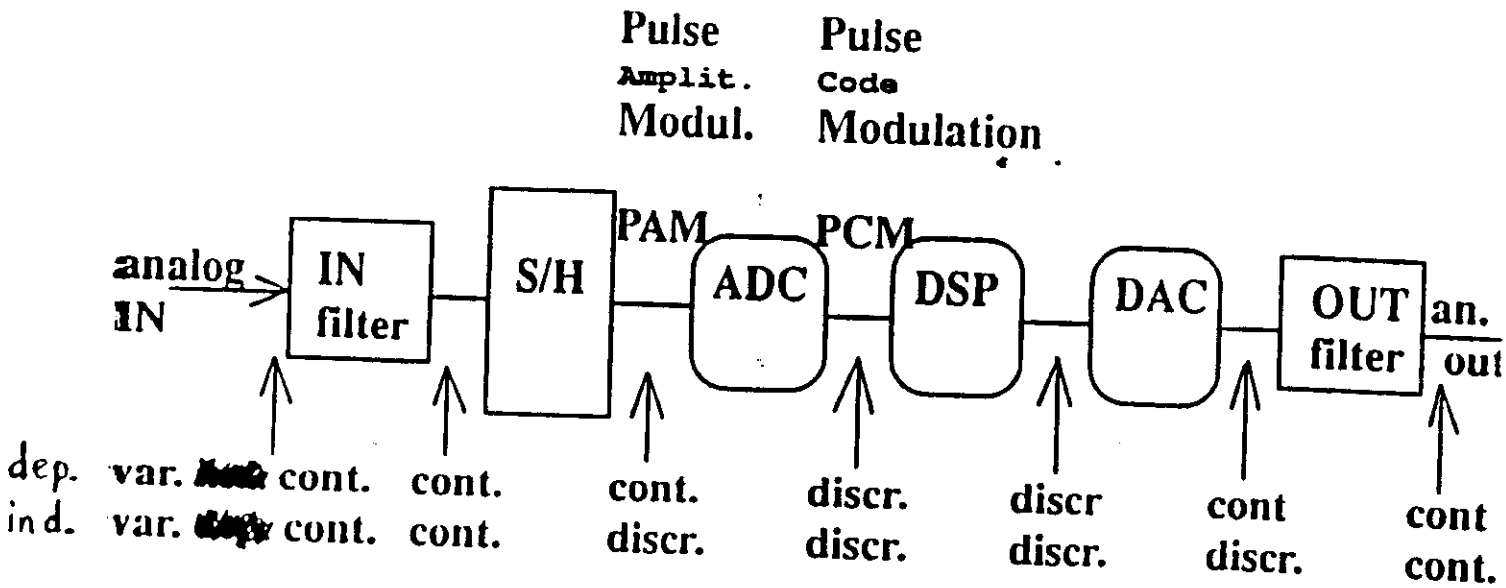



Figure 2b. Block diagram of the units used in a digital processing analog signals

# CONVERSION TECHNIQUES

## 1) D/A Converter

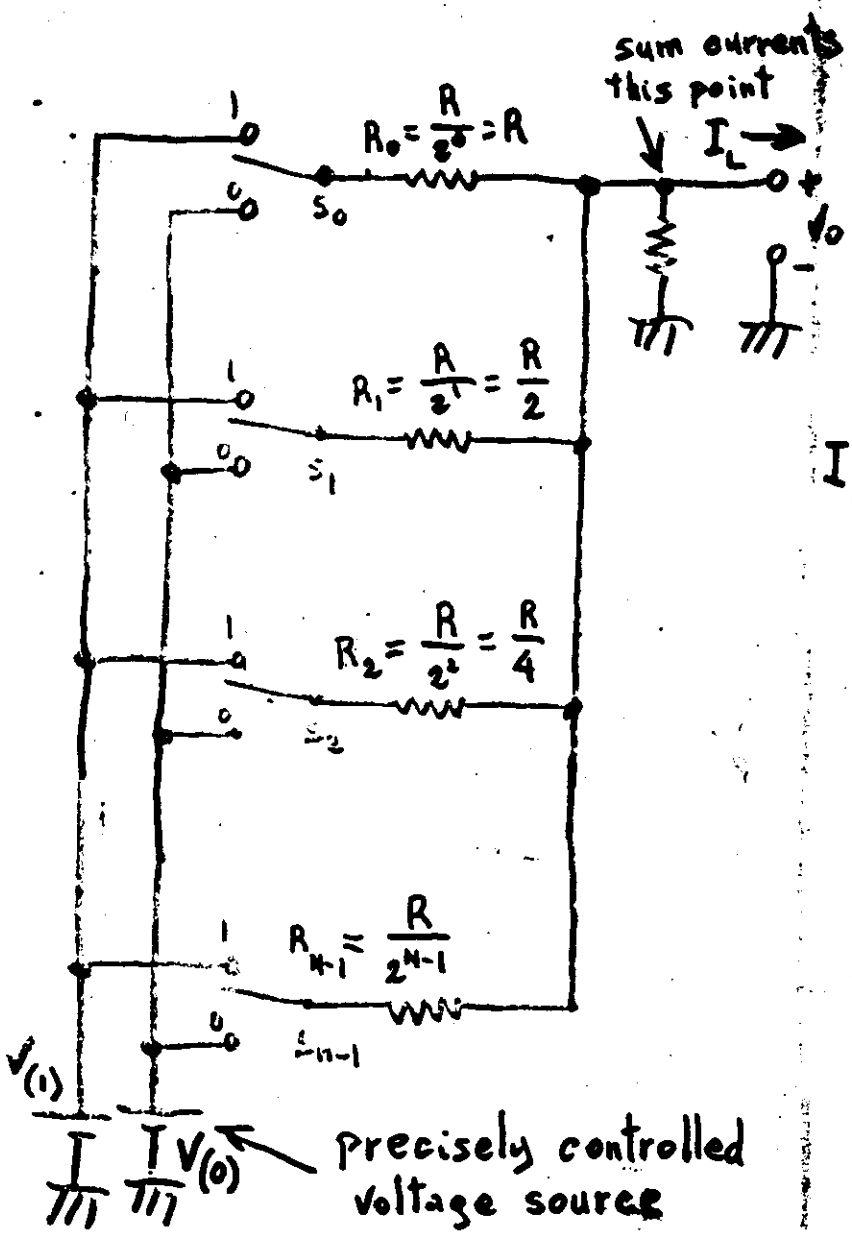
- Weighted Resister
- R-2R Resistive Ladder
- Current
- Voltage

## 2) A/D Converter

- Comparator Converter
- Successive approximation converters
- Counter converters
- Voltage to Frequency
- Voltage to Time
- The dual-slope
- Tracking type (used in communication)
- Parallel Ripple
- Variable Threshold
- Synchronous VTF A/D system.

Example of a circuit converting digital representation to analog form.

# THE WEIGHTED-RESISTOR D/A Converter

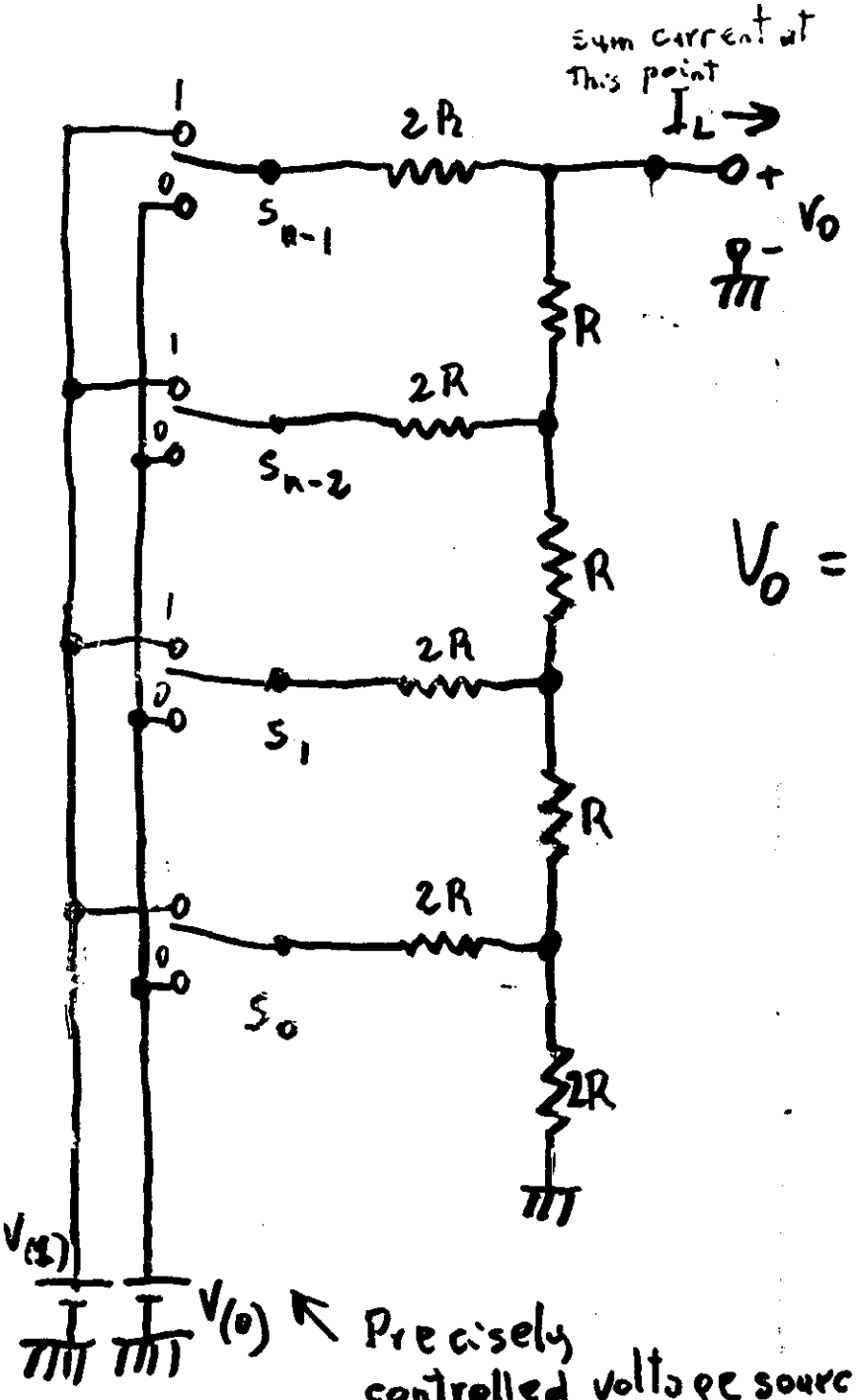



$$I_{LS} = V_R \left( \frac{S_{N-1}}{R_{N-1}} + \frac{S_{N-2}}{R_{N-2}} + \cdots \frac{S_0}{R_0} \right)$$

$$= \frac{V_R}{R} \left( S_{n-1} 2^{N-1} + S_{N-2} 2^{N-2} + \cdots + S_0 2^0 \right)$$

-Let us assume that $V_{(1)} = V_R$, a fixed reference voltage, that $V_{(0)} = 0$, that is, all 0 switch positions are grounded and that the load $R_L = 0$ (in which case $V = 0$). Then the output current $I_L$ is readily calculated in terms of the switch positions.

# R 2R Ladder network D/A Converter




$$V_0 = V_{(1)}\left(\frac{1}{2}S_{n-1} + \frac{1}{4}S_{n-2} + \cdots \frac{1}{2^n}S_0\right)$$

↖ Precisely controlled voltage source

# SPECIFICATIONS for a D/A converte

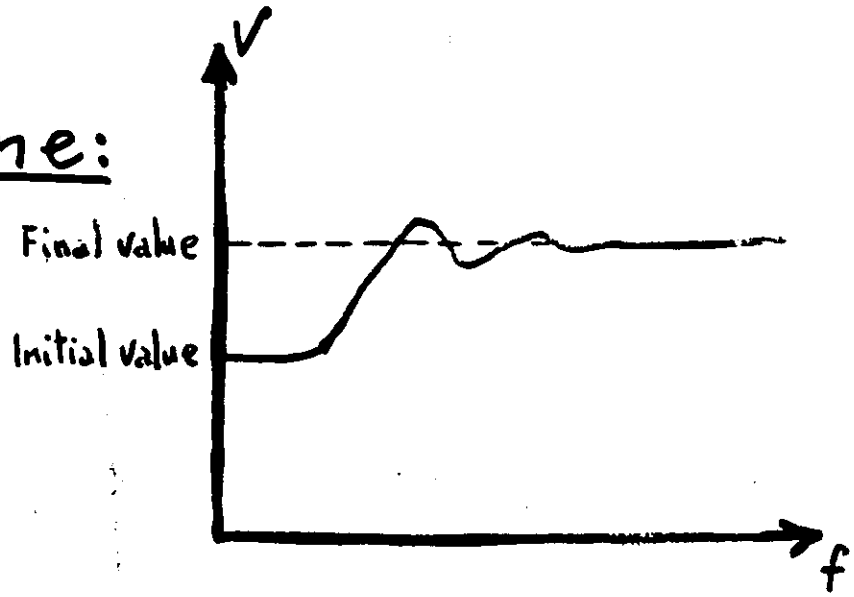
**Resolution**: This term specifies the number of bits the converter can accommodate and correspondingly the number of output voltage (or currents). i.e. the number of possible output voltages of a converter which can accept 10 input bits is $2^{10} = 1,024$. The smallest possible output change in output voltage is $\frac{1}{1024}$ of full scale output range. ~ resolution 1 part in 1000 or 0.1 percent.

**Linearity**: In an ideal D/A converter equal increments in the numerical significance of the digital-input should yield equal increments in the analog output.

**Accuracy**: The accuracy of a converter is a measure of the difference between the actual analog output voltage and what the output should be in the ideal case. Lack of linearity contributes to inaccuracy.

## Settling time:

When the digital input to a converter changes, switches open and close and abrupt voltage changes appear.




Not only there is a finite time required to reach the new output level, but also an oscillation may occur.

The interval that elapses from the input change to the time when the output has come close enough to its final value is called the settling time. The settling time depends, among other things, on how we define "close enough". Typically a general purpose converter might have a settling time given as "500 ns to 0.2% full scale".

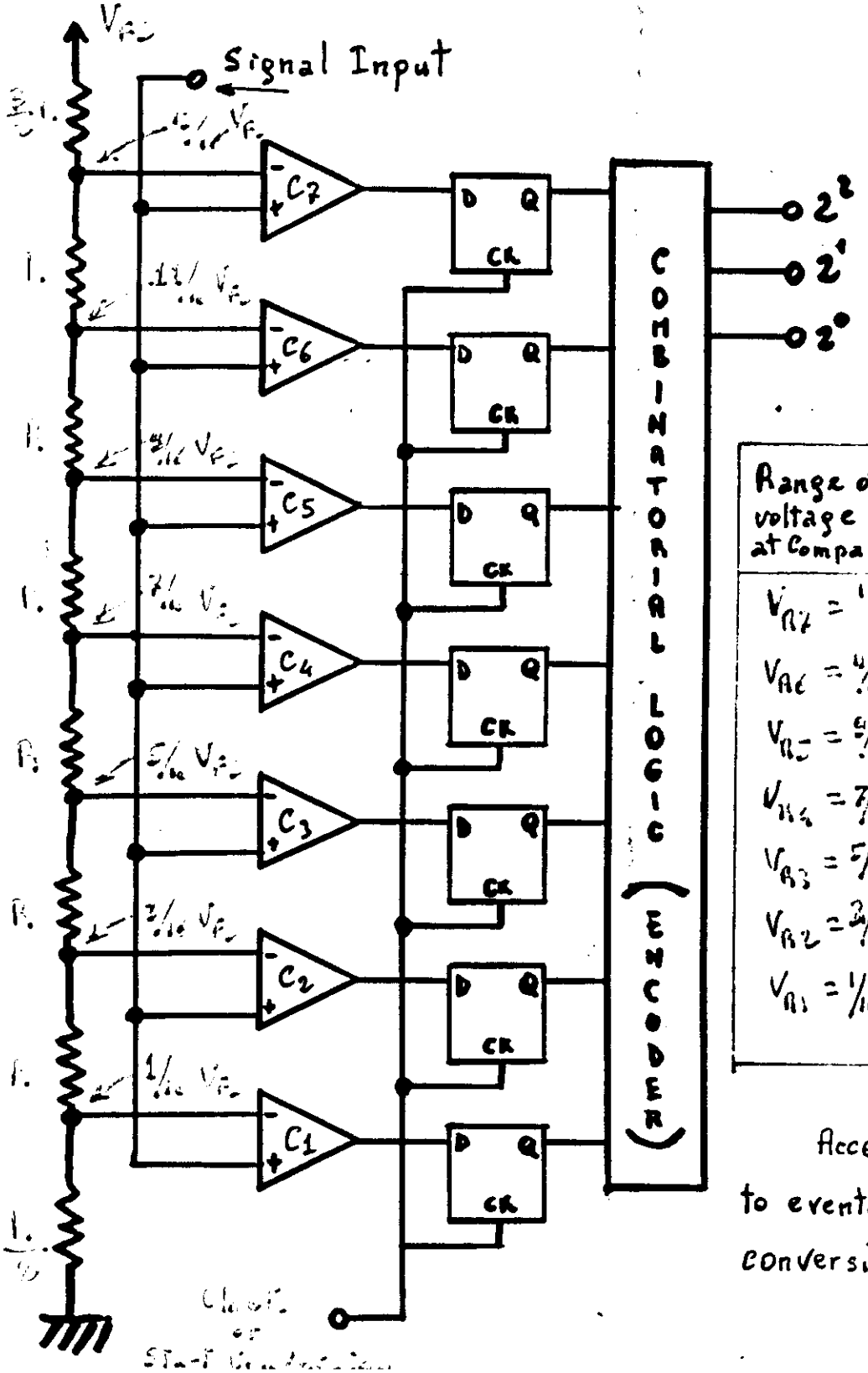
**Temperature sensitivity**: At any fixed digital input, the analog output will vary with temperature.

# PARALLEL OR FLASH A/D

The unknown $V_x$ input voltage is simultaneously compared to seven different reference voltages.

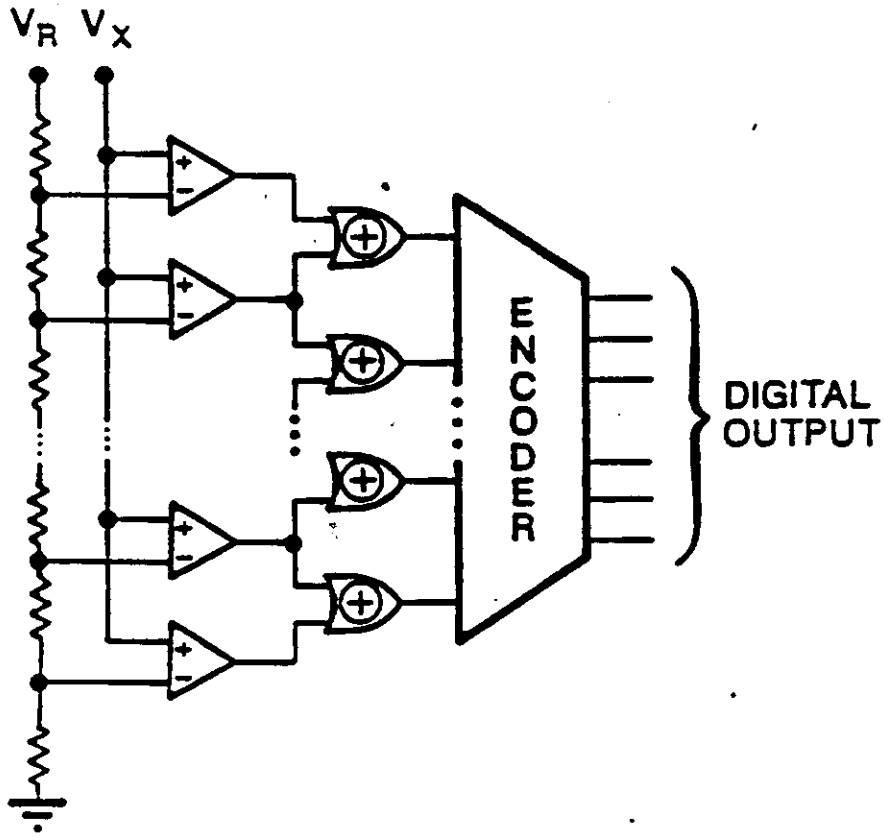
$2^{n-1}$ COMPARATORS are needed for n-bit CONVERTER

CONVERSION RATE 10 ÷ 100 MHz




| Range of analog voltage input at Comparator | Binary Digital output | Analog Volt Output fr D/A |
|---|---|---|
| $V_{R7} = 13/16\ V_{FS}$ | 1 1 1 | $7/8\ V_{FS}$ |
| $V_{R6} = 11/16\ V_{FS}$ | 1 1 0 | $3/4\ V_{FS}$ |
| $V_{R5} = 9/16\ V_{FS}$ | 1 0 1 | $5/8\ V_{FS}$ |
| $V_{R4} = 7/16\ V_{FS}$ | 1 0 0 | $1/2\ V_{FS}$ |
| $V_{R3} = 5/16\ V_{FS}$ | 0 1 1 | $3/8\ V_{FS}$ |
| $V_{R2} = 3/16\ V_{FS}$ | 0 1 0 | $1/4\ V_{FS}$ |
| $V_{R1} = 1/16\ V_{FS}$ | 0 0 1 | $1/8\ V_{FS}$ |
| | 0 0 0 | 0 |

Access to resistor "R" ladder to eventually form a non linear conversion law (compression for exa




# PARALLEL A/D CONVERTER

- HIGH SPEED, $f_s$ = 10MHz ⟶ 500MHz
- COMPLEX, REQUIRES $2^N$ COMPARATORS (256 FOR 8 BITS)
- USED MAINLY IN VIDEO AND RADAR PROCESSING FOR LOW RESOLUTION, HIGH SPEED

# Summary of High Speed ADC Performance

This table is a summary of data points on pubished high-speed ADCs over the last 8 years, in order of pubilcation.

Notes:

1. F/M1 is ratio of sampling rate to equivalent technology ft multipled by $10^3$
2. F/M2 is area in square mils normalized by a factor (feature size in microns)$^2$. This is really not very useful since of course pads don't scale. However, it gives a general indication of trends. This was done only for the CMOS converters

| Author | Type | rate | bits | tech | S/H? | PSV | Pwr | Area | F/M1 | F/M2 |
|---|---|---|---|---|---|---|---|---|---|---|
| Sekino,Sony ISSCC82 | 2step | 30M | 8 | 4Gbip | N | 5V | 0.7 | 35K | 7.5 | |
| Tsukada,Hitachi ISSCC85 | FL | 25M | 8 | 2uCMOS | Y | 5V | 0.3 | 33K | 16 | 8.2K |
| Dingwall, RCA ISSCC85 | 2step | 5M | 8 | 2uCMOS | Y | 5V | 0.15 | 6K | 3.3 | 1.5K |
| Peetz, HP ISSCC86 | FL | 250M | 8 | 7Gbip | N | 5 | 12 | 48K | 36 | |
| Lewis,UCB ISSCC86 | Pipe | 5M | 9 | 3uCMOS | Y | 10 | 0.18 | 10K | 7.2 | 1.1K |
| V.D.Grift,Phil ISSCC87 | Fold | 50M | 8 | 7.5Gbip | N | 5 | 0.3 | 10K | 6.6 | |
| Yoshi,Sony ISSCC87 | FL | 350M | 8 | 10Gbip | N | 5 | 1.5 | 22K | 35 | |
| Akazawa,NTT ISSCC87 | FL | 400M | 8 | 18Gbip | N | 5 | 2.7 | 65K | 22 | |
| Tsutomoto,NTT ISSCC88 | FL | 2G | 6 | 26Gbip | N | 5 | 2 | 18K | 76 | |
| V.D.Plaasche,Ph ISSCC88 | Fold | 100M | 8 | 12Gbip | N | 5 | 0.8 | 17K | 8.3 | |

| | | | | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|
| Matsuura,Hita ISSCC88 | 2step | 20M | 8 | 2u | Y | 5 | .0.2 | 11K | 13 | 2.75K |
| Song,Univ Ill ISSCC88 | Pipe | 1M | 12 | 1.5CMOS | Y | 5 | 0.4 | 7.8K | 0.4 | 3.5K |
| Shimitzu ISSCC88 | 2step | 20M | 10b | 4.5Gbip | Y | 5 | 0.9 | 40K | 4.4 | |
| Kerth, Xtal CICC88 | 2step | 1M | 12b | 3uCMOS | Y | 10 | .7 | 150K | 1.4 | 16.6K |
| Masayuki,NTT ISSCC89 | 2st | 40M | 8b | 1uCMOS | Y | 5 | 0.6 | 20K | 8.0 | 20K |
| Chin, Nat ISSCC89 | 2st | 1.5M | 10b | 2uCMOS | N | 5 | 0.15 | 15K | 1.0 | 3.7K |
| Fukishima,Sony ISSCC89 | 2st | 40M? | 8b | 1.4CMOS | Y | 5 | 0.1 | 8.1K | 22.2 | 3.7K |
| Robertson, AD ISSCC90 | Pipe | 20M | 10b | BICMOS | Y | 5 | 1.0 | 85K | 10.0 | |
| Song, Univ Ill ISSCC90 | 2step | 15M | 10b | 1uCMOS | Y | 5 | 0.250 | 4K | 3.0 | 4K |
| Zojer,Seimens ISSCC90 | 2step | 75M | 10b | 7Gbip | Y | 5 | 2 | 23K | 10.7 | |
| Mats,Mistub ISSCC90 | 2st | 30M | 10b | 7GBCMOS | Y | 10 | 0.75 | 40K | 4.3 | |
| Lin, UCB VLSI90 | Pipe | 2.5M | 13b | 3uCMOS | Y | 5V | 0.1 | 40K | 3.6 | 4.4K |
| | | | | | | | | | | |

# Flash A/D Converters

Flash Converters hold the Speed Records

>1Gsample/sec in HBT
>300Mhz in SI Bipolar

Many Key Design Issues:

Nonlinear Distortion in Sample/Hold

Jitter on Sampling Clock

Capacitive Loading on Source

Comparator Kickback

Supply Noise and Packaging

[redacted]

Flash Converters are Hardware Intensive

Area, Power large expecially at or above 8 bits

Alternatives preferable if speed can be acheived

Most flash converters of commercial importance are bipolar to get max speed

## Problem: How Do We Implement High-throughput ADC Functions(ie one Output Sample per clock) at High Resolutions (ie >10bits)

Traditional Approaches:

1. Flash Converters

    a. Exponentially increasing hardware

    b. Impractical above 8 bits

    c. Large power dissipation and input capacitance

2. Two-step Flash Converters

    a. Requires multiple clocks per conversion

    b. Still exponential hardware with resolution

Alternative Approach:

3. Feedforward, or Pipelined Approach

    a. High degree of concurrency

    b. Approximately linear hardware with resolution

    c. Difficult analog design challenge

# Summary of High Speed ADC Performance

This table contains all the ADC dats points sorted by speed figure of merit. Both CMOS and Bipolar are included.

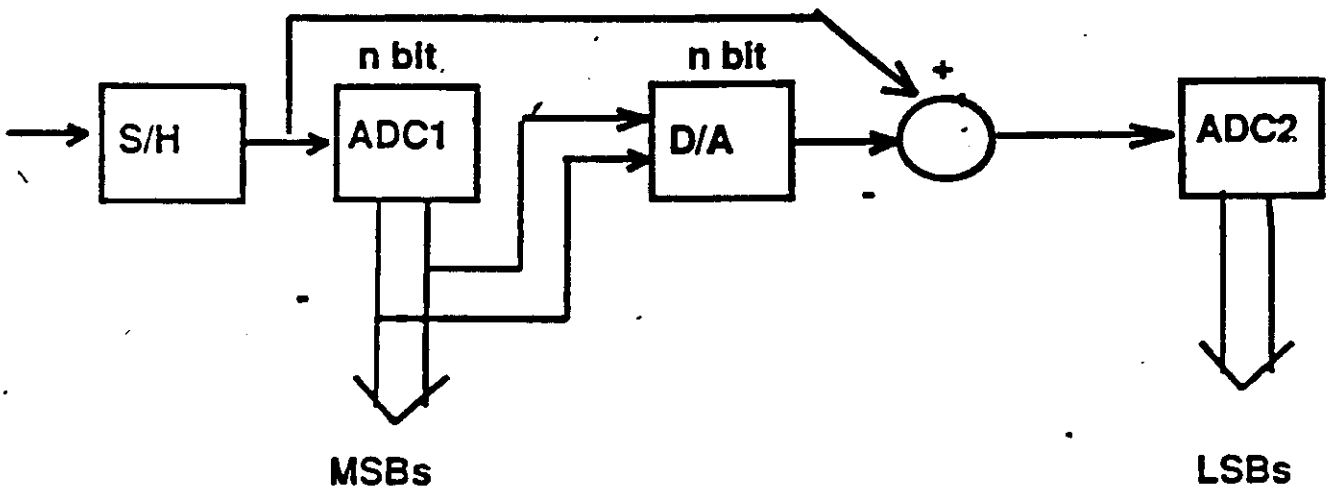
Notes:

1. F/M1 is ratio of sampling rate to equivalent technology ft multipled by $10^3$
2. F/M2 is area in square mils normalized by a factor (feature size in microns)$^2$. This is really not very useful since of course pads don't scale. However, it gives a general indication of trends. This was done only for the CMOS converters

| Author | Type | rate | bits | tech | S/H? | PSV | Pwr | Area | F/M1 | F/M2 |
|---|---|---|---|---|---|---|---|---|---|---|
| Tsutomoto,NTT | FL | 2G | 6 | 26Gbip | N | 5 | 2 | 18K | 76 | |
| Peetz,HP | FL | 250M | 8 | 7Gbip | N | 5 | 12 | 48K | 36 | |
| Yoshi,Sony | FL | 350M | 8 | 10Gbip | N | 5 | 1.5 | 22K | 35 | |
| Fukishima,Sony | 2st | 40M? | 8b | 1.4CMOS | Y | 5 | 0.1 | 8.1K | 22.2 | 3.7K |
| Akazawa,NTT | FL | 400M | 8 | 18Gbip | N | 5 | 2.7 | 65K | 22 | |
| Tsukada,Hitachi | FL | 25M | 8 | 2uCMOS | Y | 5V | 0.3 | 33K | 16 | 8.2K |
| Matsuura,Hita | 2step | 20M | 8 | 2u | Y | 5 | 0.2 | 11K | 13 | 2.75K |
| Zojer,Seimens | 2step | 75M | 10b | 7Gbip | Y | 5 | 2 | 23K | 10.7 | |

| Author | Type | rate | bits | tech | S/H? | PSV | Pwr | Area | F/M1 | F/M |
|---|---|---|---|---|---|---|---|---|---|---|
| Robertson,AD | Pipe | 20M | 10b | BICMOS | Y | 5 | 1.0 | 85K | 10.0 | |
| V.D.Plaasche,Ph | Fold | 100M | 8 | 12Gbip | N | 5 | 0.8 | 17K | 8.3 | |
| Masayuki,NTT | 2st | 40M | 8b | 1uCMOS | Y | 5 | 0.6 | 20K | 8.0 | 20K |
| Sekino,Sony | 2step | 30M | 8 | 4Gbip | N | 5V | 0.7 | 35K | 7.5 | |
| Lewis,UCB | Pipe | 5M | 9 | 3uCMOS | Y | 10 | 0.18 | 10K | 7.2 | 1.1I |
| V.D.Grift,Phil | Fold | 50M | 8 | 7.5Gbip | N | 5 | 0.3 | 10K | 6.6 | |
| Shimitzu | 2step | 20M | 10b | 4.5Gbip | Y | 5 | 0.9 | 40K | 4.4 | |
| Mats.,Mistub | 2st | 30M | 10b | 7GBCMOS | Y | 10 | 0.75 | 40K | 4.3 | |
| Lin,UCB | Pipe | 2.5M | 13b | 3uCMOS | Y | 5V | 0.1 | 40K | 3.6 | 4.4I |
| Dingwall,RCA | 2step | 5M | 8 | 2uCMOS | Y | 5V | 0.15 | 6K | 3.3 | 1.5I |
| Song,Univill | 2step | 15M | 10b | 1uCMOS | Y | 5 | 0.250 | 4K | 3.0 | 4K |
| Kerth,Xtal | 2step | 1M | 12b | 3uCMOS | Y | 10 | .7 | 150K | 1.4 | 16.( |
| Chin,Nat | 2st | 1.5M | 10b | 2uCMOS | N | 5 | 0.15 | 15K | 1.0 | 3.7 |
| Song,Univill | Pipe | 1M | 12 | 1.5CMOS | Y | 5 | 0.4 | 7.8K | 0.4 | 3.5 |

# Two-Step Flash ADC




Advantages:

Much less area than straight flash

Disadvantages:

→ Requires at least three full clocks

Requires precisioninterstage processing

Grows exponentially with number of overall bits

Widely used in 1 -1.5 micron CMOS for 20Mhz 8bit video ADC

# Summary of Two-Step ADC Performance(ISSCC)

This table is a summary of data points on pubished on CMOS two-step flash converters over the last 8 years, in order of publication.

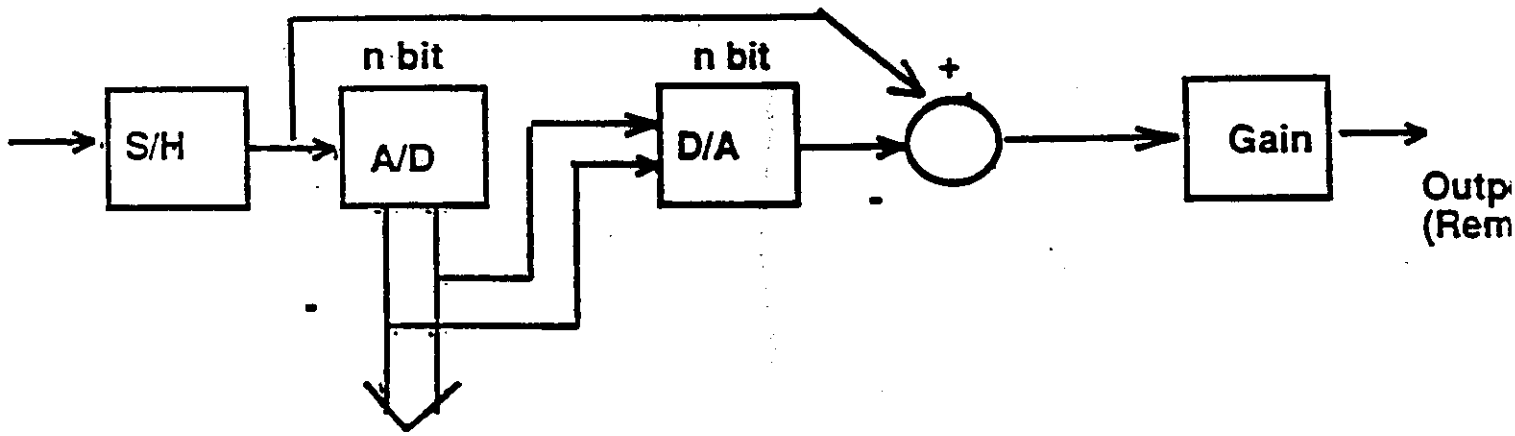
Notes:

1. F/M1 is ratio of sampling rate to equivalent technology ft multipled by $10^3$

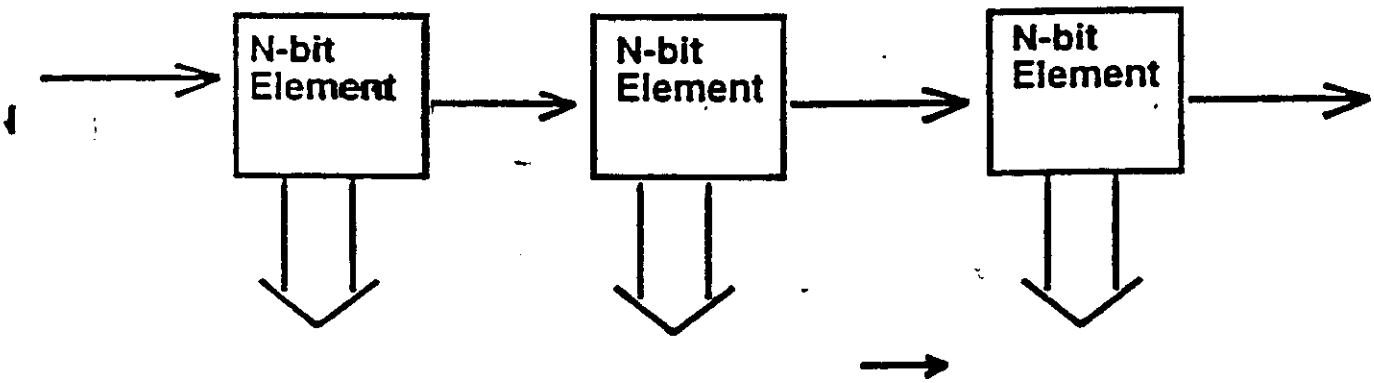
2. F/M2 is area in square mils normalized by a factor (feature size in microns)$^2$. This is really not very useful since of course pads don't scale. However, it gives a general indication of trends. This was done only for the CMOS converters

| Author | Type | rate | bits | tech | S/H? | PSV | Pwr | Area |
|---|---|---|---|---|---|---|---|---|
| Dingwall, RCA<br><br>ISSCC85 | 2step | 5M | 8 | 2uCMOS | Y | 5V | 0.15 | 6K |
| Matsuura,Hita<br>ISSCC88 | 2step | 20M | 8 | 2u | Y | 5 | 0.2 | 11K |
| Shimitzu<br>ISSCC88 | 2step | 20M | 10b | 4.5Gbip | Y | 5 | 0.9 | 40K |
| Kerth, Xtal<br>CICC88 | 2step | 1M | 12b | 3uCMOS | Y | 10 | .7 | 150K |
| Masayuki,NTT<br>ISSCC89 | 2st | 40M | 8b | 1uCMOS | Y | 5 | 0.6 | 20K |
| Chin, Nat<br>ISSCC89 | 2st | 1.5M | 10b | 2uCMOS | N | 5 | 0.15 | 15K |
| Fukishima,Sony<br>ISSCC89 | 2st | 40M? | 8b | 1.4CMOS | Y | 5 | 0.1 | 8.1K |
| Song, Univ Ill<br>ISSCC90 | 2step | 15M | 10b | 1uCMOS | Y | 5 | 0.250 | 4K |
| Zojer,Seimens<br>ISSCC90 | 2step | 75M | 10b | 7Gbip | Y | 5 | 2 | 23K |
| Mats.,Mistub<br>ISSCC90 | 2st | 30M | 10b | 7GBCMOS | Y | 10 | 0.75 | 40K |
| | | | | | | | | |

# Quantized Feedforward ADCs




N-bit Element




Complete A/D Converter

Advantages:

Same throughput as flash

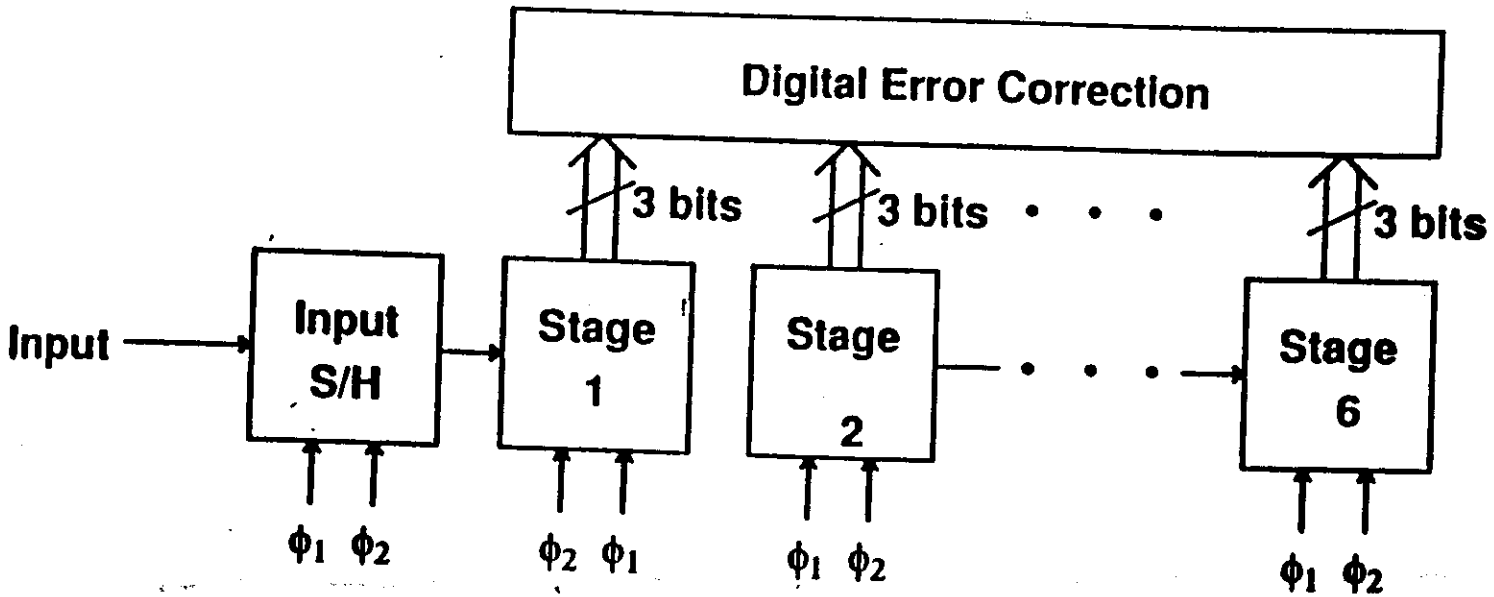
Much less hardware than flash

Digital correction, self-cal

Disadvantages:

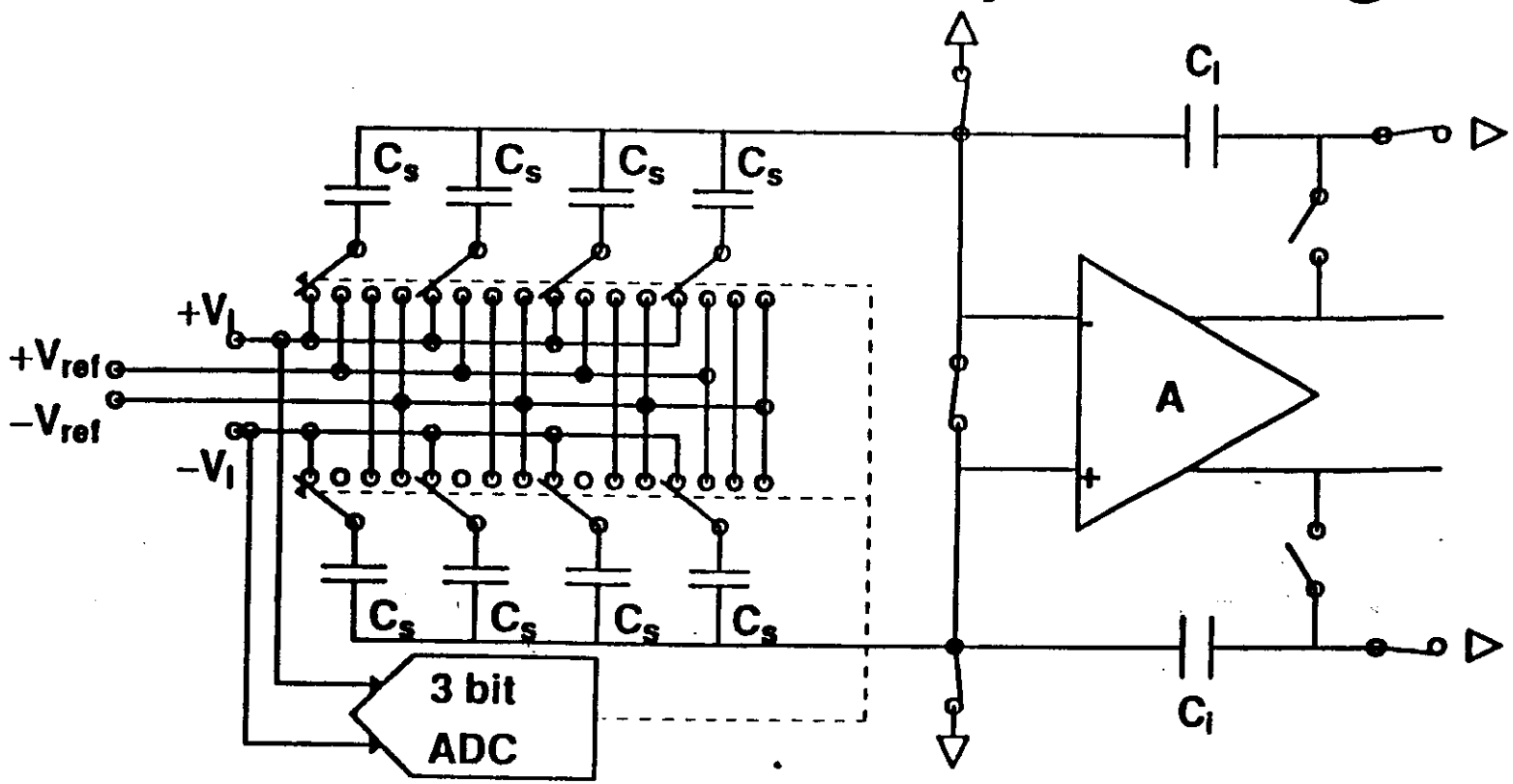
Requires Fast Interstage Processing

# 13 Bit Pipelined ADC Prototype




- 6 stages, 3 bits/stage
- Digital error correction
- 1st & 2nd stage are calibrated
- Fully differential

# Block Diagram of Pipeline Stage




| | S/H | 1st | 2nd | 3rd | 4th | 5th | 6th |
|---|---|---|---|---|---|---|---|
| $\sum C_s$ | 4 pF | 4 pF | 2 pF | 1 pF | 1 pF | 1 pF | 1 pF |
| Interstage gain | 2 | 4 | 4 | 4 | 4 | 4 | — |
| Digital error correction | — | yes | yes | yes | yes | yes | no |
| Calibration | no | yes | yes | no | no | no | no |

# Summary of High Speed ADC Performance

This table is a summary of data points on pubished high-speed pipeline ADCs over the last 8 years, in order of pubilcation.

Notes:

1. F/M1 is ratio of sampling rate to equivalent technology ft multipled by $10^3$

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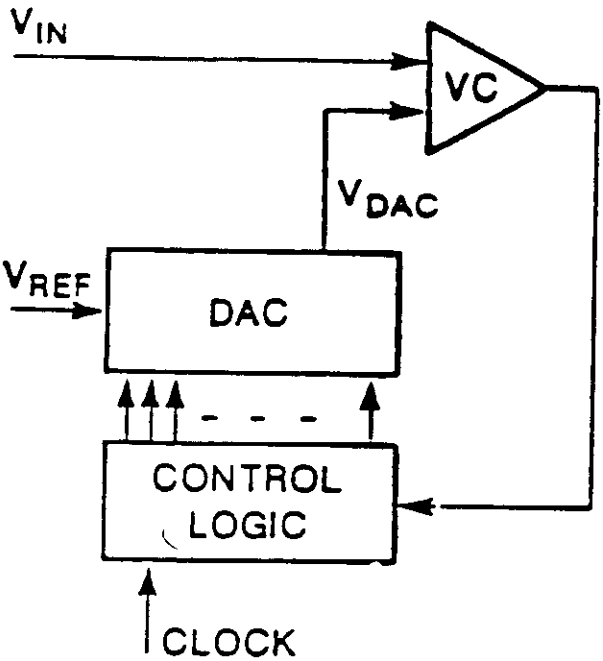
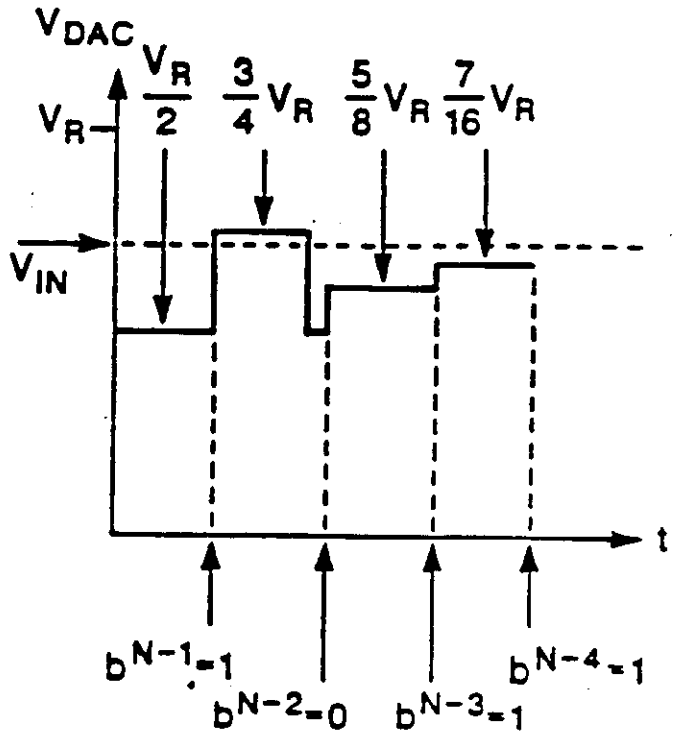
| Author | Type | rate | bits | tech | S/H? | PSV | Pwr | Area | F/M1 | F/M |
|---|---|---|---|---|---|---|---|---|---|---|
| Lewis,UCB ISSCC86 | Pipe | 5M | 9 | 3uCMOS | Y | 10 | 0.18 | 10K | 7.2 | 1.1K |
| Song,Univ Ill ISSCC88 | Pipe | 1M | 12 | 1.5CMOS | Y | 5 | 0.4 | 7.8K | 0.4 | 3.5K |
| Robertson, AD ISSCC90 | Pipe | 20M | 10b | BICMOS | Y | 5 | 1.0 | 85K | 10.0 | |
| Lin, UCB VLSI90 | Pipe | 2.5M | 13b | 3uCMOS | Y | 5V | 0.1 | 40K | 3.6 | 4.4K |

# SUCCESSIVE-APPROXIMATION A/D CONVERTERS




EXAMPLES

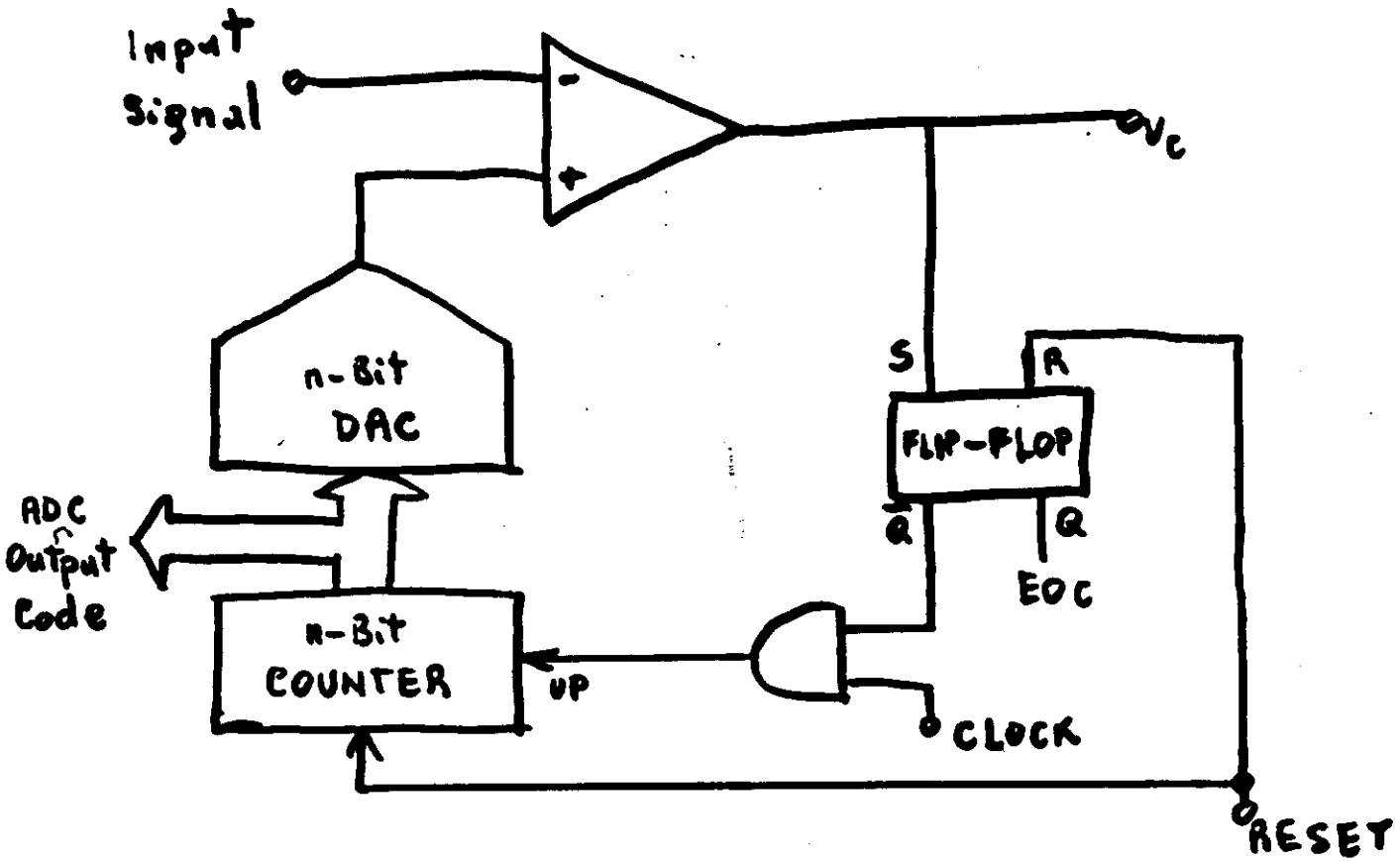
- TRADITIONAL DAC-BASED
- ALGORITHMIC CONVERTERS

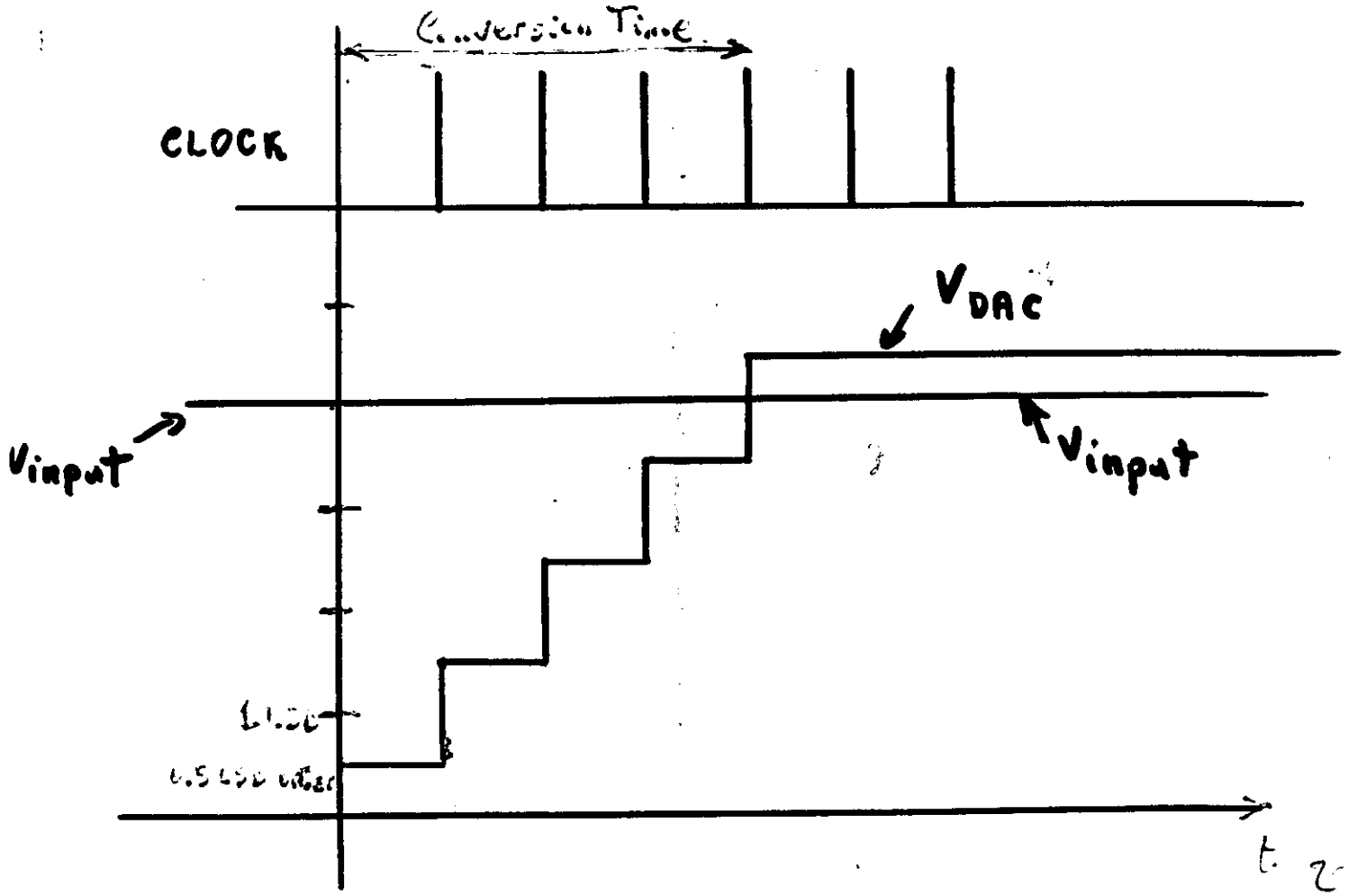
ADVANTAGE

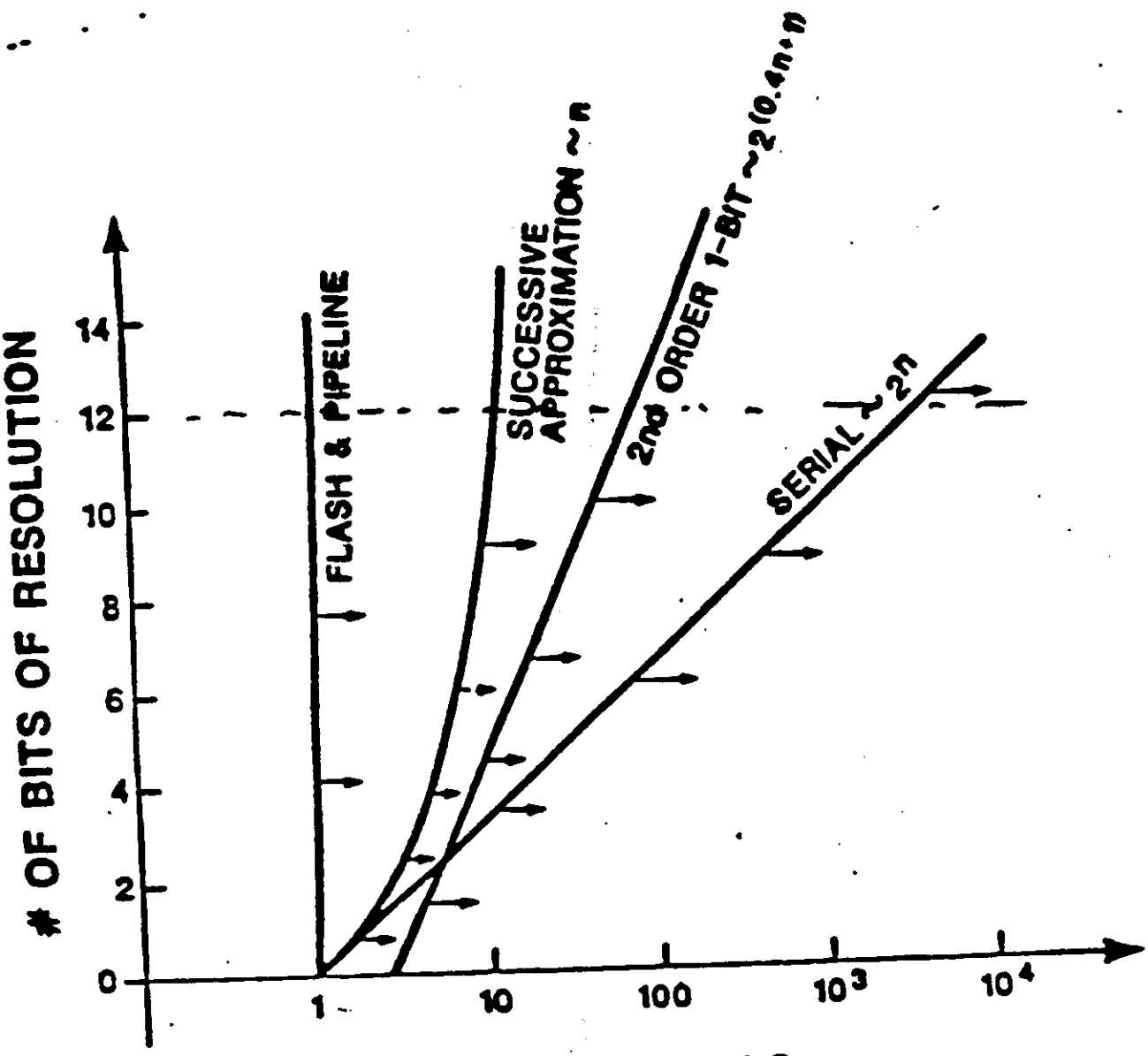
- HIGH-SPEED-CONVERTS IN N CLOCK PERIODS.
  $t_c$ - 20μs

DISADVANTAGE

- DAC REQUIRES COMPONENT MATCH TO $\frac{1}{2^N}$ FOR 1/2 LSB INTEGRAL LINEARITY


Input
Signal
$V_c$
n-Bit
DAC
S
R
FLIP-FLOP
Q̄
Q
EOC
ADC
Output
Code
n-Bit
COUNTER
UP
CLOCK
RESET

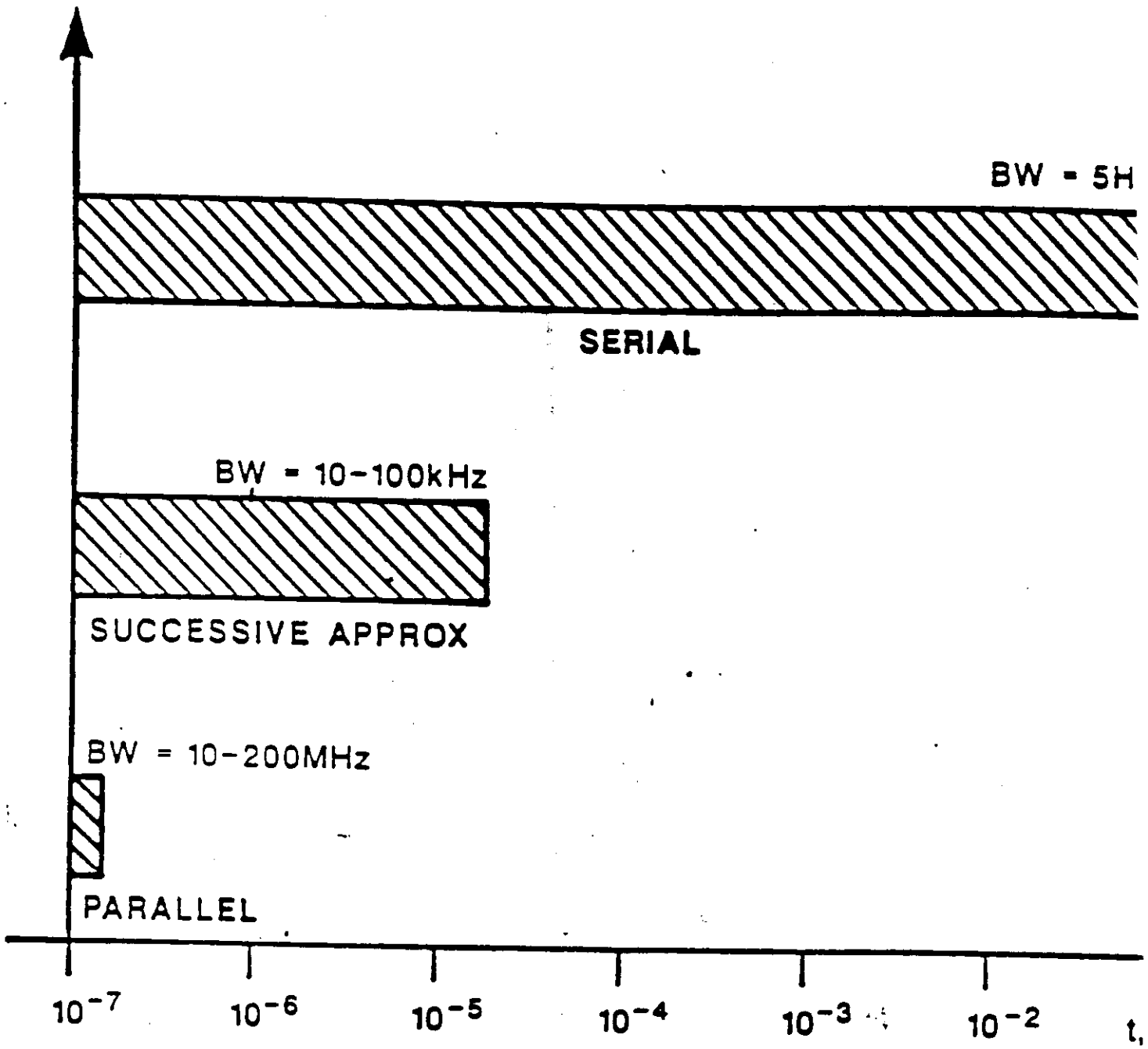

Conversion Time
CLOCK
$V_{DAC}$
Vinput
Vinput
t




# A/D TECHNIQUE THROUGHPUT RATE COMPARISON

KEY POINT:

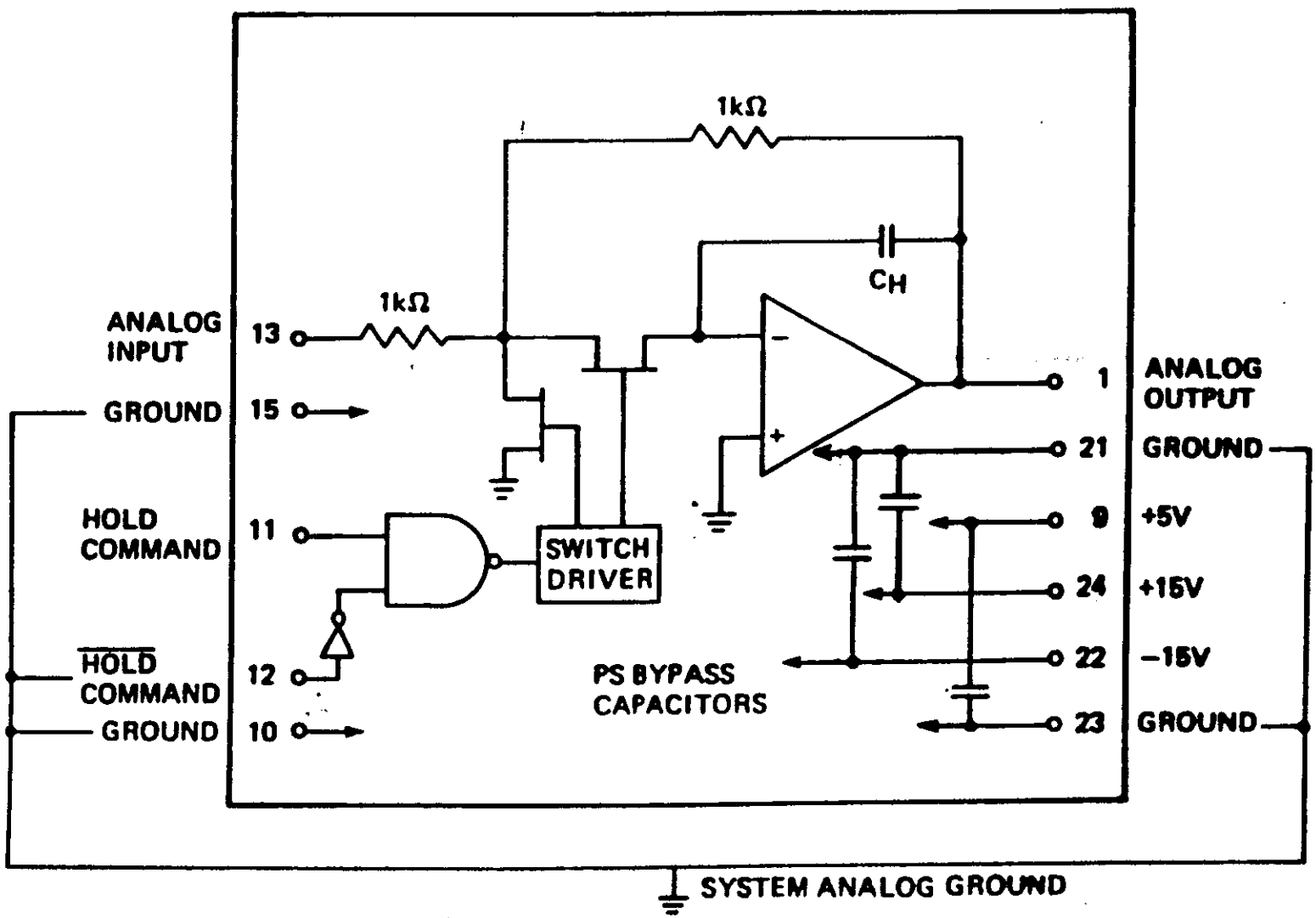
TECHNIQUES COMPLEMENT EACH OTHER




# CONVERSION TIME (LOG SCALE)

## COMPARISON OF CONVERSION TIME FOR ADC TECHNIQUES

## Functional Block Diagram



Estrat.

## Closed Loop T/H Amplifier – HTC-0300A

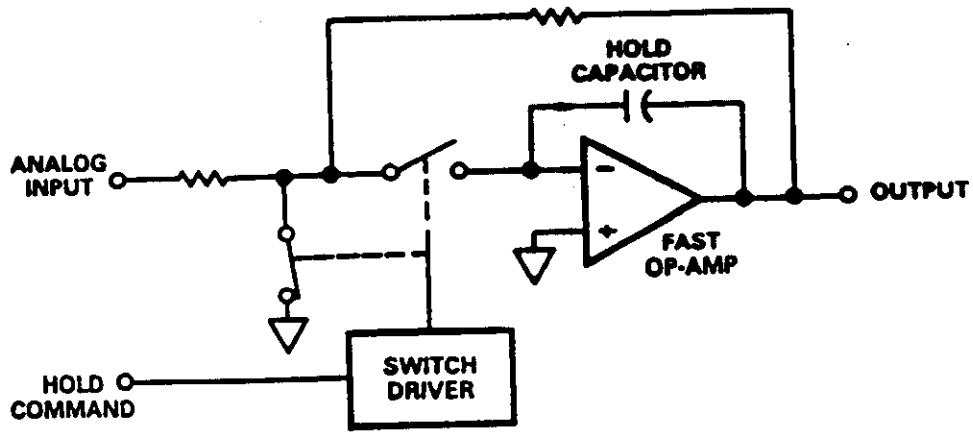



FIG. II-2

## Open Loop T/H Amplifier – HTS-0010

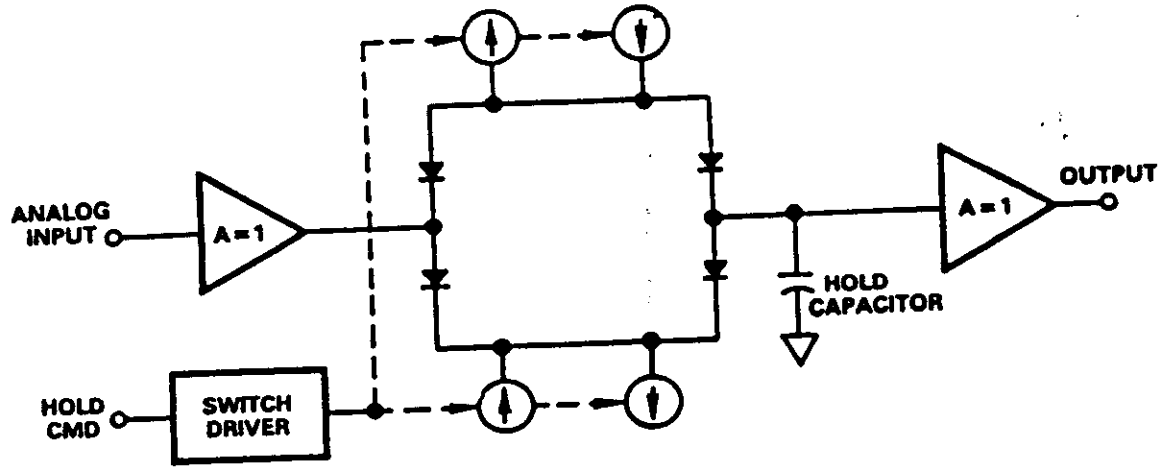
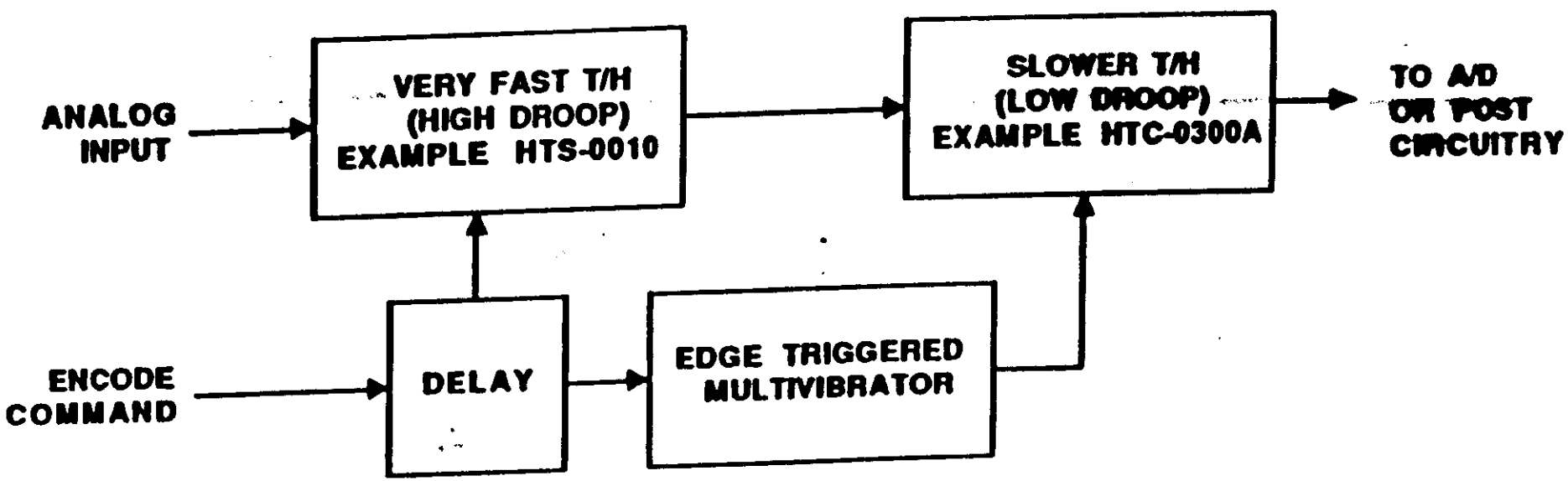


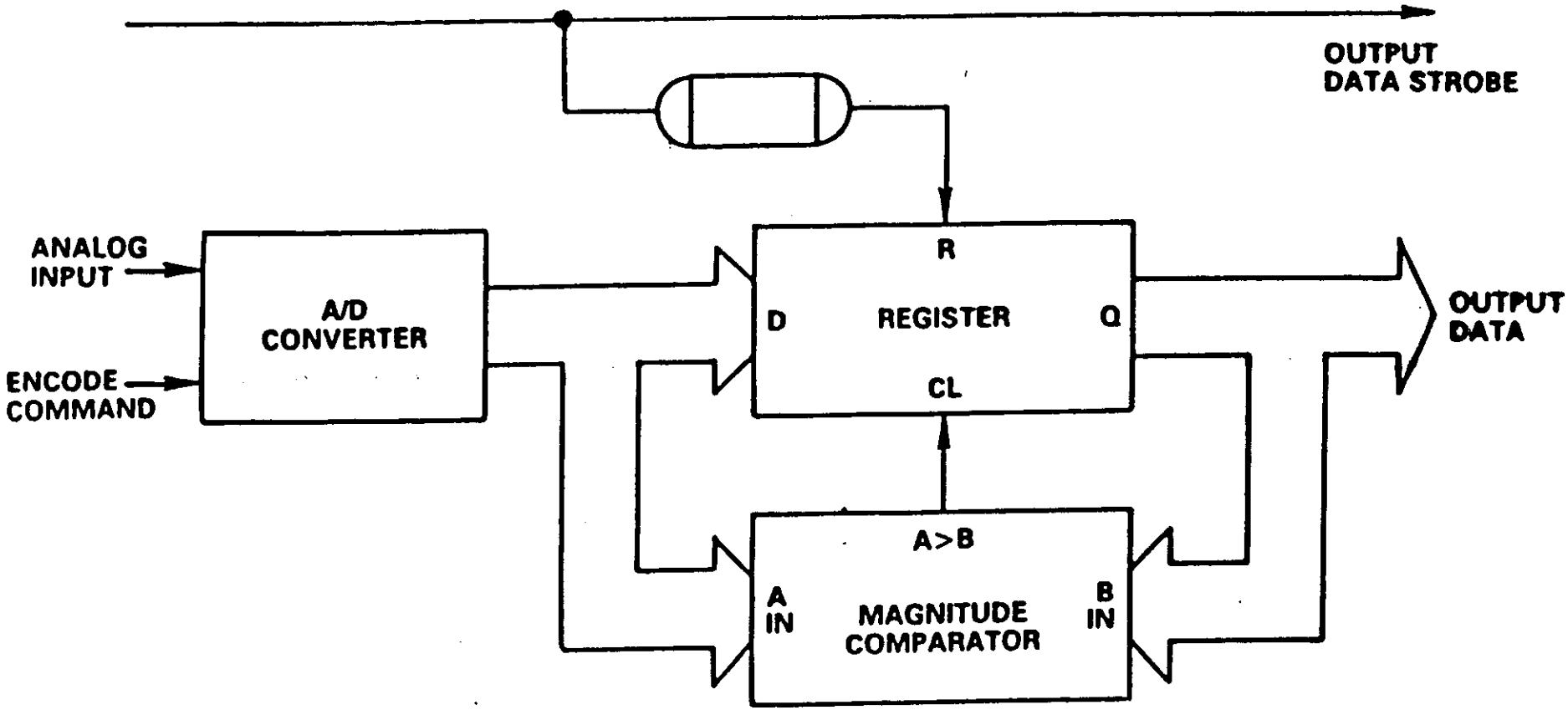

FIG. II-3

# Acquiring Fast Pulses for Slow, High-Accuracy A/D

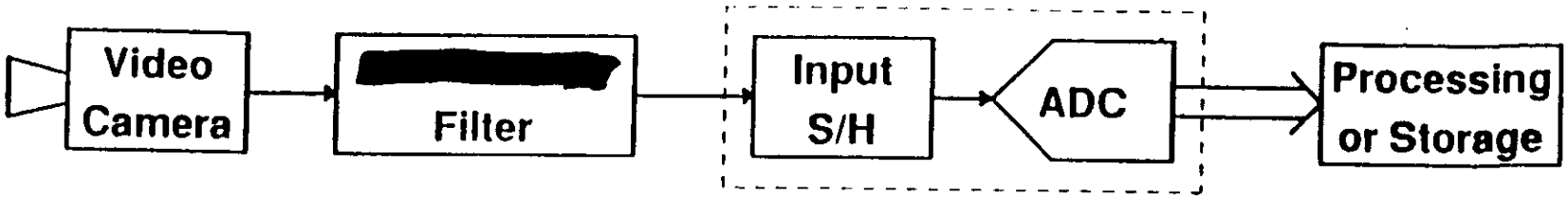



- Delay Needed for HTS-0010 to Hold and Settle
- Edge-Triggered Multivibrator Generates Long Hold Time for HTC-0300A

# Absolute Peak Detector



# High-Resolution Video System




**Requirements: 12-13 bit resolution at 15M samples/s**

**Implementation limitations:**

- **High conversion rate**
- **High accuracy**
- **Input S/H nonlinearity**

# High-Performance Imaging Applications

Example: Full-motion Digitally enhanced Surveilance System

1200x900 Pixels, 60 Frames/sec = $65 \times 10^6$ Pixels/sec

need 75Mhz/sec, 12-bit Res, 8-bit Lin

# Physics Instrumentation Application

Example: All-Digital SSC Calorimeter Channel

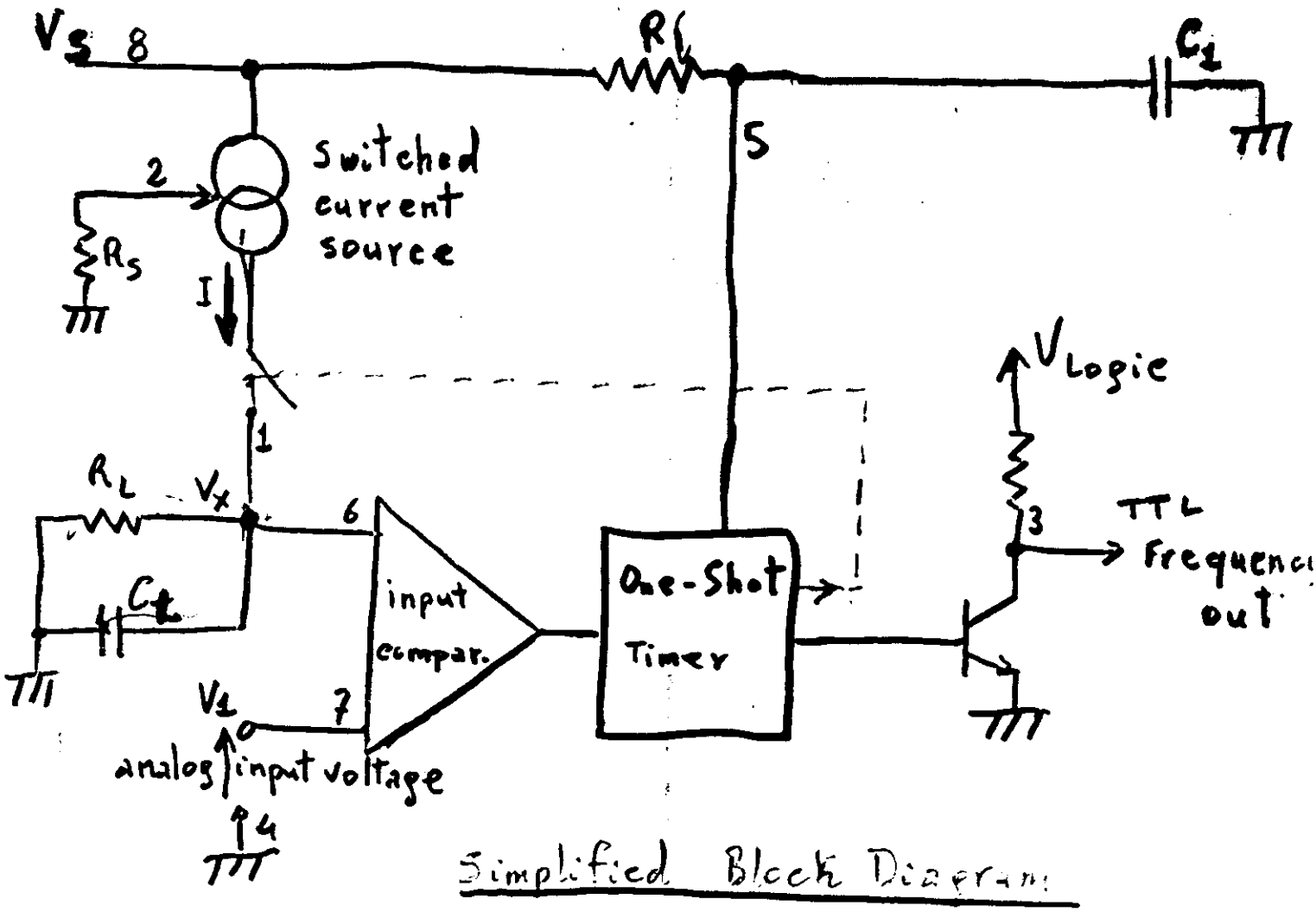
60 Ms/sec

14-16 bit dynamic Range

8-12 bit linearity

$10^5$ to $10^6$ Channels

# Principles of operation of a simplified Voltage-to-frequency converter




Simplified Block Diagram

If $V_I > V_X$, the comparator triggers the one-shot timer The timer turn ON both the frequency output transistor and the switched current source for a period $\sim R_t C_t$

Provide a fixed amount of charge $Q = i \cdot t$ into the capacitor $C_L$. This normally charges $V_X$ up to a high level than $V_I$. At the end of timing period the curre will turn off.

Capacitor $C_L$ will be gradually discharged by $R_L$

National Semiconductor

# LM131A/LM131, LM231A/LM231, LM331A/LM331 Precision Voltage-to-Frequency Converters

## General Description

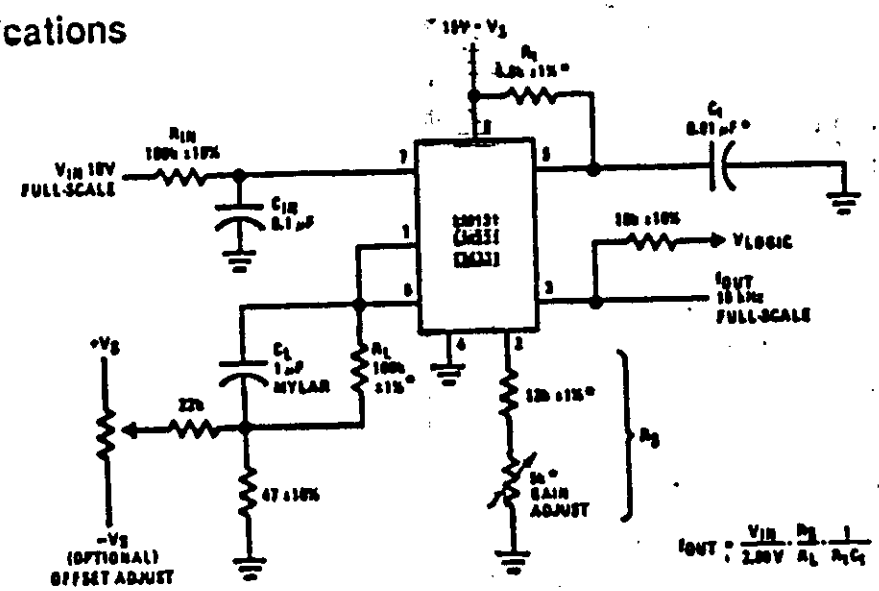
The LM131/LM231/LM331 family of voltage-to-frequency converters are ideally suited for use in simple low-cost circuits for analog-to-digital conversion, precision frequency-to-voltage conversion, long-term integration, linear frequency modulation or demodulation, and many other functions. The output when used as a voltage-to-frequency converter is a pulse train at a frequency precisely proportional to the applied input voltage. Thus, it provides all the inherent advantages of the voltage-to-frequency conversion techniques, and is easy to apply in all standard voltage-to-frequency converter applications. Further, the LM131A/LM231A/LM331A attains a new high level of accuracy versus temperature which could only be attained with expensive voltage-to-frequency modules. Additionally the LM131 is ideally suited for use in digital systems at low power supply voltages and can provide low-cost analog-to-digital conversion in microprocessor-controlled systems. And, the frequency from a battery powered voltage-to-frequency converter can be easily channeled through a simple photoisolator to provide isolation against high common mode levels.

The LM131/LM231/LM331 utilizes a new temperature-compensated band-gap reference circuit, to provide excellent accuracy over the full operating temperature range, at power supplies as low as 4.0V. The precision timer circuit has low bias currents without degrading the quick response necessary for 100 kHz voltage-to-frequency conversion. And the output is capable of driving 3 TTL loads, or a high voltage output up to 40V, yet is short-circuit-proof against $V_{CC}$.

## Features

- Guaranteed linearity 0.01% max
- Improved performance in existing voltage-to-frequency conversion applications
- Split or single supply operation
- Operates on single 5V supply
- Pulse output compatible with all logic forms
- Excellent temperature stability, ±50 ppm/°C max
- Low power dissipation, 15 mW typical at 5V
- Wide dynamic range, 100 dB min at 10 kHz full scale frequency
- Wide range of full scale frequency, 1 Hz to 100 kHz
- Low cost

## Typical Applications




*Use stable components with low temperature coefficients. See Typical Applications section.

FIGURE 1. Simple Stand-Alone Voltage-to-Frequency Converter with ±0.03% Typical Linearity (f = 10 Hz to 11 kHz)

# SELECTION GUIDE

Consult Customers Data Books:

- TRW
- BURR-BROWN
- ANALOG DEVICES
- DATEL-INTERSIL
- MOTOROLA
- NATIONAL SEMICONDUCTORS
- HARRIS
- SIEMENS
- THOMSON

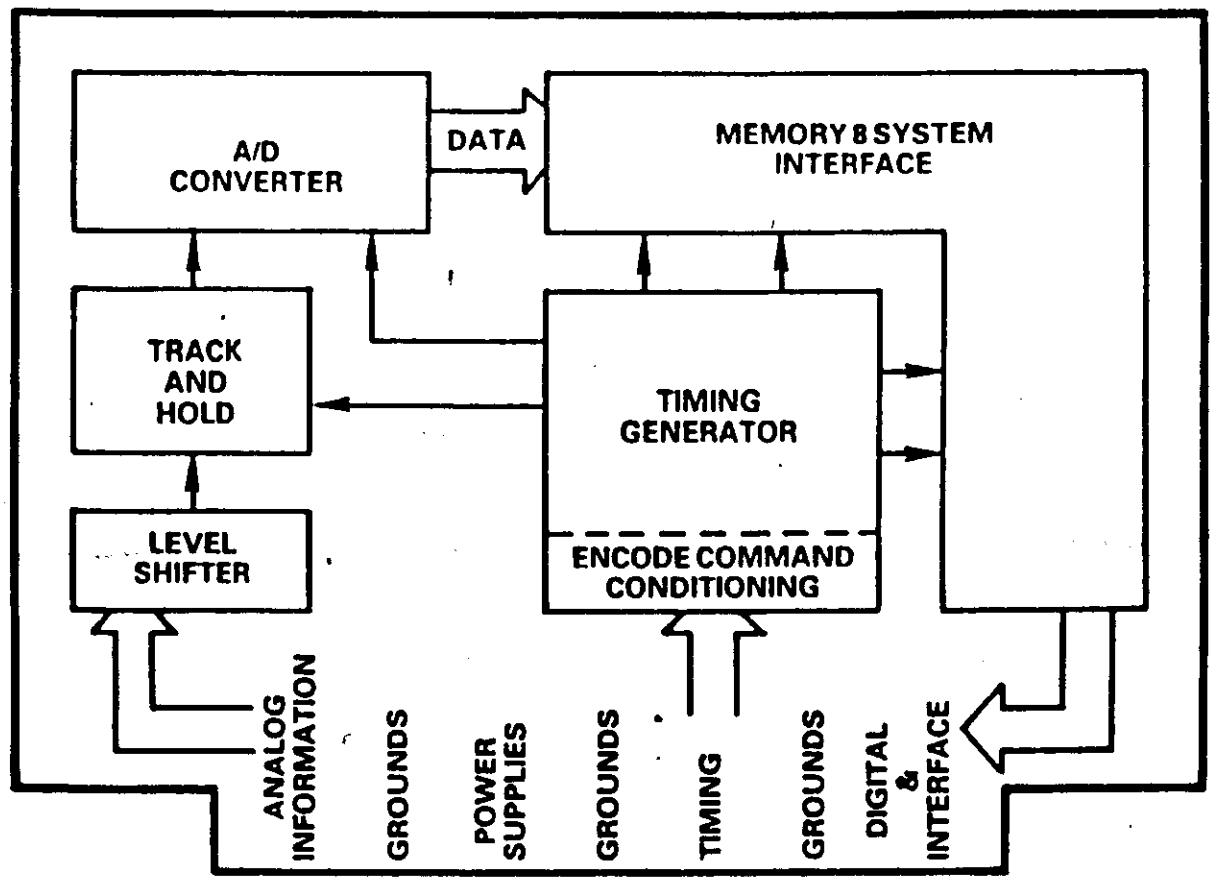
# D/A Converters:



1) General Purpose Low Cost
   a) Current mode
   b) Voltage mode
   c) unipolar or bipolar output
2) High Performance (Speed and Accuracy)
   a) High speed
   b) high resolution
   c) Very wide temperature range
3) Low Power and Multiplying
   a) 2-quadrant multiplying
   c) High speed multiplying
4) Digitally-Buffered (DATA-BUS Compatible)
5) On-chip voltage reference
6) Special-Purpose
   a) PCM Audio Converter

# A/D Converters:

1) General Purpose
   a) differential input
   b) internal or external reference voltage
   c) DVM converters (Digital Voltmeter)
2) High performance (speed and Accuracy)
   a) High speed
   b) High resolution
3) LOW POWER, CMOS
4) BUS COMPATIBLE (3 state-outputs)
5) Multichannel




**PCB "FLOW CHART" LAYOUT**

## GROUNDING PHILOSOPHIES

- Single Point or "Star" Ground
- Where is the Star?
- What about Split Analog and Digital Ground?
- Is an A/D Converter Analog or Digital?
- Does the System "Star" Follow the Device?
- Most High Speed Analog Signals are Single-Ended Making Differential Techniques Difficult

## HIGH SPEED COMPONENT GROUNDING

- A High Speed Data Conversion Device Usually Has Both Analog and Digital Ground Pins
- These Pins May or May Not be Connected Together Within the Package
- Connect Each *Directly* to a Single Large Area PC Board Ground Plane Unless Data Sheet States Otherwise
- Extend Ground Plane Underneath Components
- Use Lots of Ground Plane (> 75% of One Side of a Double-Sided Board)
- Use Multilayer PC Board with Dedicated Ground Plane Layer for Dense Layouts

# DEALING WITH SYSTEMS HAVING ISOLATED ANALOG AND DIGITAL GROUNDS

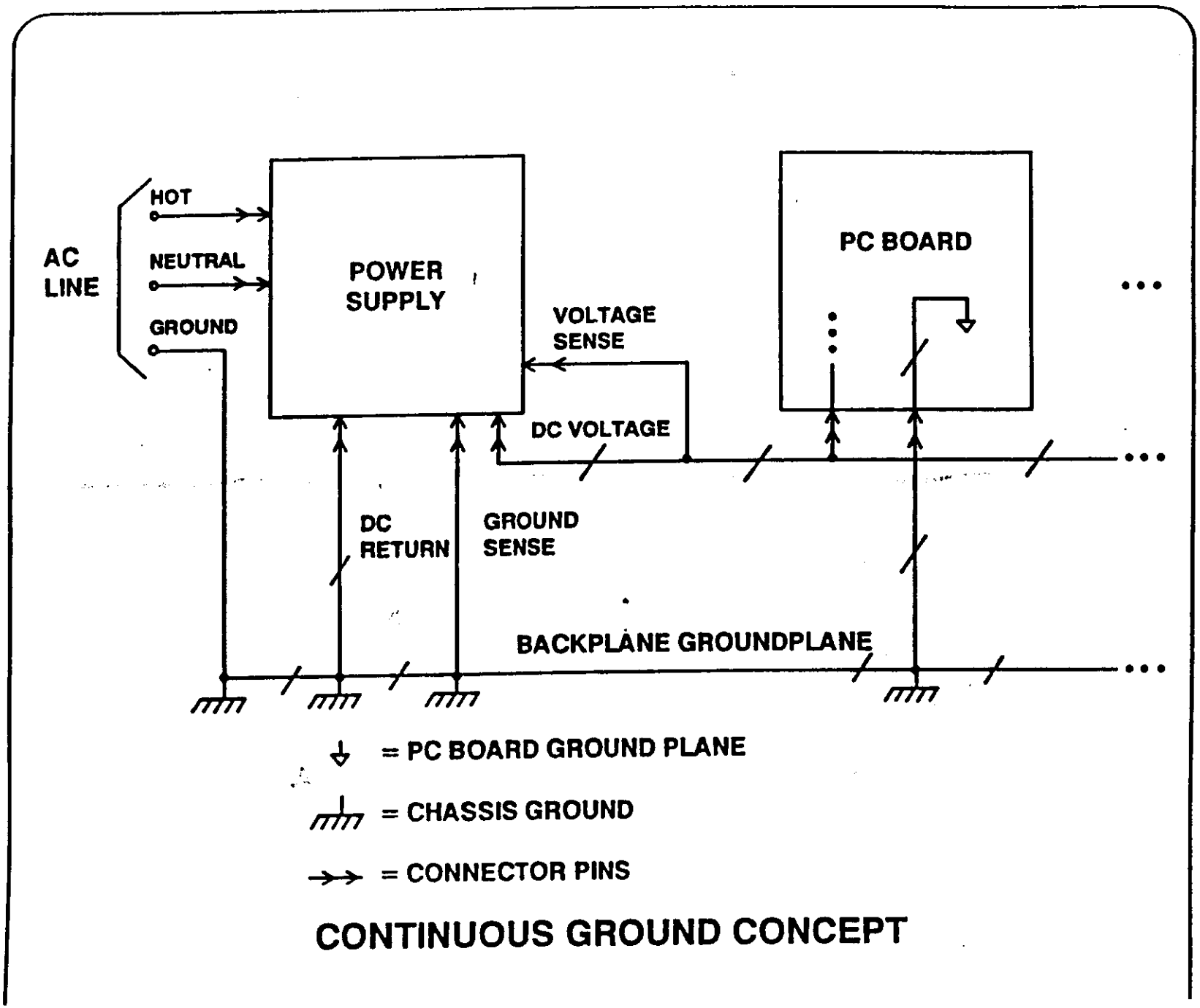
- Treat A/D or D/A as an "Analog" Component – Use Analog Ground Plane for Ground Connections
- Tie Analog and Digital Grounds Together at A/D (May Cause System Problems)
- Equalize DC Potentials with Ferrite Beads
- Equalize AC Potentials with Ceramic Capacitors
- Use Caution and Experiment!
- Consult Component Data Sheets!

## POWER SUPPLY DECOUPLING AND SELECTION

- 0.01$\mu$F to 0.1$\mu$F Ceramic Capacitors for High Frequencies at Package Pins. Surface Mount Chip Capacitors may be Required in Some Cases
- Minimize Lead Inductance
- 3$\mu$F to 20$\mu$F Tantalum Capacitors for Low Frequencies Near PC Board Connector Pins
- Ferrite "Beads" May Help Decouple, But Watch Out for Resonance with Bypass Capacitors
- Linear Supplies Preferred Over "Switchers"
- Steel or Mu-Metal Shielding (EMI)
- Three Terminal Regulators Useful

## INTEGRATING PC BOARDS INTO SYSTEMS

- Extend Continuous Ground Plane Concept
- Use Back Plane "Mother Board" Ground Plane or Ground "Screen"
- Make Chassis Ground Part of Continuous Ground Plane




CONTINUOUS GROUND CONCEPT

# HIGH SPEED PROTOTYPING TECHNIQUES

- No "Vector Board" Please!
- Use Double-Sided Copper-Clad Board
- Use "Pin Sockets" for Critical Components
- Use Short Point-to-Point Interconnections
- Follow Good Bypassing Procedures
- Use Evaluation Boards if Possible
- Go to CAD Layout First
- Use Lots of Ground Plane

## HIGH SPEED PC BOARD SIGNAL ROUTING

- Physically Separate Analog and Digital Signals
- Avoid Crossovers Between Analog and Digital Signals
- Be Careful with Sampling Clock and A/D Converter Analog Input Runs
- Be Careful with High Impedance Points
- Use Lots of Ground Plane
- Use Microstrip Techniques for Controlled Impedances

## USE OF IC SOCKETS

- Don't!
- Use Individual "Pin Sockets" for Each Component Pin Such as AMP Part No. 5-330808-3 (Capped) and 5-330808-6 (Uncapped)

# SYSTEM SIGNAL DISTRIBUTION

- Use Microstrip Techniques with Terminated Transmission Lines
- Differential, Properly Terminated ECL
- Use Short Runs for TTL or CMOS
- Use Properly Terminated Coax Cable for Critical Analog Runs
- Single-Ended to Differential High Speed Amplifiers with Matching Receivers Would be Ideal

# Design Problems and Solutions

| Problem | Solution |
| --- | --- |
| • Power Supply Noise | Fully-differential |
| • Speed | Fast Opamp<br>Flash Subconverters<br>Few-Medium Bits/Stage |
| • Linearity | Digital Correction<br>R-String DAC<br>Medium-Many Bits/Stage |
| • Area | Compact ADC/DAC<br>Medium Bits/Stage |

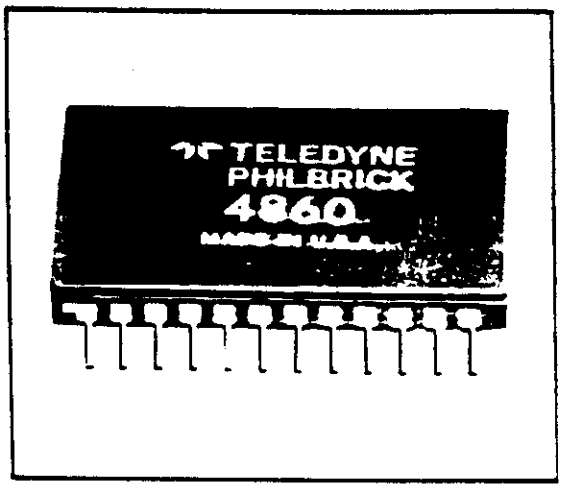
# Fastest 12 Bit Track-Hold Amplifier

# 4860

The 4860 is the fastest high resolution sample/hold (track/hold) amplifier available. It is the only high speed sample/hold that guarantees acquisition time and sample-to-hold settling time (a S/H's two throughput limiting specifications) to ±0.01% and not to only ±0.1% or ±1%. The 4860 will acquire a full 10V signal to ±0.01%FS (equivalent to ±0.005%FSR or ±1mV) in 200nsec maximum. The unit will then track signal components up to 16MHz. In the track mode, offset error is typically ±0.5mV, and gain error is typically ±0.05%. When commanded to the hold mode (aperture time is 6nsec and aperture jitter is ±50psec), the 4860's output will settle to within ±0.01%FS (±1mV) of its final value in 100nsec maximum. Pedestal is a low ±2.5mV. Once in hold, output droop rate is a low 5μV/μsec maximum. Feedthrough attenuation at 2.5MHz is an impressive 74dB.

A 24 pin dual-in-line package, a gain of −1, an input/output range of ±10V, and TTL compatibility make the 4860 pin compatible with the Analog Devices/Computer Labs HTC-0300. Being a second generation design however, it is superior to that unit in almost every performance specification. Faster switching and better feedthrough attenuation are the result of our unique MOSFET switching scheme. Faster acquisition and settling times and considerably lower droop are the result of our own high speed, FET input op amp designs.

The 4860 is ideally suited for 12 to 14 bit high speed data acquisition/distribution systems. In a ±10V system, its ±0.01%FS (±0.005%FSR) linearity is equivalent to better the ±½LSB for 13 bits. Its low ±50ps aperture uncertainty enables it to accurately sample (to ±½LSB in 12 bits) signals with slew rates up to 24.4V/μsec. Its low 5μV/μsec output droop rate enables it to hold signals to ±½LSB in 14 bits for up to 125μsec. The 4860 is functionally laser trimmed at the factory for offset, pedestal and gain errors, and it is designed to be used without external adjustments. If system requirements call for tighter accuracies, units can be trimmed at the factory or adjustments can probably be made at the A/D or D/A used with the 4860. Full Mil-Std-883 screening is available.




## FEATURES

- 200nsec Max Acquisition Time 10V Step to ±0.01%FS
- 100nsec Max Sample-to-Hold Settling Time
- ±50psec Aperture Jitter
- 74dB Feedthrough Attenuation
- TTL Compatible
- HTC-0300 Pin Compatible

## APPLICATIONS

- Transient Recorders
- Fast Fourier Analysis
- High Speed DAS's
- High Speed DDS's
- Analog Delay and Storage

TELEDYNE PHILBRICK – MICROCIRCUITS
Allied Drive @ Rte. 128, Dedham, Massachusetts 02026
Tel: (617) 329-1600. TWX: (710) 348-6726. Tlx: 92-4439

5413

# 12-BIT FAST A/D CONVERTER 4192

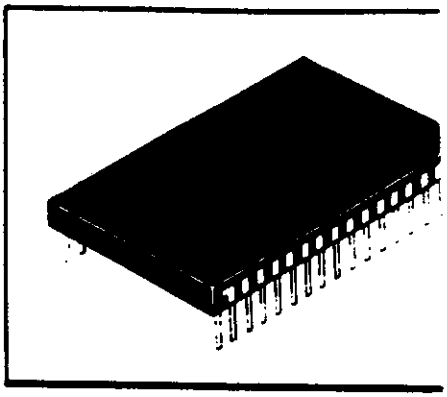
The 4192 is intended for applications requiring fast, precise analog-to-digital conversion. The maximum conversion speed is 500ns. Proven monolithic circuits and recent advanced designs are combined to produce a device with improved performance but low cost. The 4192 is manufactured using thick and thin film hybrid technology.

Three selectable input ranges are provided: 0 to +10V; ±10V and 0 to +20V. Factory laser trims adjust all parameters so that most applications will require no additional adjustment. Optional gain and offset adjustments are provided for the user's convenience.

Conversions are initiated by a single "start" pulse 50ns minimum. Two timing signals are produced by the converter. End of Convert signals data is ready at the outputs. Sample/Hold signals an external Track/Hold to begin acquiring the next analog data point. This technique reduces the overall conversion time for a combined A/D and T/H, thus increasing throughput.

Tri-state outputs are supplied for bus applications. Also included is an Overflow pin. Overflow indicates the analog signal being converted was outside the range of the converter. Power requirements are ±15 and ±5V. Power consumption is typically 1.5W.

The standard 4192 is specified for 0°C to +70°C operation. The 4192-83 is fully specified for operation over the -55°C to +125°C temperature range and meets the high reliability requirements of MIL-STD-883, Class B. May also be ordered screened to Class S.



## FEATURES

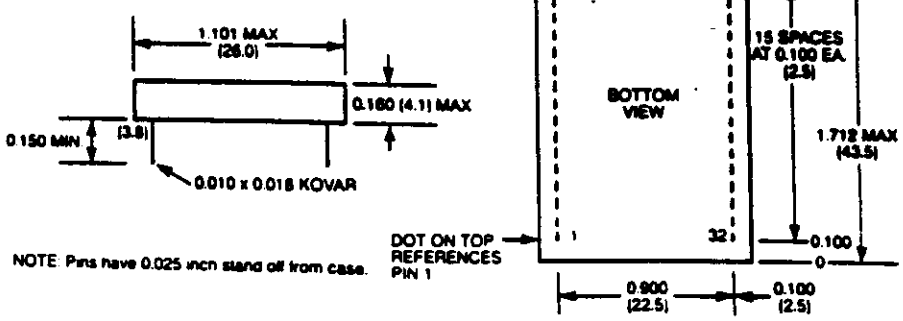
- ☐ 12-Bit Resolution
- ☐ 500ns Max. Conversion Tin
- ☐ Low Power, 1.8W Max.
- ☐ Three-State Output Buffers
- ☐ -55°C to +125°C Operatior

## APPLICATIONS

- ☐ Medical Instrumentation
- ☐ High Speed Data Acquisitio Systems

## PACKAGE DIMENSIONS

Dimensions are expressed in inches (mm).




| PIN DESIGNATIONS | |
|---|---|
| 1. +10V REF | 17. SAMPLE/HOLD CONTROL |
| 2. RANGE | 18. EOC (STATUS) |
| 3. INPUT HI | 19. BIT 12 (LSB) |
| 4. INPUT LOW | 20. BIT 11 |
| 5. OFFSET ADJUST | 21. BIT 10 |
| 6. NO CONNECTION | 22. BIT 9 |
| 7. COMP'SR | 23. BIT 8 |
| 8. OVERFLOW | 24. BIT 7 |
| 9. ENABLE (BITS 7-12) | 25. BIT 6 |
| 10. ENABLE (BITS 1-6— & OF) | 26. BIT 5 |
| 11. +5V POWER | 27. BIT 4 |
| 12. DIGITAL GROUND | 28. BIT 3 |
| 13. +15V POWER | 29. BIT 2 |
| 14. -15V POWER | 30. BIT 1 (MSB) |
| 15. -5V POWER | 31. START CONVERT |
| 16. ANALOG GROUND | 32. GAIN ADJUST |

TEL ■ 617-329-1600 TLX ■ 212711 FAX ■ 617-326-6

4

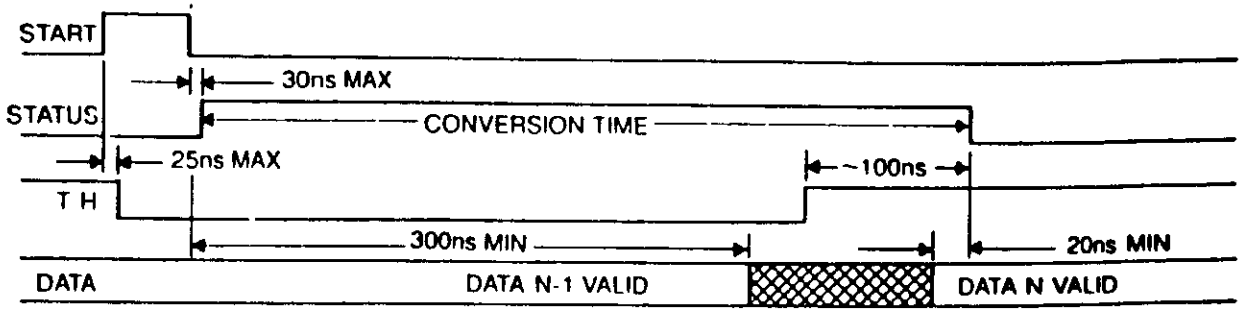



**Figure 2. Conversion Timing**

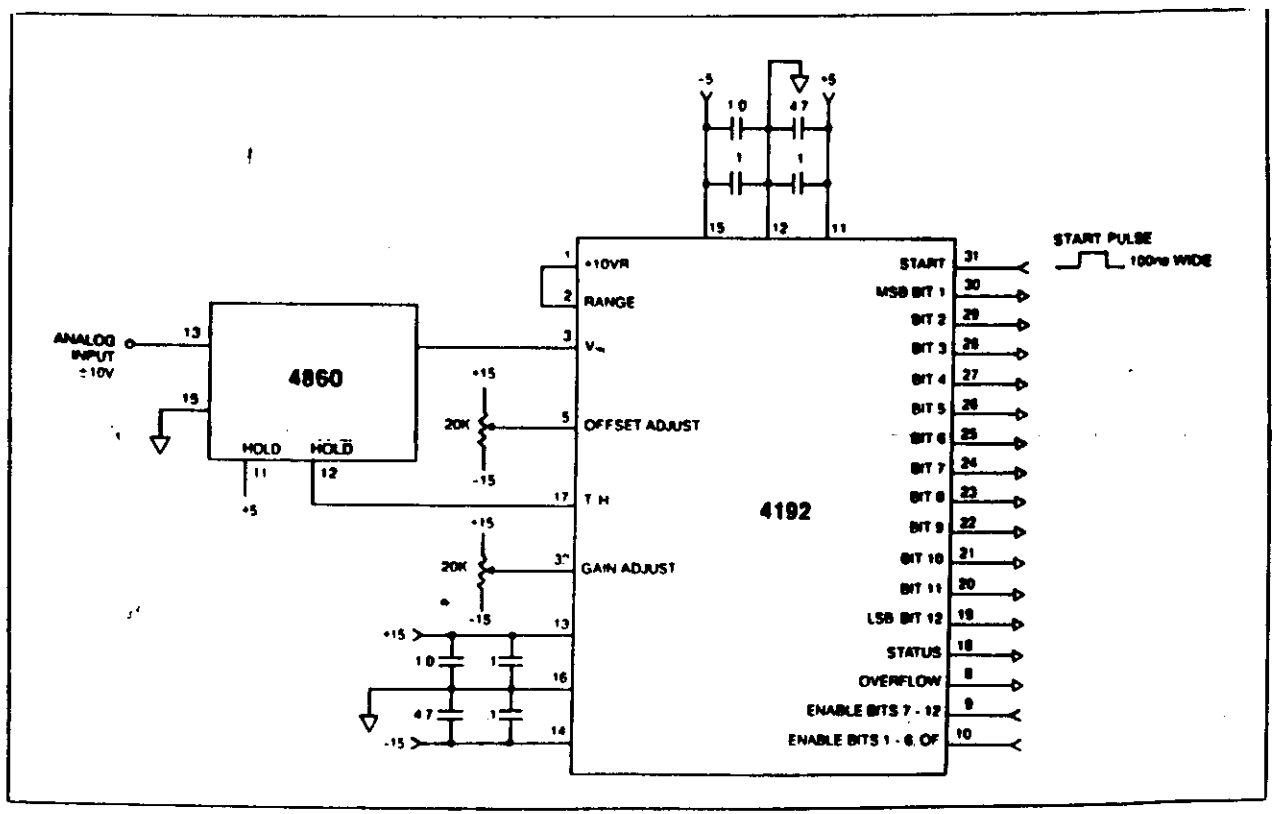
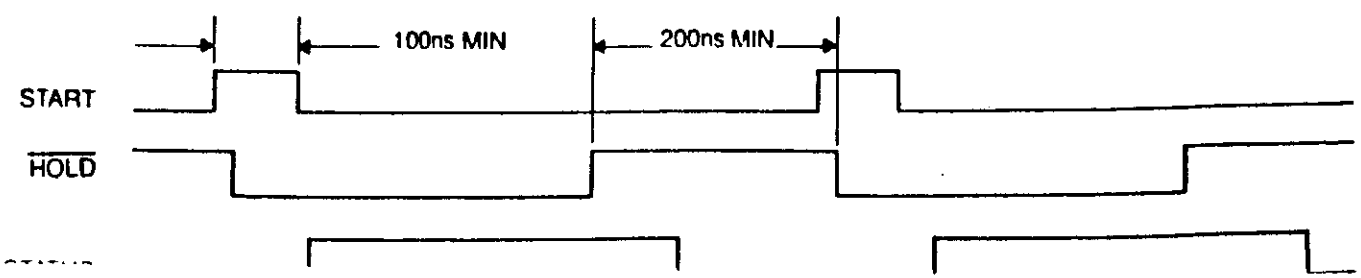
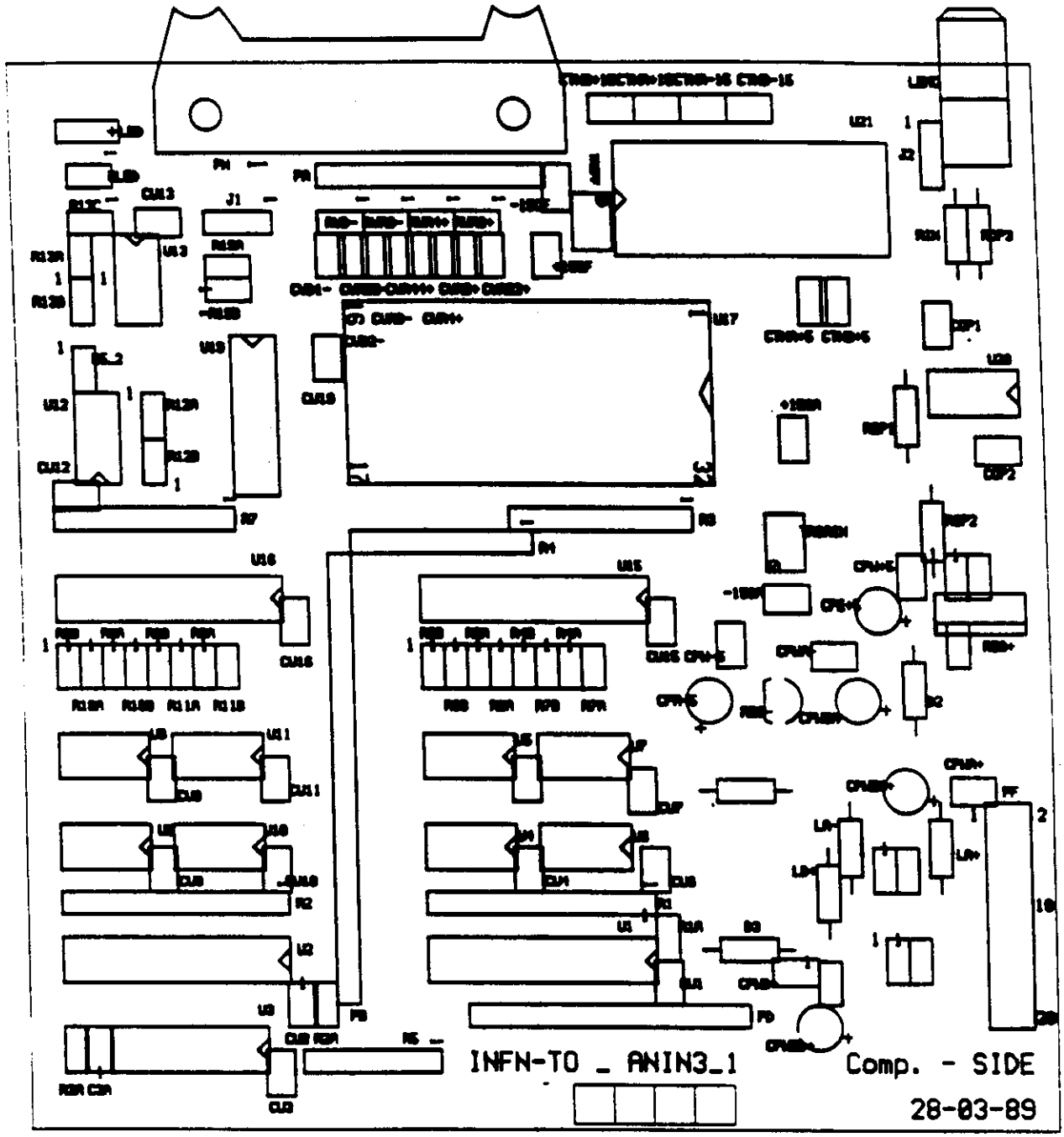
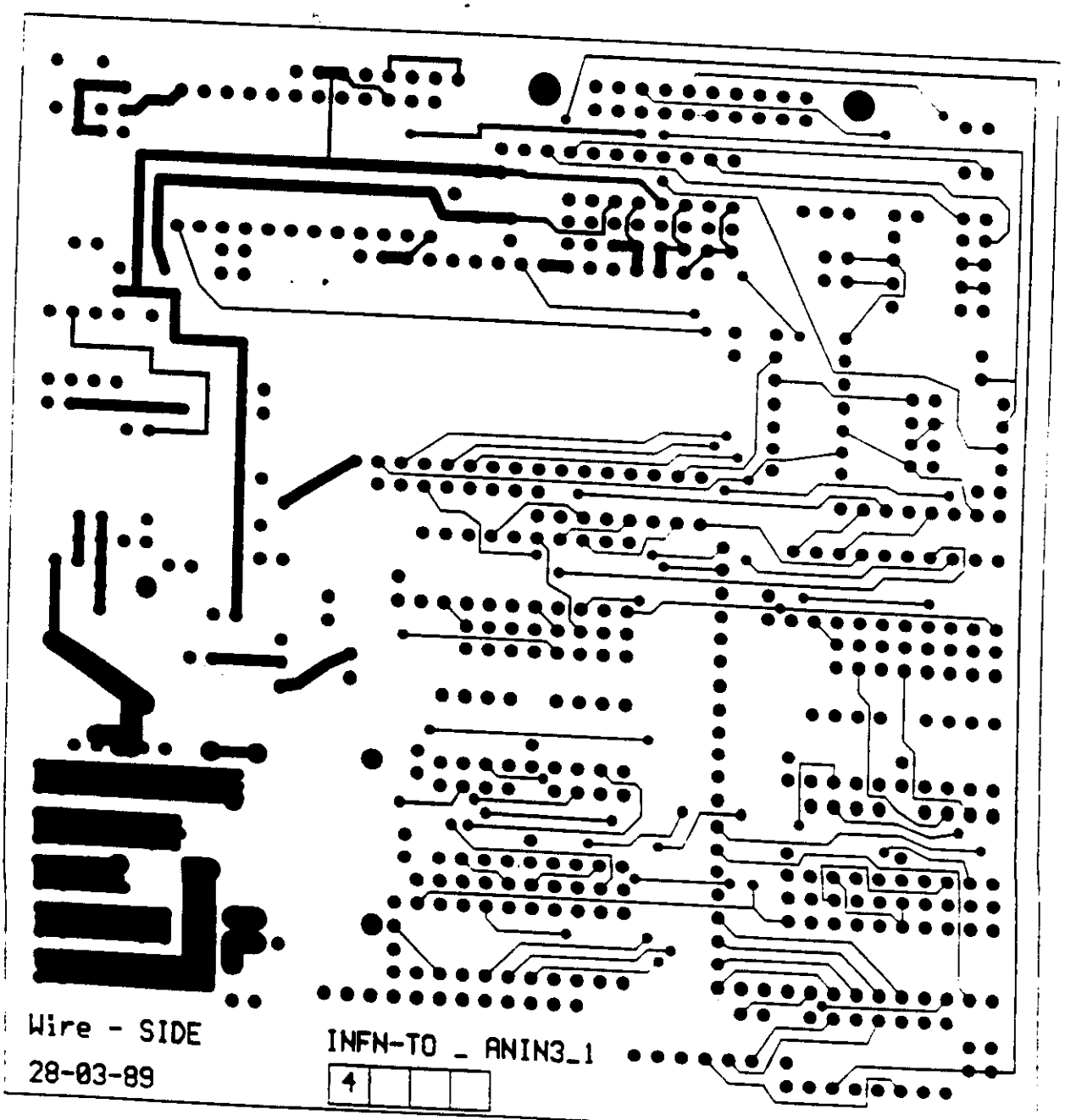
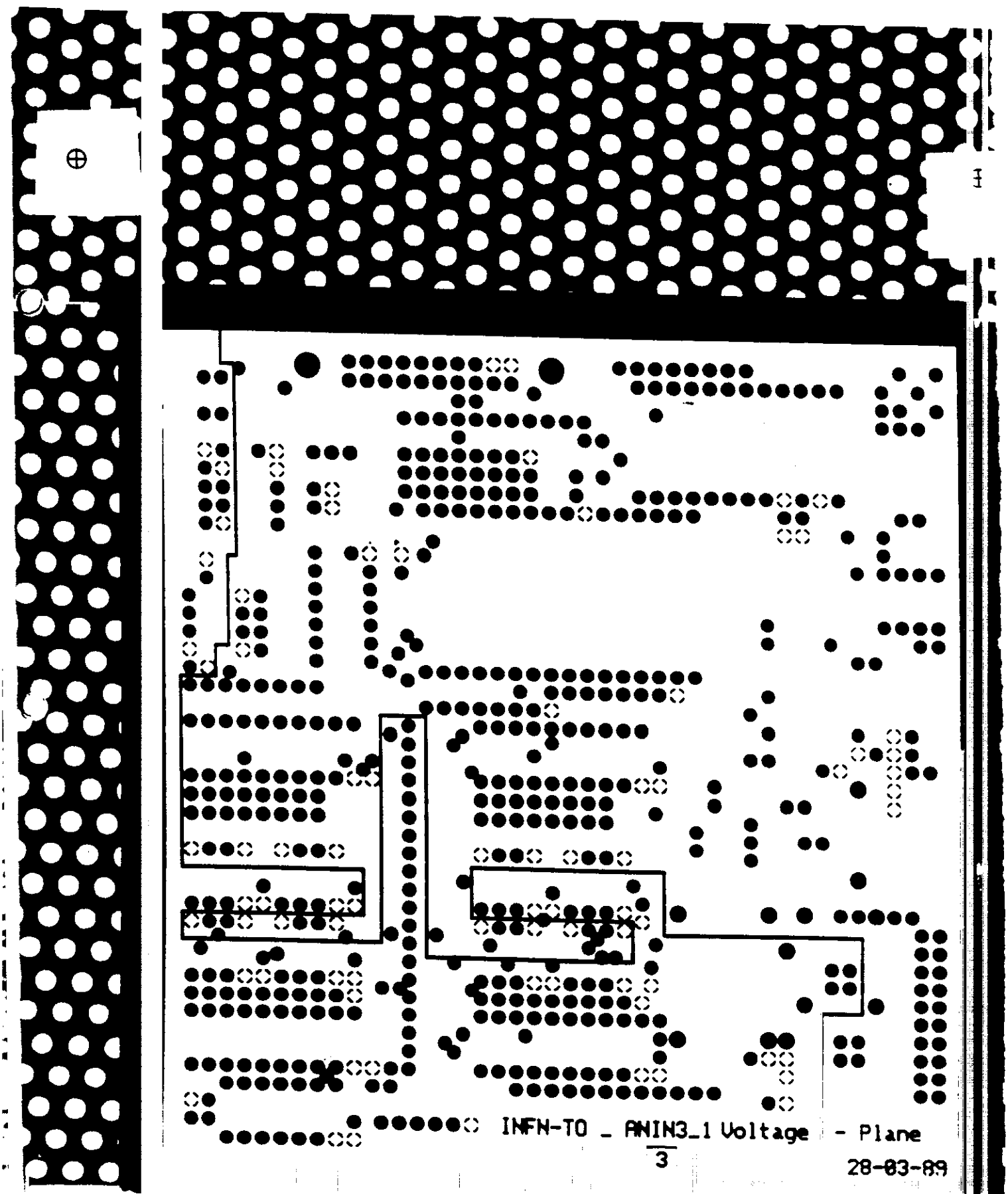


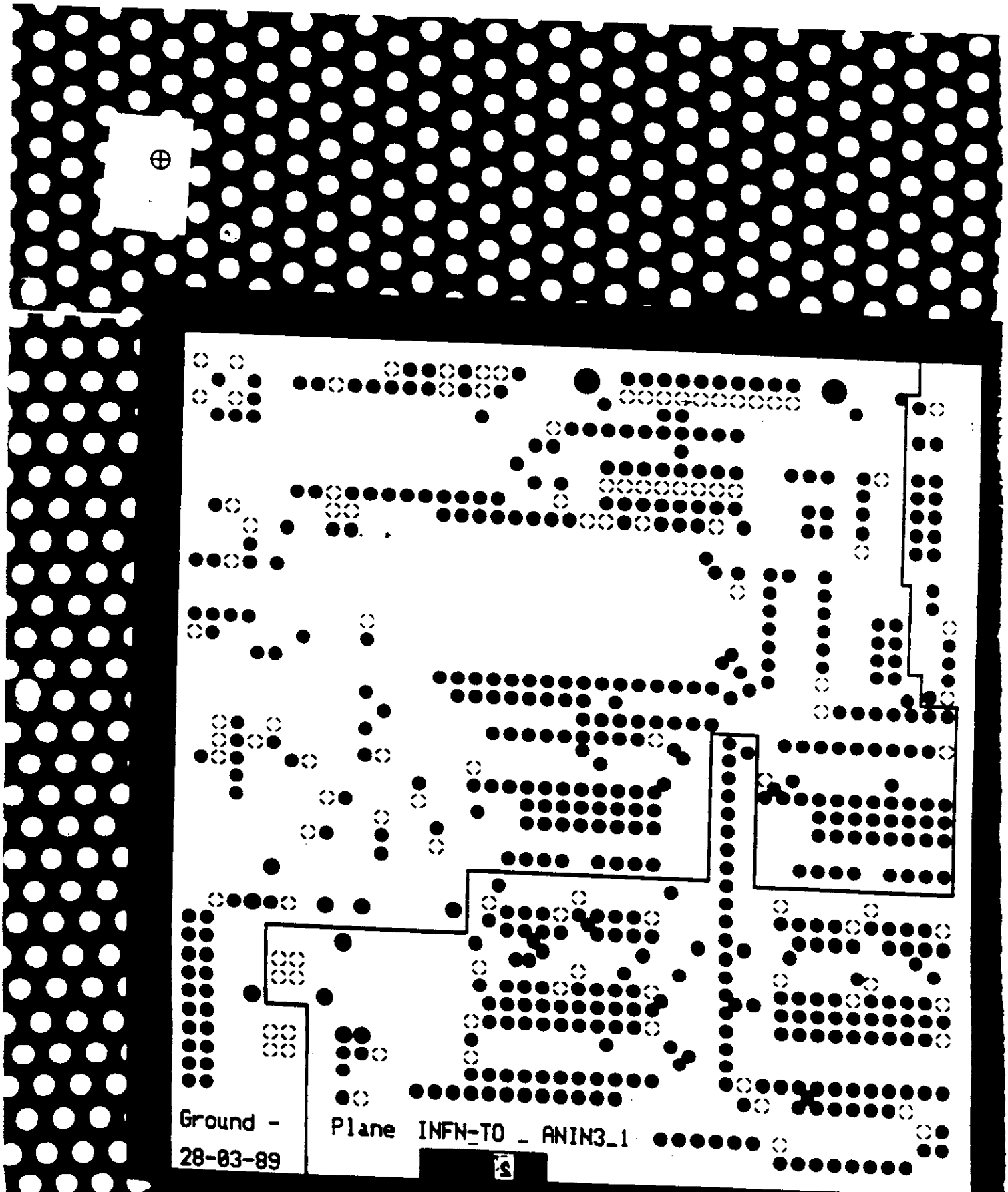

**Figure 3. 1.33. MSPS Using 4192 and 4860**

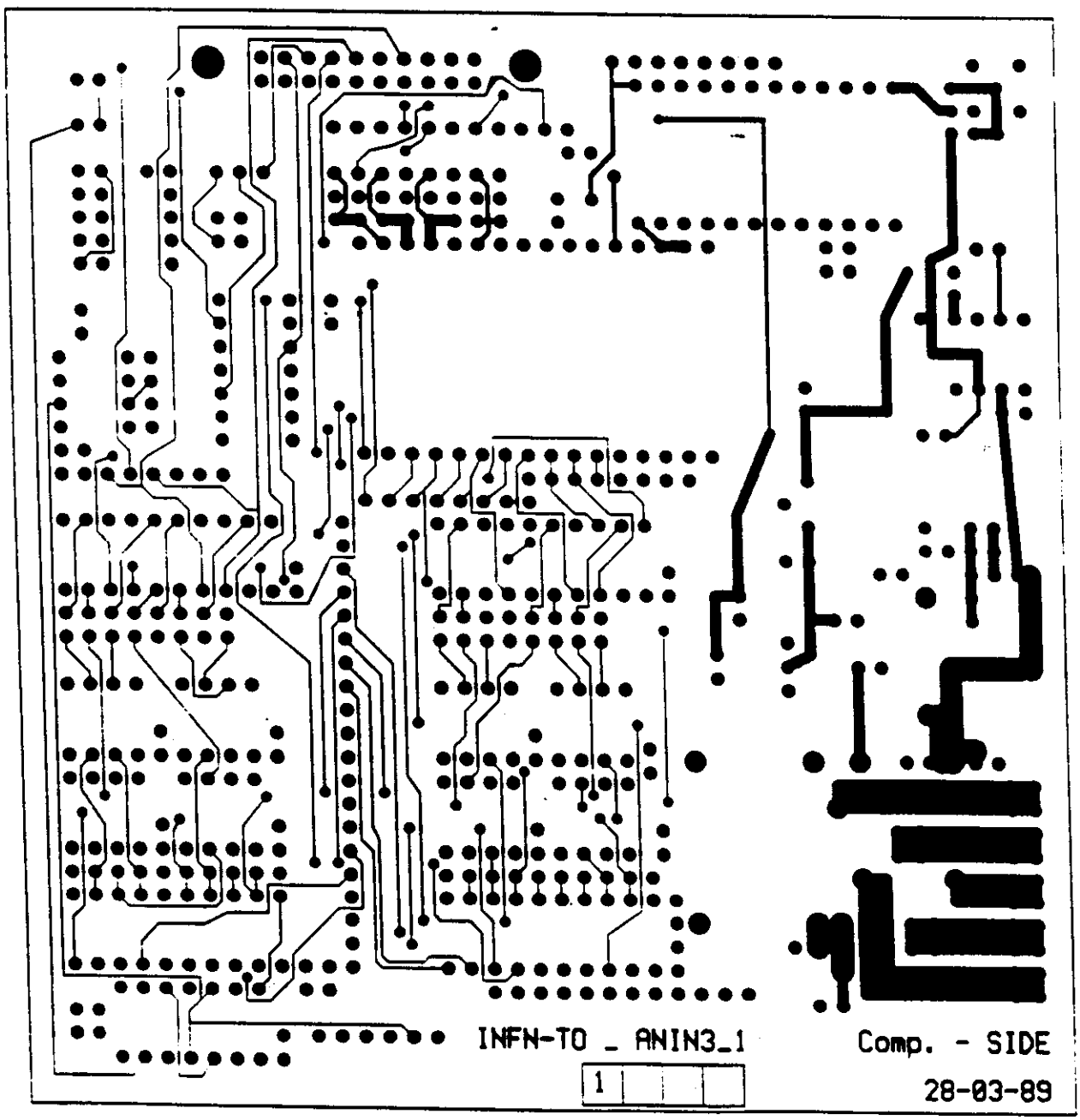


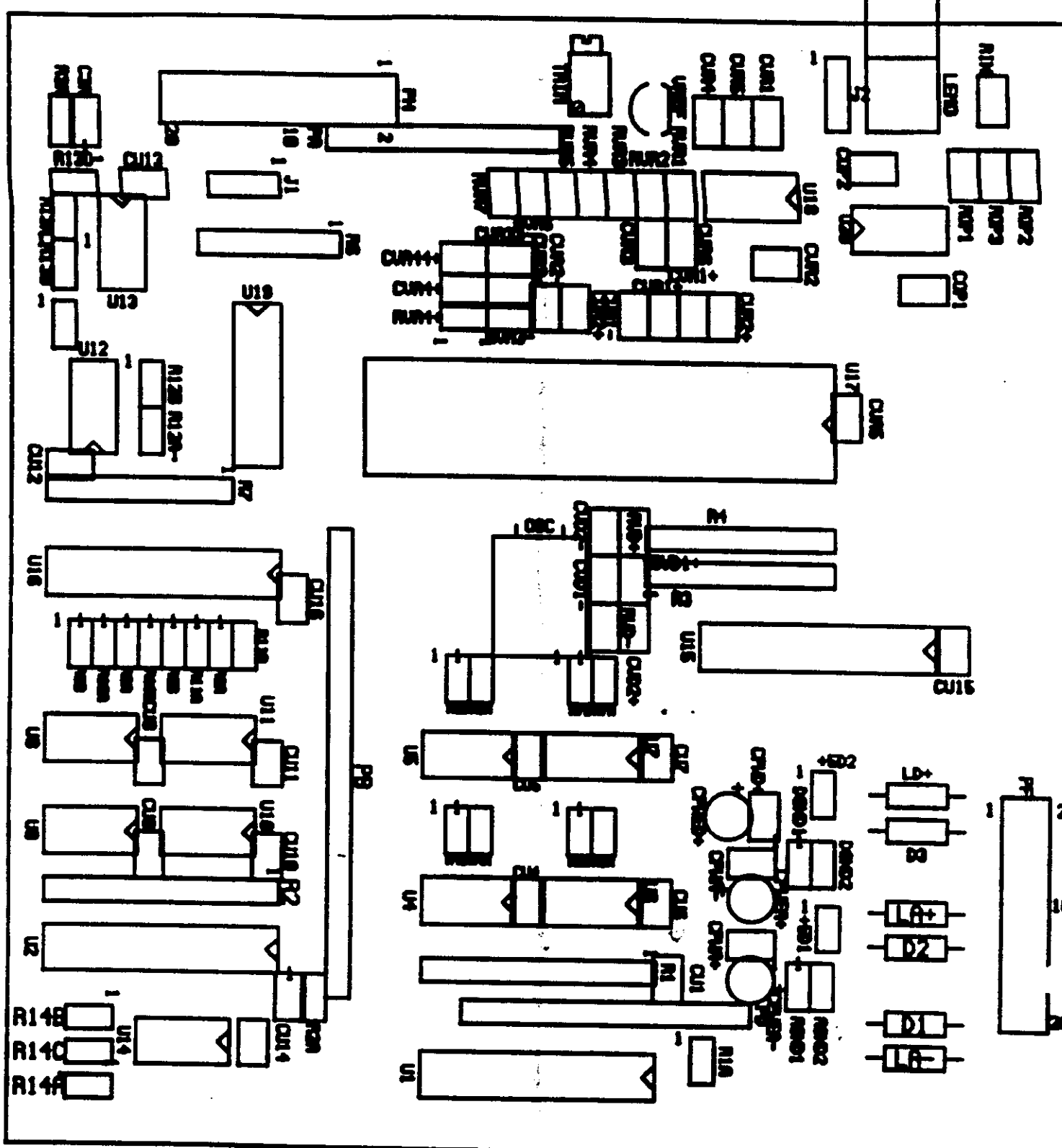

INFN-TO _ ANIN3_1
Comp. - SIDE
28-03-89

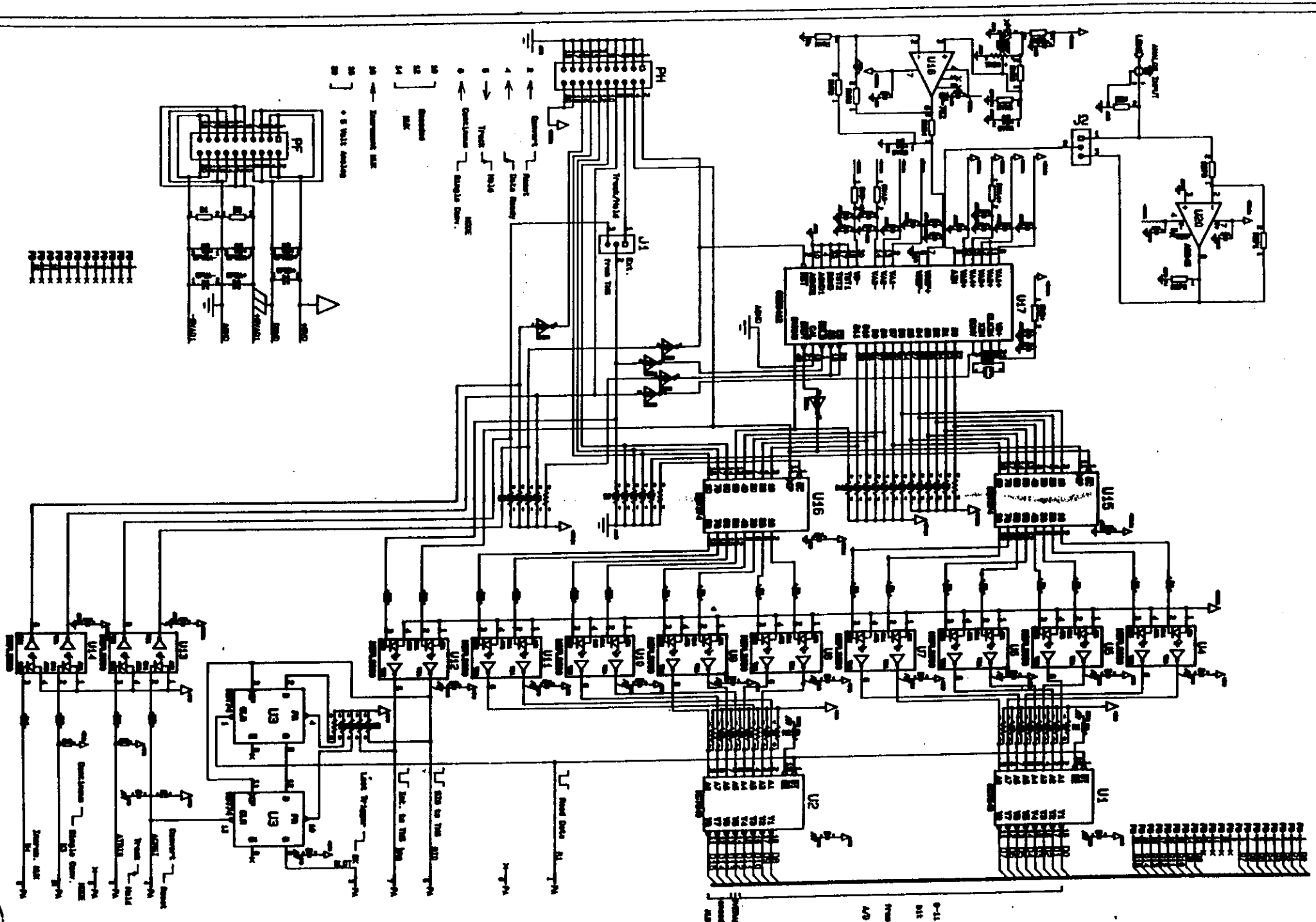

Wire - SIDE
28-03-89
INFN-TO _ ANIN3_1
4


INFN-TO _ ANIN3_1 Voltage - Plane
3
28-03-89


Ground -
28-03-89
Plane INFN-TO _ ANIN3_1


INFN-TO _ ANIN3_1
Comp. - SIDE
1
28-03-89

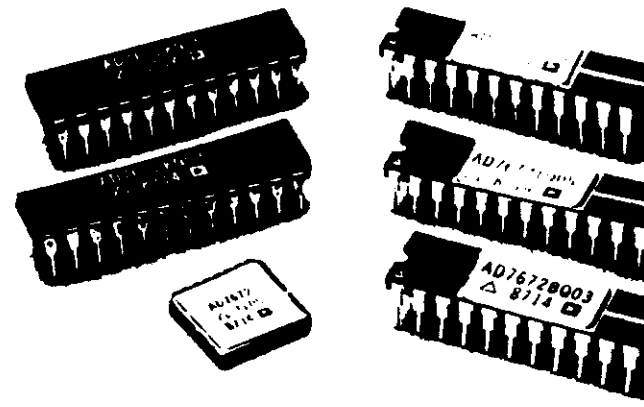

U19
U12
U13
R148
R140
R144
LA+
LA-
D1
D2



| | | | | | | |
|---|---|---|---|---|---|---|
| INFN ISTITUTO NAZIONALE DI FISICA NUCLEARE Sezione di TORINO | DESIGNED BY: D. CROSETTO | DATE DESIGNED: 1st Mar. 1999 | DATE REVISED: | TITLE: ANIN2 | Analog Input module for the VSAT detector | FILE NAME: ANIN2.SCH / DRAWING: 1 of 7 |

**FEATURES**

**12-Bit Resolution and Accuracy**
**Fast Conversion Time**
**AD7672XX03 – 3μs**
**AD7672XX05 – 5μs**
**AD7672XX10 – 10μs**
**Unipolar or Bipolar Input Ranges**
**Low Power: 110mW**
**Fast Bus Access Times: 90ns**
**Small, 0.3", 24-Pin Package**



## GENERAL DESCRIPTION

The AD7672 is a high-speed 12-bit ADC, fabricated in an advanced, mixed technology, Linear-Compatible CMOS ($LC^2MOS$) process, which combines precision bipolar components with low-power, high-speed CMOS logic. The AD7672 uses an accurate high-speed DAC and comparator in an otherwise conventional successive-approximation loop to achieve conversion times as low as 3μs while dissipating only 110mW of power.

To allow maximum flexibility the AD7672 is designed for use with an external reference voltage. This allows the user to choose a reference whose performance suits the application or to drive many AD7672s from a single system reference, since the reference input of the AD7672 is buffered and draws little current. For digital signal processing applications where absolute accuracy and temperature coefficients may be unimportant, a low-cost reference can be used. For maximum precision, the AD7672 can be used with a high-accuracy reference, such as the AD588, when absolute 12-bit accuracy can be obtained over a wide temperature range.

An on-chip clock-circuit is provided which may be used with a crystal for accurate definition of conversion time. Alternatively, the clock input may be driven from an external source such as a microprocessor clock.

The AD7672 also offers flexibility in its analog input ranges, with a choice of 0 to +5V, 0 to +10V and ±5V.

The AD7672 is also designed to operate from nominal supply voltages of +5V and −12V. This makes it an ideal choice for data acquisition cards in personal computers where the negative supply is generally −12V.

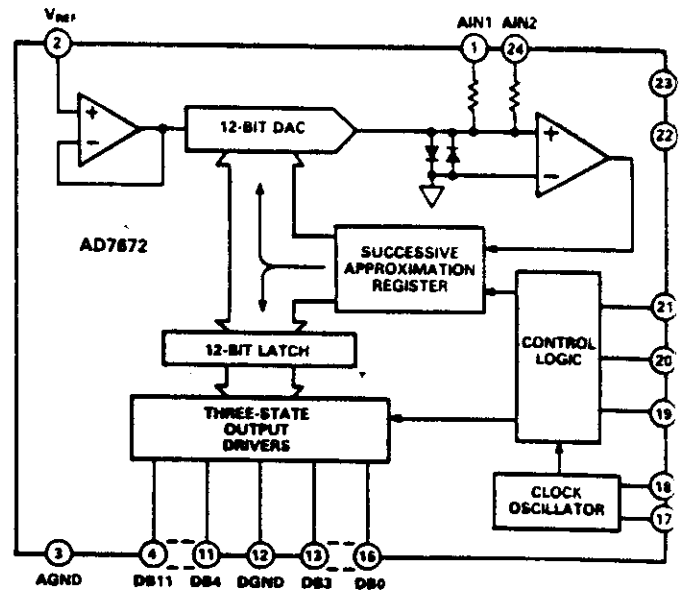
The AD7672 has a high-speed digital interface with three-state data outputs and standard microprocessor control inputs (Chip Select and Read). Bus access time of only 90ns allows the AD7672 to be interfaced to most modern microprocessors.

The AD7672 is available in a variety of space-saving packages; plastic and hermetic 24-pin "skinny" DIP and 28-pin ceramic and plastic chip carrier.



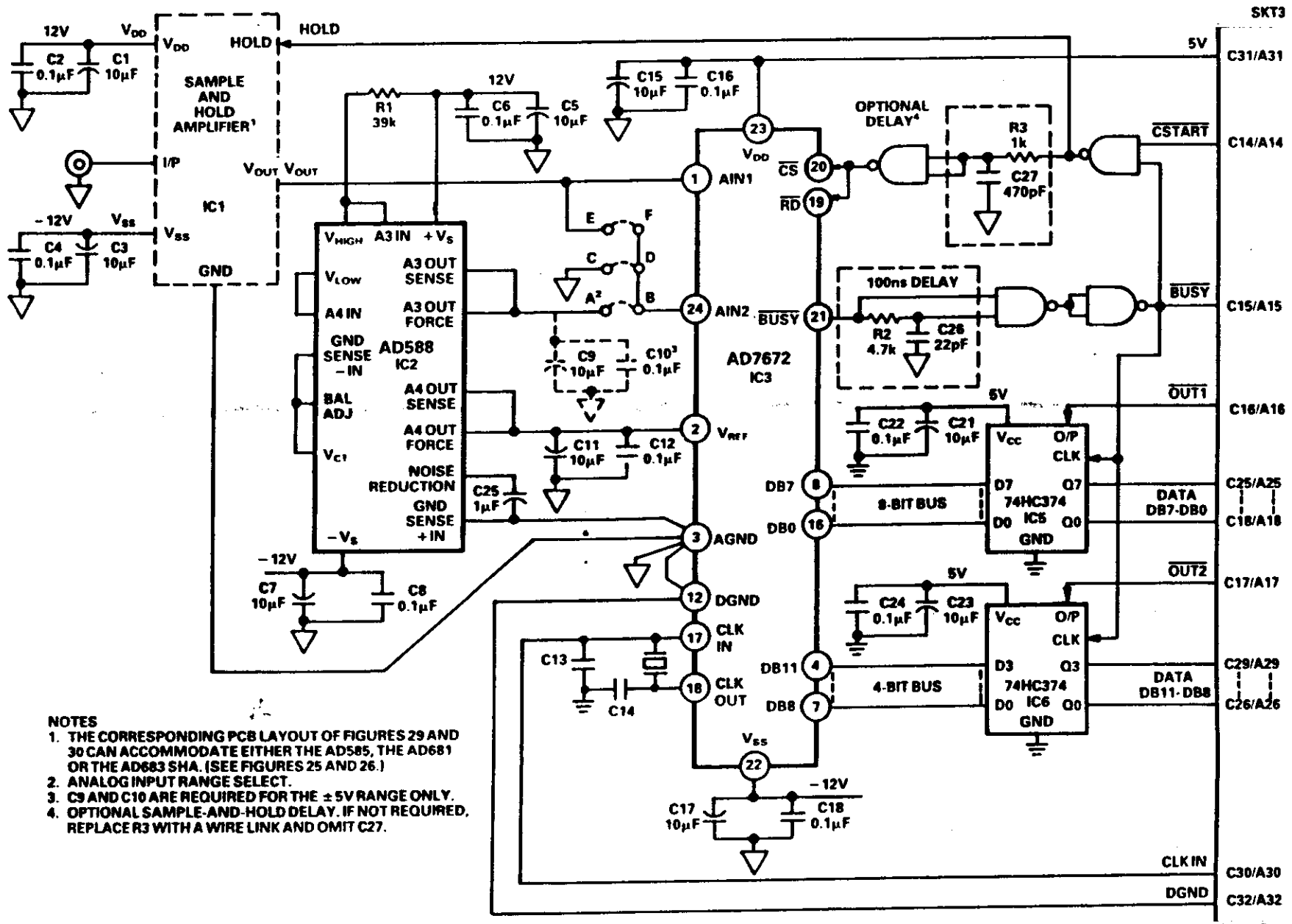
## PRODUCT HIGHLIGHTS

1. Fast, 3μs, 5μs and 10μs conversion speeds make the AD ideal for a wide range of applications in telecommunicatic sonar and radar signal processing or any high-speed data acquisition system.
2. $LC^2MOS$ circuitry gives high precision with low power d (110mW typ).
3. Choice of 0 to +5V, 0 to +10V or ±5V input ranges, ac plished by pin-strapping.
4. Fast, simple, digital interface has a bus access time of 90 allowing easy connection to most microprocessors.
5. Available in space-saving 24-pin, 0.3" DIP or surface mo package.




*Functional Block Diagram*

**One Technology Way; P. O. Box 9106; Norwood, MA 02062-9106 U**
**Tel: 617/329-4700** **Twx: 710/394**
**Telex: 174059** **Cables: ANALOG NORWOOD**




NOTES
1. THE CORRESPONDING PCB LAYOUT OF FIGURES 29 AND 30 CAN ACCOMMODATE EITHER THE AD585, THE AD681 OR THE AD683 SHA. (SEE FIGURES 25 AND 26.)
2. ANALOG INPUT RANGE SELECT.
3. C9 AND C10 ARE REQUIRED FOR THE ±5V RANGE ONLY.
4. OPTIONAL SAMPLE-AND-HOLD DELAY. IF NOT REQUIRED, REPLACE R3 WITH A WIRE LINK AND OMIT C27.

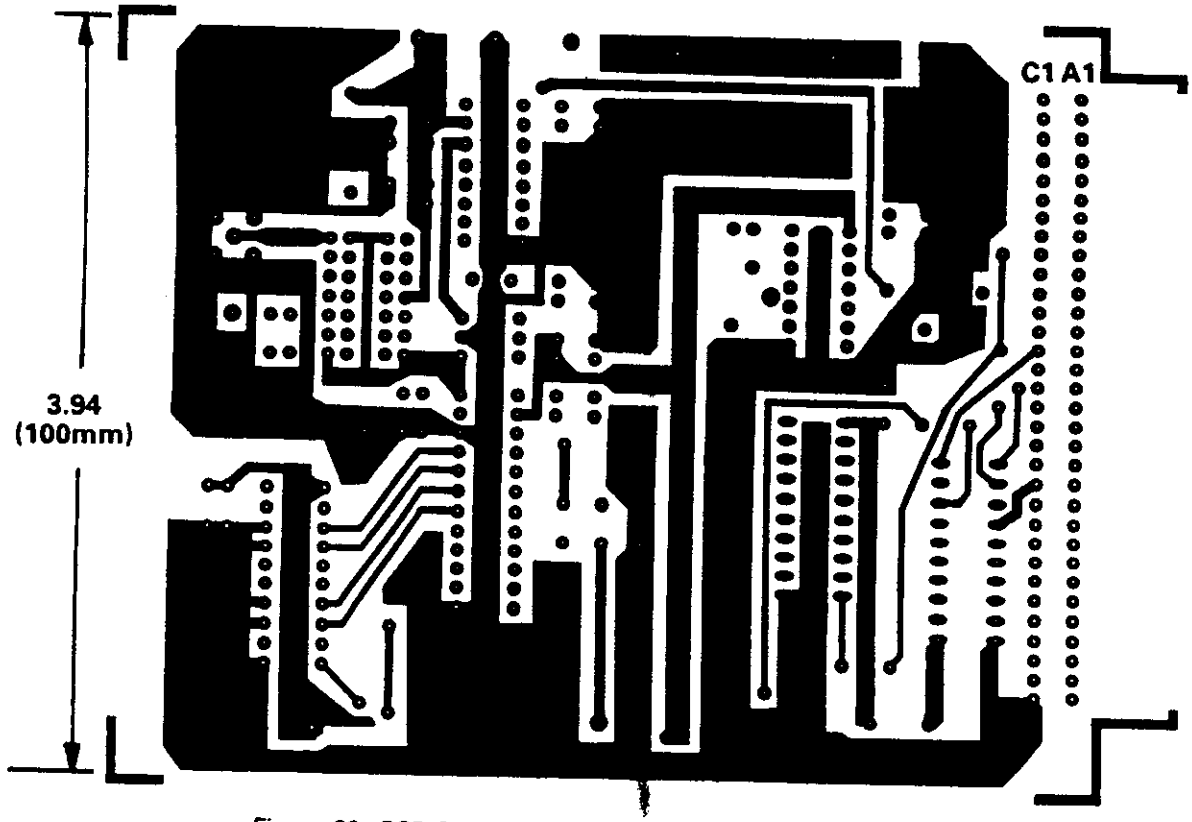



*Figure 29. PCB Component Side Layout for Figure 24*

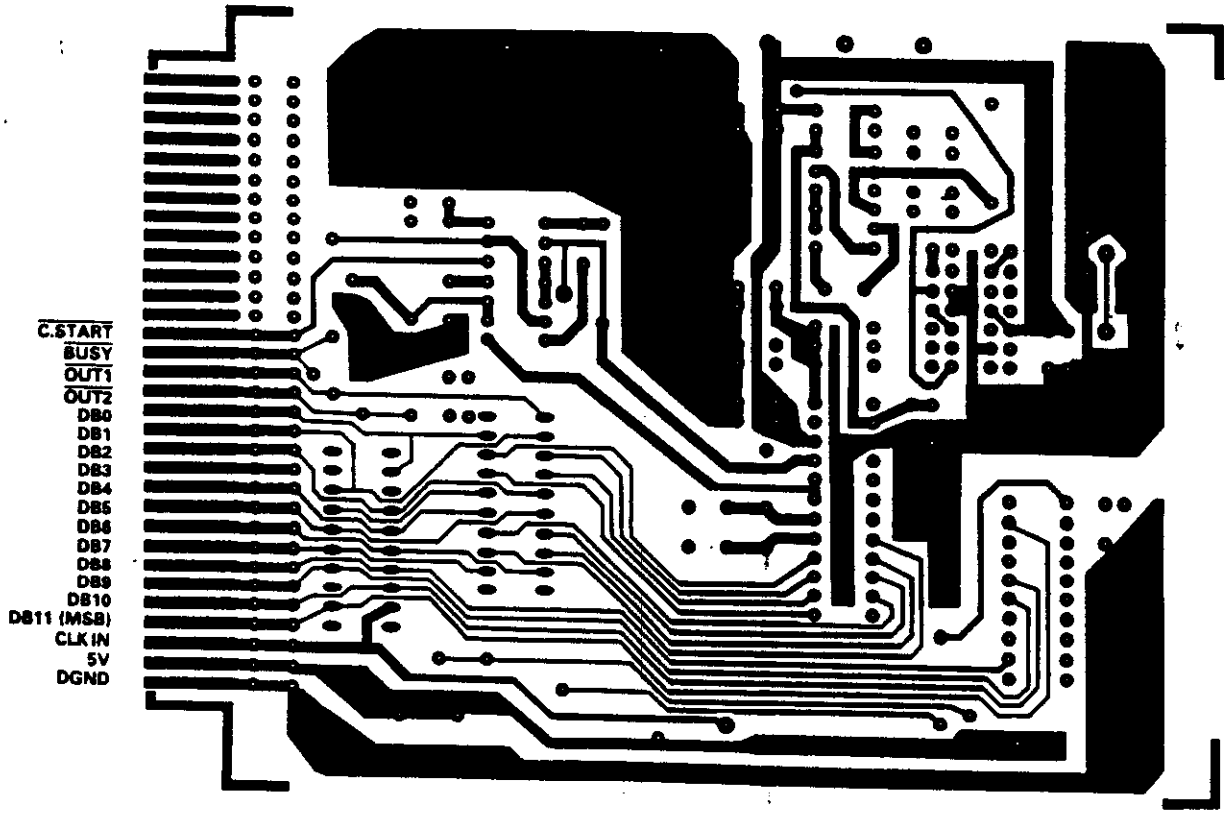



*Figure 30. PCB Solder Side Layout for Figure 24*

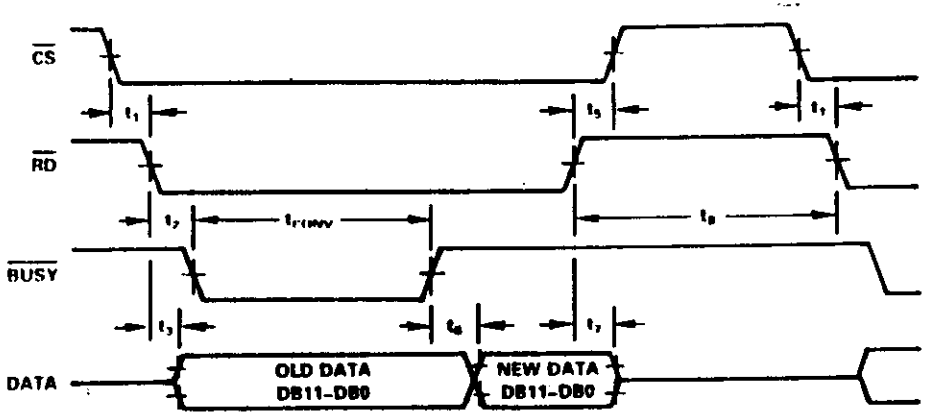



*Figure 16. Slow Memory Mode Timing Diagram*

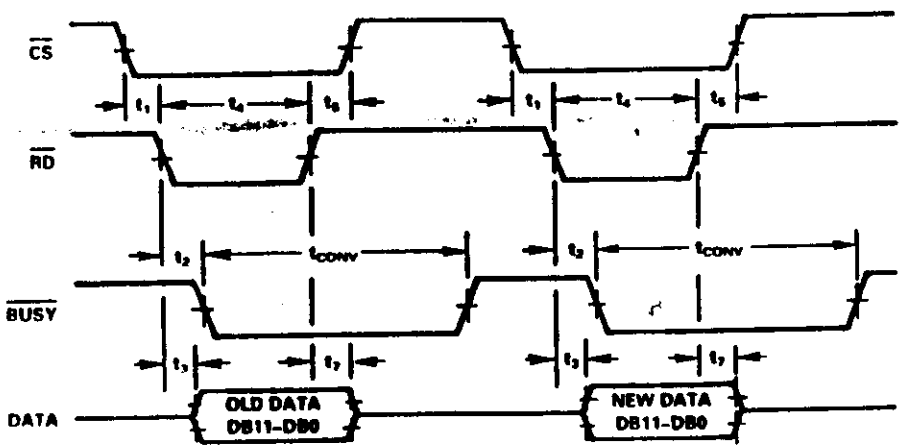



*Figure 17. ROM Mode Timing Diagram*

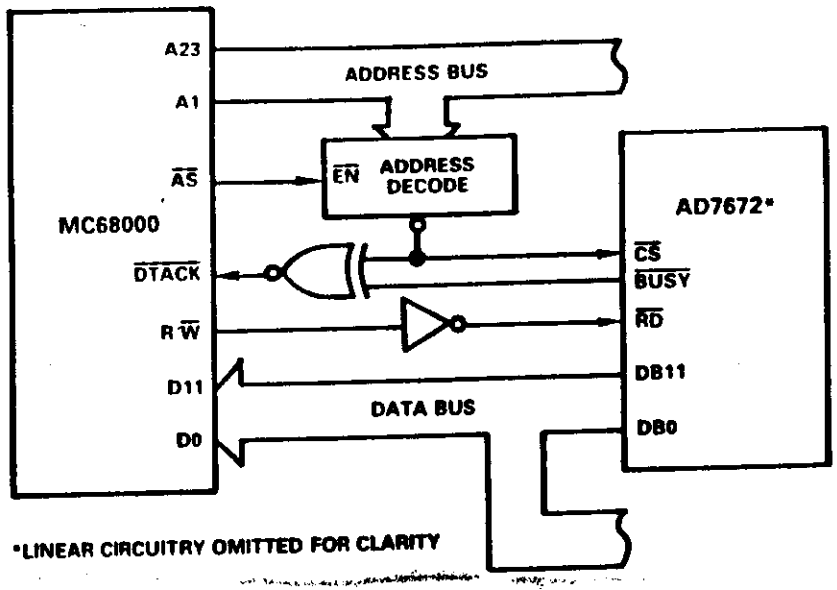



*Figure 18. AD7672 –MC68000 Interface*