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COLLEGE ON
"THE DESIGN OF REAL-TIME CONTROL SYSTEMS"
1 - 26 October

INTERFACING TO IBM-PCs.
Hardware

A. COLAVITA
Microprocessor Laboratory
ICTP
Trieste
Italy

These are preliminary lecture notes, intended only for distribution to participants.

SOFTWARE AND HARWARE INTERFACING THE IBM PC

A Set of Five Lectures

HARDWARE : Prof. Alberto Colavita, Microprocessor Laboratory,ICTP/INFN.

* Generalities. (one hour)
* The XT Bus. (one hour)

SOFTWARE : Dr.Pedro Eggarter, Microprocessor Laboratory ICTP/INFN.

* Software Drivers. (three hours)

THE IBM PC FAMILY

1974 - 1978 (Intel 8080, Zilog Z-80)

1978 Seattle Computer Co. (Intel 8086, 8 Mhz)

1981 IBM PC (Intel 8088)

1983 IBM XT (Intel 8088) + CLONES
Hard disk support

1984 IBM AT (Intel 286, 6 Mhz) + CLONES
Can accomodate up to 16 Mbytes of memory, virtual memory.
Hardware multitasking

1987 IBM PS-2 Line (Intel 286-386 16 Mhz) + CLONES
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1989 CLONES (Intel 486, 25-33 Mhz) + EISA Bus
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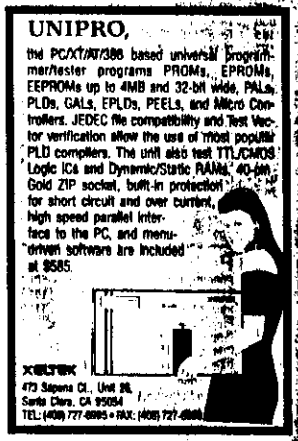

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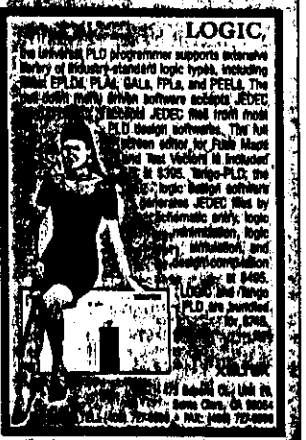

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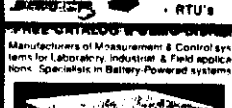

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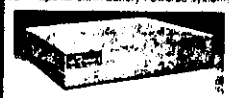

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- High speed version available. Supports baud rates up to 256KB. ... $165

Dual-Port RS-485/422 [PCL743] $175

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- Dipswitch configurable as COM1-4 (I/O & IRQ). On-board permissive resistor.

IEEE-488 Card [PC488A] $145

- Includes INSTALLABLE DOS DEVICE DRIVERS and support for BASIC.
- Additional Support for ASCII/HEX, C, Pascal and FORTRAN. ... $ 50
- IRQ (1-6), DMA channel (1 or 2). Up to 4 boards per computer.
- Compatible with most IEEE-488 Software packages for IBM PC (e.g. ASYST, TAPT-GPIB, Labtech Notebook). Compatible with NI's GPIB-PCII.

IEEE-488 Card [PC488B] with Built-In Bus Analyzer $345

- Software Support for BASICA, QuickBASIC and C/WASM.
- Additional libraries for C, Pascal, FORTRAN. Assembly available. $50 (all).
- Full range of Talker, Listener, Controller, Serial/Parallel Poll, SRQ, etc.
- Powerful menu-driven BUS ANALYZER can be run in the background while 488 programs or commands are executed. Features Program Stepping, Break points, Real Time Bus Data Capture (4K buffer), Instant Screen Toggling.
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- NEC-7210 based card (compatible with NI's GPIB-PCII). ... $465

DIGITAL I/O Card [PCL720] $175

- Inputs: 32 TTL compatible channels. Input load is 0.2 mA at 0.4 V.
- Outputs: 32 TTL compatible channels. Sink: 24 mA (0.5 V); Source: 15 mA (2.4 V).
- Counter/Timer: DC to 2.4 MHz; 3 channels; 16 bit counters; 5 counting modes.
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LOW COST DATA ACQUISITION & CONTROL CARDS FOR PC/XT/AT

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- A/D converter: 8 single-ended channels. Device: AD574. Conversion time ... bit (less 25 usec). Input ranges: ±5V; software Trigger mode only.
- D/A converter: 1 channel, 12 bit resolution. 0 to +5V/+10V Output Range.
- Digital I/O: 16 Input / 16 Output channels. All I/Os TTL compatible.
- External Wiring Terminal Board with mounting accessories included.
- Utility Routines and Demo/Sample Programs for BASIC and Quick-BASIC.

12 bit A/D & D/A [PCL812] $395

- A/D converter: 16 single ended inputs. Device: AD574. Conversion time less ... than 25 usec). Built-in programmable gain: Input ranges: ±10V, ±5V, ±1V.
- D/A converter: 2 channel, 12 bit resolution. Output Range 5 V.
- Digital I/O: 16 Input / 16 Output channels. All I/Os TTL compatible.
- Counter: 3 channel programmable interval counter/timer. Uses Intel 8254.
- DMA and interrupt capability. Utility software for Basic included.

ASYST 12 bit A/D & D/A [PCL718] $795

- A/D converter: 16 single ended or 8 differential channels. 12 bit resolution. Programmable gain with Built-in Interrupt and DMA control circuitry. Conversion time: 25 usec (software trigger). 10 usec (hardware triggered).
- Input ranges: Bipolar: ±10V, ±5V, ±2.5V, ±1V, ±0.5V. Unipolar: 0-10V, ...
- D/A converter: 2 channels. Resolution: 12 bits resolution. Settling time: 5 usec. ±5V
- Digital I/O: 16 OUT, 16 IN: TTL compatible. All I/Os TTL compatible.
- Counter: 16 bit prog. interval counter/timer. Uses Intel 8254. Power clock.
- Software: Utility software for BASIC and Quick-BASIC included. Supported by LabDAS (DYNAPAR), ASYST, LABTECH, UnitedSystems.

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- Digital I/O: 16 digital inputs and 16 digital outputs. TTL compatible.

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ADVANTAGES OF USING PCs :

There are approximately 35.000.000 PCs in the world.

Cheap (400-20.000 US$), reliable, service available everywhere in the world. The first commodity computer.

The largest assortment of add-on boards and application programs. All known languages available.

MS-DOS, small, fast, it has no Input-Output protection. The user can change without restriction the interrupt vectors, etc. Most of the times a multitasking, multiuser environment is not needed. (pity the 640 kb limit).

It can handle different operating systems :

MS-DOS, DR DOS (romable) (640 kb limit)

XENIX , Unix like

UNIX , multitasking, multiuser, large and slow;

Santa Cruz Operation (U$S 2.000)

Mark Williams (only US$100)

MINIX, Unix like, public domain

WINDOWS 3.0, multitasking, uses all the memory but it needs compatible programs. They are coming out fast. (a winner)

PICK, Very good operating system to manage large data bases.

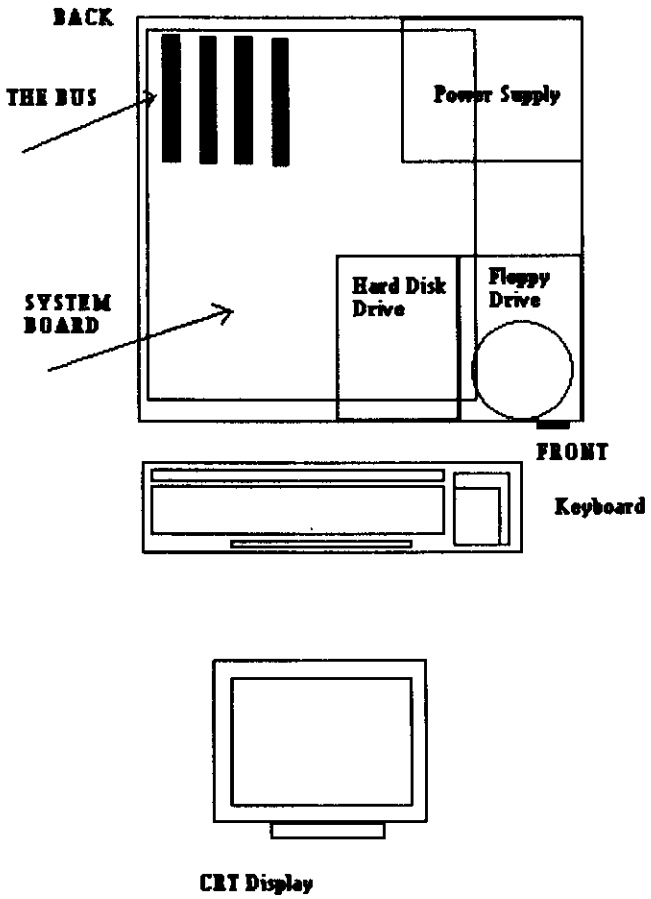
OS-2 Multitasking, uses all the memory. (a loser)

DISADVANTAGES OF THE PC FAMILY

It shouldn't be used for teaching. Memory segmentation is difficult to understand and manage. The new 80386 and 486 driven systems could be used as teaching platforms, but without MS-DOS.

THE WORSE OFFENDER IS MS-DOS ITSELF WITH ITS 640 KB MEMORY LIMIT. Otherwise we would live in a mono-computer world.

THE PARTS OF AN IBM XT LIKE COMPUTER



OPTIONS

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MonoChrome Display Adapter (MCDA)
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Color Graphics Adapter (CGA)
Enhanced Graphic Adapter (EGA)
Professional Graphics Adapter (PGA)
Video Graphics Array (EGA)

All the above video monitors and adapter are supported in all models of the PCs and Dos versions.

Floppy Drives :

5 1/4" drives 160kb-1.2 Mb
3 1/2" drives 720 kb - 1.4 Mb

DOS versions 3.2 and under don´t not support 3 1/2" drives.

DOS FLOPPY DISK FORMATS

FORMAT	TRACKS	SECTORS PER TRACK	TOTAL SECTORS	USABLE CAPACITY
SSDD	40	8	320	160 KB
DSDD	40	8	640	320 KB
SSDD-9	40	9	360	180 KB
DSDD-9	40	9	720	360 KB
QD-9	80	9	1420	720 KB
QD-15	80	15	2400	1.2 MB
QD-18	80	18	2880	1.4 MB

Hard Disks :

Capacities from 10 Mb to 1 Gb. Disk controllers available in MFM, RLL, IDE, SCSI, etc.

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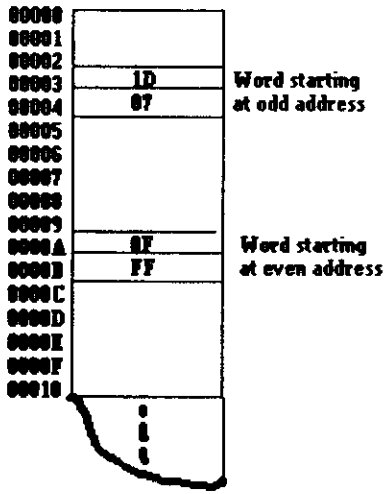
ETC,ETC

The 8086 and the 8088 differ in the external data bus. The 8088 is an 8-bit bus version of the 8086. Its instruction set and basic architecture are identical to the 8086. They differ also in speed, generally the 8088 is a 4.77 Mhz chip (the NEC V20 reaches 12 Mhz) while the 8086 is an 8 Mhz chip.

The 8088/86 memory structure

The chips manage up to 1 Mbyte of memory from 00000 to FFFFF in hexadecimal notacion. It requires 20 bit for the external bus address.

Two consecutive bytes form a word.
The smallest of the two byte addresses is the word address.
When the address of the word is an even number, the word is said to start at an even address,else it is an odd address.



In a word, bits from 0-7 are called the low order byte, while bits from 8-15 is the high order byte.
The address of the word is the lower of the two addresses of the bytes comprising the word, consequently the byte with the lower address is the low order byte of the word.
MOTOROLA STORES A WORD IN EXACTLY THE OPPOSITE ORDER.

In the 8088-86 memory structure words appear as being stored backwards.

The words stored in memory at odd and even addresses are :

071Dh and FF0Fh

A paragraph is a piece of contiguous memory containing 16 bytes. The paragraph address is the address address of the lowest byte contained in the paragraph. The 1 Mb address space of the 8088 in paragraphs can be seen as

Paragraph address	**Bytes within the paragraph**
00000	00000-0000F
00010	00010-0001F
....	....
FFFF0	FFFF0-FFFFF

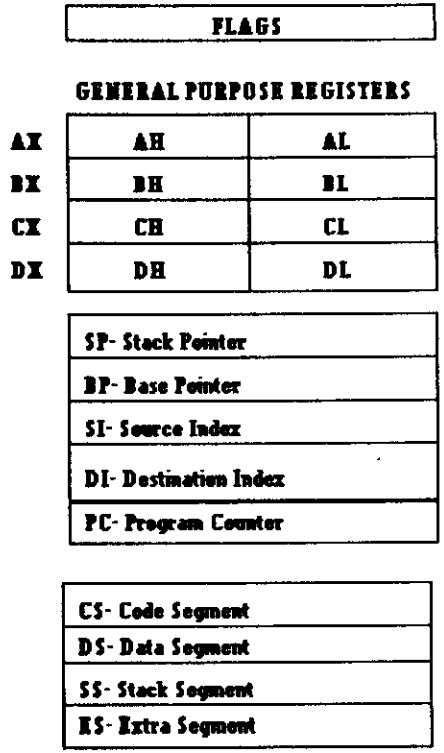
There is a total of 64k paragraphs in the 1 Mb memory space.

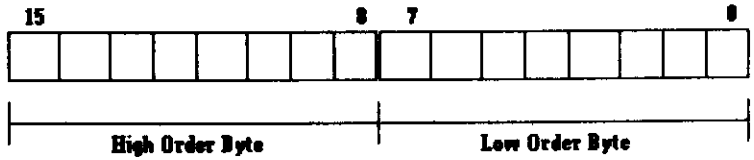
Memory segmentation

The absolute address of a byte or word requires 20 bits. However the 8088 is a 16 bit CPU. To obtain a 20 bit address out of 16 bit registed Intel organized the memory space in segments. (this is the reason why the 8088 is no good for teaching)

One segment is any number of bytes up to a maximum of 64 kbytes. A segment may start at any place in memory as long as it is in a paragraph boundary. This means that the absolute address of any segment will always start with address that ends with a 0. (i.e. xxxx0h)
The segment address is 16 bit number.
To reference a byte within a segment, as the segment is 64 kb long, we need another 16 bit number (the byte offset)

The 8088-86 chip has 16 bit register, this means that the largest "address" that can be internally calculated is 16 bits long. But as we want to address 1Mb of extern memory we need a 20 bit address.
a) By splitting memory into paragraphs (16 bytes) any paragraph in memory can be represented by a 16 bit number.
b) Since a segment (64 kb) starts at a paragraph boundary, a byte can be referenced by means of a 16 bit offset from the start of the segment boundary plus the segment address.





A single 16 bit register comprised og two eight bit bytes

Memory Segmentation and Segment registers

Any program running under MS-DOS is allowed to to specify up to four distinct segments for simultaneous use within the program. Because any segment is limited to 64 kb, the programs is limited to referencing a total of 254 kb.

The intended purpose of each of these segments is identified by its name :

Code Segment : is the segment tha contains the program instructions.

Data Segment : contains the program´s data.

Extra Segment : may be used for storing additional data or for holding and manipulating strings.

Stack Segment : contains the programs run time stack, used for calling subroutines and passing arguments between routines.

REGISTERS IN THE 8088-86 ARCHITECTURE

General Registers : AX, BX, CX and DX (not related to Citroen automovile models) these 16 bit general purpose registers can also be considered as two 8 bit registers called AL, AH, BL, BH, etc.

Pointer and Index registers : The Stack Pointer points to the current top of the stack "within the stack segment". The Base Pointer contains an offset from the stack pointer to retrieve data placed on the stack. The Source Index and Destination Index are used for string operations but they are also general purpose index registers. The string instructions are a subset of the 8088 instruction set.

Segment Registers : CS,DS, ES and SS point to segments as explained before.

Program Counter : (instruction pointer) points to the next instruction to be executed. It is used with the CS register to fetch the next instruction from memory.

FLAGS

Nine flags that indicate the condition of the chip after the execution of the last instruction. The flags are tested and according to the result of the test the 8088 continues with the execution of the next instruction or branches to some other address.

FLAG	MNEMONIC AND NAME	FUNCTION
OF	OverFlow	Set if result has overflowed a range.
DF	Direction Flag	Determines the direction of string instructions.
IF	InterruptEnable	Allows-disallows interrupts to be processed.
TF	Trap Flag	If set the 8088 single steps, for program debugging.
SF	Sign Flag	Set when result is negative
ZF	Zero Flag	Set when result is zero.
AF	Auxiliary Flag	Set when a carry is generated from the least significant four bits of the last result.
PF	Parity Flag	Set when parity of result is even
CF	Carry Flag	Set if result has generated a carry.

INPUT/OUTPUT STRUCTURE

There are special instruction to address I/O ports, IN and OUT. The 8088 is capable of addressing 64 k ports.

INTERRUPTS

An interrupt allows the computer to suspend whatever it was doing and switch to some other task based on something that causes the interruption.

When the micro is interrupted "a record" of what it was doing is kept on the stack in order for the micro to resume the work where it left it.

There are three types of interrupts : hardware interrupts, exception interrupts and software interrupts.

You have already heard a lot about hardware and software interrupts.

Exception interrupts are generated when during the execution of a program the chip finds an instruction that, for example doesn´t exist in its "repertoire" or when we are trying to divide by zero. In the previous

cases the chip generates an "exception interrupt" to abort what it was doing ,that was irreparably flawed, and recover itself from the difficulty.

THE IBM PC BUS (I/O CHANNEL)

The IBM bus (I/O channel) is a set of 62 lines connected to five card-edge connectors. Non system hardware is added to the PC by simply plugging cards into the connectors. (see pin-out in next transparency)

The lines can be classified according to the function they perform : (details in the IBM spec-sheets)

Address - A0-A19

Data - D0-D7

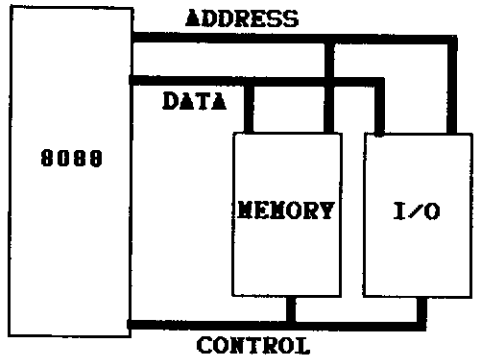
Control - MEMW, MEMR, IOR, IOW (All active low), ALE, AEN, I/O CH RDY, RESET DRV

Direct Memory Addressing (DMA) - DRQ1-DRQ3, DACK1-DACK3, TC

Interrupt - IRQ2-IRQ7

Clocks - OSC, CLK

Power Supply - +5, -5, +12, -12, GND



The address lines are 20. They can code memory addresses from 00000h to FFFFFh (1 Mb).

But only 16 lines are active during an I/O cycle . This limits the I/O port to addresses from 0000h to 0FFFFh (64 k). In the IBM PC only the lower 10 of these lines are decoded during an I/O instruction limiting further the range of I/O channels to 1 k.

The main control lines needed to connect an I/O card are :

IOR I/O read, active low during I/O read.
IOW I/O write, active low during I/O write.

A memory read or write cycle uses four clock cycles while an I/O read or write uses five clock cycles that can even be complemented by several wait cucles under request from the I/O card.

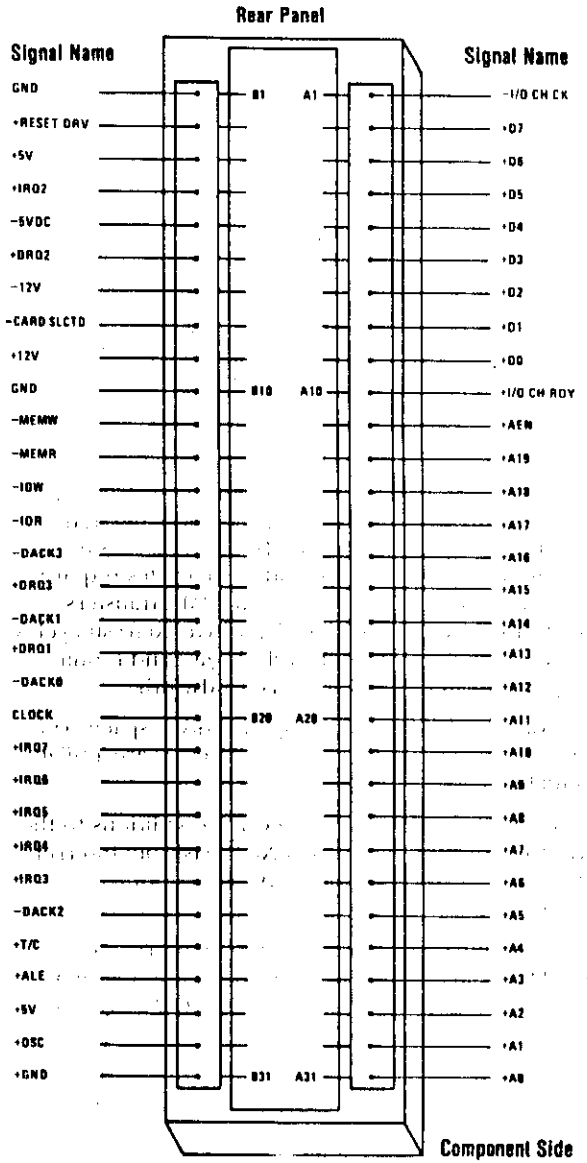
PROCESSOR INITIATED BUS CYCLES

Designing an interface requires a good understanding of bus cycles and of its timing restrictions.

We are only interested in I/O read and write cycles although a memory cycle is not much different.

The clock signal is a 2 to 1 mark space ratio with a low time of 140 ns and a high of 70. A single bus access requires five clock cycles. Hence, an I/O cycle can be completed in a minimum of 1.02 microsec at 4.77 MHz.

You can extend the I/O read-write cycle by a period asserting the I/I CH RDY line .The PC senses this level on the leading edge of T2.



I/O Channel Description

The following is a description of the IBM Personal Computer XT I/O Channel. All lines are TTL-compatible.

Signal	I/O	Description
OSC	O	Oscillator: High-speed clock with a 70-ns period (14.31818 MHz). It has a 50% duty cycle.
CLK	O	System clock: It is a divide-by-three of the oscillator and has a period of 210 ns (4.77 MHz). The clock has a 33% duty cycle.
RESET DRV	O	This line is used to reset or initialize system logic upon power-up or during a low line voltage outage. This signal is synchronized to the falling edge of clock and is active high.
A0-A19	O	Address bits 0 to 19: These lines are used to address memory and I/O devices within the system. The 20 address lines allow access of up to 1 megabyte of memory. A0 is the least significant bit (LSB) and A19 is the most significant bit (MSB). These lines are generated by either the processor or DMA controller. They are active high.
D0-D7	I/O	Data Bits 0 to 7: These lines provide data bus bits 0 to 7 for the processor, memory, and I/O devices. D0 is the least significant bit (LSB) and D7 is the most significant bit (MSB). These lines are active high.
ALE	O	Address Latch Enable: This line is provided by the 8288 Bus Controller and is used on the system board to latch valid addresses from the processor. It is available to the I/O channel as an indicator of a valid processor address (when used with AEN). Processor addresses are latched with the failing edge of ALE.
$\overline{\text{I/O CH CK}}$	I	-I/O Channel Check: This line provides the processor with parity (error) information on memory or devices in the I/O channel. When this signal is active low, a parity error is indicated.

Signal	I/O	Description
I/O CH RDY	I	I/O Channel Ready: This line, normally high (ready), is pulled low (not ready) by a memory or I/O device to lengthen I/O or memory cycles. It allows slower devices to attach to the I/O channel with a minimum of difficulty. Any slow device using this line should drive it low immediately upon detecting a valid address and a read or write command. This line should never be held low longer than 10 clock cycles. Machine cycles (I/O or memory) are extended by an integral number of CLK cycles (210 ns).
IRQ2-IRQ7	I	Interrupt Request 2 to 7: These lines are used to signal the processor that an I/O device requires attention. They are prioritized with IRQ2 as the highest priority and IRQ7 as the lowest. An Interrupt Request is generated by raising an IRQ line (low to high) and holding it high until it is acknowledged by the processor (interrupt service routine).
$\overline{\text{IOR}}$	O	-I/O Read Command: This command line instructs an I/O device to drive its data onto the data bus. It may be driven by the processor or the DMA controller. This signal is active low.
$\overline{\text{IOW}}$	O	-I/O Write Command: This command line instructs an I/O device to read the data on the data bus. It may be driven by the processor or the DMA controller. This signal is active low.
$\overline{\text{MEMR}}$	O	Memory Read Command: This command line instructs the memory to drive its data onto the data bus. It may be driven by the processor or the DMA controller. This signal is active low.
$\overline{\text{MEMW}}$	O	Memory Write Command: This command line instructs the memory to store the data present on the data bus. It may be driven by the processor or the DMA controller. This signal is active low.

Signal	I/O	Description
DRQ1-DRQ3	I	DMA Request 1 to 3: These lines are asynchronous channel requests used by peripheral devices to gain DMA service. They are prioritized with DRQ3 being the lowest and DRQ1 being the highest. A request is generated by bringing a DRQ line to an active level (high). A DRQ line must be held high until the corresponding DACK line goes active.
$\overline{\text{DACK0}}$-$\overline{\text{DACK3}}$	O	-DMA Acknowledge 0 to 3: These lines are used to acknowledge DMA requests (DRQ1-DRQ3) and to refresh system dynamic memory (DACK0). They are active low.
AEN	O	Address Enable: This line is used to de-gate the processor and other devices from the I/O channel to allow DMA transfers to take place. When this line is active (high), the DMA controller has control of the address bus, data bus, read command lines (memory and I/O), and the write command lines (memory and I/O).
T/C	O	Terminal Count: This line provides a pulse when the terminal count for any DMA channel is reached. This signal is active high.
$\overline{\text{CARD SLCTD}}$	I	-Card Selected: This line is activated by cards in expansion slot J8. It signals the system board that the card has been selected and that appropriate drivers on the system board should be directed to either read from, or write to, expansion slot J8. Connectors J1 through J8 are tied together at this pin, but the system board does not use their signal. This line should be driven by an open collector device.

The following voltages are available on the system-board I/O channel:

+5 Vdc ± 5%, located on 2 connector pins
-5 Vdc ± 10%, located on 1 connector pin
+12 Vdc ± 5%, located on 1 connector pin
-12 Vdc ± 10%, located on 1 connector pin
GND (Ground), located on 3 connector pins

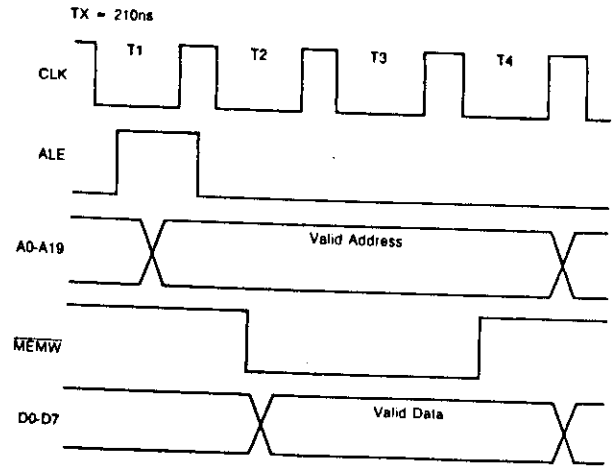


Figure 14-5 Memory-Write Bus Cycle

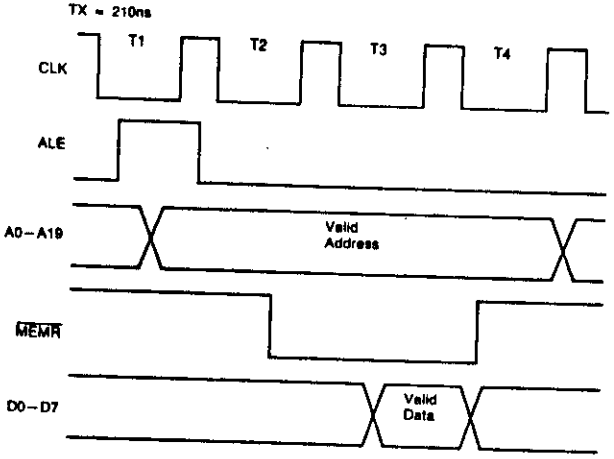
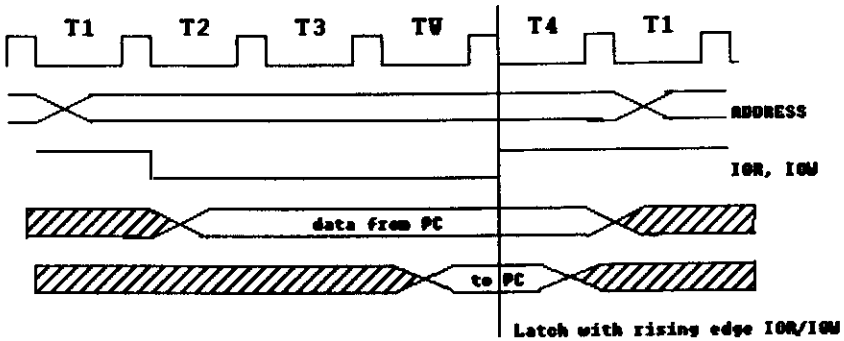


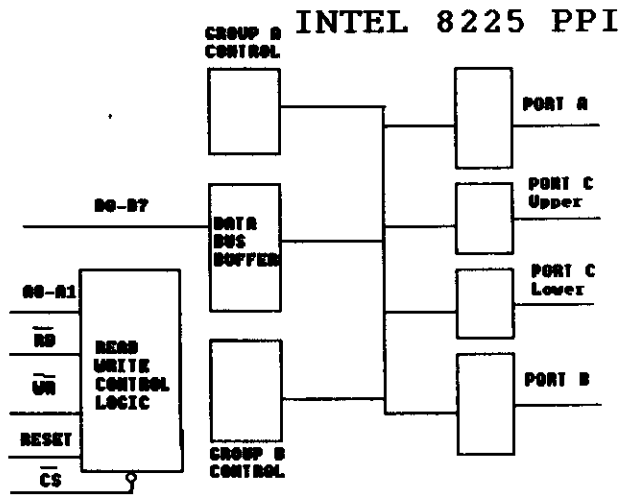
Figure 14-6 Memory-Read Bus Cycle



I/O cycle , T:210 ns. No I/O CH RDY asserted else TW1 would be inserted before TW.

As we said before, the IBM PC has the annoying restriction that only A0-A9 are decoded when performing I/O. IBM assigns standard I/O locations to many devices in this 1 k space. These assignments are shown in the corresponding table. A free address position has to be found before plugging in a card.

DESIGNING A VERY SIMPLE INTERFACE CARD



Because it belongs to the 8088 family we will use the 8225 Programmable Peripheral Interface adapter.

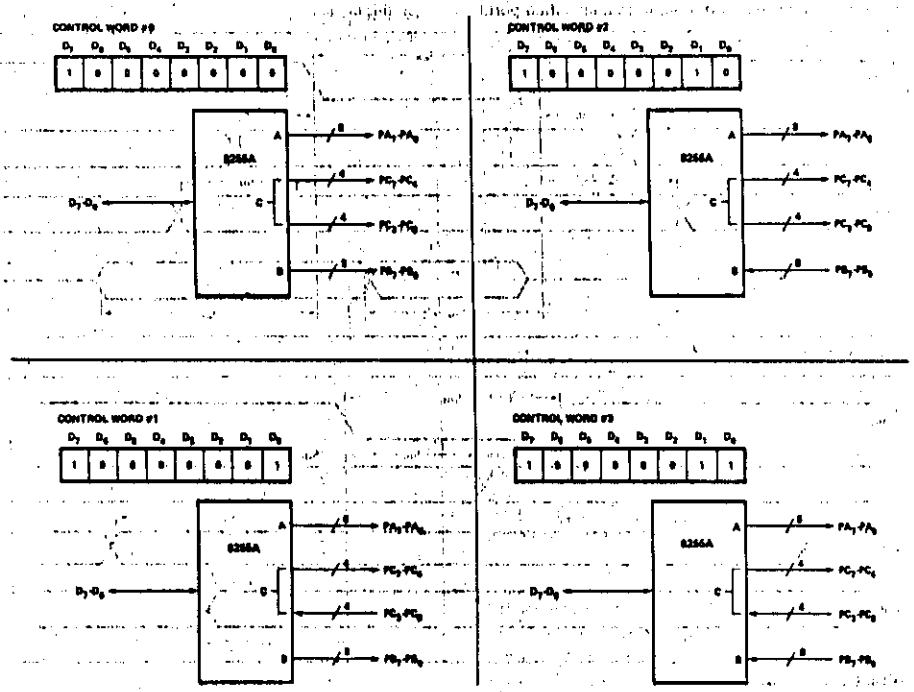
The basic operations of the 8225 are :

A1	A0	RD	WR	CS	Input Operation (read)
0	0	0	1	0	Port A to Data bus
0	1	0	1	0	Port B to Data bus
1	0	0	1	0	Port C to Data bus
					Output Operation (write)
0	0	1	0	0	Data Bus to Port A
0	1	1	0	0	Data Bus to Port B
1	0	1	0	0	Data Bus to Port C
1	1	1	0	0	Data Bus to Control
					Disable Functions
X	X	X	X	1	Data Bus in 3-state
1	1	0	1	0	Illegal condition
X	X	1	1	0	Data Bus in 3-state

MODE 0 Port Definition

A		B		GROUP A			GROUP B	
D_4	D_3	D_1	D_0	PORT A	PORT C (UPPER)	#	PORT B	PORT C (LOWER)
0	0	0	0	OUTPUT	OUTPUT	0	OUTPUT	OUTPUT
0	0	0	1	OUTPUT	OUTPUT	1	OUTPUT	INPUT
0	0	1	0	OUTPUT	OUTPUT	2	INPUT	OUTPUT
0	0	1	1	OUTPUT	OUTPUT	3	INPUT	INPUT
0	1	0	0	OUTPUT	INPUT	4	OUTPUT	OUTPUT
0	1	0	1	OUTPUT	INPUT	5	OUTPUT	INPUT
0	1	1	0	OUTPUT	INPUT	6	INPUT	OUTPUT
0	1	1	1	OUTPUT	INPUT	7	INPUT	INPUT
1	0	0	0	INPUT	OUTPUT	8	OUTPUT	OUTPUT
1	0	0	1	INPUT	OUTPUT	9	OUTPUT	INPUT
1	0	1	0	INPUT	OUTPUT	10	INPUT	OUTPUT
1	0	1	1	INPUT	OUTPUT	11	INPUT	INPUT
1	1	0	0	INPUT	INPUT	12	OUTPUT	OUTPUT
1	1	0	1	INPUT	INPUT	13	OUTPUT	INPUT
1	1	1	0	INPUT	INPUT	14	INPUT	OUTPUT
1	1	1	1	INPUT	INPUT	15	INPUT	INPUT

MODE 0 Configurations



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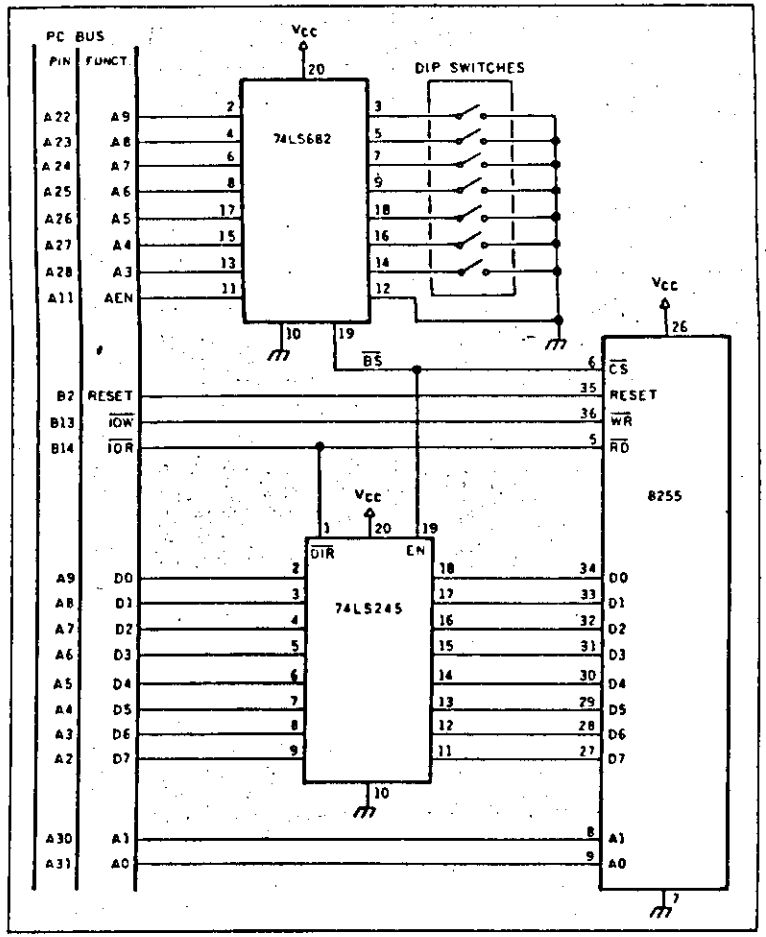

Figure 4: *A minimal interface circuit using the 8255. The 8255 response time is sufficient, so you don't need to use I/O CH RDY to extend PC I/O cycles. You do not use address line A2.*

TABLE 15-1 I/O CHANNEL PORT ASSIGNMENTS

Port values (Hex)	Function
200-20F	Game control
210-217	Expansion unit
220-24F	Reserved
278-27F	Reserved
2F0-2F7	Reserved
2F8-2FF	Asynchronous communications (secondary)
300-31F	Prototype card
320-32F	Fixed disk
378-37F	Printer
380-38C	SDLC communications
380-389	Binary synchronous communications (secondary)
3A0-3A9	Binary synchronous communications (primary)
3B0-3BF	IBM monochrome display/printer
3C0-3CF	Reserved
3D0-3DF	Color/graphics
3E0-3F7	Reserved
3F0-3F7	Diskette
3F8-3FF	Asynchronous communications (primary)

example, the system board ignores IN or OUT instructions addressing port 300H. By decoding address lines A10–A15, we could design a decoding scheme that expanded port 300H into 64 different ports.

A15	A14	A13	A12	A11	A10	A9	A8	A7	A6	A5	A4	A3	A2	A1	A0
X	X	X	X	X	X	1	1	0	0	0	0	0	0	0	0
Ignored by system						Decoded by system									

Thus ports 300H, 700H, 0B00H, 0F00H, 1300H, . . . could be uniquely decoded. This technique should prevent you from running out of ports.

RODUCTION TO LOGIC GATES

We provide this introduction for those who are unfamiliar with the subject or notation. Readers experienced in this area should proceed to the next section.

Figure 15-1 shows five elementary gates from which one can build almost anything. Four of the gates have two inputs and one output. The input and output values are restricted to either zeros or ones. The output value of each gate is completely determined by the input values as shown in the "truth tables." A circle present on an input or output indicates the presence of an internal inverter. The OUT shown in the truth table for the NAND (Negative AND) gate is the inverse of the OUT in the truth table for the AND gate due to the inverter. The one gate with a single input merely inverts the input signal.

unmask
procedu

As an example, the shortest possible latency on INTR is 13 μs, if it is assumed that an instruction has just finished and no higher-priority interrupts are executing. The longest latency (if no higher-priority interrupts are executing) is 56 μs (43 μs + 13 μs). Even longer latencies can occur.

USING INTERRUPTS IN THE I/O CHANNEL

The IR2–IR7 pins of the system's 8259A are connected directly to the I/O channel, where they appear as IRQ2–IRQ7. The IBM PC Technical Reference Manual specifies the following uses for these interrupts:

IRQ2 Reserved
IRQ3 Asynchronous Communications (Secondary)
SDLC Communications
BSC (Secondary)
IRQ4 Asynchronous Communications (Primary)
SDLC Communications
BSC (Primary)
IRQ5 Fixed Disk
IRQ6 Diskette
IRQ7 Printer

Although it appears at first glance that all the IRQ lines are in use, most systems will have several free. IRQ2 is currently not in use although it may be reserved for a future IBM product. IRQ5 is free unless your system has a fixed disk. At any rate, if you wish to service I/O devices on an interrupt basis, you must configure your system so that at least one of the IRQ lines is free.

It should be mentioned in passing that it is possible to connect several interrupting sources to one IRQ line. Connect an inverter to the IRQ line and feed the inverter with hardware so that the interrupt service routine can determine which device