INTERNATIONAL ATOMIC ENERGY AGENCY
UNITED NATIONS EDUCATIONAL, SCIENTIFIC AND CULTURAL ORGANIZATION
INTERNATIONAL CENTRE FOR THEORETICAL PHYSICS
I.C.T.P., P.O. BOX 586, 34100 TRIESTE, ITALY, CABLE: CENTRATOM TRIESTE

UNITED NATIONS INDUSTRIAL DEVELOPMENT ORGANIZATION

INTERNATIONAL CENTRE FOR SCIENCE AND HIGH TECHNOLOGY

SMR/542 - 11

ICTP-INFN
SECOND COURSE ON BASIC VLSI DESIGN TECHNIQUES
18 February - 15 March 1991

Design of Analogue Circuits on CMOS Technology

Ignatius S.A. BEZZAM
Centre for Development of Advance Computing
Pune University Campus
Pune 411 007
India

Design of Analog Circuits

on

CMOS Technology

Circuit Components Available on Standard CMOS Technology

- Analog Switches
- Current Mirrors
- Inverters with Active Load
- Source Followers
- Differential Stages
- Voltage Dividers
- Level Shifters
- Current and Voltage References

Design Techniques to Improve Performance

1. Cascoding
2. Feed Back
3. Bootstrapping

— Linear (or Triode) Region

$V_{GS} > V_{TH}$, $V_{DS} < V_{GS} - V_{TH}$

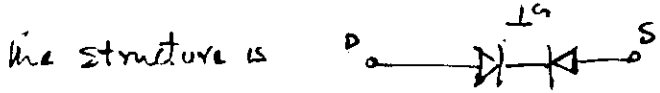
$$I_D = \mu C_{ox} \frac{W}{L} \left[(V_{GS} - V_{TH}) V_{DS} - \frac{V_{DS}^2}{2} \right]$$

For continuity

$$I_D = \mu C_{ox} \frac{W}{L} \left[(V_{GS} - V_{TH}) V_{DS} - \frac{V_{DS}^2}{2} \right] \cdot (1 + \lambda V_{DS})$$

A voltage variable resistor/

— Weak Inversion (Subthreshold) Region . $V_{GS} < V_{TH}$

the structure is 

$$I_S = I_{DO} e^{q V_G / nkT} \cdot e^{-q V_B / nkT}$$

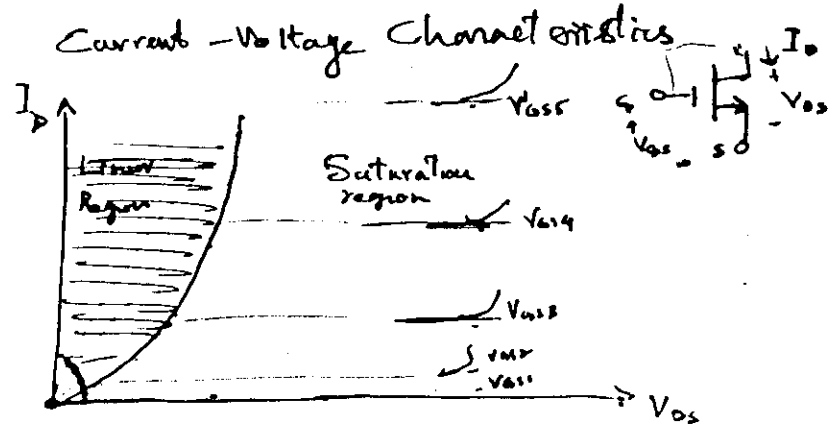
$$I_D = I_{DO} e^{q V_G / nkT} e^{-q V_B / nkT} \left[1 - e^{-q V_{DS} / kT} \right]$$

Behavior similar to Bipolar Transistors

— Cutoff . $V_{GS} << V_{TH}$

MOS Transistor Behavior

Current – Voltage Characteristics



Regions of operation with reference to V_{TH}

- Saturation Region, $V_{GS} > V_{TH}$ & $V_{DS} > V_{GS} - V_{TH}$

$$I_D = \frac{1}{2} \mu C_{ox} \cdot \frac{W}{L} \cdot (V_{GS} - V_{TH})^2$$ – Ideal eqn

$$\boxed{I_D = \frac{1}{2} \mu C_{ox} \frac{W}{L} (V_{GS} - V_{TH})^2 (1 + \lambda V_{DS})}$$

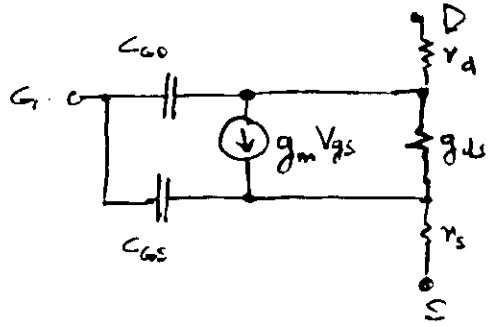
λ – channel length modulation (0.05/V)

$$\lambda = \epsilon / q N_A L^2$$

ϵ – permittivity of Silicon
q – electron charge
N_A – substrate doping
L – Channel length (effective)

→ λ is important for Analog Circuits
→ determines the impedance of the device ($1/\lambda I_D$)
→ $K = \mu C_{ox}$ is the process transconductance parameter. $K_n \sim 35 \mu A/V^2$

SIMPLIFIED SMALL SIGNAL EQUIVALENT CIRCUIT



THE OUTPUT CURRENT SOURCE IS LINEARISED AS

$$I_D = I_D(V_{GS}, V_{DS})$$

$$g_m = \frac{\partial I_D}{\partial V_{GS}} \cdot \text{transconductance}$$

$$g_{ds} = \frac{\partial I_D}{\partial V_{DS}} \quad \text{Drain Output conductance}$$

For normal range of operations

$$r_d, r_s \ll 1/g_{ds}$$

THERE IS ALSO A SUBSTRATE TRANSCONDUCTACE

$$g_{mb} = \frac{\partial I_D}{\partial V_{BS}}$$

if Body effect exists. (neglected)

TRANSCONDUCTANCE g_m

- SATURATION REGION

$$g_m = \mu C_{ox} \frac{W}{L} \cdot (V_{GS} - V_{TH})$$

$$= \frac{2 I_D}{(V_{GS} - V_{TH})}$$

$$= \sqrt{2 \mu C_{ox} \left(\frac{W}{L}\right) \cdot I_D}$$

HENCE g_m ONLY IMPROVES AS ROOT OF CURRENT

IN PRACTICE g_m IS EVEN SMALLER THAN ABOVE.

LIMITATION COMPARED TO BIPOLAR

- SUBTHRESHOLD REGION

$$g_m = \frac{I_D}{n \cdot KT/q}$$

Like a Bipolar Transistor

DRAIN OUTPUT CONDUCTANCE (g_{ds})

- SATURATION REGION

$$g_{ds} = \lambda I_D$$

- LINEAR REGION

$$g_{ds} = \mu C_{ox} \frac{W}{L} (V_{GS} - V_{TH} - V_{DS})$$

For $|V_{DS}| \ll 1$. $g_{ds} = \mu C_{ox} \frac{W}{L} (V_{GS} - V_{TH})$

CAPACITANCES

MOS CAPACITANCE $C_i = C_{ox} WL$

OVERLAP CAPACITANCES

- SATURATION DEVICE REGION

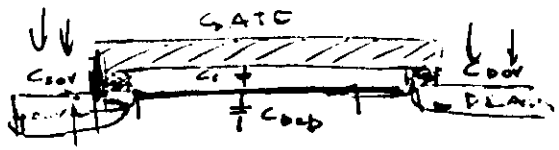
$$C_{GS} = C_{GS,ov} + \frac{2}{3} C_i$$

$$C_{DD} \cong C_{GD,ov}$$

- LINEAR REGION

$$C_{GS} = C_{GS,ov} + C_i/2$$

$$C_{GD} = C_{GD,ov} + C_i/2$$



Threshold Voltage V_{TH} of MOS Devices

Def: The voltage required to generate a conductive channel between source and drain

If substrate bias is zero i.e. $V_{SB} = 0$

$$V_{TO} = V_{FB} - 2\phi_F + \gamma\sqrt{2\phi_F}$$

V_{FB} – Flat band Voltage

ϕ_F – Fermi potential

$\gamma = \frac{\sqrt{2q\varepsilon N_A}}{C_{ox}}$. The body effect coefficient

V_{TO} is specified as Zero Bias Threshold.

When a substrate bias exists

$$V_{TH} = V_{TO} + \gamma\left[\sqrt{|-2\phi_F + V_{SB}|} - \sqrt{|2\phi_F|}\right]$$

This causes a conisderable shift in

⇒ effective threshold voltage.

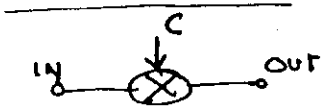
To be taken into account for devices

... N_well / P_well

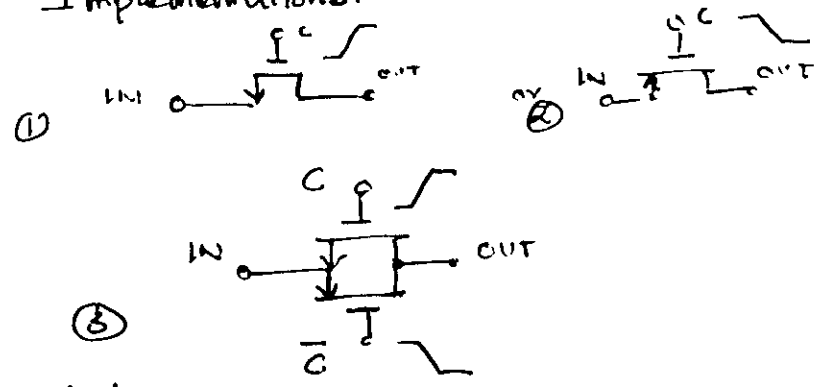
Analog Switches

Transmission Gates

Symbol



Implementations



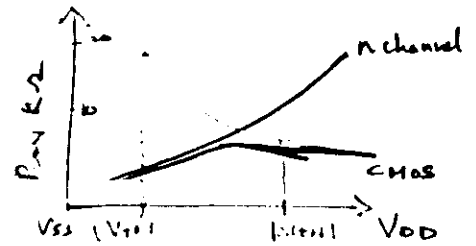
Operation

In steady state $V_{OUT} = V_{IN} \Rightarrow V_{DS} \approx 0$

In linear region the ON-resistance

$$R_{ON} = \frac{1}{g_{ds}} = \frac{1}{\mu C_{ox}\frac{W}{L}.(V_{GS} - V_{TH})}$$

For minimum size devices $\frac{W}{L} = 1$, $R_{ON,n} \approx 3k\Omega$, $R_{ON,p} \approx 9k\Omega$



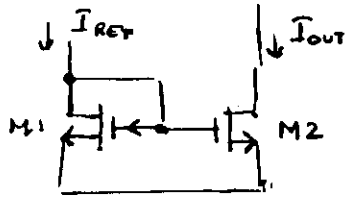
– Very good to switch charge

CURRENT MIRRORS

Def: A CURRENT MIRROR GIVES A REPLICA OR MATCHING OF A BIAS CURRENT OR SIGNAL CURRENT.

APPLICATIONS: D/A CONVERTORS, SINE WAVE GENERATORS OPAMPS etc.

SIMPLE CURRENT MIRROR



Small Signal Eqn.

$$I_{REF} = \frac{k'}{2}\cdot\left(\frac{W}{L}\right)_1 (V_{GS1} - V_{TH})^2 (1+\lambda V_{DS1})$$

$$I_{OUT} = \frac{k'}{2}\left(\frac{W}{L}\right)_2 (V_{GS2} - V_{TH})^2 (1+\lambda V_{DS2})$$

$$V_{DS1} = V_{GS1} = V_{GS2}$$

For FIRST ORDER neglecting λV_{DS} term

$$\boxed{I_{OUT} = \frac{(W/L)_2}{(W/L)_1} I_{REF}}, \quad r_{out} = \frac{1}{\lambda I_2}$$

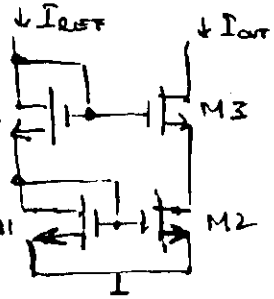
$$\boxed{r_{out} = r_{ds2} = 1/\lambda I_2}$$

⇒ BETTER CURRENT MATCHING THAN BIPOLAR (NO BASE CURRENTS)

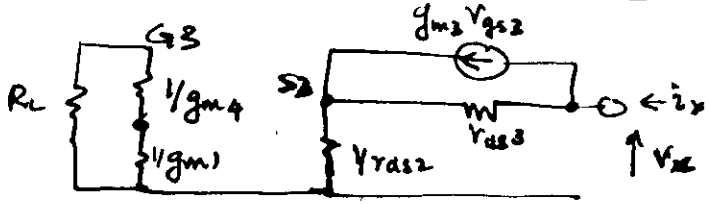
PERFORMANCE LIMITED BY — THRESHOLD MISMATCH
— Channel length modulation λ
— Geometrical Mismatch

DESIGN TECHNIQUES FOR IMPROVED PERFORMANCE

BY IMPROVING OUTPUT RESISTANCE
LARGE CHANNEL LENGTHS
— CASCODING.



Small Signal Equivalent



$$V_x = r_{ds2} I_x + r_{ds3}(1 + g_{m2} r_{ds2}) I_x$$

$$\boxed{r_{out} \cong r_{ds3}\, g_{m2}\, r_{ds2}}$$

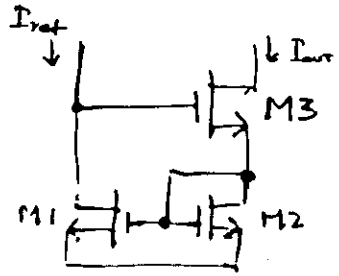
i.e. The output impedance of M2 is increased by a factor of $(r_{ds3} g_{m3})$ OF THE CASCODE TRANSISTOR M3.

⇒ ADVANTAGE IMPROVED OUTPUT RESISTANCE
BETTER MATCHING FOR OUTPUT VOLTAGE VAR.

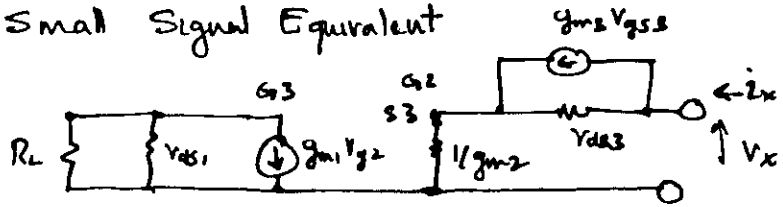
DISADVANTAGE → DECREASED OUTPUT SWING

- FEEDBACK to INCREASE OUTPUT RESISTANCE

WILSON CURRENT MIRROR



Small Signal Equivalent



$$v_{g2} = v_{s3} = i_x/g_{m2}$$

$$v_{g3} = -g_{m1} v_{g2} r_T \qquad (r_T = R_L // r_{gs1})$$

$$v_x = i_x/g_{m2} + (i_x - g_{m3} v_{gs3}) r_{ds3}$$

$$v_{out} = \frac{v_x}{i_x} \simeq \frac{1}{g_{m2}} + r_{ds2}\left[1 + \frac{g_{m3}}{g_{m2}} + \frac{g_{m3}}{g_{m2}} g_{m1} r_T\right]$$

$$v_{out} \simeq r_{ds3} \cdot \frac{g_{m3}}{g_{m2}} \cdot g_{m1} r_T$$

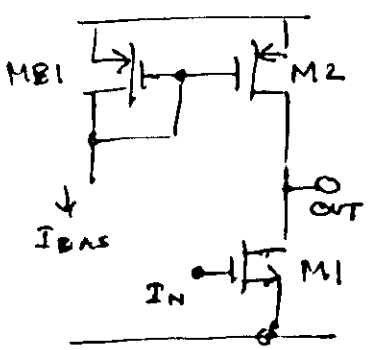
→ Large Output resistance for large R_L

⇒ OFFSET OF $V_{DS1} = V_{DS2} + V_{GS3}$

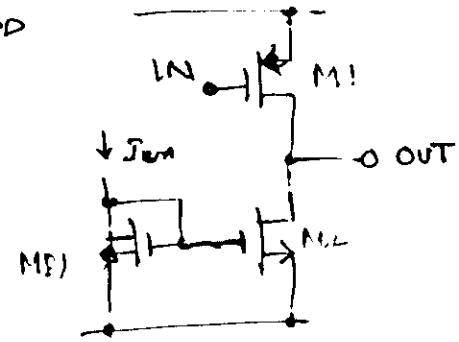
— FEEDBACK INCREASES SPEED

GAIN STAGES

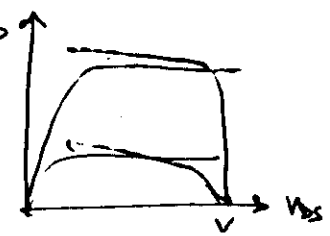
- SIMPLEST – INVERTOR WITH ACTIVE LOAD

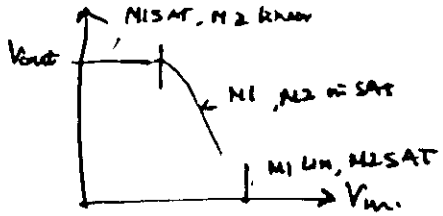


N-channel



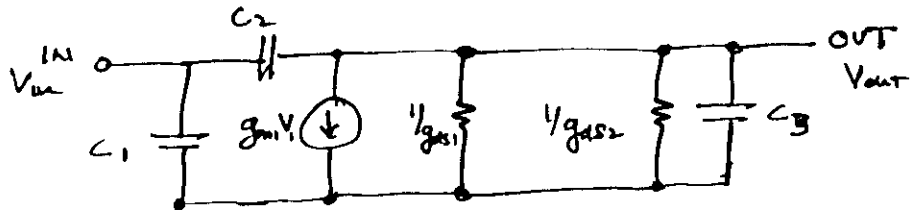
P-channel





UNLIKE IN DIGITAL BOTH TRANSISTORS NEED TO OPERATE IN SATURATION TO GIVE A VOLTAGE GAIN

Small Signal Equivalent



VOLTAGE GAIN $A_v = \frac{V_{out}}{\ldots}$

SINGLE STAGE GAIN

AT LOW FREQUENCIES (DC GAIN)

$$A_v = \frac{V_{out}}{V_{in}} = -\frac{g_{m1}}{g_{ds1} + g_{ds2}}$$

$$g_{m1} = \sqrt{2\mu C_{ox} \frac{W}{L} I_D}$$

$$g_{ds} = \lambda I_D$$

Hence

$$\boxed{A_v = \frac{\sqrt{2\mu C_{ox}(W/L)_1}}{\sqrt{I_D}\,(\lambda_n + \lambda_p)}}$$

DC GAIN INCREASES AS BIAS CURRENT IS DECREASED. (60dB)

MAXIMUM VALUE IS OBTAINED IN SUBTHRESHOLD WHERE IT DOES NOT CHANGE WITH I_D.

AT HIGH FREQUENCY

- OUTPUT CAPACITANCE $= C_2 + C_3$
- OUTPUT RESISTANCE $= 1/(g_{ds1} + g_{ds2})$
- TRANSFER FUNCTION HAS A POLE

$$s_p = \frac{g_{ds} + g_{ds2}}{C_2 + C_3} = \frac{(\lambda_n + \lambda_p) I_D}{C_2 + C_3}$$

THUS IN THE OVERALL CONFIGURATION g_{ds1} and g_{ds2} CAN BE NEGLECTED WITH RESPECT TO g_{ds3}.

AT LOW FREQUENCIES

$$g_{m1} V_{in} = -g_{m2} V_1 = -g_{ds3} V_0$$

HENCE

$$A_v = -\frac{g_{m1}}{g_{ds3}}$$

$$\boxed{A_v = -\frac{\sqrt{2\mu C_{ox}(W/L)_1}}{\sqrt{I_D}\,\lambda_p}}$$

FOR HIGH FREQUENCIES:

- OUTPUT CAPACITANCE C_3
  IMPEDANCE $1/g_{ds3}$
- POLE ASSOCIATED WITH OUTPUT NODE

$$f_{p,out} = \frac{1}{2\pi} \frac{g_{ds3}}{C_3}$$

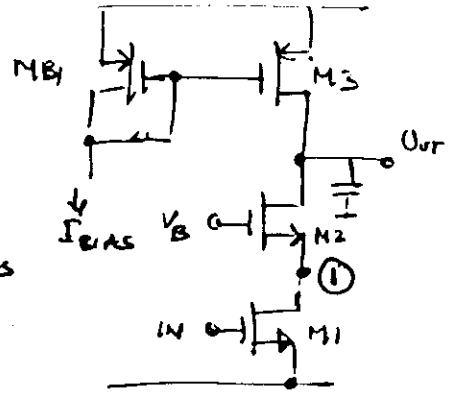
TO MAKE THIS THE DOMINANT POLE

$$g_m \gg g_{ds}$$

$$\boxed{GBW = f_p \cdot A_v = \frac{1}{2\pi} \frac{g_{m1}}{C_3}}$$

IMPROVED SINGLE STAGE GAIN

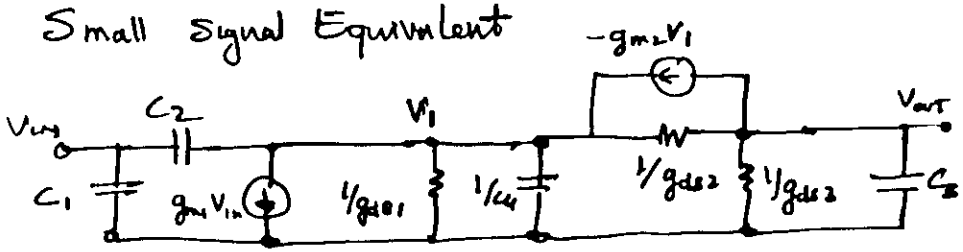
- CASCODE STAGE



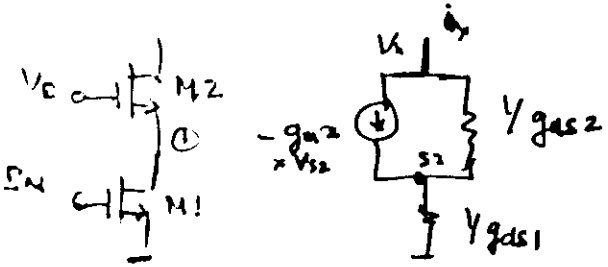
BIAS VOLTAGE V_B keeps M1 in SATURATION

$$V_B > V_{SAT,1} + V_{TH2} + \sqrt{\frac{2 I_{BIAS}}{\mu_n C_{ox} W_2}}$$

Small Signal Equivalent



IMPEDANCE AT DRAIN OF M2



$$V_x = \frac{i_x}{g_{ds1}} + \frac{i_x + g_{m2}V_{s2}}{g_{ds2}} = i_x\left[\frac{1}{g_{ds1}} + \frac{1 + g_{ds2}/g_{ds1}}{g_{ds2}}\right]$$

$$r_{D2} = r_{ds1} + r_{ds2}(1 + g_{m2}/g_{ds1}) \approx g_{m2} r_{ds1} r_{ds2}$$

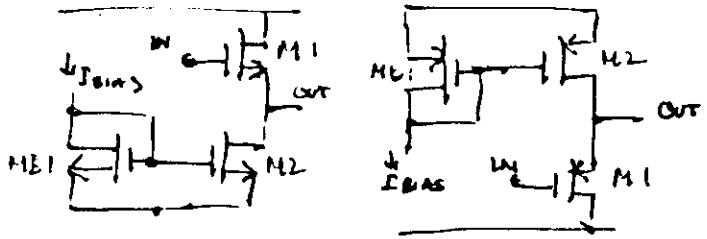
THUS THERE IS A LARGE IMPEDANCE AT DRAIN OF M2

CASCODE WITH CASCODE LOAD

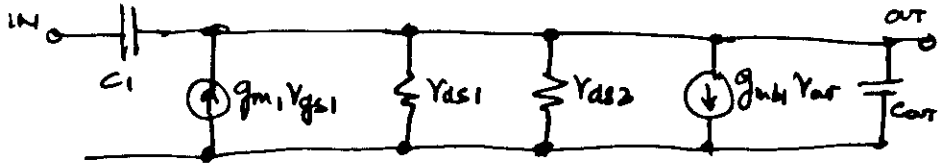
$$A_v = \frac{1}{2}(g_m r_{ds})^2$$

SOURCE FOLLOWER

USED AS BUFFER OR DC-LEVEL SHIFTER.



Small signal Equivalent Circuit



At LOW FREQ: $V_{gs1} = V_{in} - V_{out}$

$$(g_{ds1} + g_{ds2})\,V_{out} + g_{mb1} V_{out} - g_{m1} V_{gs1} = 0$$

$$A_V = \frac{V_{out}}{V_{in}} = \frac{g_{m1} / (g_{ds1} + g_{ds2} + g_{mb1})}{g_{m1} / (g_{ds1} + g_{ds2} + g_{mb1}) + 1}$$

If $g_{m1} >> g_{ds1} + g_{ds2} + g_{mb1}$

$$A_V \approx 1$$

AT HIGH FREQ: $A_V = C_1 / (C_1 + C_{out})$

$C_1 \cong C_{gs1}$

$$R_{OUT} \approx \frac{1}{g_{m1} + g_{ds1} + g_{ds2} + g_{mb1}} \approx \frac{1}{g_{m1}}$$

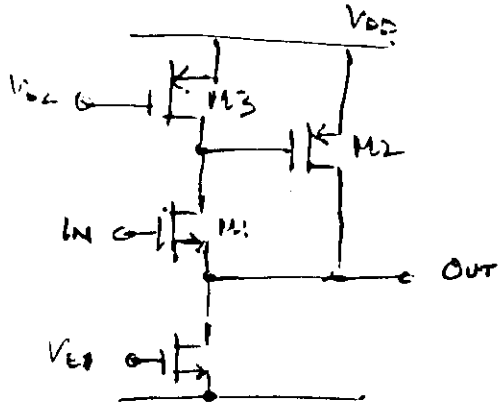
SOURCE FOLLOWER. ...

FOR THE ABOVE, OUTPUT SWING IS NOT SYMMETRICAL.

$V_{OUT,max} = V_{DD} - V_{GS1}$

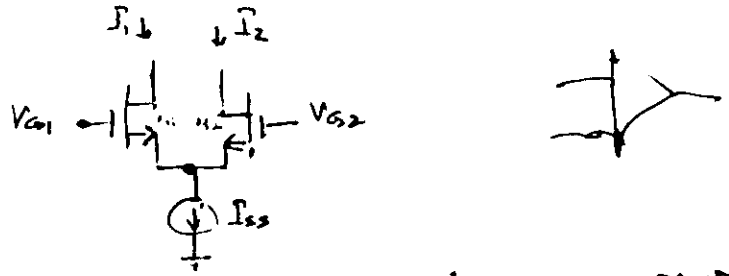
$V_{OUT,min} = V_{GS2}$

IMPROVED PERFORMANCE WITH FEEDBACK



$$R_{OUT} = \frac{1}{g_{m1} + g_{ds4} + g_{m1} g_{m2} r_{ds3}}$$

DIFFERENTIAL STAGE



OPERATING CONDITION : M1, M2 ARE MATCHED PAIR IN SATURATION

$$I_1 = \frac{k'}{2}\left(\frac{W}{L}\right)_1 (V_{GS1} - V_{TH})^2$$

$$I_2 = \frac{k'}{2}\left(\frac{W}{L}\right)_1 (V_{GS2} - V_{TH})^2$$

SPLITTING V_{GS} INTO COMMON AND DIFFERENTIAL SIGNALS

$$V_{GS1} = V_{GS0} + \frac{V_i}{2}$$

$$V_{GS2} = V_{GS0} - V_i/2$$

$$\Delta I = I_1 - I_2 = k' \frac{W}{L} \cdot (V_{GS0} - V_{TH}) \cdot V_i \quad -(1)$$

$$I_{SS} = I_1 + I_2 = k' \frac{W}{L} \cdot (V_{GS0} - V_{TH})^2 \quad -(2)$$

COMBINING (1) and (2)

$$\boxed{\Delta I = \sqrt{k \frac{W}{L} \cdot I_{SS}} \cdot V_i}$$

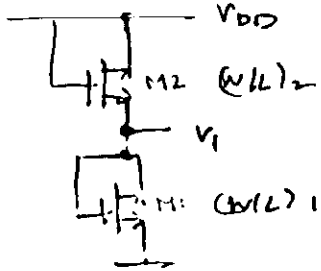
VALID FOR LARGE SIGNALS

FOR SMALL SIGNALS $\boxed{\Delta i = g_m \cdot v_i}$

VOLTAGE DIVIDER

- FOR DC BIAS VOLTAGES
- RESISTIVE OR CAPACITIVE DIVIDERS ARE MORE COMPLEX OR AREA CONSUMING

MOS TRANSISTORS IN DIODE CONFIGURATION



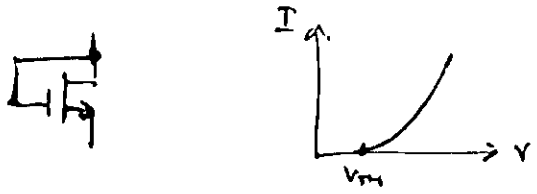
$$\alpha_1 = \sqrt{(W/L)_1} \qquad \alpha_2 = \sqrt{(W/L)_2}$$

$$V_1 = \frac{\alpha_2}{\alpha_1 + \alpha_2} V_{DD} + \frac{\alpha_1 V_{TH1} - \alpha_2 V_{TH2}}{\alpha_1 + \alpha_2}$$

A VOLTAGE DIVISION + OFFSET

LEVEL SHIFTERS

- SIMPLE LEVEL SHIFTER

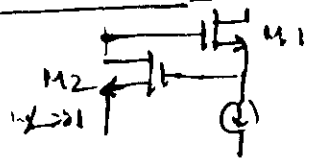


$$\Delta V = \sqrt{\frac{2}{k'}\frac{L}{W}\cdot I} + V_{TH}$$

$$V_{out} = 1/g_m$$

AFFECTED BY THRESHOLD

- SHUNT FEEDBACK LEVEL SHIFTER

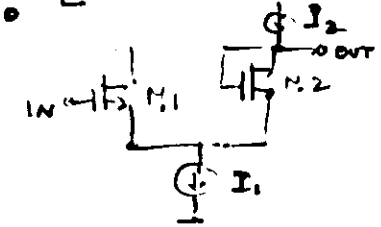


$$\Delta V = V_{GS1} + V_{GS2}$$

$$= V_{TH1} + V_{TH2} + \sqrt{\frac{2}{k'}\left(\frac{L}{W}\right)_1 I_1} + \sqrt{\frac{2}{k'}\frac{L}{W} I_2}$$

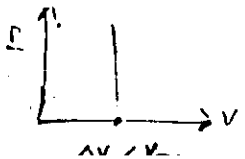
AFFECTED BY TWICE THRESHOLD

- LEVEL SHIFT THRESHOLD-INDEPENDENT



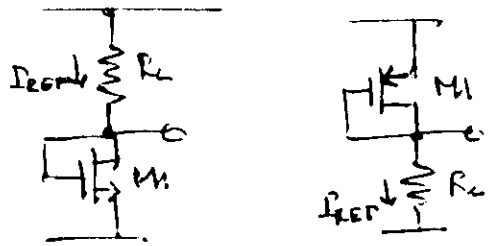
$$\Delta V = \sqrt{\frac{2}{k'}}\left[\sqrt{\left(\frac{L}{W}\right)_1 (I_1 - I_2)} - \sqrt{\left(\frac{L}{W}\right)_2 I_2}\right]$$

$\Delta V < V_{TH}$



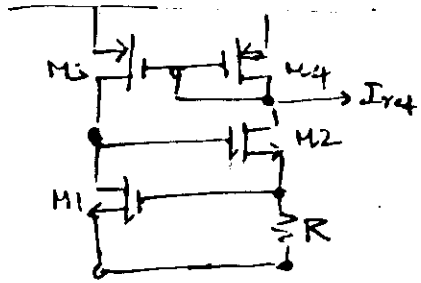
CURRENT REFERENCE

1. SUPPLY DEPENDANT / USING A REFERENCE VOLTAGE



$$I_{ref} = \frac{V_{DD} - V_{DS1}}{R_L}$$

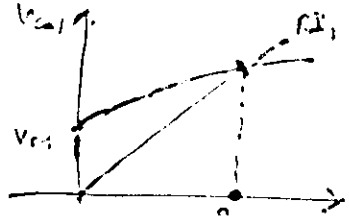
2. Self biased (BOOTSTRAPPED) CURRENT REFERENCE



$$(W/L)_3 = (W/L)_4$$

$$I_1 = I_2 = \frac{k'}{2}\left(\frac{W}{L}\right)_1 (V_{GS1} - V_{TH})^2$$

$$RI_2 = RI_1 = \sqrt{\frac{2I_1}{k'}\left(\frac{L}{W}\right)_1} + V_{TH}$$



VOLTAGE REFERENCES

- Bipolar V_{BE} MULTIPLIER
- THRESHOLD VOLTAGE DIFFERENCE
- BAND GAP REFERENCE
- ZENER ON-CHIP REFERENCE

CONCLUSIONS

1.) MOST OF THE LINEAR CIRCUIT ELEMENTS OF BIPOLAR TECHNOLOGY CAN BE REALISED ON STANDARD CMOS TECHNOLOGY.

2. PERFORMANCE IMPROVEMENTS CAN BE ACHIEVED WITH SPECIAL CKT. TECHNIQUES

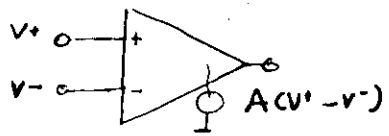
3. SWITCHES, CURRENT MIRRORS & HIGH IMPEDANCES ARE BETTER REALISED IN MOS PROCESSES

4. TRANSCONDUCTANCE, GAIN AND FREQUENCY RESPONSE ARE BETTER IN BIPOLAR TECH.

5. ANALOG & DIGITAL FUNCTIONS CAN BE INTEGRATED ON THE SAME CMOS CHIP.

OPERATIONAL AMPLIFIERS

IDEAL OPAMP IS A VOLTAGE CONTROLLED VOLTAGE SOURCE WITH INFINITE GAIN, INFINITE INPUT IMPEDANCE AND ZERO OUTPUT IMPEDANCE



PRACTICAL OPAMPS NEED TO HAVE A HIGH VOLTAGE GAIN (>1000) SO THAT THE INPUTS FORM A VIRTUAL SHORT. THE INPUT CURRENT SHOULD BE NEGLIGIBLE TO FORM A NULLATOR EQUIVALENT AT THE INPUT i.e. A ZERO VOLTAGE, ZERO CURRENT SOURCE AT INPUT.

PRACTICAL OPAMPS USED IN FEEDBACK CONFIGURATIONS GIVE ALL THE DESIRED ANALOG FUNCTIONS.

TO BE STABLE IN FEEDBACK CONFIG. THE OPAMP MUST BE STABLE i.e. COMPENSATED TO HAVE A GOOD GAIN/PHASE MARGIN. Otherwise the negative feedback would be positive at certain frequencies giving rise to instability or oscillations.

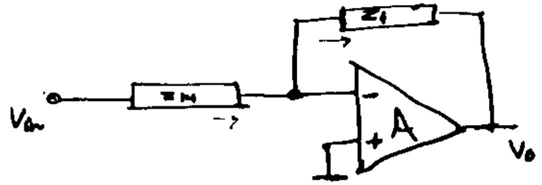
IF THE OPAMP DOES NOT DRIVE RESISTIVE LOADS IT IS NOT NECESSARY TO HAVE A LOW OUTPUT IMPEDANCE. PURE CAPACITATIVE LOADS/FEEDBACKS CAN SELF-COMPENSATE OPAMPS.

FIG. 1. OPAMP - INTERNAL FUNCTIONS

REQUIREMENT: CLOSED LOOP STABILITY
MORE THAN 2 GAIN STAGES DIFFICULT TO COMPENSATE

INSIDE THE CHIP - ONE OR MORE BLOCKS MAYBE COMBINED OR OMMITED COMPLETELY Depending on PARTICULAR USE.

OP AMPS ... (contd.)



$$V_o = -\frac{Z_f}{Z_{in}} V_{in}$$

Various values of Z_f and Z_{in} give various functions.

1. For $Z_f = R_f$, $Z_{in} = R_i$

A VOLTAGE AMPLIFIER OF CONSTANT GAIN

$$V_o = -\frac{R_f}{R_i} V_{in}$$

CONSIDERING A NON IDEAL OPAMP OF GAIN A

$$V_o = \frac{-R_f/R_i \quad V_{in}}{(R_f/R_i)/A + 1}$$

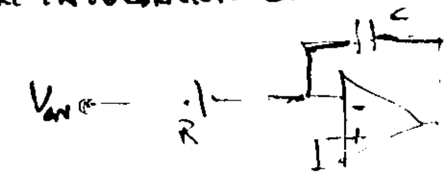
SO IF THE VOLTAGE GAIN REQUIRED R_f/R_i IS small compared to A, i.e. $A >>> R_f/R_i$ EVEN A NON IDEAL OPAMP WOULD GIVE IDEAL RESPONSE

$$V_o \simeq -\frac{R_f}{R_{in}} . V_{in}$$

Internal DC [illegible]

2. FOR $Z_f = C_f$ CAPACITOR
   $Z_{in} = R$ RESISTOR

AN INTEGRATOR OF TIME CONSTANT RC



$Z_f = 1/sC$
$Z_{in} = R$

$$V_o(s) = -\frac{1}{sCR} V(in)$$

$$V_o(t) = V_o(0) - \frac{1}{RC}\int_0^t V_{in}(t)\,dt$$

For $V_o(0) = 0$

$$V_o(t) = \frac{-1}{RC}\int_0^t V_{in}(t)\,dt$$

FOR A NON IDEAL OP AMP

- INPUT LEAKAGE CURRENTS WOULD EFFECT THE CHARGING OPERATION – Error.
- MODERATE DC GAIN IS SUFFICIENT
- NOISE VOLTAGES/CURRENTS DETERMINE MIN. SIGNAL.

MOS OPAMPS FORM GOOD INTEGRATORS AS THE INPUT LEAKAGE CURRENTS ARE PRACTICALLY ZERO.

WHEN DRIVING ONLY ONCHIP NON-RESISTIVE LOADS THEY NEED NOT EXPENSIVE OUTPUT STAGES.

3.

VOLTAGE FOLLOWER

$V_{OUT} = V_{IN}$ for ideal OPAMP

WHEN $V_{IN} = 0V$, $V_{OUT} = 0V$.

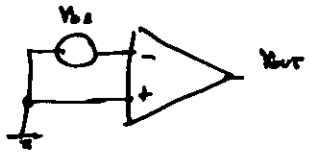
FOR NON IDEAL OPAMP

- EVEN FOR A LARGE VOLTAGE GAIN $A \to \infty$

$V_o = V_{IN}\,(1/1+1/A)$

WHEN $V_{IN} = 0$, $V_{OUT} \neq 0$ but $V_{OUT} = V_{OS}$

THIS IS DUE TO THE OFFSET VOLTAGE OF OPAMP



- OFFSET CAN BE CALCULATED AT A VOLTAGE INPUT OR MEASURED IN THE ABOVE UNITY GAIN CONFIGURATION.
OFFSET CANCELLATION CAN BE IMPLEMENTED

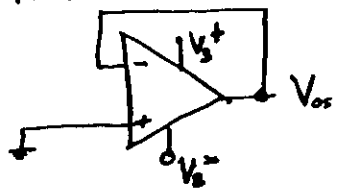
- HOWEVER OFFSET VOLTAGE VARIES WITH THE INPUT VOLTAGE!

VARIATION OF OFFSET WITH INPUT VOLTAGE IS DUE TO COMMON MODE GAIN.

In fact $CMRR = -\dfrac{A_{dm}}{A_{cm}} = 1/\dfrac{\partial V_{os}}{\partial V_{IN}}$

... N ... Rejection Ratio

- OFFSET VOLTAGE ALSO VARIES WITH BIAS SUPPLY VOLTAGES

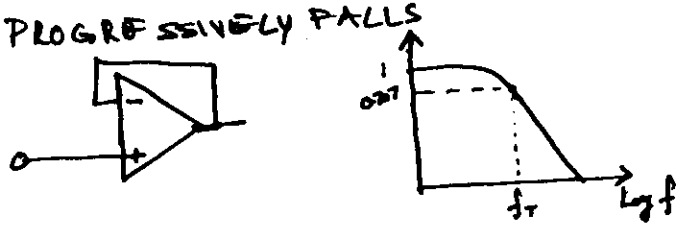


POWER SUPPLY REJECTION

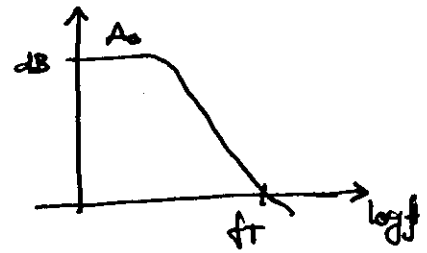
$PSRR^+ = 1 / \dfrac{\partial V_{os}}{\partial V_s^+}$

$PSSRR^- = 1 / \dfrac{\partial V_{os}}{\partial V_s^-}$

- AT HIGH FREQUENCIES THE GAIN PROGRESSIVELY FALLS

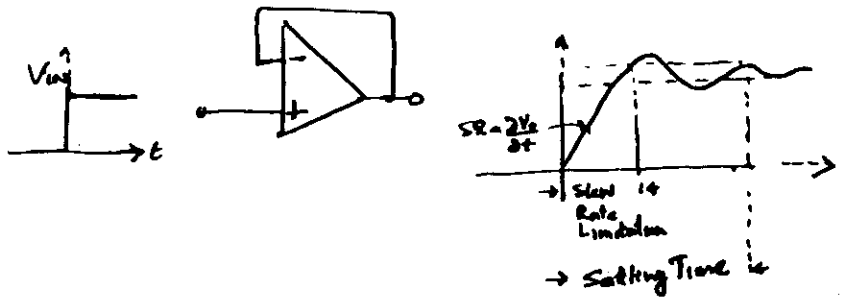


UNITY GAIN BANDWIDTH IS THE FREQUENCY AT WHICH THE OPEN LOOP GAIN (dB) IS ZERO.



THIS IS A BASIC TECHNOLOGY LIMITATION

- FOR HIGH SPEED SIGNALS.



SLEW RATE (SR) : FOR A LARGE STEP INPUT THE MAXIMUM RATE OF CHANGE AT OUTPUT dV_o/dt.

SLEW RATE FOR POSITIVE AND NEGATIVE GOING SIGNALS CAN BE DIFFERENT, DEPENDING ON DESIGN

SETTLING TIME IS THE PERIOD REQUIRED FOR THE OUTPUT TO SETTLE TO WITHIN ±0.1% FINAL VALUE

- FREQUENCY COMPENSATION REQUIRED FOR STABILITY IN CLOSED LOOP OPERATION

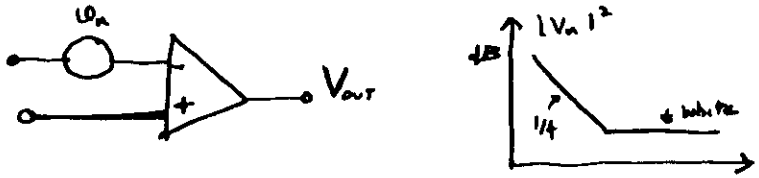
IF THE PHASE SHIFT THROUGH THE AMPLIFIER EXCEEDS 180° FOR FREQUENCIES WITH LOOP GAIN UNITY OR GREATER NEGATIVE FEEDBACK BECOMES POSITIVE.

PHASE COMPENSATION IS USED TO REDUCE GAIN AT FREQUENCIES FOR WHICH PHASE SHIFT IS HIGH

PHASE MARGIN DIRECTLY EFFECTS SETTLING TIME

COMPENSATION TECHNIQUES FOR MOS AMPLIFIERS |

- NOISE FROM THE DEVICES AND COMPONENTS DETERMINE THE SIGNAL SENSITIVITY OR THE MINIMUM SIGNAL THAT CAN BE MEASURED



EQUIVALENT INPUT NOISE.

NOISE IS A FUNDAMENTAL DEVICE LIMITATION
IMPROVED PERFORMANCE WITH CMRR, PSRR.
LOW NOISE DESIGN REQUIRES OPTIMISATION OF W/L OF INPUT TRANSISTORS.

Low 1/f Noise → Large (W·L)

Low White Noise → Large W/L
Small L.

NOISE CAN BE REDUCED (S/N ratio increased) BY INCREASING POWER CONSUMPTION
i.e. LARGER g_m and I_D values.

– OTHER OPAMP PARAMETERS.

1. INPUT COMMON MODE RANGE IS THE MAXIMUM RANGE OF THE INPUT VOLTAGE WHICH CAN BE APPLIED WITHOUT CAUSING A SIGNIFICANT DROP OF THE DIFFERENTIAL GAIN

2. OUTPUT VOLTAGE SWING IS THE SWING OF THE OUTPUT NODE WITHOUT GENERATING HARMONIC DISTORTION ABOVE A SPECIFIED VALUE.

3. POWER CONSUMPTION

   Related to SPEED of THE CIRCUIT

   QUALITY FACTOR → SPEED . POWER PRODUCT

BASIC CMOS AMPLIFIER

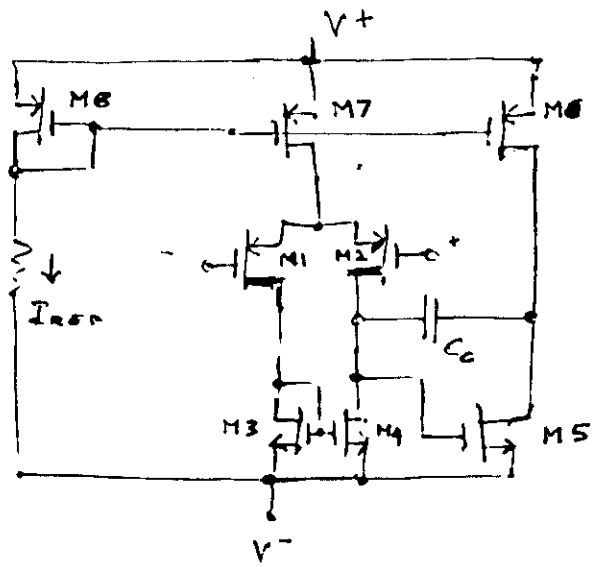
DESIGN FACTORS

- VOLTAGE GAIN
- DC OFFSET . PSRR
- Compensation, SLEW RATE
- DRIVE CAPABLITY
- NOISE
- SUPPLY CAPACITANCE
- POWER DISSIPATION

REALISTIC SPECIFICATIONS

GAIN	>5000 (74dB)
UNITY GAIN FREQ	4 MHz
Settling Time	~500nS . Unity, CL=5pF
SLEW RATE	5 - 20 V/μsec
CMRR	80dB
PSRR dc	90 dB
1kHz	60 dB
50kHz	40 dB
Systematic OFFSET	0.1 mV
RANDOM OFFSET	2 mV (3-σ)
INPUT COMMON MODE	+4 , -3V for ±5V supply
OUTPUT SWING	RAIL-TO-RAIL ±5V supply
EQUIVALENT INPUT NOISE	100nV/√Hz @ 1kHz
AREA	<50,000 sq. λ
POWER DISSIPATION	0.5 mW

BASIC CMOS AMPLIFIER



- **OPEN LOOP GAIN.**

First Stage Gain $A_{V1} = \dfrac{g_{m1}}{g_{ds2} + g_{ds4}}$ ~ 100

Second Stage $A_{V2} = \dfrac{g_{m5}}{g_{ds5} + g_{ds6}}$ ~ 100

$$A_V = A_{V1} A_{V2} = \frac{K'}{I_{REF}} \frac{\sqrt{\left(\frac{W}{L}\right)_1 \left(\frac{W}{L}\right)_3}}{\sqrt{\left(\frac{W}{L}\right)_5 \left(\frac{W}{L}\right)_6}} \quad (1)$$

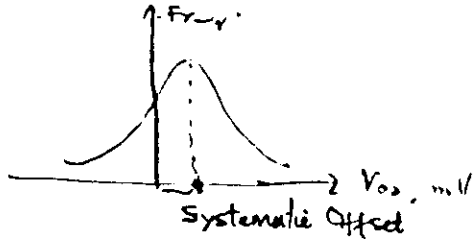
BIAS CONDITIONS ARE SUCH THAT

ALL TRANSISTOR OVERDRIVES $(V_{GS} - V_{TH})$

ARE AT THAT LEVEL OF SEVERAL 100's mV.

PAUL GRAY & ROBERT MEYER 'MOS OP AMP DESIGN'

DC BIASING, OFFSET, PSRR



Systematic OFFSET

FOR ZERO DIFFERENTIAL INPUT V_{OUT} SHOULD BE 0V.

Quiscent Voltage at Drain of M4 should

FORCE THE GATE OF M5 SUCH THAT

OUTPUT VOLTAGE = 0V.

THE (W/L) RATIOS OF M3, M4, M5

MUST BE SUCH THAT THE CURRENT DENSITIES

IN THESE DEVICES ARE EQUAL.

(2)

$$\frac{(W/L)_3}{(W/L)_5} = \frac{(W/L)_4}{(W/L)_5} = \frac{\frac{1}{2}(W/L)_1}{(W/L)_6} = \frac{\frac{1}{2}I_{REF}}{I_{REF}}$$

TO MAINTAIN THIS OVER PROCESS VARIATIONS

$L_3 = L_4 = L_5$, and RATIOS OBTAINED BY W.

USE OF IDENTICAL CHANNEL LENGTH IS NOT

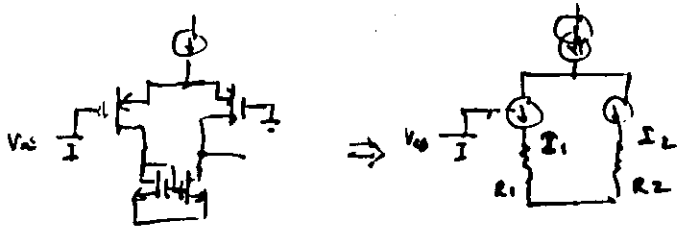
BEST FOR OPTIMISING FOR

- LOW NOISE
- AND FREQUENCY RESPONSE

- RANDOM OFFSET

DUE TO GEOMETRICAL MISMATCHING AND PROCESS DEPENDANT INACCURACIES

DOMINATED BY OFFSET OF THE INPUT STAGE



$\frac{\Delta I}{I} = \frac{-\Delta R}{R}$ $\quad \Delta R$ mismatch of Resistors, ΔI absolute difference of currents to keep $V_{out}=0$

$\Delta I = V_{os} g_m$

$\therefore V_{os} = \frac{\Delta R}{R} \cdot \frac{I}{g_m}$

Random OFFSET = (Mismatch) $\times \frac{I}{g_m}$

FOR SAME MISMATCH FACTOR

MOSFET $I/g_m \approx (V_{GS}-V_{TH}) = 500\,mV$

BIPOLAR $I/g_m = .026\,mV \approx 26\,mV$

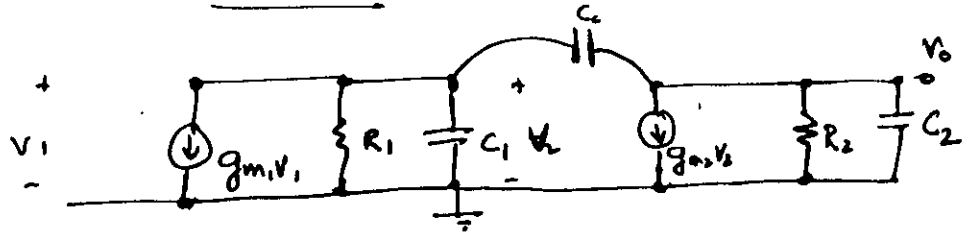
JFET $I/g_m \sim V_P \sim 1-2\,V$

TYPICAL RANDOM OFFSET ~ 5–20 mV

THE ABOVE DOES NOT CONSIDER V_{TH} MISMATCH.

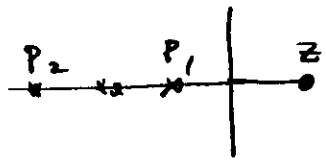
THIS MUST BE ELIMINATED THROUGH SPECIAL GEOMETRICAL LAYOUT TECHNIQUES. ~3mV

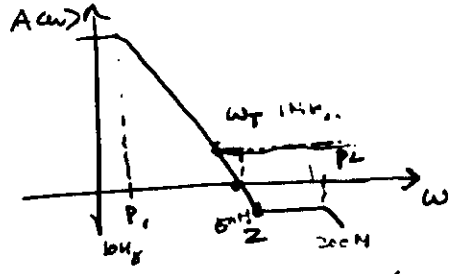
COMPENSATION



HIGH IMPEDANCE POINTS GIVE POLES

AT HIGH FREQUENCIES SIGNAL DIRECTLY PROPAGATES THROUGH C_c TO GIVE A ZERO.





$\omega_T = g_{m1}/C_c$

$P_1 \approx -\frac{1}{R_1 C_c (C_1 + g_{m2} R_2)}$

↑ MILLER EFFECT

Usually $C_c \simeq 40$ times C_1, $C_c \simeq C_2$.

$P_2 \approx \frac{-C_c g_{m2}}{C_1 C_2 + (C_1 + C_2) C_c} \approx \frac{-g_{m2}}{C_1 + C_2}$

$P_1/P_2 \approx 1/(g_{m2} R_1)^2$ - A LARGE SEPARATION!

ZERO AT $Z \simeq +g_{m2}/C_c$

$\left| \frac{P_2}{\omega_T} \right| = \frac{g_{m2}}{g_{m1}} \left[\frac{C_c}{C_1 + C_2} \right], \quad \left| \frac{Z}{\omega_T} \right| = \frac{g_{m2}}{g_{m1}}$

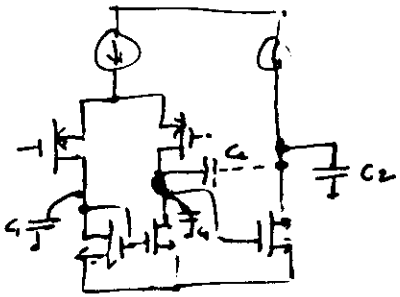
IN BIPOLAR $g_{m2} \gg g_{m1}$ SO THAT POLE SPLITTING WORKS

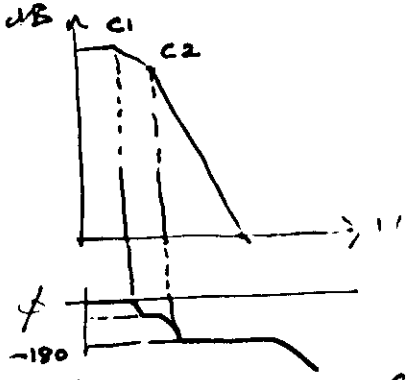
IN MOS $g_{m2} \sim g_{m1}$ SO THAT POLE SPLITTING NOT EASY

FREQUENCY RESPONSE ; COMPENSATION

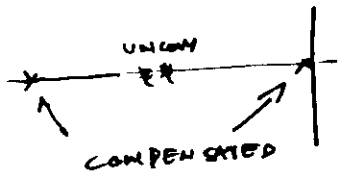
- SINGLE POLE SYSTEM IS ALWAYS STABLE
- A TWO STAGE GAIN SYSTEM WITH POLES IN THE SAME FREQUENCY RANGE. NEEDS COMPENSATION

→ SPLIT THE POLES APART TO APPROACH SINGLE (DOMINANT) POLE PERFORMANCE

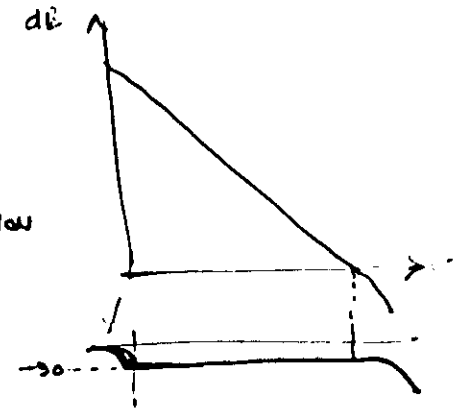




UNCOMPENSATED, $C_c = 0$



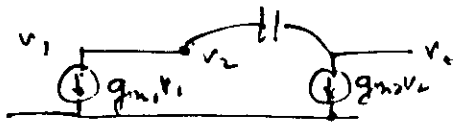
POLE-SPLITTING COMPENSATION



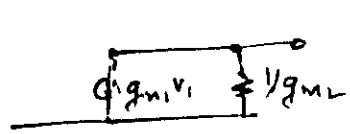
FOR MOS OPAMPS BECAUSE OF LOWER TRANS CONDUCTANCE VALUES

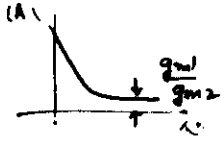
COMPENSATION (Cntd.)

Physical Effect. CONSIDER C_c, $C_2 = 0$



As $\omega \to \infty$





THUS THE CIRCUIT DISPLAYS A GAIN AT HIGH ω

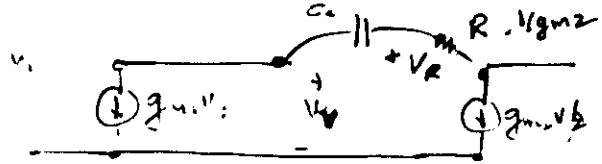
$$+ g_{m1}/g_{m2}$$

THE POLARITY OF THIS GAIN IS OPPOSITE TO THAT AT LOW FREQ - WHERE IT BEHAVES AS AN INTEGRATOR

THUS NEGATIVE FEEDBACK AROUND THE AMPLIFIER MAY TURN TO POSITIVE FEEDBACK.

SOLUTIONS

- NULLING RESISTOR



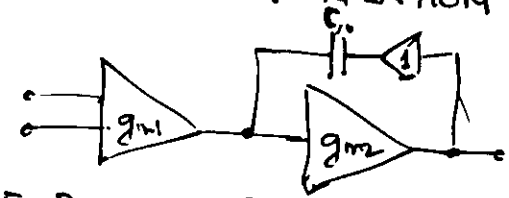
VOLTAGE ON V_R CANCELS V_2 and RHP $\to \infty$

IT CAN BE SHOWN THAT THE LOCATION OF

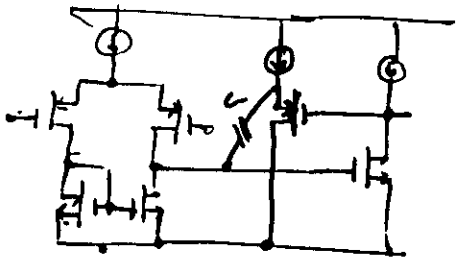
$$z = \frac{1}{C_c\left(\frac{1}{g_{m2}} - R_z\right)}$$

BY USING A MOSFET ACTIVE RESISTOR, THE EFFECT IS CANCELLED

- BUFFERED COMPENSATION



SOURCE FOLLOWER PREVENTS FEEDFORWARD



INCREASES BIAS CURRENT

- CAPACITATIVE LOAD CAPABLITY

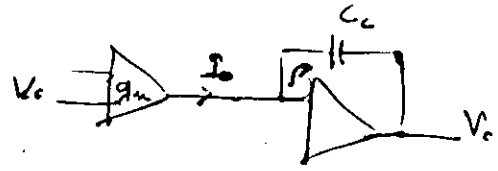
$$\left|\frac{P_2}{\omega_1}\right| \simeq \frac{g_{m2}}{g_{m1}}\left[\frac{C_c}{C_2}\right]$$

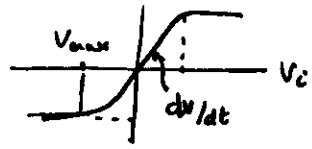
FOR STABILITY $\omega_2/\omega_1 \geq 2-4$

HENCE LOAD CAPACITANCE SHOULD NOT BE HIGHER THAN COMPENSATION CAPACITANCE

TRY TO MAKE $g_{m2} >> g_{m1}$ (?)

- SLEW RATE





$$\text{SLEW} = \frac{dV}{dt} = \frac{I_o}{C_c}$$

$$\omega_1 = g_m/C_c$$

$$\text{SLEW RATE} = \frac{I_{D1}}{g_m} \cdot \omega_1 \qquad \frac{I_o}{g_m} = V_{max}$$

$$= V_{max} \cdot \omega_1$$

FOR CMOS

$$\frac{I_o}{g_m} = \frac{\frac{\mu_n C_o \frac{W}{L}}{2}(V_{GS}-V_T)^2}{\mu_n C_o \frac{W}{L}(V_{GS}-V_T)} = \frac{(V_{GS}-V_{TH})}{2}$$

100 mV – 500 mV

FOR $\omega_1 = 2\pi(5\,MHz)$ SR ~ 12.5 V/μs

FOR BIPOLAR $V_{max} \simeq \frac{2I_{C1}}{g_{m1/2}} = 4V_T \simeq 104\,mV$

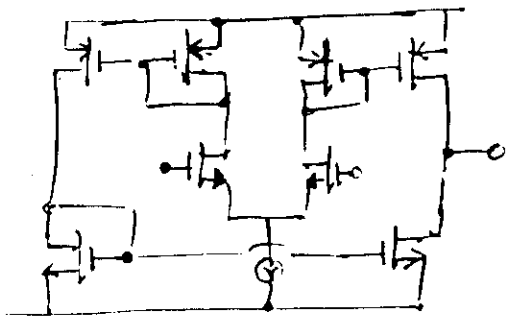
FOR $\omega_1 \simeq 2\pi(5MHz)$ SR ~ 3 V/μs

SLEW RATE FOR MOS BETTER THAN BIPOLAR

FACTORS LIMITING SLEW-R.

- UNITY GAIN BANDWIDTH ←
- INPUT STAGE DYNAMIC RANGE ←

OTA.



SIMPLE OTA

- SINGLE STAGE.
  COMPENSATED WITH CAPACITOR LOAD (if necessary)
- LARGE DC GAIN FOR CASCODES ~ $(g_m r_{ds})^2$
- LOW POWER CONSUMPTION
- BETTER PSRR

DISADVANTAGES

- LOW OUTPUT SWING
- CAN NOT DRIVE RESISTIVE LOADS
- LOW CURRENT → LOW SLEW RATE.

WHEN OPERATED IN SUBTHRESHOLD USED AS MICROPOWER OP-AMPS

- $I_b < 1\mu A$
- Required in BATTERY OPERATED SYSTEMS [illegible] HEARING AIDS [illegible]

TYPICAL PERFORMANCES

DC GAIN	95 – 100 dB
f_T	130 kHz
S.R.	0.1 V/μSec
I_c	0.5 μA
I_{tot}	2.5 μA

THE OTA CAN BE USED AS A STANDARD BUILDING BLOCK IN LARGE NUMBERS.

Like in implementation of Neural Nets

Analog VLSI – Carver MEAD.

↑

Analog Filter Implementation

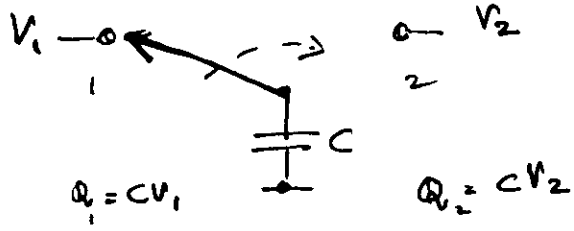
HISTORICAL PROGRESS IN MINIATURISATION

	Technique	Components
1920s	Passive R, L, C	R, C, L
end '60s	Active RC Filter Discrete boards	R, C, OPAMP
Early '70s	Hybrid Active Filters	R, C, OpAmp
end '70s	Switched Capacitor Integrated Filters	C, OpAmp Switches
'80s	Time Continuous Integrated Filters	C, Trans, OTAMPS.
'90s	?	?

RC Time Constants must be Accurate 0.1%

Switched Capacitor Circuits

Replacement of a Resistor by Capacitor



$$\Delta Q = CV_1 - CV_2 = C(V_1 - V_2)$$

If the Switching is done at a frequency

$$f = \frac{1}{\Delta t}$$

Average Current (Charge Transfer Rate)

$$I = \frac{\Delta Q}{\Delta t} = \frac{C(V_1 - V_2)}{\Delta t} = \frac{(V_1 - V_2)}{(1/fc)}$$

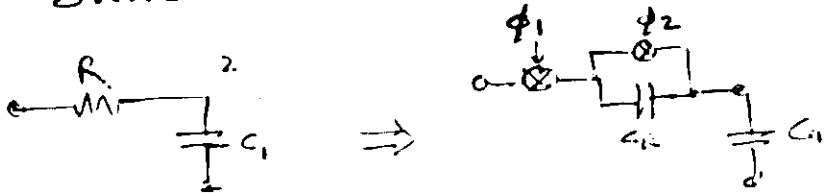
For large f compared to Changes in V_1, V_2

$$\boxed{I = (fc) \cdot (V_1 - V_2)}$$

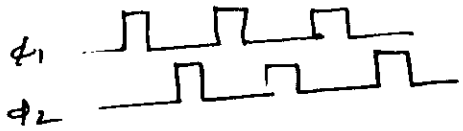
Hence an Effective Conductance of (fc) is seen between points 1 & 2

TO REALISE RC time Constants

REPLACING R WITH AN EFFECTIVE SWITCHED CAPACITOR C_R



ϕ_1 & ϕ_2 NON OVERLAPPING CLOCKS



THE EQUIVALENT SC CIRCUIT GIVES

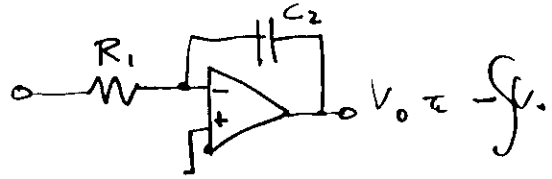
$$RC_1 = \frac{1}{fC_R} \cdot C_1 = \frac{1}{f}\cdot\frac{C_1}{C_R}$$

f - frequency of the clock can be made as accurate as necessary

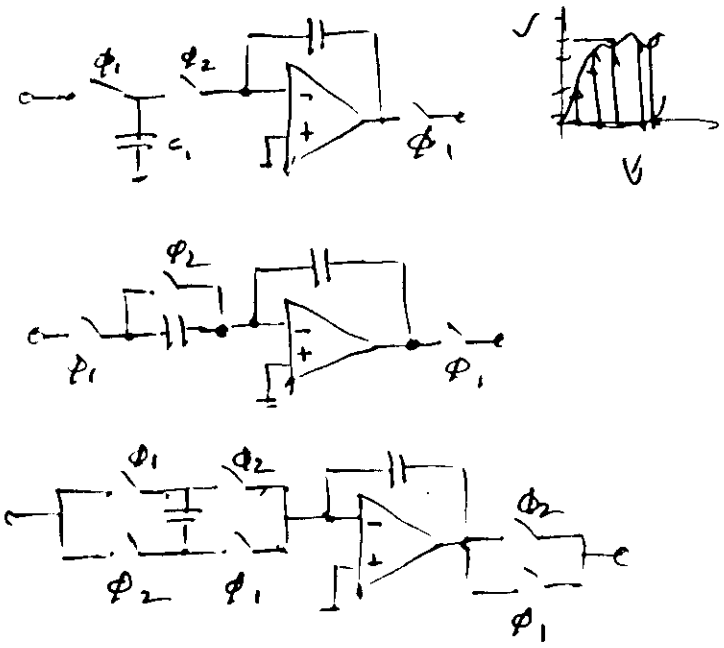
C_1/C_R - CAPACITOR AREA MATCHING ratio

HENCE ACCURATE TIME CONSTANTS CAN BE IMPLEMENTED ON MOS TECHNOLOGY [illegible] CAPACITORS.

SC EQUIVALENTS



REPLACING RESISTOR WITH EQUIVALENT:



- ALL HIGH ORDER FILTER BLOCKS CAN BE REALISED AS SC EQUIVALENTS
- NON-FILTERING APPLICATIONS TOO ARE POSSIBLE

CONCLUSIONS

CMOS TECHNOLOGY

- EXCEPTIONAL FOR REALISING EXTREMELY LOW POWER CIRCUITS
- UNIQUE FOR REALISING INTEGRATED ACTIVE FILTERS (100kHz)
- HIGHLY COMPETITIVE FOR INTEGRATING MIXED ANALOG/DIGITAL PROCESSING FUNCTIONS
- REQUIRES SPECIAL CUSTOM DESIGN TECHNIQUES TO COMPETE WITH BIPOLAR LINEAR CIRCUITS