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INTERNATIONAL CENTRE FOR THEORETICAL PHYSICS
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UNITED NATIONS INDUSTRIAL DEVELOPMENT ORGANIZATION

INTERNATIONAL CENTRE FOR SCIENCE AND HIGH TECHNOLOGY
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SECOND COURSE ON BASIC VLSI DESIGN TECHNIQUES
18 February - 15 March 1991

Additional material to lectures by

Ignatius S.A. BEZZAM
Centre for Development of Advance Computing
Pune University Campus
Pune 411 007
India

ADDITIONAL MATERIAL

TO LECTURE 5

Tomatis S.A.B.

OP AMP DESIGN

References

1. P.R.Gray, R.G.Meyer, MOS Operational Amplifier Design-A tutorial Overview, IEEE JSSC, Dec. 1982, pp 969-982.

2. D.A.Hodges, P.R.Gray and R.W. Broderson "Potential of MOS Technologies for Analog Integrated Circuits", IEEE,JSSC, June 1978, pp 285-293.

3. B.K.Ahuja, "An improved frequency compensating technique for CMOS operational amplifiers,", IEEE JSSC, Dec. 1983 pp 629-633.

4. D.B.Ribner, M.A. Copeland, "Desing techniques for cascoded CMOS opamp with improved PSRR and Common-mode input range", IEEE JSSC, Dec. 84, pp 919-925.

5. K.E.Brehmer, J.B.Wieser,"Large swing CMOS Power amplifier", IEEE JSSC, Dec.'83, pp 624-628.

6. "Design Note of a CMOS Push Pull Power amplifier", LSI Design Department.

7. Abe et al, " A single chip CMOS A/D and D/A converter for PCM audio use", IEEE Trans. on Consumer Electronics,Nov. 1984, pp 323-325.

OTA DESIGN

REFRENCES

1. "Active filter design using OTA: A Turotinal"by Dondall L.Geiger and Edger S.S. IEEE circuits devices magazine March. 1985.

2. The design of high performance Analog circuits digital CMOS chips. Ems A.Vettoz, J.S.S.C. June 1985.

3. Technological design considerations for monolithic MOS SC filtering systems. David I Austot, William C. Blade is IEEE proceedings August 1983. pp 977.

4. F krummeracher "High voltage Gain CMOS OTA for micro power SC filters. "Electron Lett. Vol. 17, pp 160-162, Feb. 1981.

5. M.R.Degrauwe F willy M. Sansen. " The current efficiency of MOS transconductance amplifiers. " J.S.S.C., June 1984. (Simulations could not be reported)

6. T.C.Choi,R.T.Kaweshro et al "Hifh frequency SC filters for communication application." J.S.S.C. Dec. 1983 ref to pp 659-661.

7. M. Degorauwe, E.Vittoz, I. Verbauwhede. " A micropower CMOS instrumentation amplifier. " J.S.S.C. June 1985.

8. Peter M.Vani petegh, I. Verbauwhede, 4 M.M.C.Sansen. "Micropower high performance SC building block for integrated low level signal processing. " J.S.S.C. August 1985.

9. Ignatius SAB. " OTA for special comparator in instrumentation". DVM. " April 1984 ibid 1984.

10. Current mirror documentation ibed 1984.

11. Miran Milkovic " Current Gain high frequency CMOS operational aplifiers" J.S.S.C. August 1985.

12. Eric A Vittoz. "MOS transistors operated in bipolar mode and then appl. for CMOS technology J.S.S.C. June 1983.

13. B.J.Mosticka, Dynamic CMOS amplifiers J.S.S.C.vol. SC-15 pp 887-894 Oct. 1980.

14. M.C.Degravwe et al.
Adaptive Biasing of CMOS amplifiers" J.S.S.C Sc 17. pp 572-578, June 1982.

VOLTAGE REFERENCES

(3) If desired, for acheiving higher accuracy modelling of breakdown behaviour, more accurate zener models (g) may be implemented on the circuit simulator.

REFERENCES

1. S.M.Sze."Physics of Semiconductor Devices", Wiley Estern Ltd. p.133.

2. P.Gray,and R.G.Meyer, "Analysis and Design of Analog Integrated Circuits" John Wiley and Sons, pp.248-261.

3. R.J.Widlar, "New Developments in IC Voltage regulators", IEEE Journal of Solid State Circuits, Vol.SC-6, No. 1. February 1971 pp.2-7.

4. K.E.Kuijik,"A precision reference voltage source", IEEE Journal of Solid State Circuits, vol SC-8, No.3 June 1973, pp. 222-226.

5. R.Ye and Y.Tsividis, "Band gap voltage reference source in CMOS Technology, "Electronics Letters, vol. 18, No.1 7th Jan. 1982, pp. 24-25.

6. R.A. Blauschild, P.A.Tucci, R.S.Muller and R.G.Meyer, "A new NMOS Temperature Stable voltage Reference, "IEEE Journal of Solid State Circuits, vol. SC-13, No.6, Dec.1978 pp.767.774.

7. S.A.B. Ignatius, "Specifications for zener reference".

8. S.Lui. R.G.Meyer and Normau Kwan, "An ion-implanted Subsurface monolithic zener diode". IEEE Journal of Solid State Circuits, vol. SC-14, No.4, Aug. 1979 pp.782-784.

9. A.K.Laha and D.W. Smart, "A zener diode model with application to SPICE-2", IEEE Journal of Solid State Circuits, Vol. SC-16, No.1, Feb. 1981, pp. 21-22.

& the gap (etching width) between adjacent capacitor p.a.
is more than 6 um, (A= 12um).

Measurements

It is intended that Measurements will be done by HP 4275A LCR meter. The most attractive feature of the instrument, which makes it suitable for low-capacitance measurements is that it can store a reference value (e.g. of a parastic capacitance) & can later, subtract this value from the value being measured for the actual intended capacitance. Its like the zero setting of a conventional multimeter. Further it can measure the required minimum values of capacitances to an accuracy which is better than 8-bit, which is our requirement.

REFERENCES

1. Mc Creary, J.L. and P.R. Gray, "All-MOS charge Redistribution Analog-to-Digital conversion Techniques-Part I, "IEEE J.SSC. Dec. 75.

2. Suarez, R.E.,P.R. Gray and D.A.Hodges, "All-MOS Charge Redistribution Analog-to-Digital Conversion Techniques" Part II", IEEE J.SSC. Dec. 1975.

3. Albarran, J.F.and D.A Hodges ," A Charge-Transfer Multiplying Digital-to-Analog Convertor", IEEE J.SSC, Dec. 1976.

4. New Comb, R,"Considerations in MOS Ratioed capacitor Layout". VLSI Design, Third Quarter 1981.

5. Smarandoiu, G,Hodges, Gray & Landsburg,"CMOS Pulse-Code-Modulation Voice Codec, "IEEE J.SSC, pp. 504-510, Aug. 1978.

6. J.L.Mc Creary, "Matching Properties, and Voltage and Temperature Dependence of MOS capacitors", IEEE J,SSC, Vol. Sc-16, No.6, pp. 608-616.

7. Shyu, J.B.,G.C.Temes & K.Yao "Random Errors in MOS Capacitors, "IEEE, J.SSC, Vol. SC-17, No.6, pp 1070-1076 Dec. 82.

8. Shyu, J.B., G.C.Temes and Francois Krummenacher & "Random Error Effects in Matched MOS capacitors and current Sources", IEEE, J.SSC, Vol. SC-19. No. 6, pp. 948-955.

9. Shyu, J.B., "The obtainable Accuracy of analog MOS Integrated circuit elements, "Ph.D. Dissertation, Univ. California, Los Angeles, 1984.

10. Yee., Y.S.L.M.Terman & L.G.Heller, "A Two-Stage" Weighted Capacitor Network for D/A-A/D conversion", IEEE J.SSC, vol. SC-14, No.4, pp. 778-781, Aug. 79.

11. Mc Creary, J.L. & P.A.Sealer, "Precision capacitor Ratio Measurement Technique for Integrated circuit capacitor Arrays, "IEEE, Trans. on Instrumentation and Measurement, vol. IM-28, No.1, March 1979.

12. Maddox.

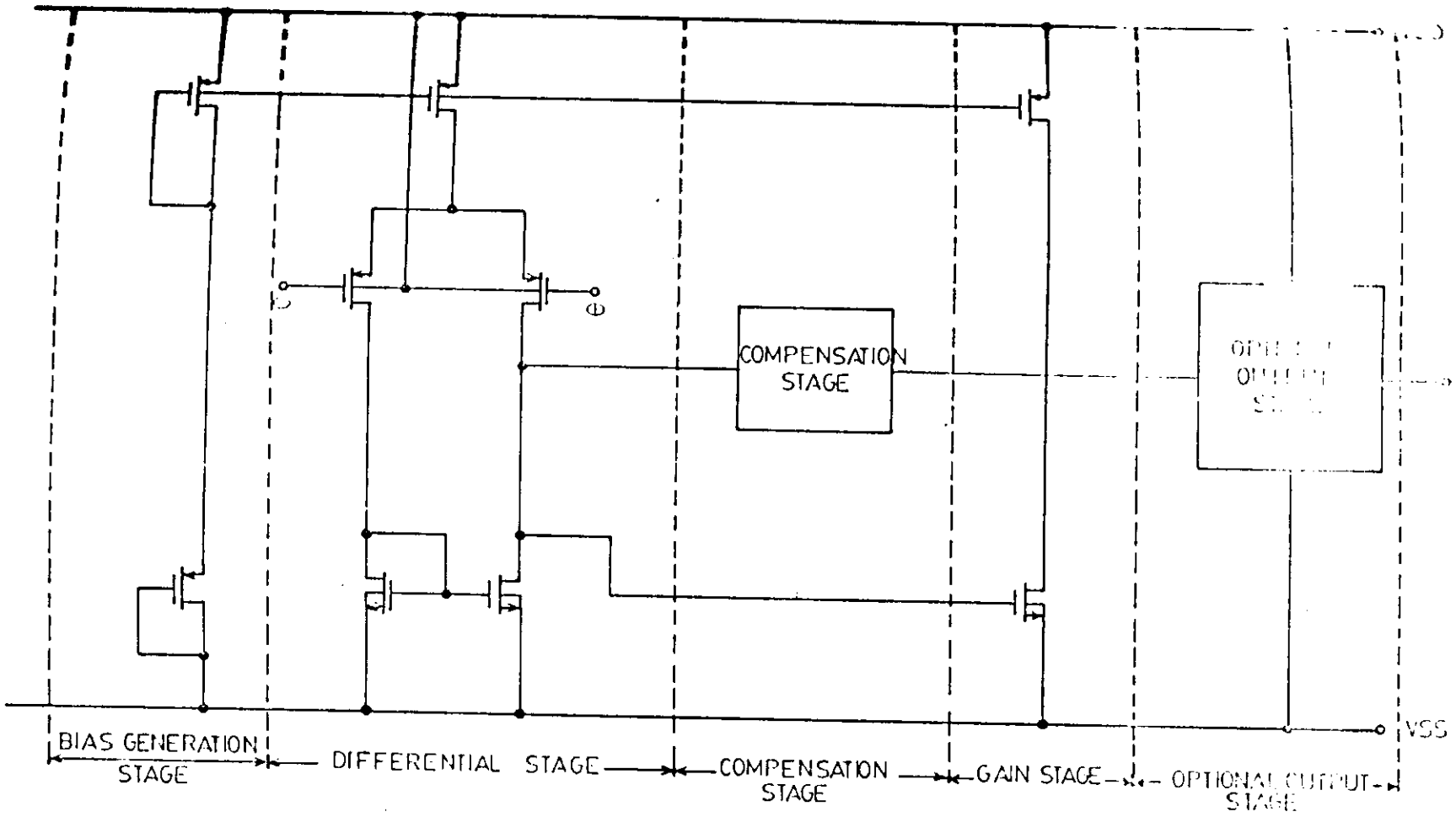
13. Stone, D.C., J.E. Schoeder, R.H.Kaplan and A.R.Smith," Analog CMOS Building Blocks for custom and Semi-custom Applications", IEEE, J.SSC, Vol. SC-19, No.1, February, 1984.

14. W.J.Helmes, "Fabrication of NMOS capacitors with a Low-Voltage Coefficient at a Silicon Foundry "IEEE, Electron Device letters, Vol. EDL-6, No.1, Jan. 1985.

15. Singh, S.P.,A. Prabhakar, A.B.Bhattacharyya, "Modified C-2C Ladder Voltage Divider for Application in PCM A/D Convertors", Electronics Letters, 15t September, 1983, Vol. 19, No.19, pp. 788-789.

16. Singh, S.P., A.Prabhakar, A.B.Bhattacharyya, "C-2C Ladder voltage dividers for application in all MOS A/D convertors, "Electron. Lett.,1982, 18, pp. 537-538.

17. Allstot D.J. & W.C.Black Jr.,"Technological Design Considerations for Monolithic MOS Switched-capacitor Filtering Systems, "Proc. of the IEEE, Vol. 71, No.8 Aug. 83.



BASIC OPAMP CONFIGURATION (P-TYPE)

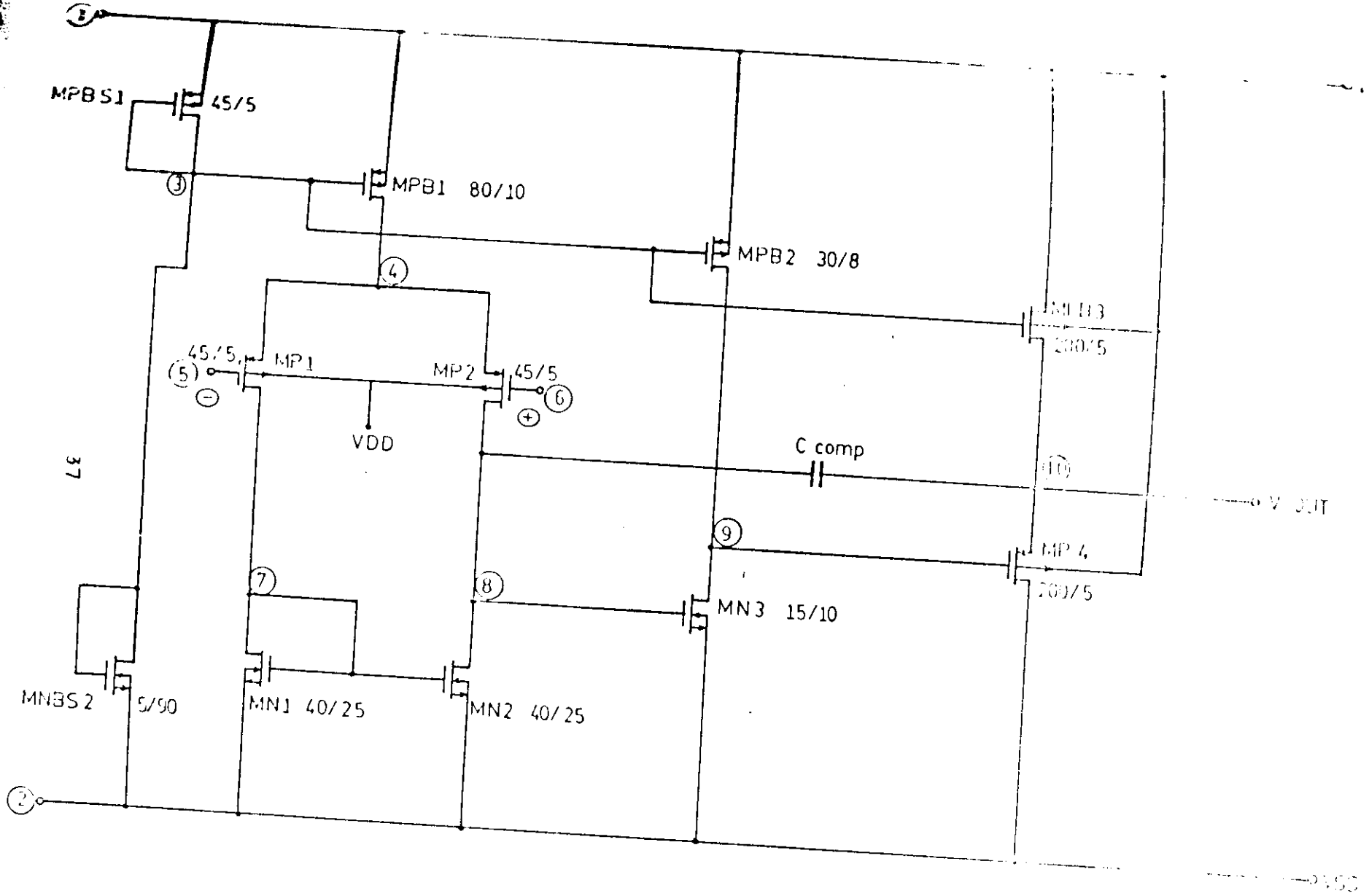
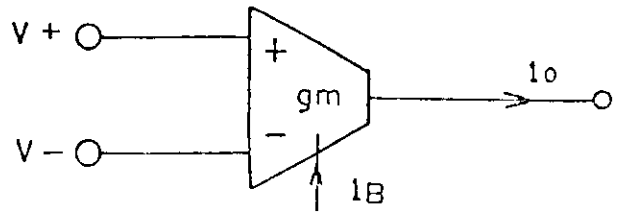
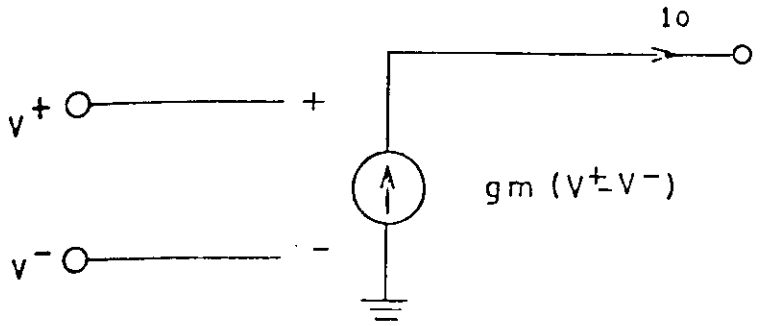


FIG. (d): COMPLETE OP AMP SCHEMATIC



FIG(1)a : OTA SUMBOL



FIG(1)b: EQUIVALENT CIRCUIT OF IDEAL OTA

FIG.(1): OTA SYMBOL AND MODEL

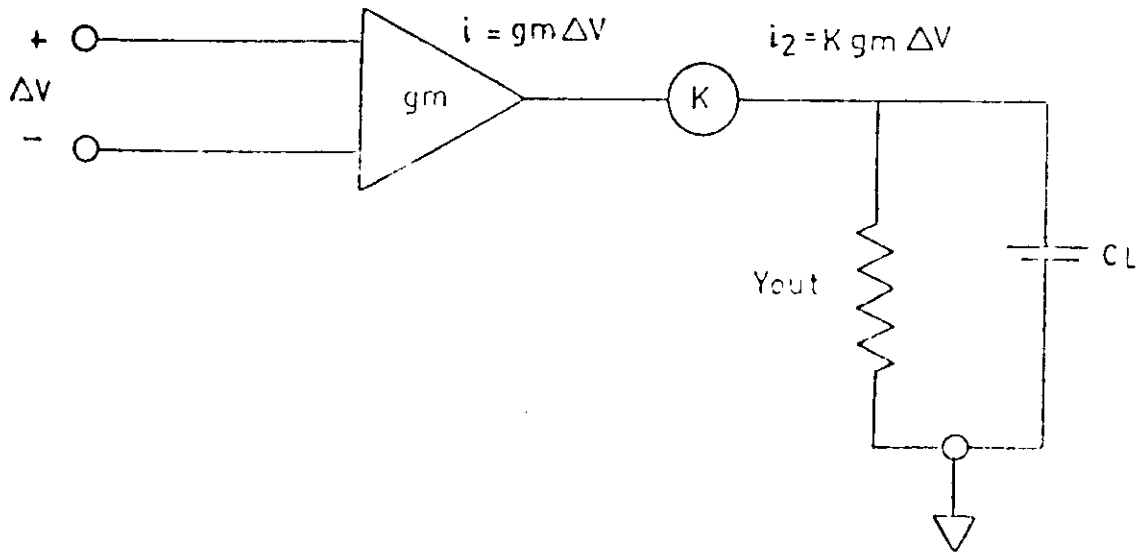


FIG.(2) a : OTA EQUIVALENT CIRCUIT

OPERATIONAL TRANSCONDUCTANCE AMPLIFIER

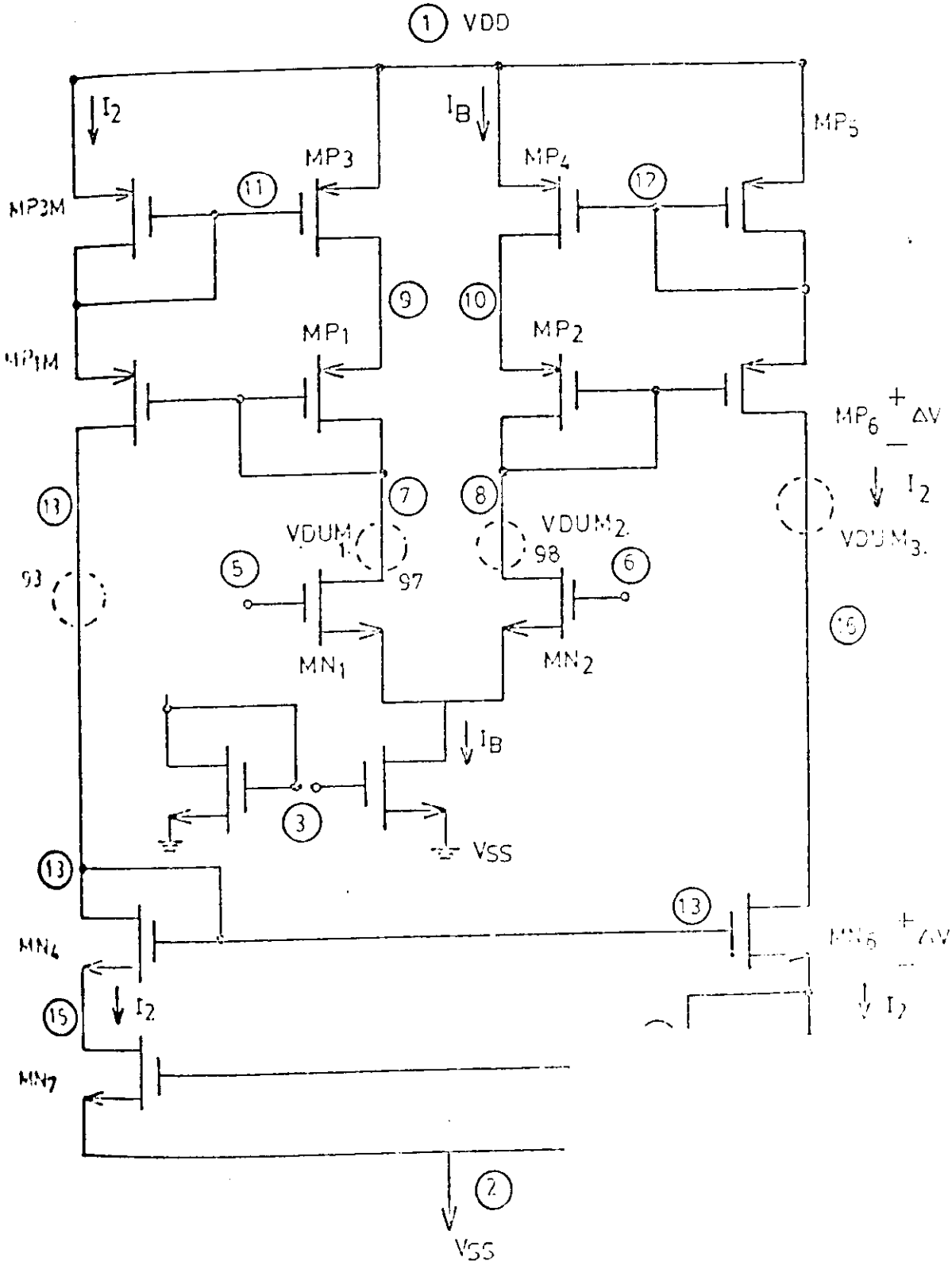


FIG. 2(b) : COMPARATOR CIRCUIT

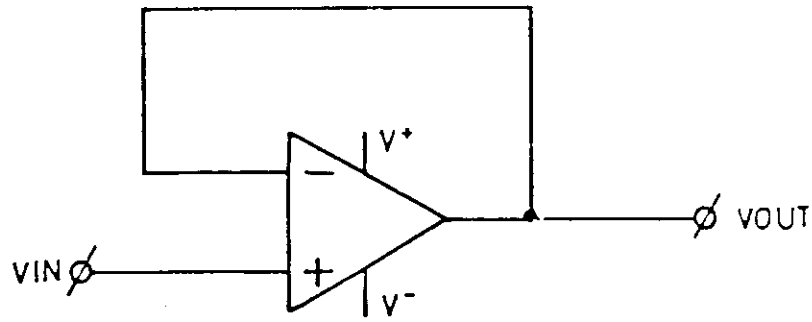


FIG. 1(a): SYMBOL OF UNITY GAIN BUFFER

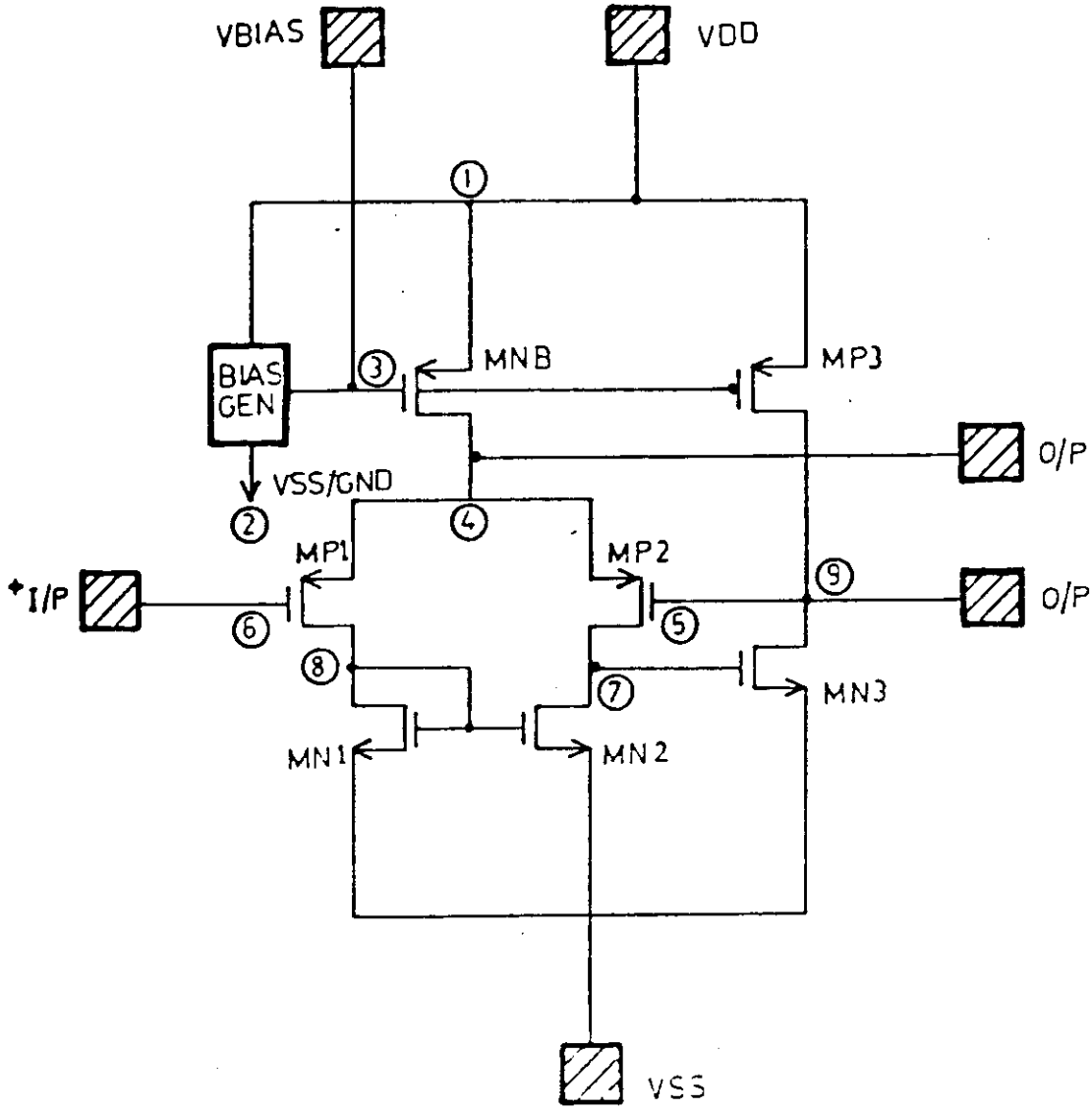


FIG. 1.(b) : SCHEMATIC OF UNITY GAIN BUFFER

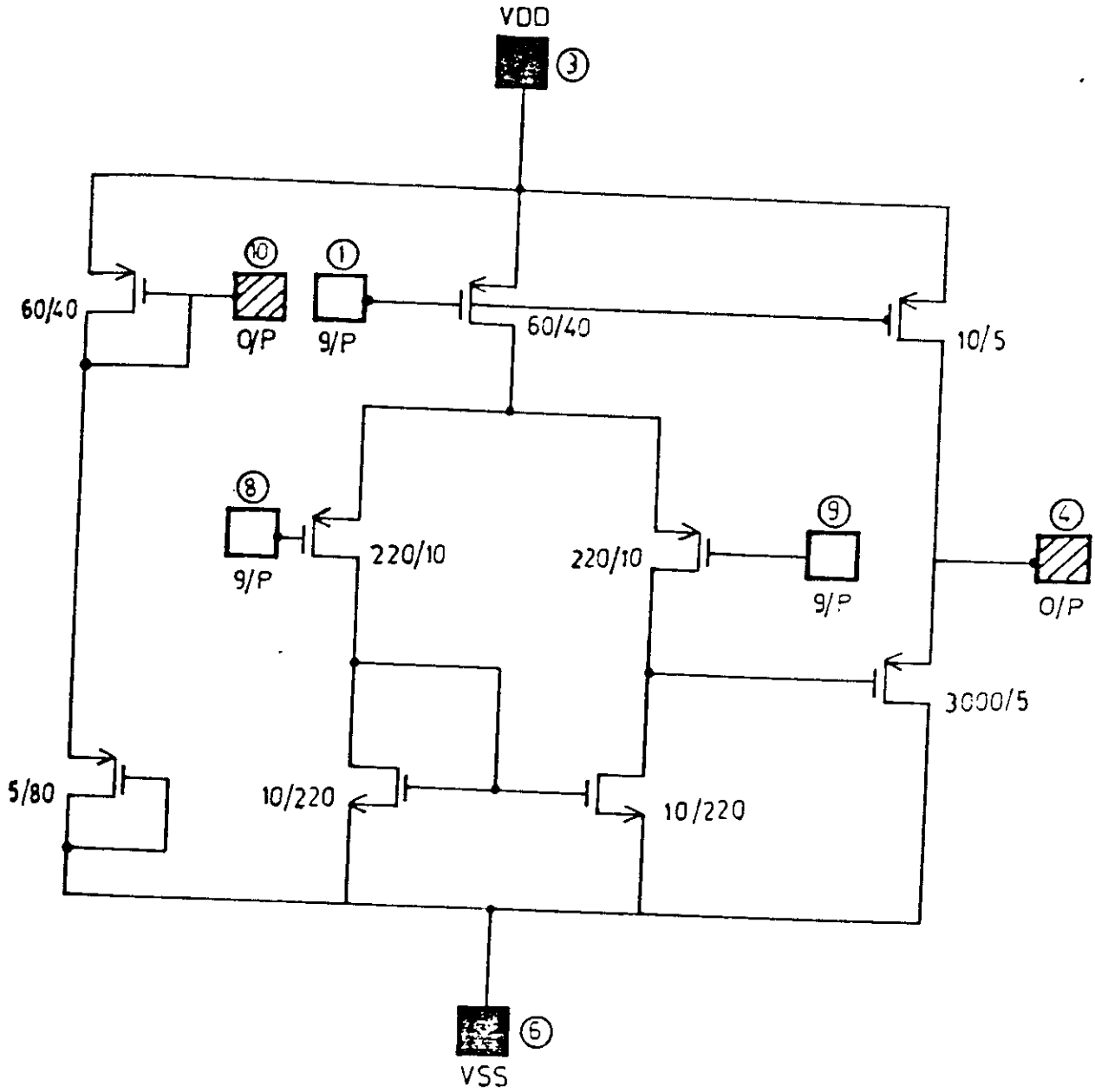


FIG. 2.:- UNITY GAIN BUFFER WITH DEVICE SIZES