INTERNATIONAL ATOMIC ENERGY AGENCY
UNITED NATIONS EDUCATIONAL, SCIENTIFIC AND CULTURAL ORGANIZATION
INTERNATIONAL CENTRE FOR THEORETICAL PHYSICS
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UNITED NATIONS INDUSTRIAL DEVELOPMENT ORGANIZATION

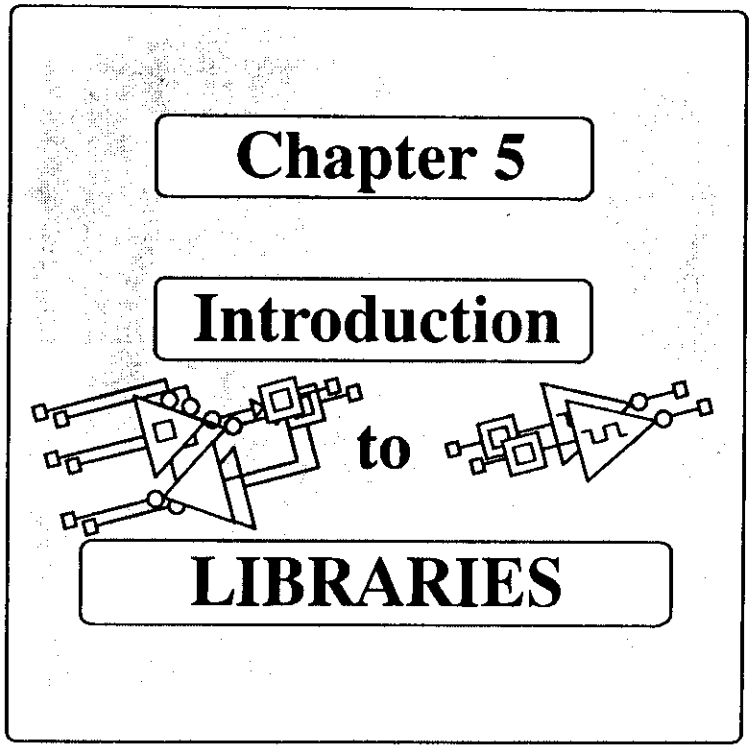
INTERNATIONAL CENTRE FOR SCIENCE AND HIGH TECHNOLOGY

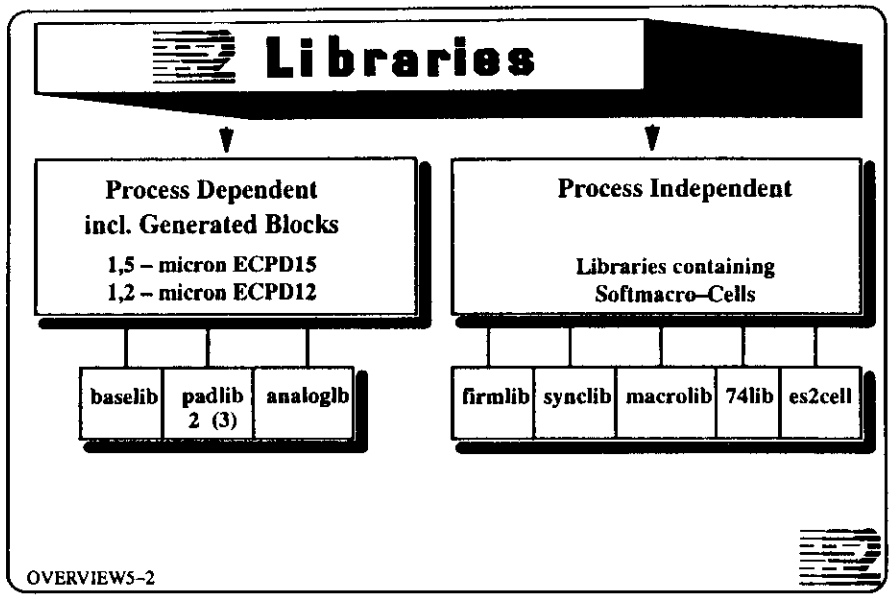
SMR/542 - 5

ICTP-INFN
SECOND COURSE ON BASIC VLSI DESIGN TECHNIQUES
18 February - 15 March 1991

INTRODUCTION TO LIBRARIES

Franck BUONANNO
European Silicon Structures (ES2)
72/78 Grand Rue
Sevres 92310
France





Overview of available ES2–LIBRARIES

Notes: _____

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BASELIB 5–3 **BASELIBRARY**

Part	Type	Cell Name	Description
Primitives	AND	and2	2–Input
		and3	3–Input
		and4	4–Input
	NOR	nor2	2–Input
		nor3	3–Input
		eqv	Exclusive
	NAND	nand2	2–Input
		nand3	3–input
		nand4	4–input
	OR	or2	2–Input
		or3	3–Input
		wired or	Wired
		xor	Exclusive
	INVERTER	not	
	WIRE	wire	connect buses
	BOOLEAN	andnor12	$\overline{i1 + (i2*i3)}$
		andnor13	$\overline{i1 + (i2*i3*i4)}$
		andnor22	$\overline{(i1*i2) + (i3*i4)}$
		andnor23	$\overline{(i1*i2) + (i3*i4*i5)}$
		ornand12	$\overline{i1*(i2 + i3)}$
		ornand13	$\overline{i1*(i2 + i3 + i4)}$
		ornand22	$\overline{(i1 + i2)*(i3 + i4)}$
		ornand23	$\overline{(i1 + i2)*(i3 + i4 + i5)}$
		ornand33	$\overline{(i1 + i2 + i3)*(i3 + i4 + i5)}$
Flip–flops	clocked	bdff	
		bdffc	with Clear
		bdffn	with Set, Clear
		bdffs	with Set
	clocked transmission	(bdffct)	with Clear
		(bdffsct)	with Set, Clear
		(bdffst)	with Set
	clocked scan	bsdff	
		(bsdffn)	with Set
	transparent latches	latch	
		latchc	with Clear
		latchn	with Set, Clear
		latchs	with Set
Inverting Buffers		buffer2	(2 x drive)
		:	:
		buffer10	(10 x drive)
	Tristate	tribuf1/not	(1 x drive)
		:	:
		tribuf6	(6 x drive)
Adder		sumcar	Full
		sum	Boolean
		carry	Boolean

MODEL Part Headers for Baselib Parts

and2:	and [a(1:2)] –> b
andnor12:	andnor (1,2) [a(1:m),b(1:n)] –> out
buffer2:	buffer2 [a] –> b
ceqv:	ceqv [a,abar,b,bbar] –> out
cxor:	cxor [a,abar,b,bbar] –> out
eqv:	eqv [a,b] –> out
nand2:	nand [a(1:2)] –> b
nor2:	nor [a(1:2)] –> b
not:	not [a] –> b
or2:	or [a(1:2)] –> b
ornand12:	ornand (1,2) [a(1:m),b(1:n)] –> out
sumcar:	sumcar [cin,a,b] –> sumbar,coutbar
sum:	sum [coutbar,a,b,cin] –> sumbar
carry:	carry [cin,a,b] –> coutbar
tribuf2:	tribuf2 [c,cbar,a] –> b
trinot:	trinot [c,cbar,a] –> b
wire:	wire [a(1:*)] –> b(1:*)
wired or:	wired or [a(1:*)] –> out
xor:	xor [a,b] –> out

BASELIB 5–4

MODEL part Headers

The cell name as referenced by draft is on the left and the corresponding model code calls are on the right. Model part calls are generated automatically for circuits calls that are designed in schematic form. Parts designed in "text form" directly in model code must use the corresponding functions as stated in the right column.

Notes: _____

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SOLO 1400 V3.02 LIBS – BASELIB

MODEL Part Headers for Baselib Parts

bdff:	bdff [clk, din] –> q, qbar
bdffc:	bdffc [clk, din, clearbar] –> q, qbar
bdffct:	bdffct [clkbar, d, clearbar] –> q, qbar
bdffn:	bdffn [clk, din, clearbar, setbar] –> q, qbar
bdffs:	bdffs [clk, din, setbar] –> q, qbar
bdffsct:	bdffsct [clkbar, d, clearbar, setbar] –> q, qbar
bdffst:	bdffst [clkbar, d, setbar] –> q, qbar
bsdff:	bsdff [clk, a, b, s] –> q, qbar
bsdffn:	bsdffn [setbar, data, serial data, scanbar, clock] –> q, qbar
latch:	latch [load, din] –> q, qbar
latchc:	latchc [load, din, clearbar] –> q, qbar
latchn:	latchn [load, din, clearbar, setbar] –> q, qbar
latchs:	latchs [load, din, setbar] –> q, qbar

BASELIB 5–5

MODEL part Headers

Notes: _____

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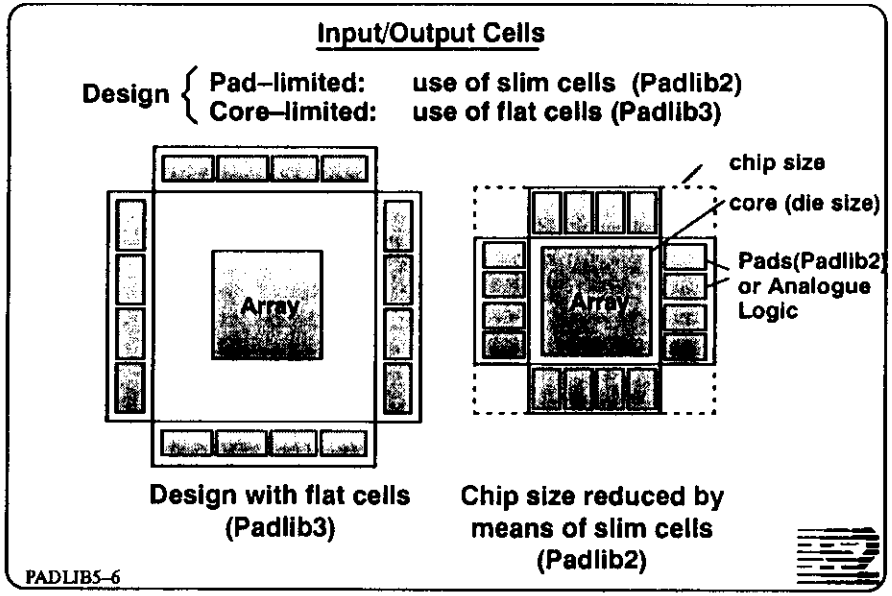
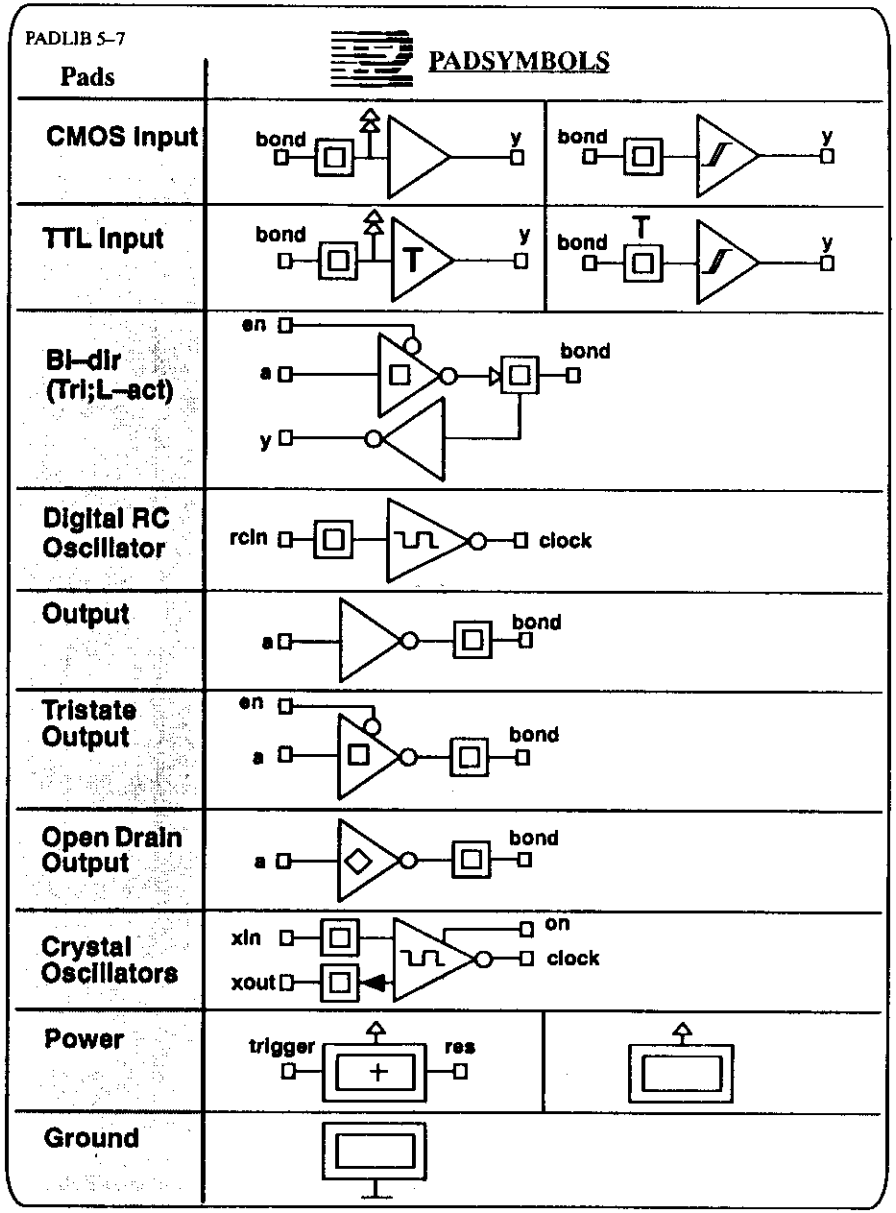


Input / Output Cells

Using slim cells (Padlib2) for padlimited designs saves unused silicon. Padlib2 pads are all 581 um tall and the minimum width is 150 um. Flat cells (Padlib3) are all 319 um tall and minimum width is 623 um.

Notes:



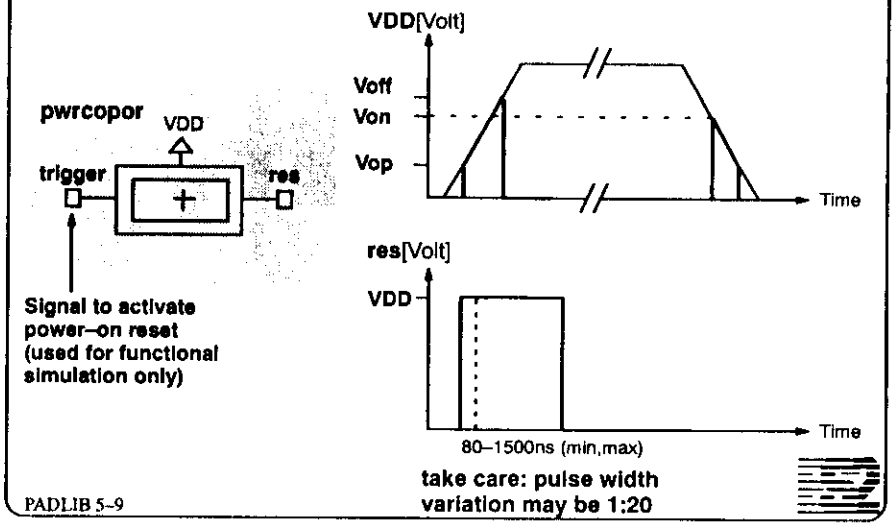
PADLIB 5–8

PADLIB

Pads	Padlib2 (slimpads)		Padlib3 (flatpads) only 2/1.5um	
	Name	Description	Name	Description
CMOS Input	ips8b ips8c ips8d ips1e ips4e	125 kΩ pull–up (typical) 9 kΩ pull–up (typical) Schmitt Trigger(invert) Schmitt Trigger (high drive/non–invert)	ipf8b ipf8c ipf8d	125 kΩ pull–up (typical) 9 kΩ pull–up (typical)
TTL Input	ips8g ips8h ips8i ips1j ips4j	125 kΩ pull–up 9 kΩ pull–up Schmitt Trigger(invert) Schmitt Trigger (high drive/non–invert)	ipf8g ipf8h ipf8i	125 kΩ pull–up 9 kΩ pull–up
Bi–dir (Tri;L–act)	ios1k ios2k ios4k ios6k	CMOS input, 4mA CMOS input, 8mA CMOS input, 16mA CMOS input, 24mA	iof1k iof2k/3k	CMOS input, 4mA CMOS input, 8mA
	ios1p ios2p ios4p ios6p	TTL input, 4mA TTL input, 8mA TTL input, 16mA TTL input, 24mA	iof1p iof2p/3p	TTL input, 4mA TTL input, 8mA
Digital RC Oscillator	drco2	10 Hz< f < 700 kHz		
Output	ops1u ops2u ops4u ops6u	4mA 8mA 16mA 24mA	opf1u opf2u/4u	4mA 8mA
Tristate Output	ops1w ops2w ops4w ops6w	4mA 8mA 16mA 24mA	opf1w opf2w/3w	4mA 8mA
Open Drain Output	ops1z ops2z ops4z ops6z	4mA 8mA 16mA 24mA	opf1z opf2z/4z	4mA 8mA
Crystal Oscillators	osc1 osc2 osc3	5 MHz –>30 MHz 100kHz –> 5 MHz Low–power, 32 kHz		
Power	pwrco pwrcopor pwrpy	Core Core,Power–on Reset Periphery	vccfr vccf	Primary (Reference Pad) Secondary
Ground	gndco gndpy	Core Periphery	vssf	

Cell currents: Sink / Source (Military worst case)

Power–on Reset



PADLIB 5–9

Power–on Reset

The pwrcopor can replace one pwrco cell, where power–on–reset is needed.

Operating Voltage V_{op} (1V typ) gives the minimum supply voltage when res is active.

When VDD exceeds V_{off} (2.86V typ), res will be inactive.

When VDD drops below V_{on} (2.65V typ), res will be active.

To make the por cells testable always follow the corresponding application note !

Notes: _____

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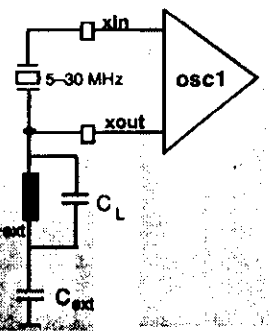
External Components of Crystal Oscillators

osc1 can be used with fundamental and overtone crystals in the range 5–30 MHz;

If overtone crystals are used, the fundamental frequency must be suppressed with a corresponding LC network. Example :30 MHz crystal 3rd harmonic, Lext = 9uH, f_{fund} = 10MHz

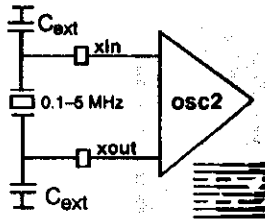
$w_0 = 2 \cdot 3{,}14 \cdot f_0 = \frac{1}{\sqrt{L_{ext} \cdot C_L}}$ => C_L = 3,1 pF;

$w_{fund} = 2 \cdot 3{,}14 \cdot f_{fund} = \frac{1}{\sqrt{L_{ext} \cdot C_{ext}}}$ => C_{ext} = 28,1 pF;



osc2 is designed for use with fundamental crystals in the range 0.1–5 MHz;

	Frequency range:	
Cext=0	5 MHz	(typ)
Cext=20pF	2MHz	(typ)
Cext=50pF	0.4MHz	(typ)
Cext=200pF	0.1MHz	(typ)



PADLIB 5–10

External Components of Crystal Oscillators

The osc3 is for 32 kHz use only and needs no external capacitors.

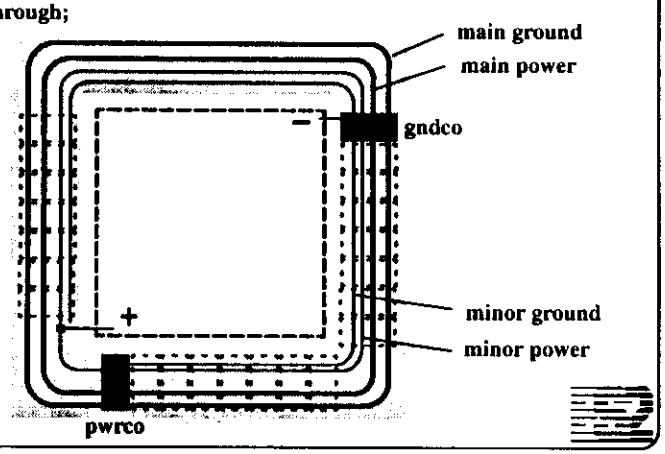
Take care when using the osc cells in applications different from the ones described here.

Notes:

Digital Power Rail Concept for Padlib2

- minor ground rail does not pass through the bottom left;
- Padlib3 –> minor rails do not exist

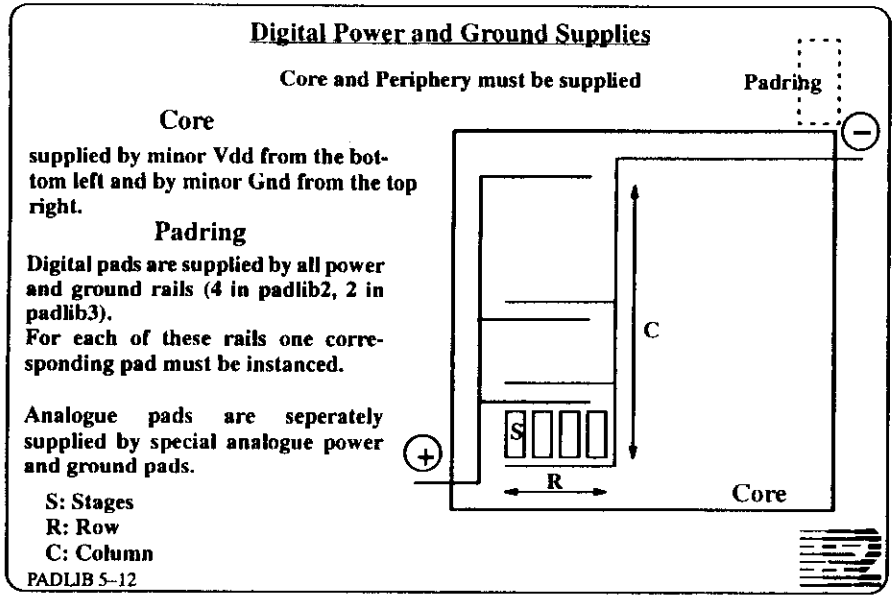
if top right corner has Padlib3 pads on either sides, main power does not pass through;



PADLIB 5–11

Digital Power Rail Concept for Padlib2

Notes:



Digital Power and Ground Supplies

Always keep in mind that additional power pads (i.e. pins) may be necessary in order to properly supply the chip !

Notes: _____

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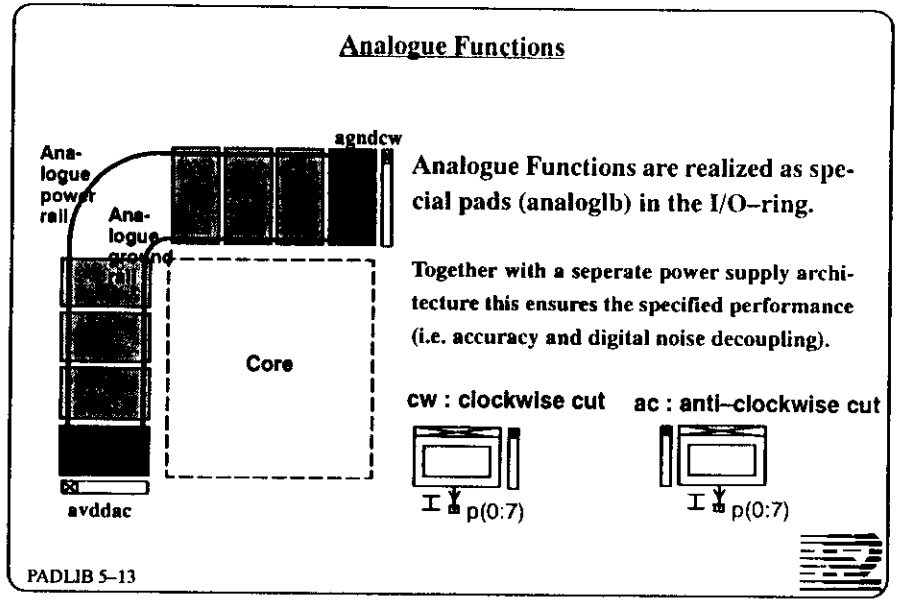

Analogue Functions

Because the analogue functions are realized in the same process as their digital counterparts, the supply– and input/output voltage limits are the same (i.e. 5V).

Notes: _____

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Available Power and Ground Pads

Digital (padlib2)

pwrpy	power for periphery (connects to main Vdd)
gndpy	ground for periphery (connects to main Vss)
pwrco	power for core (and periphery) (connects to minor Vdd)
pwrcopor	as pwrco, but with power–on reset
gndco	ground for core (and periphery) (connects to minor Vss)

Analogue (analoglb)

avddac	power supply pad (anti–clockwise rail cut)
avddcw	power supply pad (clockwise rail cut)
agndcw	ground (clockwise)
agndac	ground (anti–clockwise)

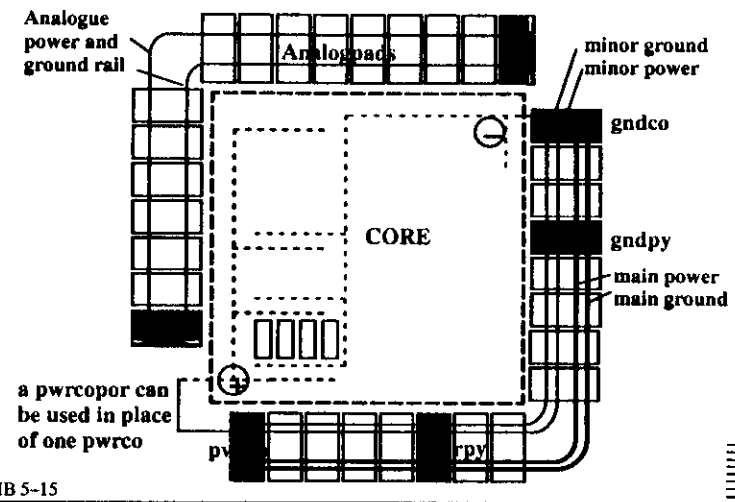
benefits: core is isolated from output buffer switching noise, and input and output buffers are decoupled

PADLIB 5–14

Avaiable Power and Ground Pads

Notes:

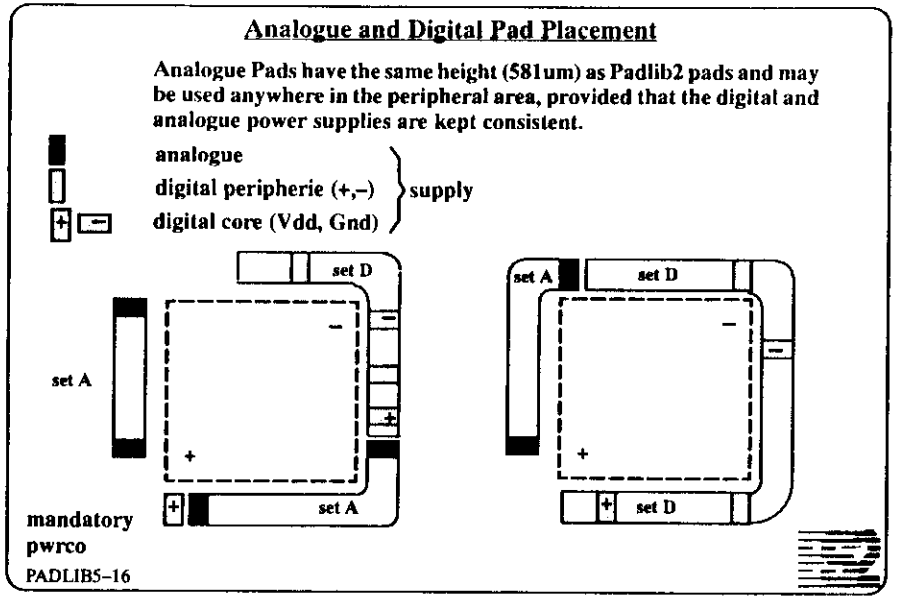
Mixed Analogue – Digital



PADLIB 5–15

Mixed Analogue – Digital

Notes:



Analogue and Digital Pad Placement

Notes: _____

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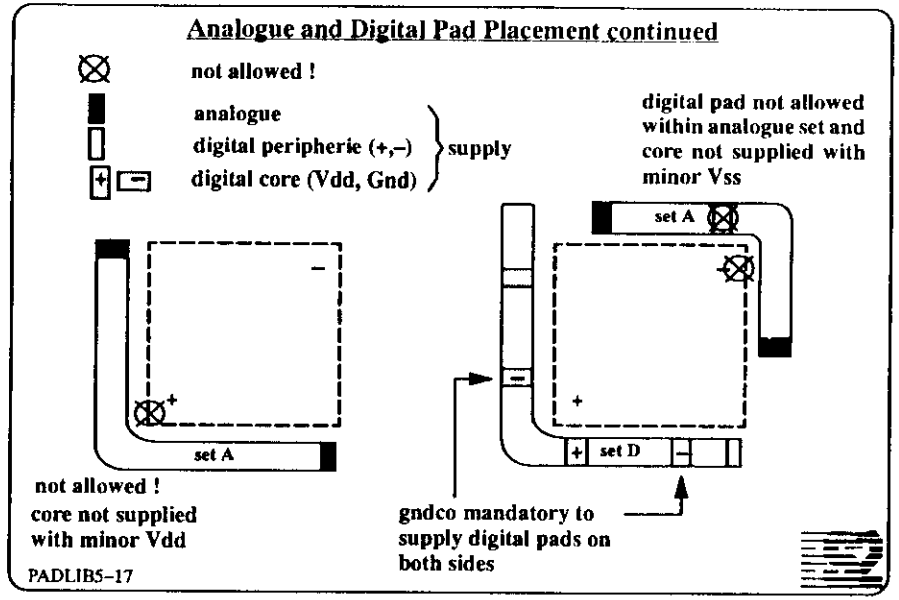
SOLO 1400 V3.02 LIBS – PADLIB



Analogue and Digital Pad Placement

Notes: _____

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Power and Ground Cell Rules

– Placement
– Electrical Rules } checked by Solo command PADAUDIT

- Core must be adequately powered :
  – one pair of pwrco (bottom left) and gndco (upper right) for max. 40 mm^2 core and 68 Pads
  – must be placed within 16 Pads of the corner

- Peripheral output cells must be adequately powered :
  current limits:

pwrpy:	80 mA	(ind) (20 ops1u)
gndpy:	64 mA	(ind) (16 ops1u)

if the current limits are not exceeded the max. distance is:

pwrpy–pwrpy:	15 mm	(worst)
gndpy–gndpy:	8 mm	(worst)

PADLIB5–18

Power and Ground Cell Rules

Notes: _____

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Relaxed Power and Ground Cell Rules

relax option (on) to PADAUDIT allows

– a relaxation of all standard rules by a factor of 2
– double bonding

But parametric figures cannot be guaranteed –> Derating:

0.4V for VIH and VIL
0.2V for VOH and VOL

e.g.	TTL input	VIL	max	=	0.4V (std. 0.8V)
		VIH	min	=	2.4V (std. 2.0V)
	CMOS output	VOH	min	=	4.0V (std. 4.2V)
		VOL	max	=	0.7V (std. 0.5V)

with double bonding the following limits exist for the corresponding py–pads:

I < 48mA (ind)

PADLIB5–19

Relaxed Power and Ground Cell Rules

Take care of reduced specs when using the "relaxed" option !

Notes: _____

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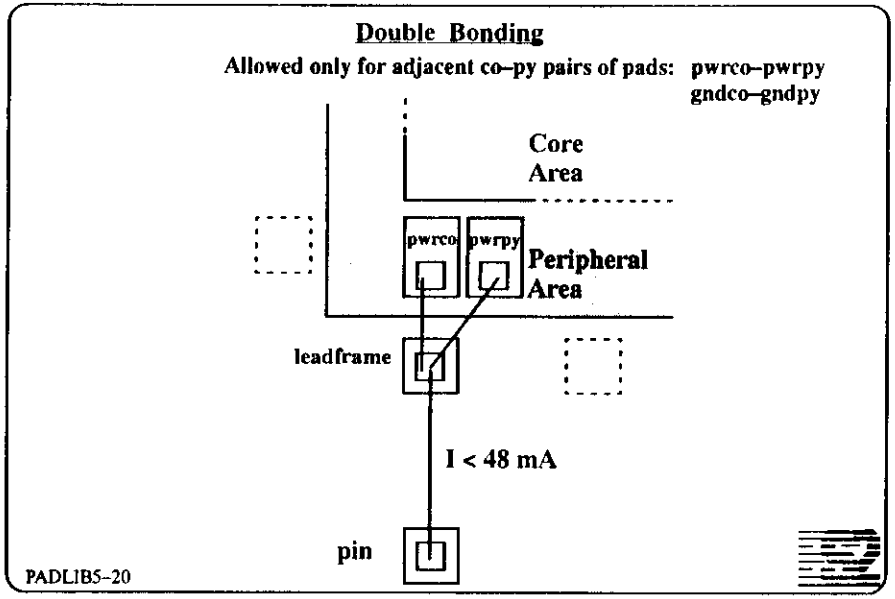

Double Bonding

Notes: _____

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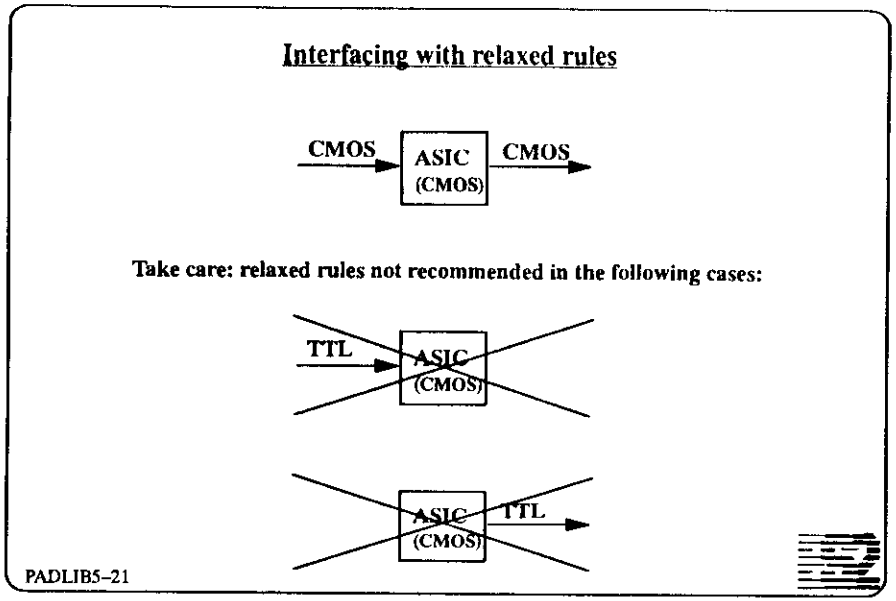
SOLO 1400 V3.02 LIBS – PADLIB



Interfacing with relaxed rules

When working with relaxed rules especially the derated VIL and VOL limits can cause problems when interfacing to TTL.

Notes: _____

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ANALOGLIB5–22

ANALOGLIBRARY

Part Type	Cell Name	Description
Converter	ADC8 (adc8p&adc8s)	8–Bit Suc. Appr. , 5.6us
	ADCMX4 (adcmx4p&adc8s) ADCMX8 (adcmx8p&adc8s)	8–Bit Suc. Appr. with four/eight Multiplexed Inputs , 5.6us
	dac	8 Bit Resolution 1/4 Bit Non–Linearity Potentiometric DAC
	dac2	10 Bit potentiometric
Operational Amplifiers	op11,12,13 op21,22,23 op31,32,33 op41,42,43	High speed High drive capability Low power High speed, line driver
Comparators	comp21,22,23 comp31,32,33 comp41,42,43	Low power High speed; rail to rail common mode Zero offset; strobed; sample & hold; common mode
Input/Output Multiplexer	aimux1,aomux1 aimux2,aomux2	High Channel Separation Low On–Resistance
Voltage References	bgr vref2	1.25V Band Gap Reference Potentiometric Reference
RC–Oscillators	vco1 arco	Voltage Controlled (sym. duty cycle) Resistor– Capacitor(asym. duty cycle)
Digitally Programmable Gain Amplifier	pgadec1,2,3 pgalin1,2,3 pgalog1,2,3	8 different gain steps; decimal 16 different gain steps; linear 16 different gain steps; logarithmic
Triplex LCD	lcdcom1,2,3 lcdvref lcdxyz	6 Phase Backplane Voltage Reference Voltage Pad 6 Phase Segment Voltage
Wired OR	analogwiredor	Connecting analogue outputs
Pads	avddac avddcw agndac agndcw ain aout	Power Pad anti–clockwise Power Pad clockwise Ground Pad anti–clockwise Ground Pad clockwise Analogue input Analogue output

Analogue Simulation

An accurate analogue simulator (such as SPICE) is generally "slow", when compared to their digital counterparts.

For this reason ES2 has developped the following solution :

1. Characterisation of analogue cells via H–SPICE.
2. Extraction of the results into a digital simulation model (incorporating constraint checking e.g. Common Mode).
3. Thus the analogue functions can be simulated with a digital simulator.

ANALOGLIB5–23

Analogue Simulation

Notes:

Representing Analogue Signals Digitally

8–bit digital bus –> represents a single analogue wire

Decimal	Value on Bus Binary	Hex	Voltage Represented
0	0	0	0.0000
1	1	1	0.0196
8	1000	8	0.1569
15	1111	F	0.2941
63	11 1111	3F	1.2353
128	1000 0000	80	2.5098
160	1010 0000	A0	3.1373
192	1100 0000	C0	3.7647
240	1111 0000	F0	4.7059
255	1111 1111	FF	5.0000

ANALOGLIB5–24

Representing Analogue Signals Digitally

The minimum resolution is 19.6mV.

Notes: _____

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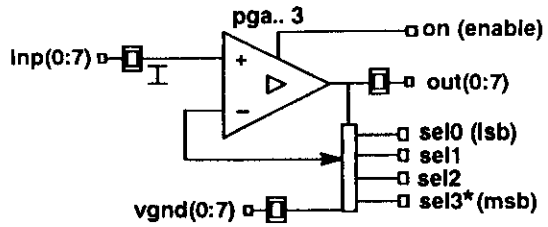
Programmable Gain Amplifier



DECADE Gain	sel2	sel1	sel0
1	0	0	0
1.25	0	0	1
2	0	1	0
5	0	1	1
10	1	0	0
20	1	0	1
50	1	1	0
100	1	1	1

LINEAR Gain	sel3	sel2	sel1	sel0
1	0	0	0	0
2	0	0	0	1
3	0	0	1	0
4	0	0	1	1
.	.	.	.	.
15	1	1	1	0
16	1	1	1	1

LOGARITHMIC Gain		sel3	sel2	sel1	sel0
dB					
0	1	0	0	0	0
2	1.26	0	0	0	1
4	1.58	0	0	1	0
6	1.99	0	0	1	1
.	.	.	.	.	.
30	31.6	1	1	1	1

ANALOGLIB5–25

Programmable Gain Amplifier

Non–inverting PGA consist of an OpAmp with a resistor network. Digital decoding logic is used to select different gains. Note the use of the standby mode with on (input) at low level, out is connected to vgnd (virtuell ground) via the resistor network.

Decade: gain from 1 to 100 in 8 different steps.
Linear: gain from 1 to 16 in steps of one.

Logarithmic: gain from 0 dB to 30 dB in steps of 2 dB .

Notes: _____

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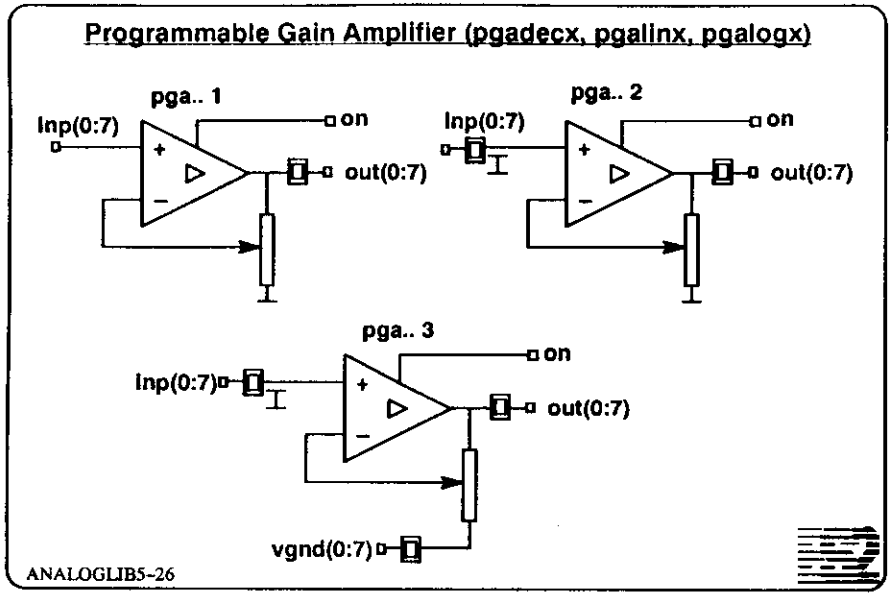


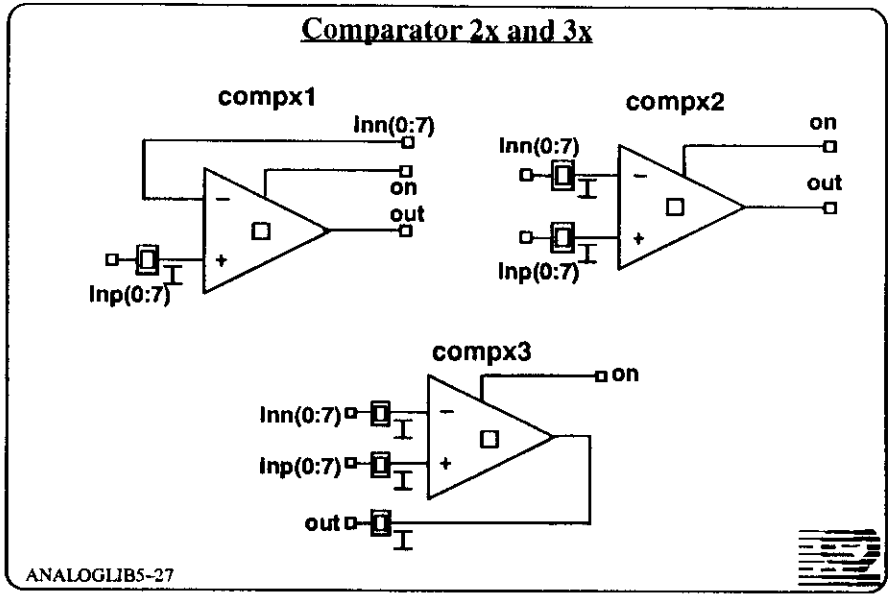
Programmable Gain Amplifier continued

Each series of PGAs has three different bond versions.

If an input is stated " I " it may additionally be connected to an internal analogue signal !

Notes:

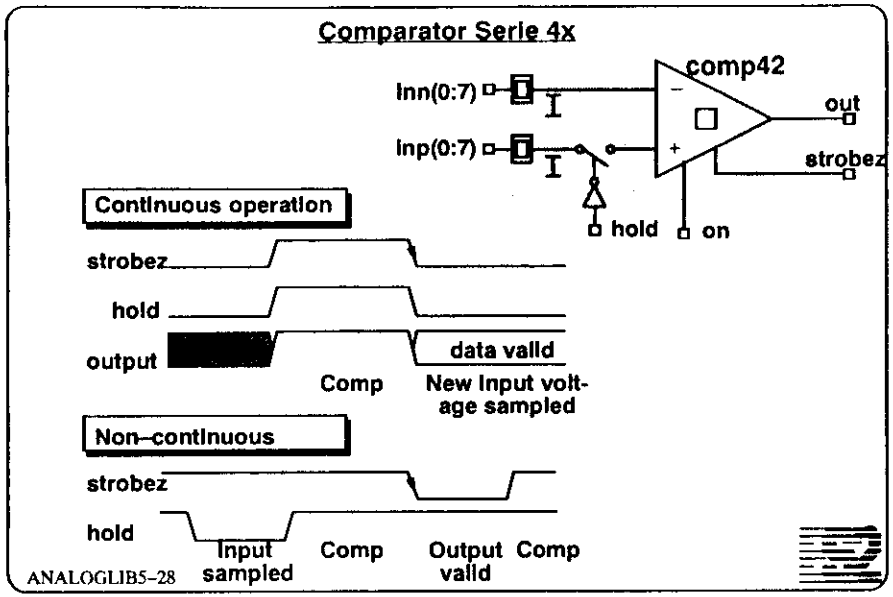
SOLO 1400 V3.02 LIBS – ANALOGLIB



Comparator 2x and 3x

Note the use of the 'standby' mode, output high Z, with on (input) at low level.

Notes:



Comparator 4x

Strobed comparator with offset compensation; **inp(0:7)** is sampled while **hold** is low.

Comparison after **hold** changes from low to high.

The output signal is valid after strobez changes from high to low. The output is high when **strobez** is high.

Out (Output) low if **on** at low level.

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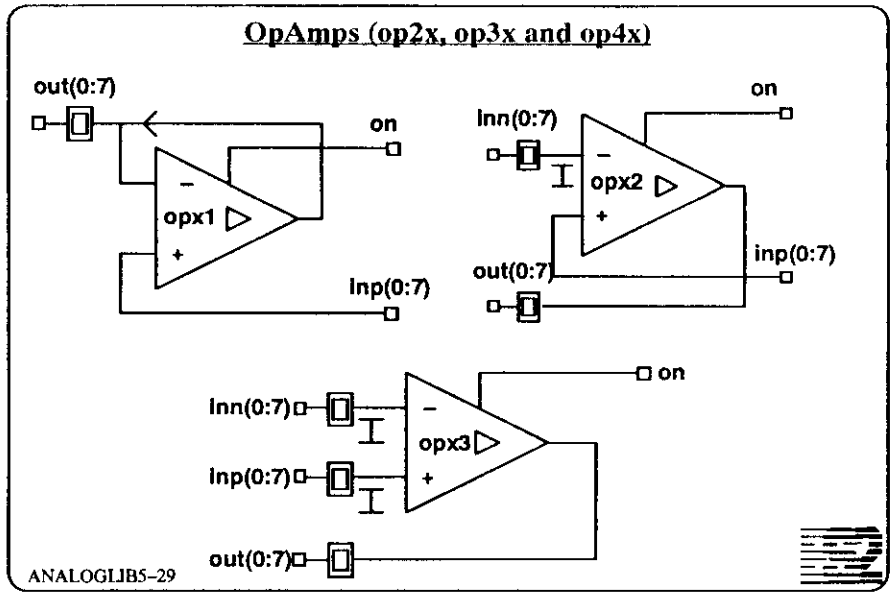

Operational Amplifiers

Notes: _____

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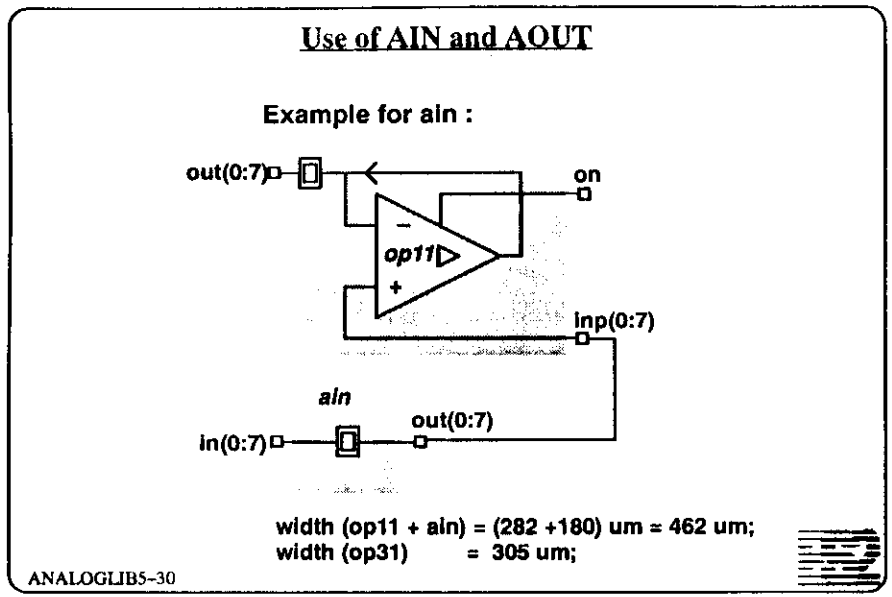
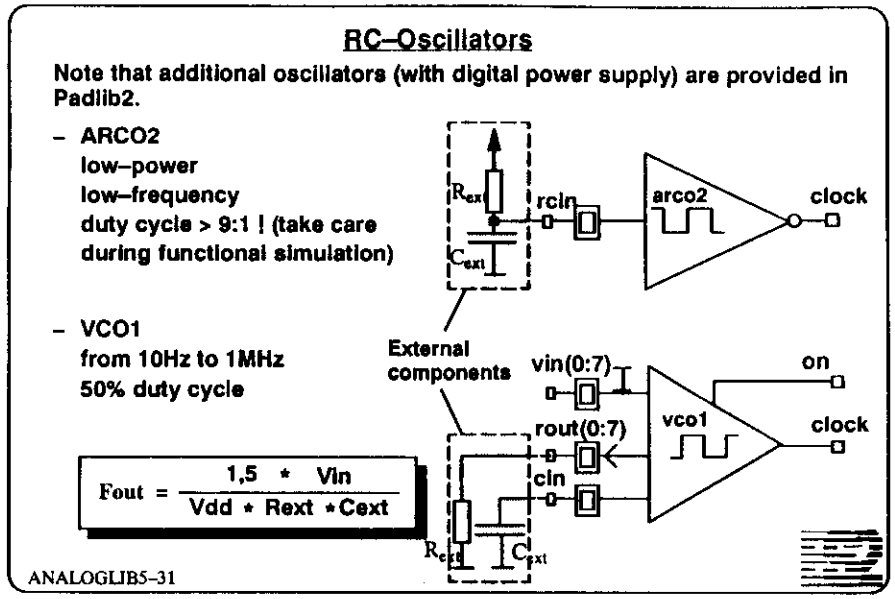


Use of AIN and AOUT

Notes:

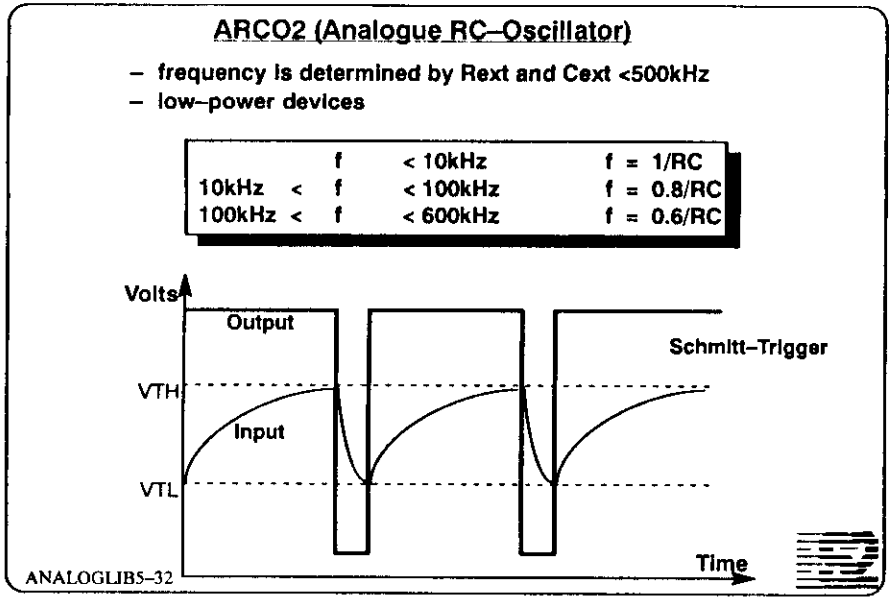


RC – Oscillators

ARCO2 has a frequency that depends on the values of R_{ext} (connected to Vdd) and C_{ext} (connected to Gnd or Vdd).

The frequency of the VCO1 is determined by Vin, Vdd, R_{ext}, C_{ext}. The output clock of the VCO1 is low during standby mode (on at low level).

Notes:



ARCO2

Notes: _____

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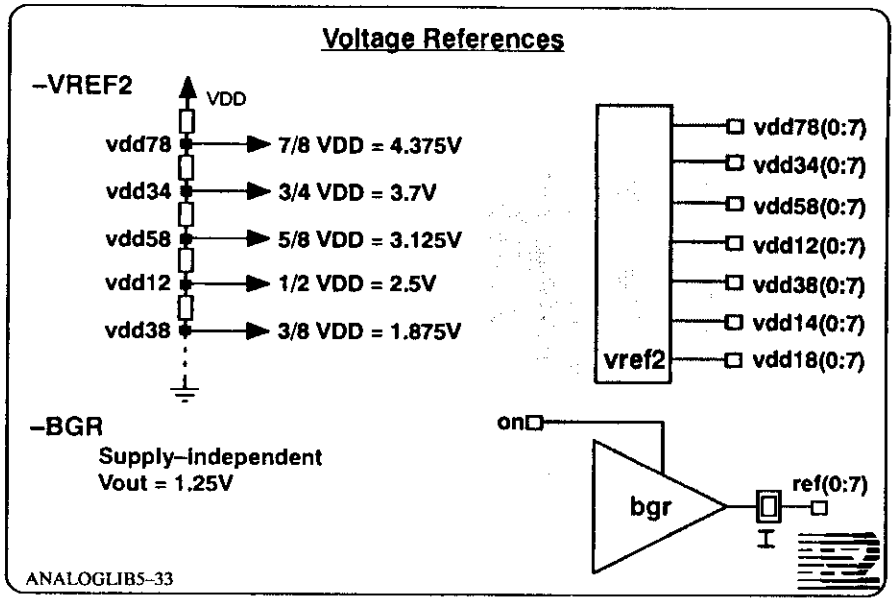

Voltage References

Notes: _____

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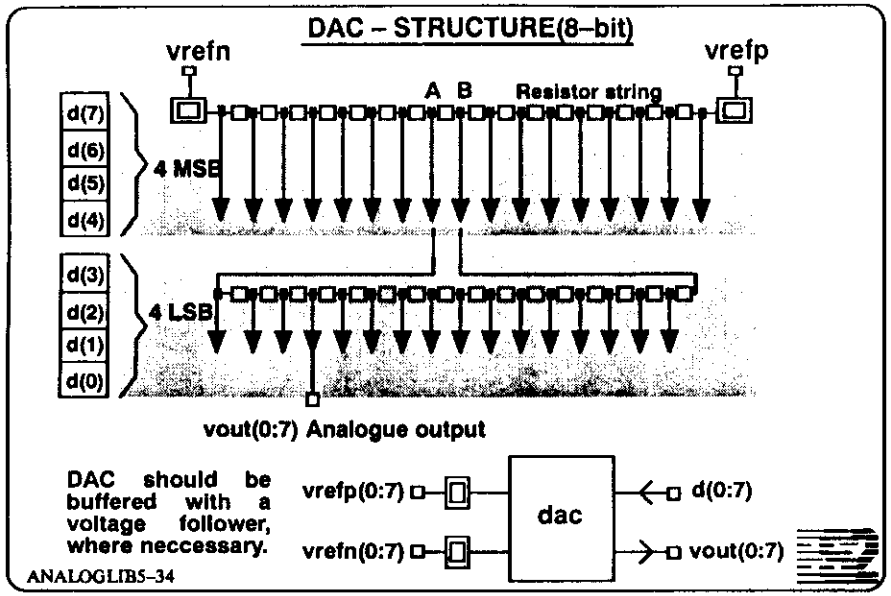
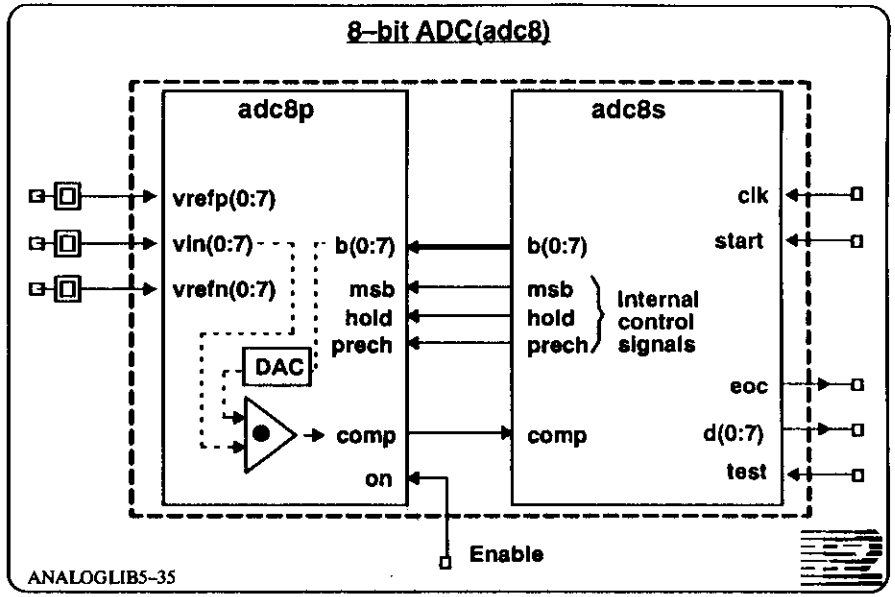


DAC – Structure

The DAC is based on a string of sixteen poly-silicon resistors connected between vrefp and vrefn. The four most significant bits select two tap–off points to be connected to A and B. The voltage difference AB is then applied across a string of transmission gates. The four least significant bits select a tap–off point to be connected to the analogue output vout.

If the output is buffered the output range is reduced to the common mode range of the voltage follower.

Notes:

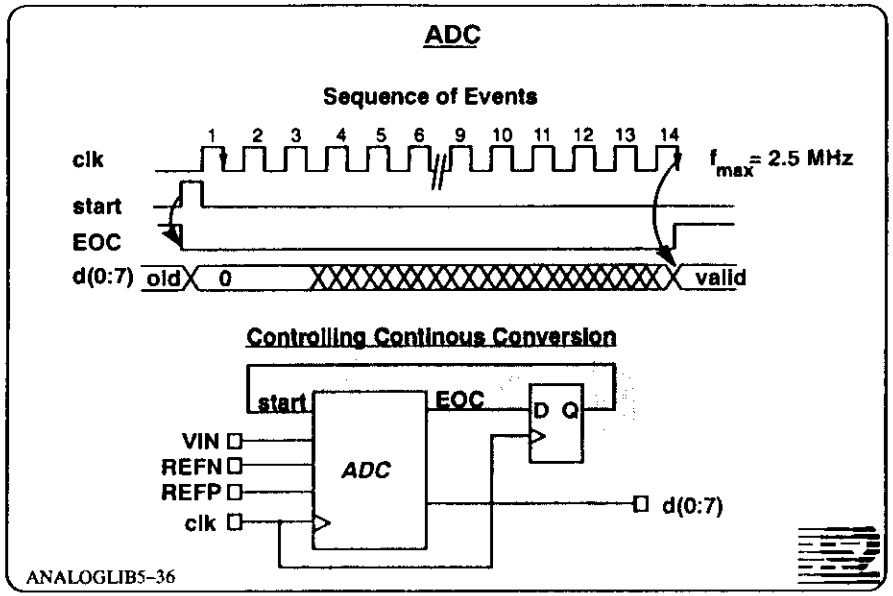


Analogue Digital Converter

The division (adc8s and adc8p) minimises the pad size, because the digital functions are implemented by means of optimised array logic as part of the ASIC core.
– Successive approximation
– Sample and Hold to store **vin** during one conversion.
– 8–bit DAC to provide internal analogue voltages.
– A rail–to–rail comparator that compares the sampled input voltage with the internal DAC reference voltage.

For functional simulation test (input) is at low level. In testmode (test=high) vin is automatically sampled again before lsb–compare to set all 8 bits.

Notes:



Analogue Digital Converter

The conversion process involves the following steps:
–All bits of the digital output bus d(0:7) are set to 0.
–Conversion begins when start goes from high to low and continues for 14 clock cycles.
–vin(0:7) is sampled for two clock cycles.
–EOC output goes high at the end of 14 clock cycles to indicate that conversion is complete and that the output data d(0:7) is valid.

Notes: _____

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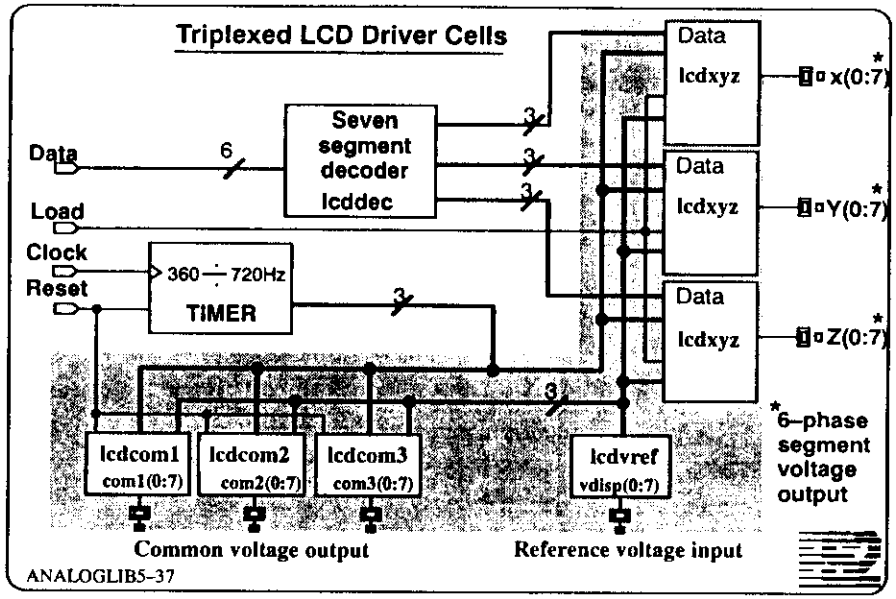


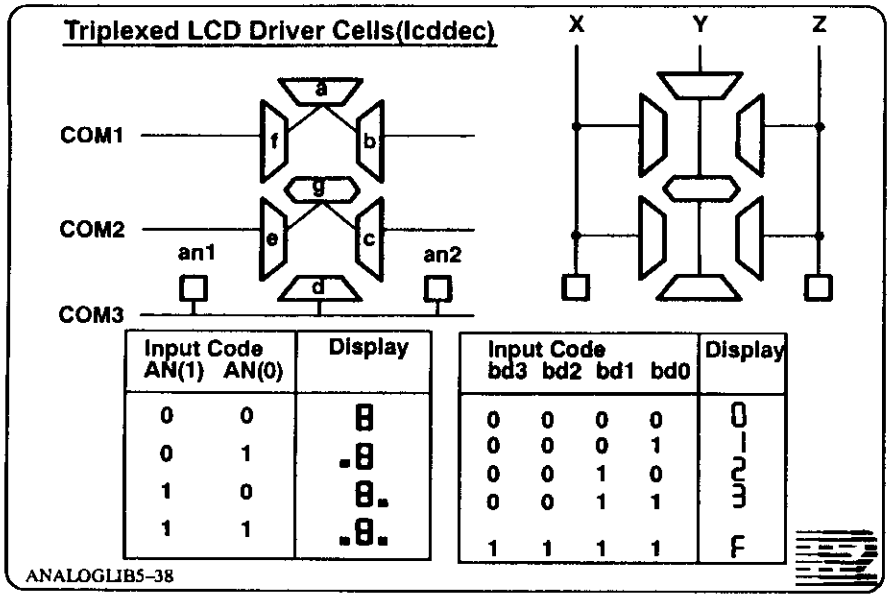
Triplexed LCD Driver Cells

To drive one LCD digit and two annuciators you need all these cells. For each additional digit you need to add an lcddec cell and three lcdxyz cells. The lcdcom cells are common to all digits (up to 10) in a display.

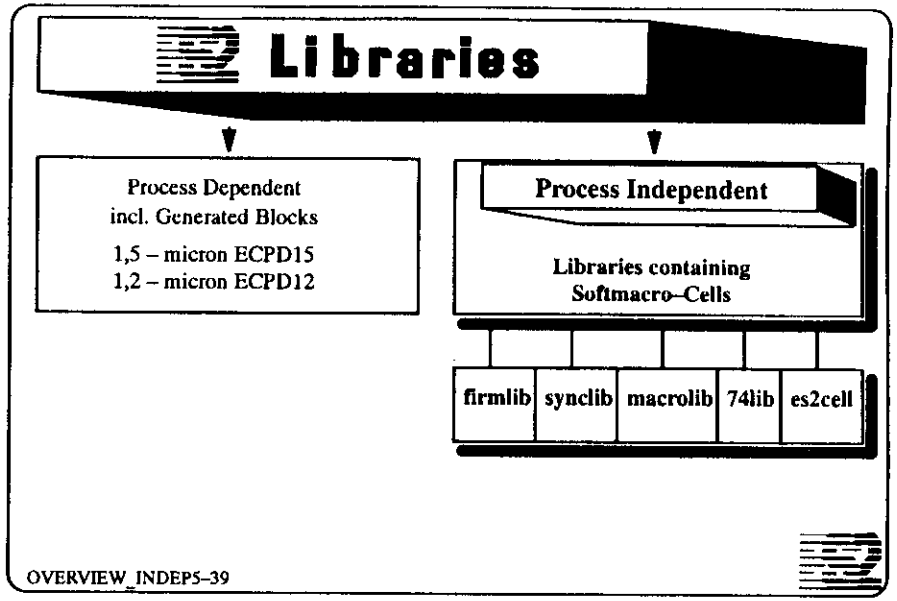
Notes: _____

_____

_____



Triplexed LCD Driver Cells continued



Process Independent Libraries

ASIC designs using process–independent libraries can be manufactured by any of the foundry processes supported by the Solo software. Note that these softmacro–cells do not define either relative placement on silicon of the cells they use, or the lengths of the interconnections between them until the whole design has been placed and routed.

Notes:

Notes:

FIRMLIB5–40 **FIRMLIB** Parametrisable Parts

Part	Type	Cell Name	Description
Buffers	standard	es2buff9	drive strength = 9
	tristate	es2tri3	drive strength = 3
		es24tri3	Combination of four
		es2ntri	
		es2nbuff	Generic
		es2ninv	Non–Inverting
n–Input Gates		es2and	AND
		es2nand	NAND
		es2nor	NOR
		es2or	OR
Flip–flops	D	es2dffrn	with sync clear
		es2dffsp	with sync set
		es2syncd	to catch async signals
		es2dasc	async set and clear
		es2muxff	with mux inputs
	E	es2effrn	with sync clear
		es2effsn	with sync set
	JK	es2jkasc	async set and clear
	R/S	es2srff	
		es2rsff	active high controls
Multiplexers		es2mux	2:1 inverting
		es2mux21	2:1
		es2mux41	4:1
		es24mux21	Combination of four 2–to–1
Registers		es2reg4	4–bit
	n–bit	es2regd	uses D–type flip–flops
		es2regl	uses latches
		es2regm	uses mux D–type ff
	n–bit Shift	es2sreg ps	parallel in, serial out
		es2sreg spr	serial in, parallel out, clear
		es2sreg sps	serial in, parallel out, set
		es2sreg ss	serial in, out, clear
n–bit Counters	Sync	es2ctr	parallel load , sync clear
		es2ctrac	parallel load , async clear
	Hard–coded Counter/timer	es2htimer	with clear
Adder		es2add2	2–bit full Adder
Demultiplexer		es2demux14	1–to–4 Demultiplexer

SYNCLIB5–41 **SYNCLIB** Synchronous Flip–Flops

Part Type	Cell Name	Description
D –type	dff rn	with clr
	dff sp	with set
	muxff	with input mux
E–type	eff rn	with clr
	eff sn	with set
T–type	tff rn	with clear
	tff sn	with set
E/T–type	etff rn	with ena, clr and toggle
	etff sn	with ena, set and toggle
RS–type	rsff grp rp sp	with set, clr and global clr
	rsff gsp sp rp	with set, clr and global set
	rsff rp sp	with set and prioritised clear
	rsff sp rp	with set and prioritised set

SYNCLIB

Notes: _____

MACROLIB5–42

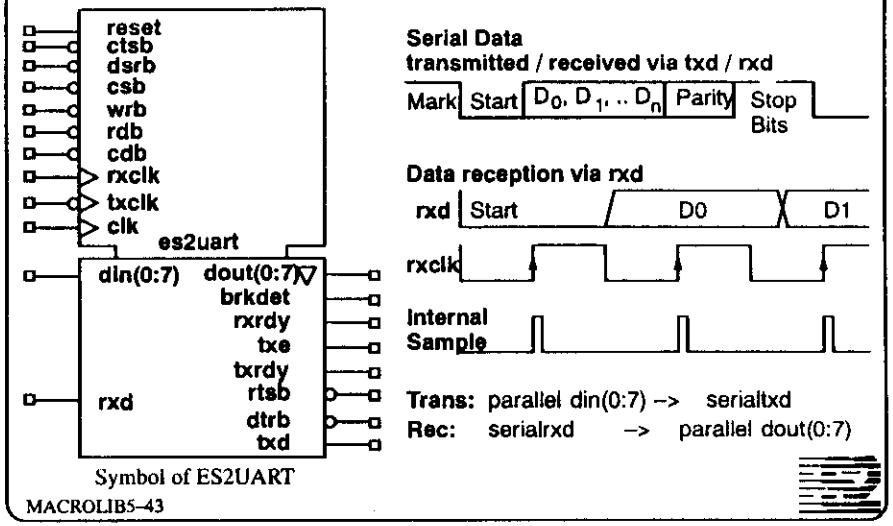
MACROLIB complex functions

Part Type	Cell Name	Description
Asynchronous Receiver / Transmitter	ASYNC REC	parameterised, hard–coded, serial IN/parallel OUT, Flags (framing, overflow, parity)
	ASYNC TRANS	parameterised, hard–coded, parallel IN/serial OUT
	ES2UART	Universal async Receiver/Transmitter
Cyclic Redundancy Checkers	CCITT BCC	Cells produce a BCC (Block Check Char) conforming to CCITT format
	CRC12 BCC	CRC12 standard
	CRC16 BCC	CRC16 standard
m by n Multipliers max: 15 x 15	PMULT	parallel–unsigned
	SMULT	serial–signed;m(sign:msb) x n(sign:msb)
	UMULT	serial–unsigned
Adders positive numbers	RIPADD	n–bit Ripple Adder , n < 16, see sumcar(baselib)
	CLADD	n–bit Carry Look–Ahead Adder

MACROLIB

Notes:

ES2UART



Symbol of ES2UART

MACROLIB5–43

ES2UART

Notes:

74LIB5-44

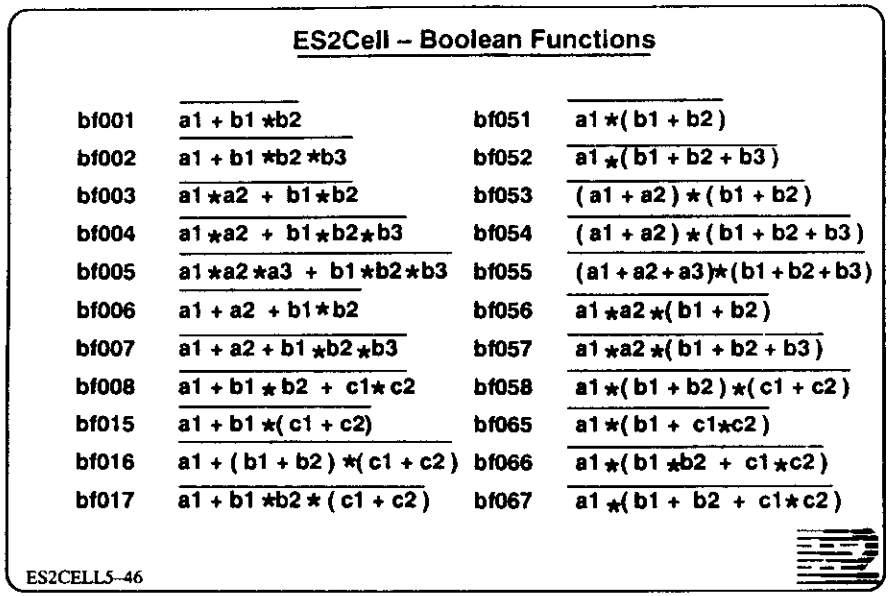
74LIB

Part	Type	Cell Name	Description
Counters		hc160c/162c	Sync 4–bit decade
		hc161c	Sync 4–bit binary, async clear
		hc163c	Sync 4–bit binary, sync clear
		hc390c/393c	4–bit bcd and bi–quinary / 4–bit binary
		hc4040c	12–bit ripple binary, async res
		hc177c	4–bit preset binary, async load/clear
	Up/Down	hc190c/t190c	sync decade / + async res
		hc191c/t191c	sync binary / + async res
		hc193c/669c	sync 4–bit binary, 2 ck (up,down) / 1 ck
Decoder/ Encoder	Decoder	hc154d	4–16 line, 2 ena(inv)
		hc155d	2x 2–4 line or 1x 3–8 line
		hc237d	1–8 line with address latches
		hc138d/137d	3–8 line /with addr latch(hc259d)
		hc139d	2–4 line
	Encoder	hc147e	10–4 line priority
		hc149e	8–8 line priority
Multiplexer		hc151m	8–1
		hc153m	4–1
		hc157m	Quad 2–1
		hc158m	Quad 2–1 (inv out)
	Tristate	hc251m	8–channel
		hc253m	4–channel
		hc257m	Quad 2–channel
		hc258m	Quad 2–channel (inverted)
Flip–flop		hc173r	Quad tristate
		hc174r	Hex with clear
		hc175f	Quad with async clear
Buffer	Tristate	hc240b	Inverting octal
		hhc240b	Inverting octal (half)
		hc241b	Octal
		hc244b	Non–inverting octal
		hhc244b	Non–inverting octal (half)
Shift Register		hc194r	4–bit bi–directional
		hc195r	4–bit parallel
		hc299r	Universal
		x299r	Universal (separate I/O)
	8–bit	hc164r/595r	serial–in –> parallel–out / +output register
		hc165r/597r	Parallel–in –> serial–out / +input register
		t165r	Parallel–in –> serial–out, reset
		hc166r	serial or parallel IN –> serial OUT, reset
		x598r	parallel IN –> serial or parallel OUT +input register
Comparator		hc521mc	two 8–bit identify, enable in, one output
		hc686mc	two 8–bit magnitude (= , >), two outputs
		hc688mc	equal to hc521mc, but two input buses
Transceiver (8–bit)		hc651b	transceiver and register
	tristate	hc245b	dir– and tristate control
Arithmetic		hc181a	ALU
		hc182g	Look–ahead carry generator

ES2CELL5–45

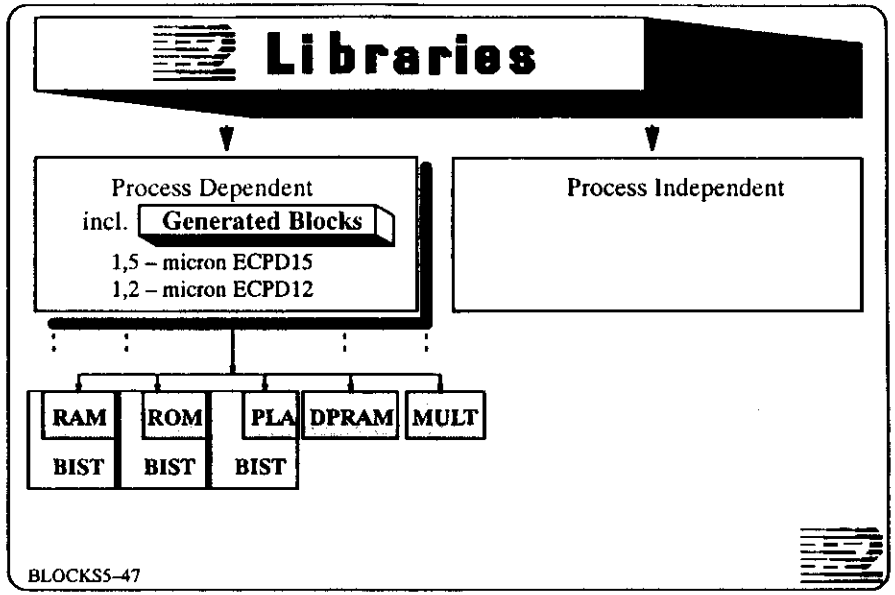
ES2Cell Philips Compatible

Part	Type	Cell Name	Description
Basic gates	AND	an210/310	2–input/3–input
		an410/510	4–input/5 input
	NAND	na210/310	2–input/3–input
		na410/510	4–input/5–input
	OR	or210/310	2–input/3–input
		or410/510	4–input/5–input
	NOR	no210/310	2–input/3–input
		no410/510	4–input/5–input
	2–input Exclusive	en210	nor
		ex210	or
Decoders/ Multiplexer	Decoder	de210	2–to–4
		de212	2–to–4 (actH enable)
	Multiplexer	mu111	2–input
		mu210	4–input
Flip–flops	pos–trig D–type	dfb20	preset, reset
		dfc20	res
		dfn20	
		dfp20	preset
	neg–trig D–type	dtb13	preset, res
		dtc13	res
		dtn11	
		dtp13	preset
	JK	jkb15	neg–trig
		jkb20	pos–trig
	Toggle	tab22	preset, res
		tac22	res
		tap22	preset
	Scan–neg–trig	sfdn1	
		sfin2	
Latches	transparent D	lah10/20	(high enable)/(2 x drive)
		lal20	(low enable)
	S/R	lab10/20	/(2 x drive)
Master and Slave Latches	Master (nor latch)	gm010	
		gm110	res
		gm210	set, res
		gm310	
		gm410	res
		gm510	set and res
		gms10	set
	Slave (nand latch)	gs010	
		gs110	res
		gs210	set, res
		gs310	
		gs410	res
		gs510	set, res
		gss10	set
Inverter		iv101	(10 x drive)
		iv110/120/130	(1 x drive)/(2 x drive)/(3 x drive)
		iv140/160/180	(4 x drive)/(6 x drive)/(8 x drive)
	Tri Inverter	iv212/222/242	(1 x drive)/(2 x drive)/(4 x drive)



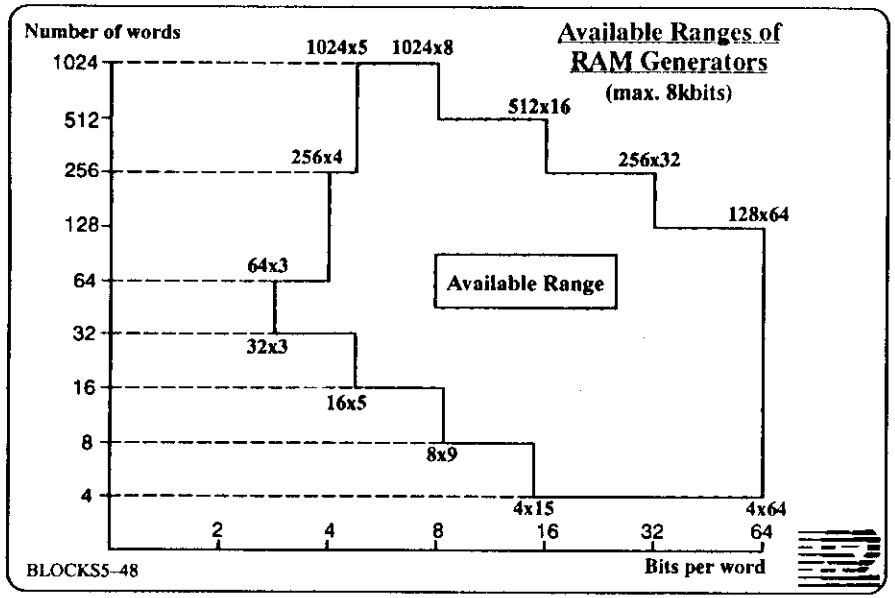
ES2CELL

Notes:



Generated Blocks

Notes:



Available Ranges of RAMs

Notes: _____

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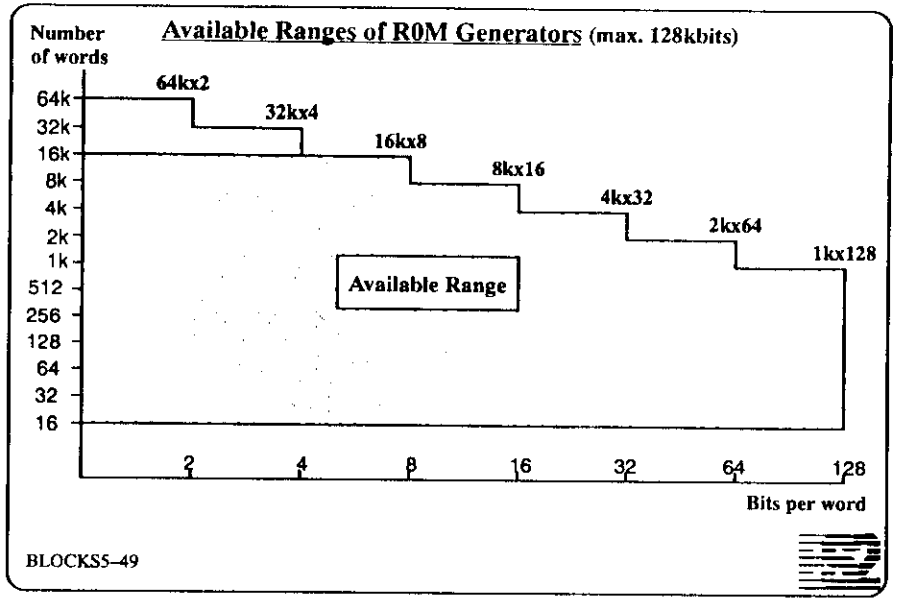

Available Ranges of ROMs

Notes: _____

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Available Ranges of PLA, MULT and DPRAM

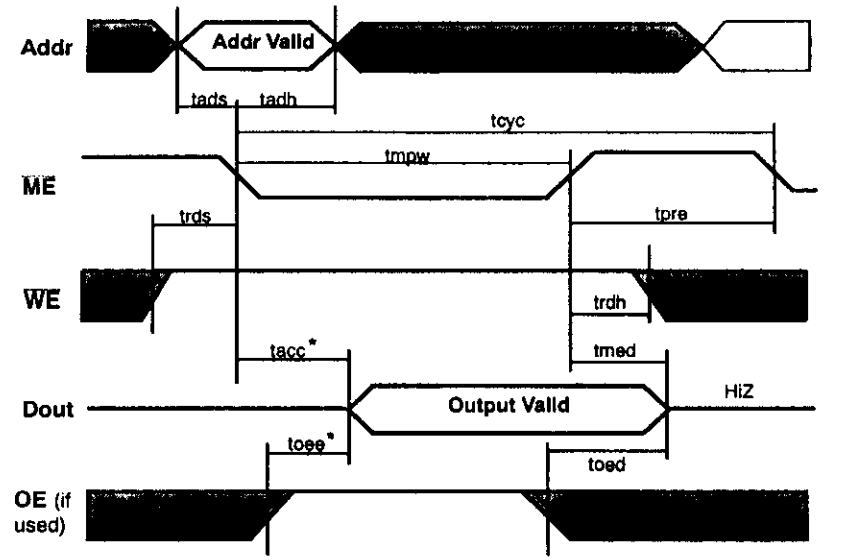
PLA	min terms max. 128	1 to 64 inputs 1 to 32 outputs			
MULT	n*m max. 32*32	8 to 32 for n,m			
DPRAM:					
Parameter	**Condition**		**Min**	**Max**	
Maximum size				16	Kbits
Number of words	Subject to maximum size		8	16K	
Bits per word	Subject to maximum size		1	64	Bits
Supported numder of words		Steps of 8 words	8	256	Words
		Steps of 16 words	272	512	Words
		Steps of 32 words	544	1024	Words
		Steps of 64 words	1088	2048	Words
		Steps of 128 words	2176	4096	Words
		Steps of 256 words	4352	8192	Words
		Steps of 512 words	8704	16384	Words
word size port A / word size port B	n is a power of 2 in the range 1/64 to 64		word size A = n x word size B		

BLOCKS5-50

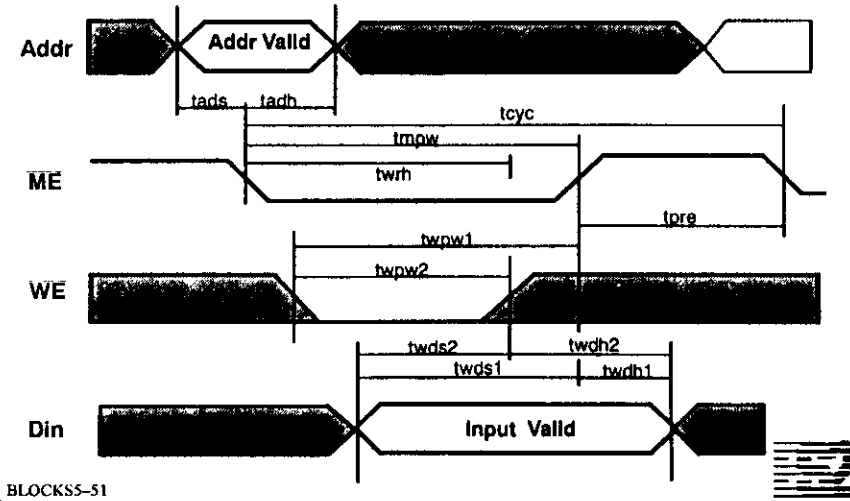
Available Ranges of PLAs, MULTIPLIERs and DPRAMs

Notes: _____

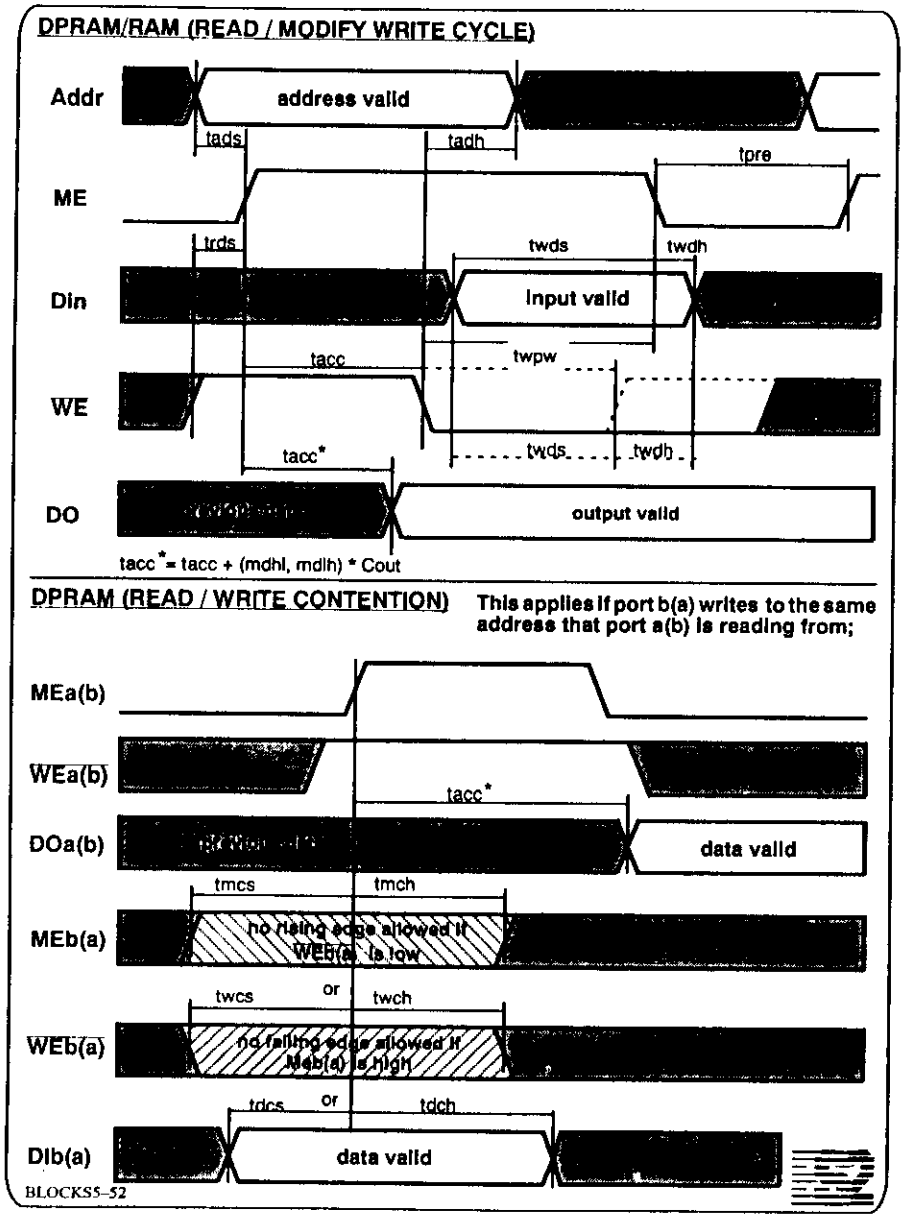
ROM/RAM : Read Cycle Timing Diagram

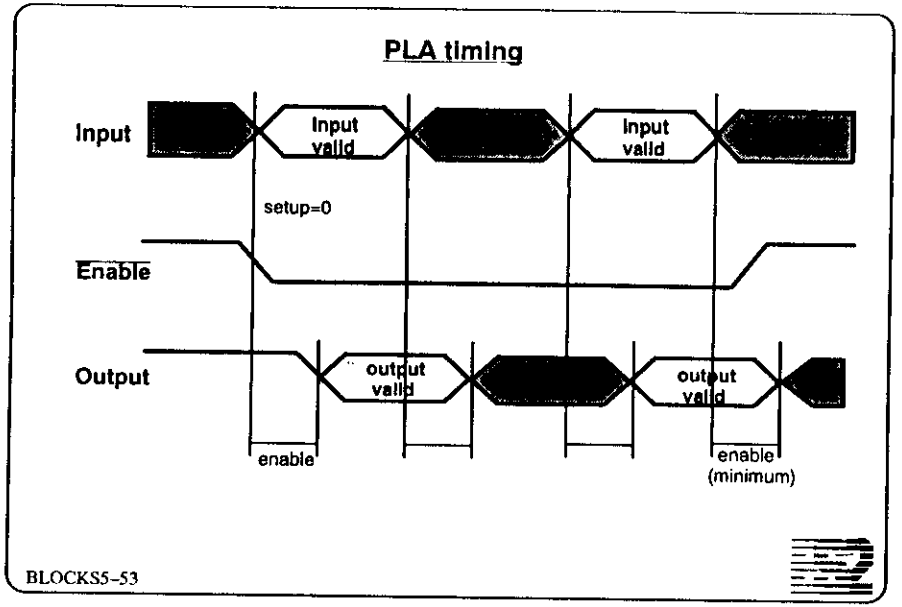


RAM : Write Cycle Timing Diagram



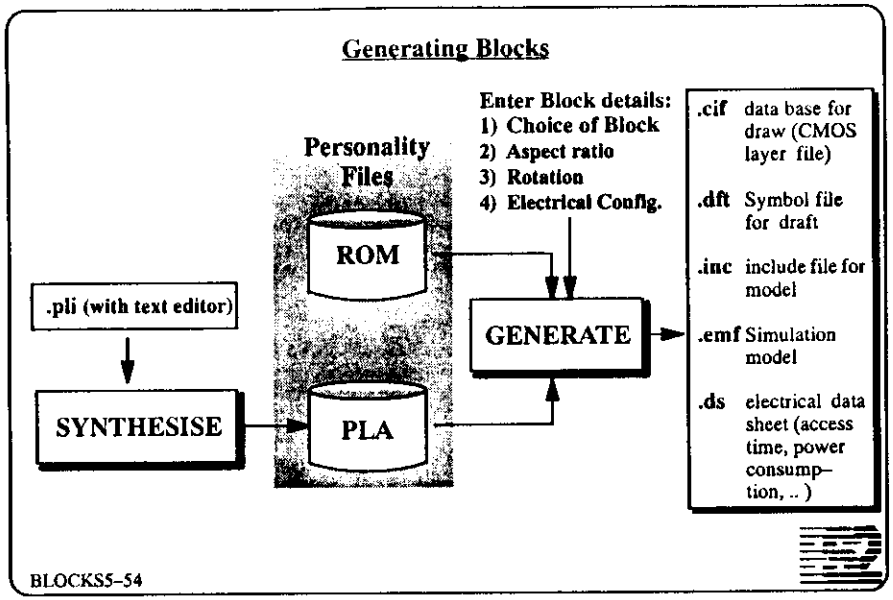
BLOCKS5-51





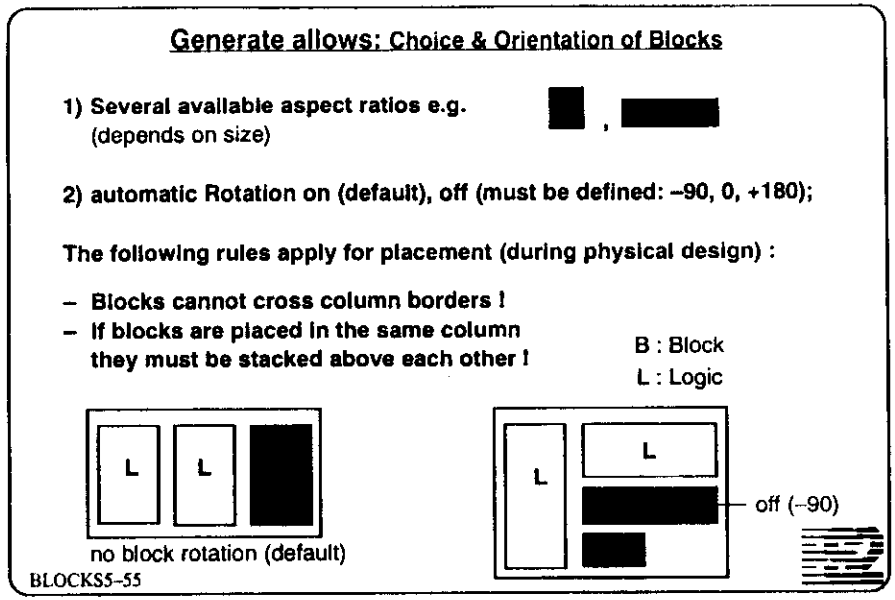
PLA Timing

Notes:



Generating Blocks

Notes:



Choice & Orientation of Blocks

Notes:

PLA and ROM Generation

PLA and ROM Generation

Personality File for PLA and ROM

```
.INPUTS 4
.OUTPUTS 7
.MINTERMS 12
.INNAMES
d0 d1 d2 d3
.OUTNAMES
s1 s2 s3 s4 s5 s6 s7
.PROG
0000  1111110
1000  0110000
0100  1101101
1100  1111001
```

```
.ADDRESS 10
.DATA 16

00  0F0F
01  1E1E
02  3C3C
:    :

63  0F0F
```

Minimizing and Checking PLA personality files via Synthesise:

1) Create Personality file with suffix .pli
2) set syn block ..
   set syn in pli
   set syn out pla
3) **synthesise**
   –> generates optimized PLA personality file with suffix .pla
4) set gen cell ..
   set gen type pla
5) **generate**
   draft
   Read Library File

BLOCKS5-56

Notes: _____

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BIST

BIST (Built–In Self Test for Generated Blocks)

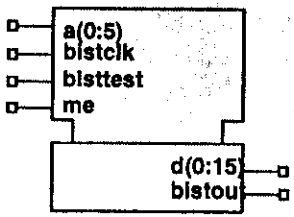
Bist incorporates the additional hardware to free the designer from creating testvectors for blocks. So contrability and observability of blocks is no longer a problem.

BIST is provided by two commands:

GENERATE (with BIST option on)

BISTPREP (create .brp file before run)

Symbol for ROM with BIST



Bistprep analyses the expected signature output of all generated Blocks and creates a test file for post fabrication test at FAB.

BLOCKS5-57

Notes: _____

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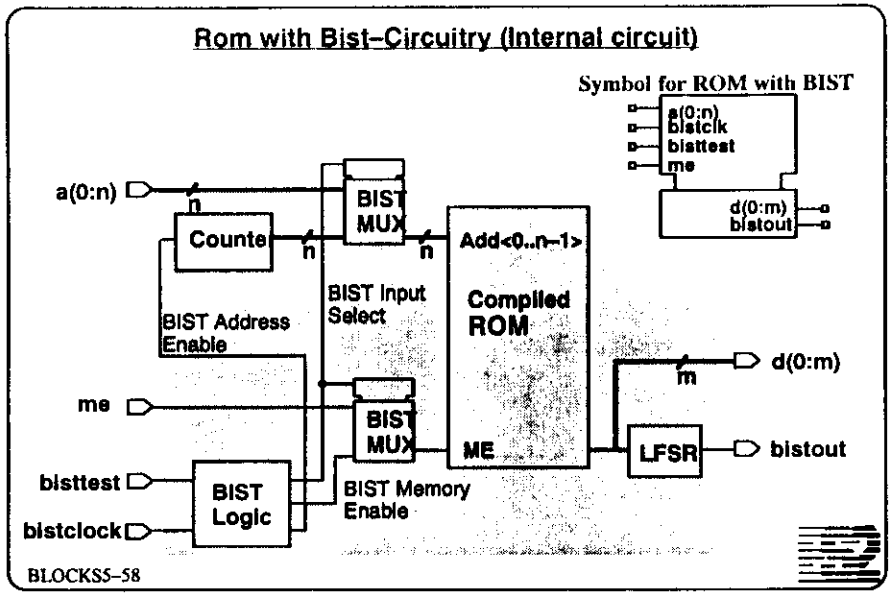

ROM with BIST–Circuitry (Internal)

Notes: _____

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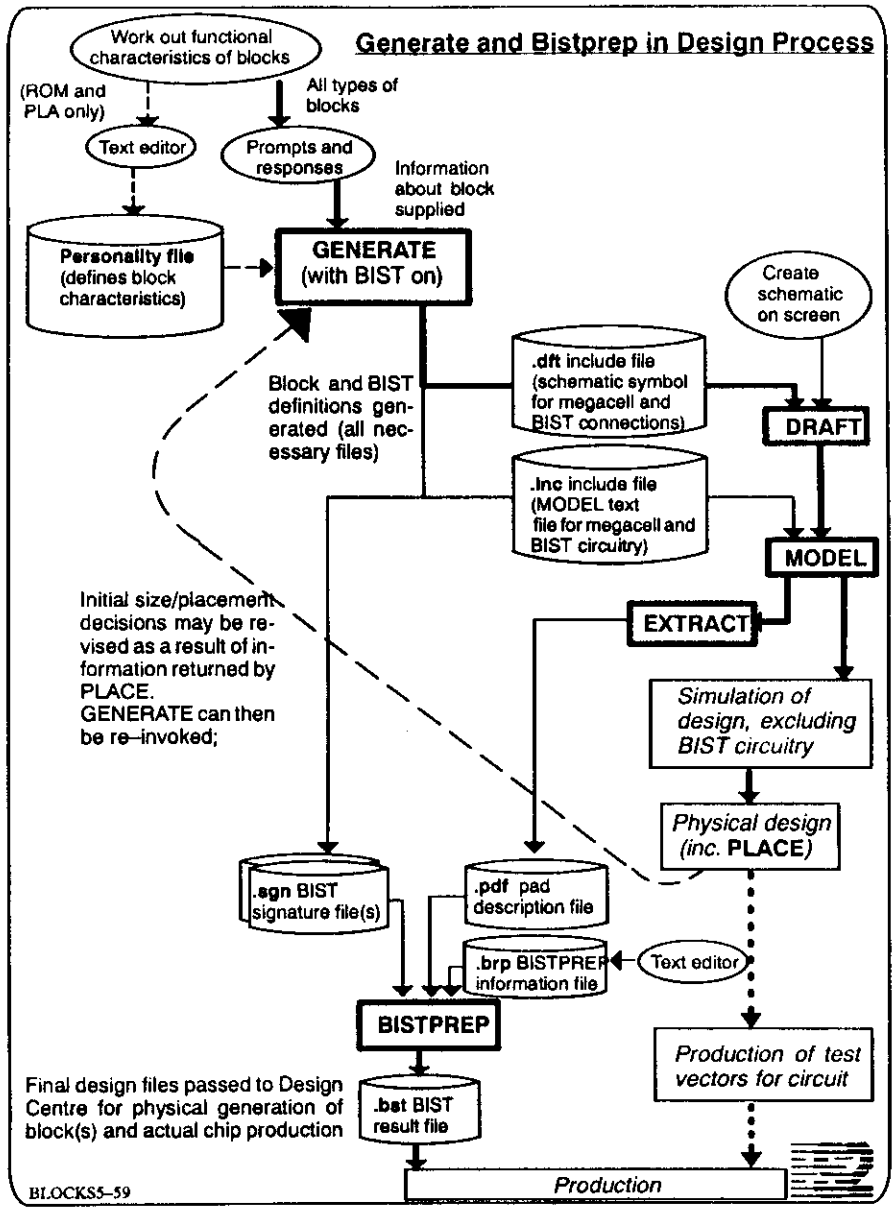
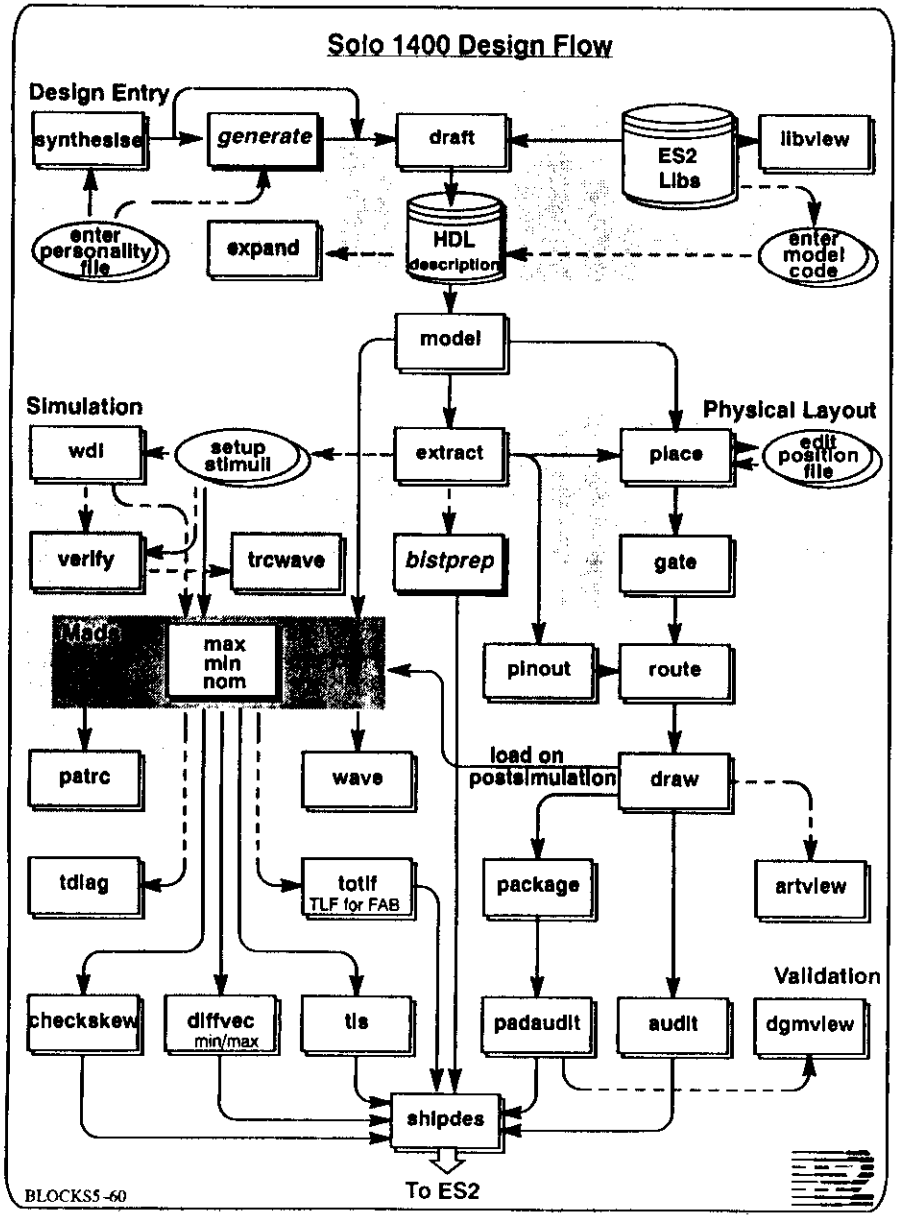
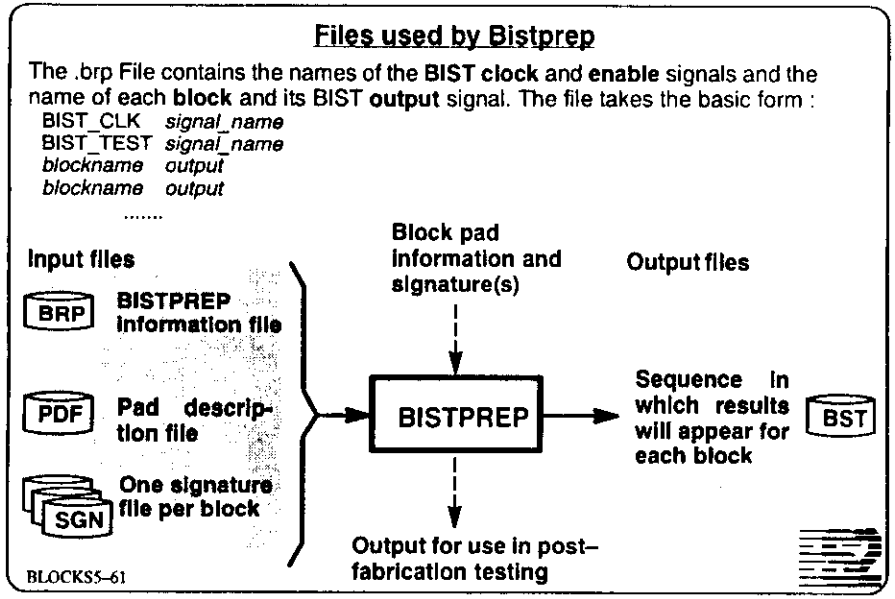


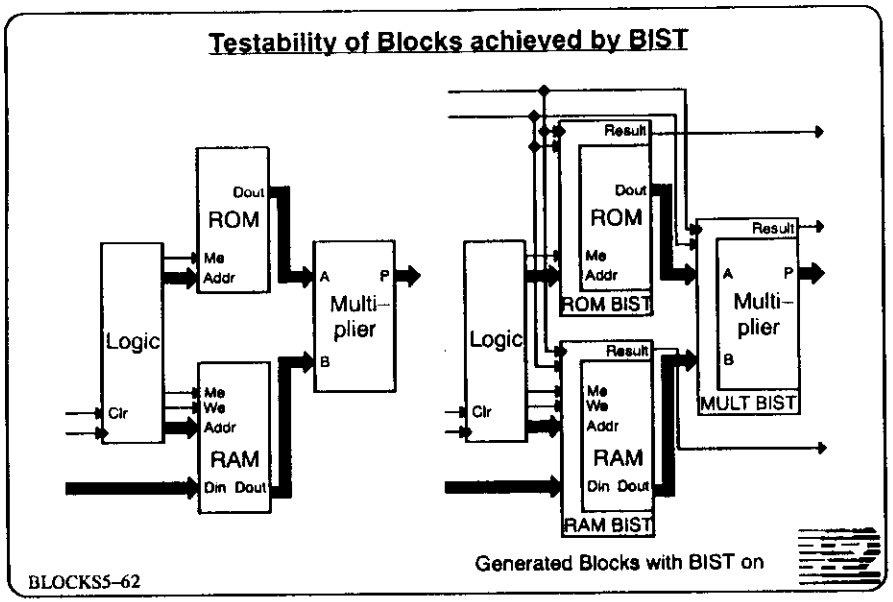


SOLO 1400 V3.02 LIBS – BLOCKS



Files used by BISTPREP

Notes: _____



Testability of Blocks achieved by BIST

Notes: