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UNITED NATIONS EDUCATIONAL, SCIENTIFIC AND CULTURAL ORGANIZATION
INTERNATIONAL CENTRE FOR THEORETICAL PHYSICS
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UNITED NATIONS INDUSTRIAL DEVELOPMENT ORGANIZATION

INTERNATIONAL CENTRE FOR SCIENCE AND HIGH TECHNOLOGY
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SMR/542 - 6

ICTP-INFN
SECOND COURSE ON BASIC VLSI DESIGN TECHNIQUES
18 February - 15 March 1991

Additional Material to Lectures by

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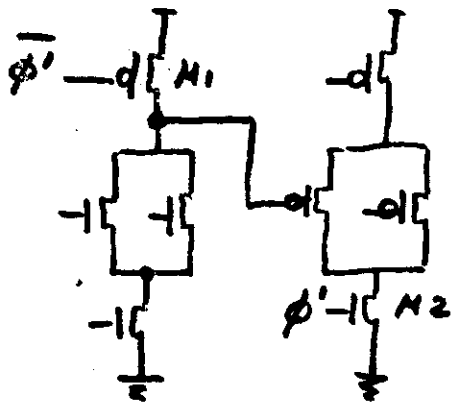
These are preliminary lecture notes, intended only for distribution to participants.

Zippee Logic

Similar to NORA but with dc "leaker" property



$\bar{\phi}'$ never gets up to V_{DD}
ϕ' never gets down to GND
So N_1 & N_2 provides DC current

Good points

It's static (low freq. operation)
Can recover from charge sharing
Better than NORA

Bad points

Dc power, uncontrolled
Still lousy for noise sensitivity

USED IN AT&T "CRISP" µP but rest of ALU didn't work

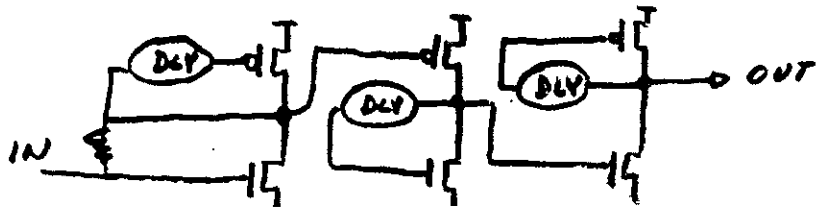
Post-Charge Logic

Data is represented by pulses, not levels:

zero : ——————

one : ——┐ ┌——
tw

Once a gate has passed an edge, it resets itself T_w later



No wasted time if logic depth > T_w

Example

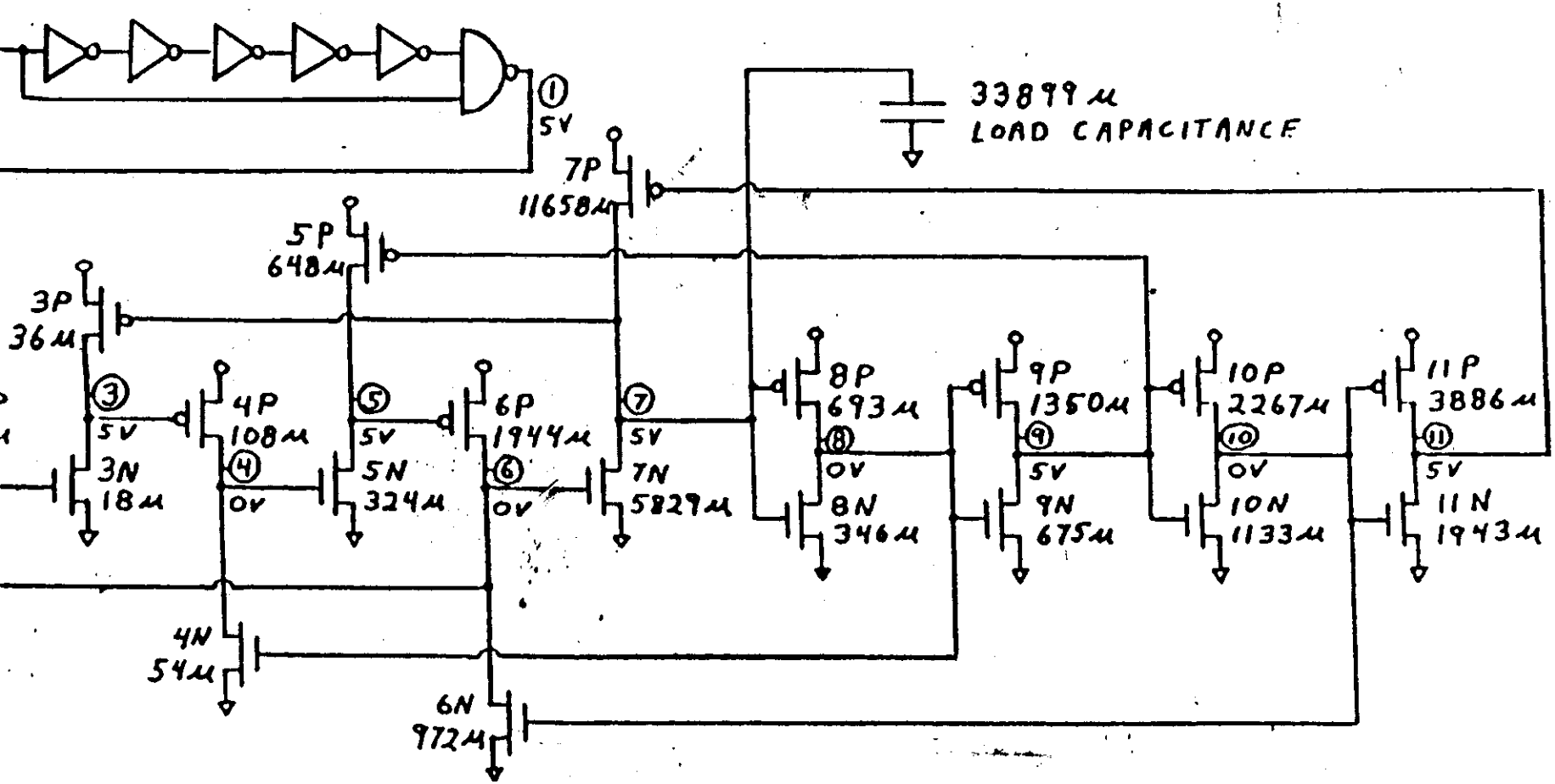
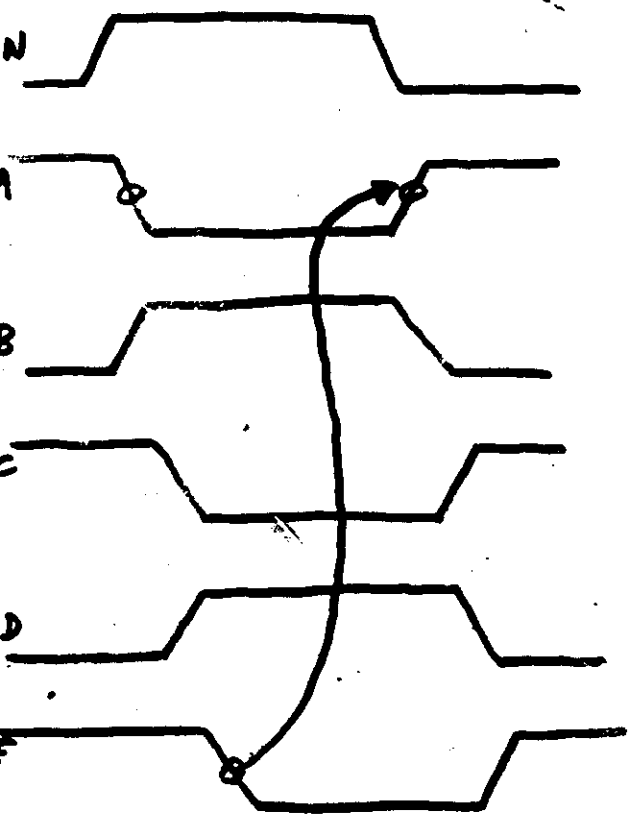


FIG. 2 POST CHARGE LOGIC BUFFER

Post-Change logic, cont'd



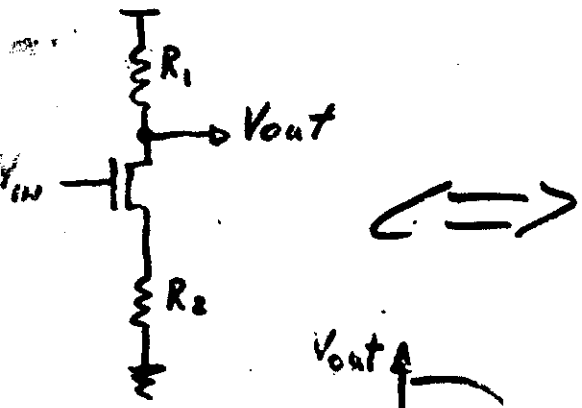
4 stages later causes the post changing

<u>Good</u> Alternating NMOS and PMOS ⇒ lower cap ⇒ faster

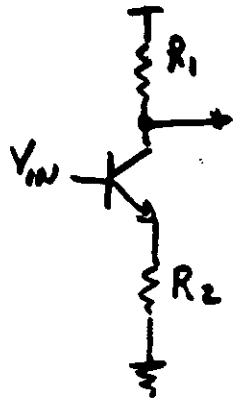
<u>Bad</u> Similar problems to NORA

Used in clocked SRAM

NTL (even faster logic family)

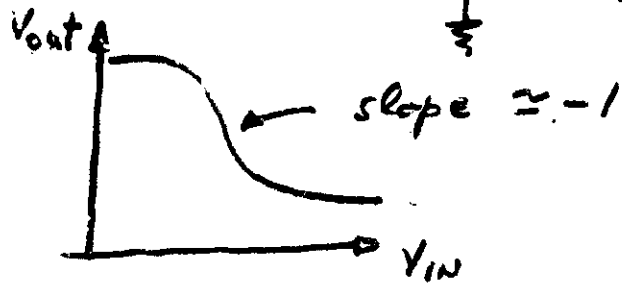


$\Longleftrightarrow$



$\text{Gain} = \frac{V_{out}}{V_{IN}} \simeq -\frac{R_1}{R_2}$

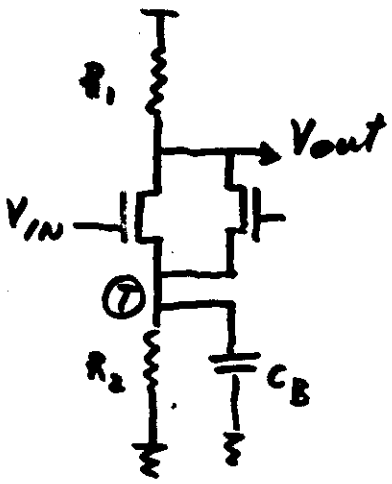
if $R_1 \simeq R_2$ Then gain is near -1



- Output begins moving even before inputs gets halfway point
- "Gain Bandwidth Product" maximizes speed since gain ≈ 1

Unfortunately poor noise rejection compared to static CMOS

NTL cont'd



R_2 supplies negative feedback so, bypass it @ high frequencies

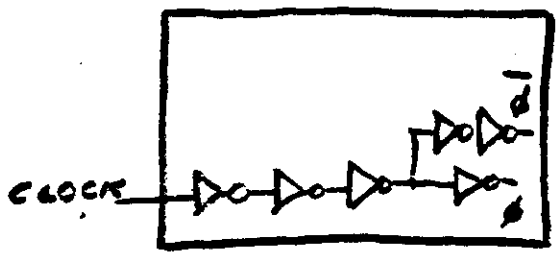
Seems to work great in simulation

BUT

- Lousy performance as V_{cc} is varied
- How to get linear resistors in MOS?
- Lousy performance as resistors vary (process variations)

CLOCK (and fast logic) (

Problem: I/O must be synchronized with external clock

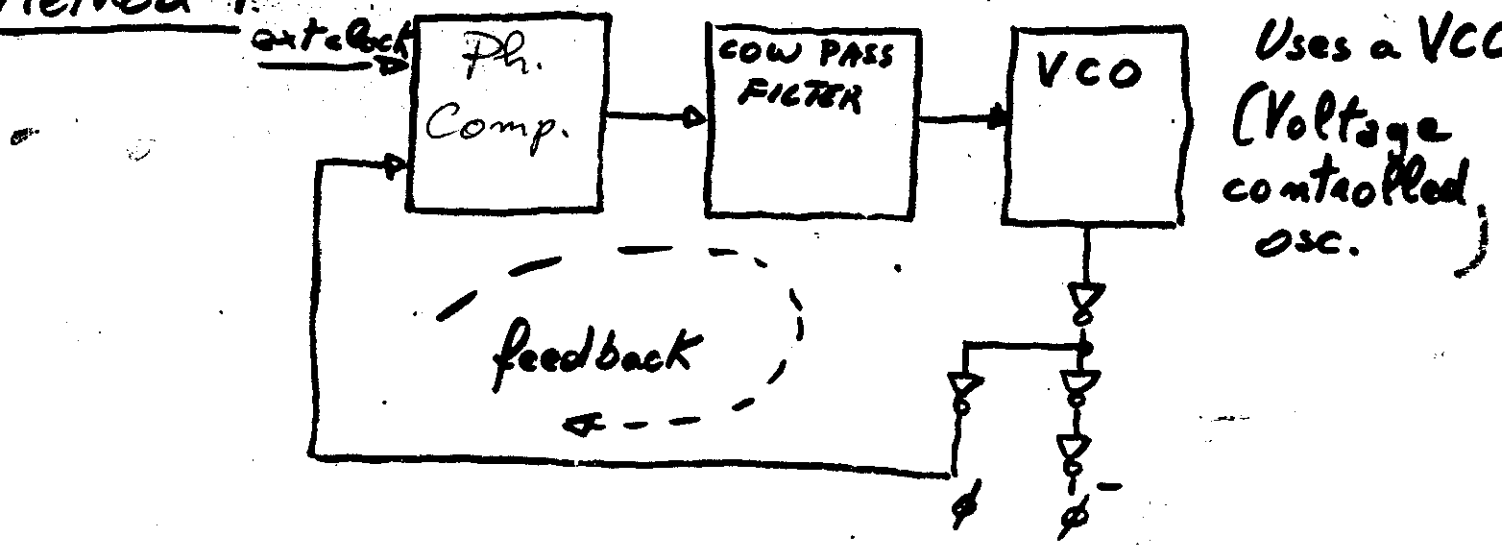


* On chip clock skewed with respect to off chip clock
* Sensitive to processing, V_{cc}, temperature ... etc.

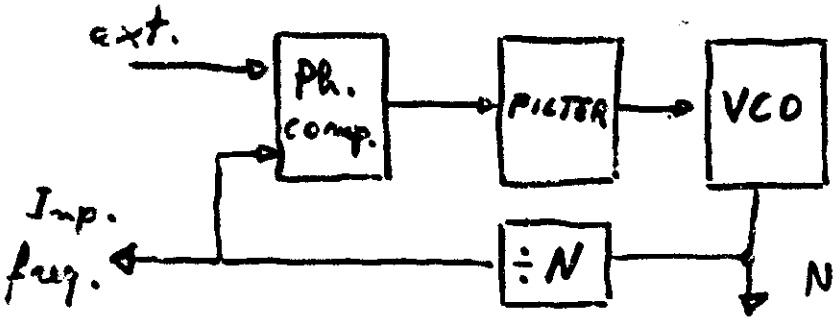
What to do if skew must be very small?

USE PLL (Phase locked loop) to generate ϕ, $\bar{\phi}$ and use feedback to align edges (PHI and CLOCK)

Method 1.



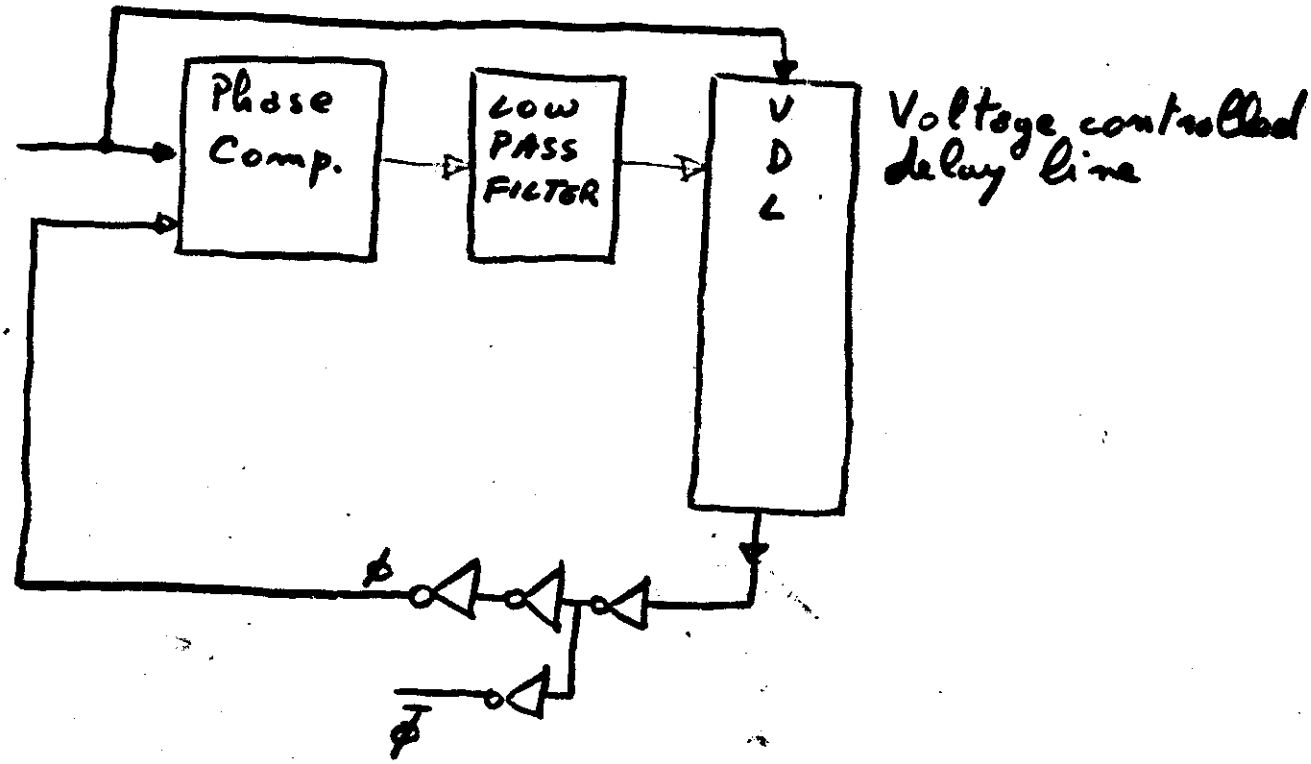
Uses a VCO (Voltage controlled osc.)

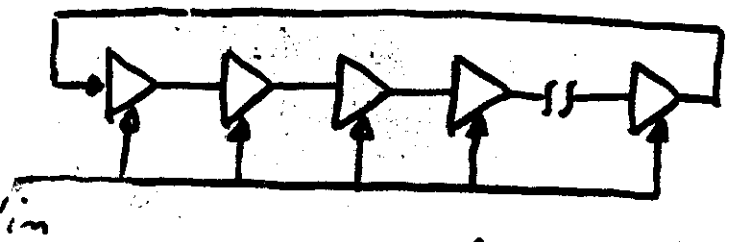


Can multiply input frequency higher

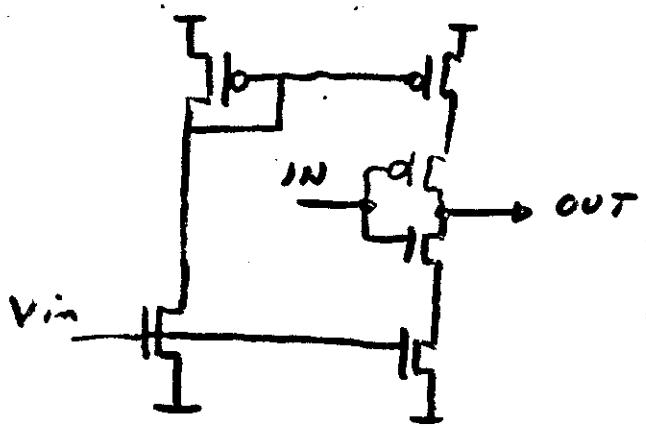
CLOCK (addendum clock #2)

Method 2



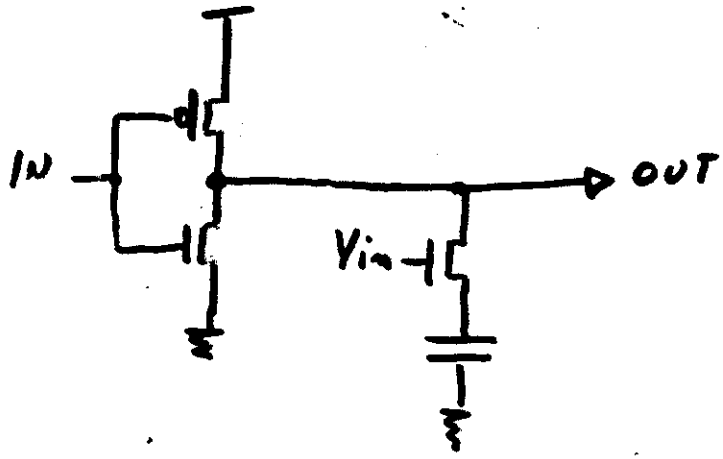


$$freq = \frac{1}{2 \cdot N \cdot T_{stage}}$$



$Delay \propto \frac{1}{V_{in}}$ best for VCO application

CLOCK (additional clock)



Delay ∝ Vin

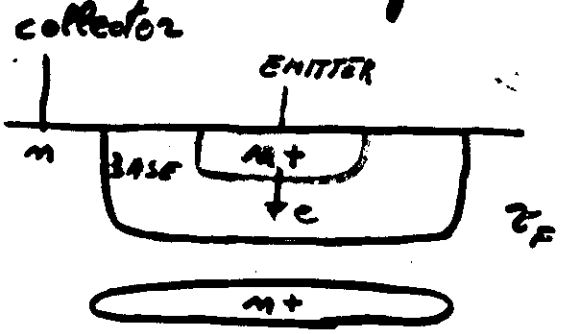
Best for VCDL application

μP with PLL

Inmos	Transputer
Motorola	88000
	68040
MIPS	R3000
Intel	80860, 80486

This is CMOS, in ECL skew must be less than 100 ps !!!!

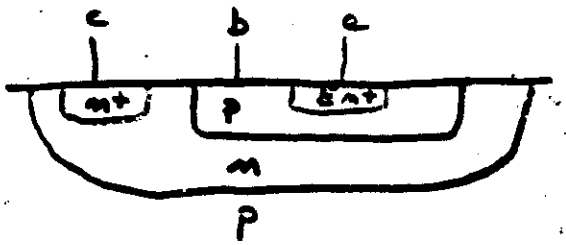
Dipolar devices (addendum #1)



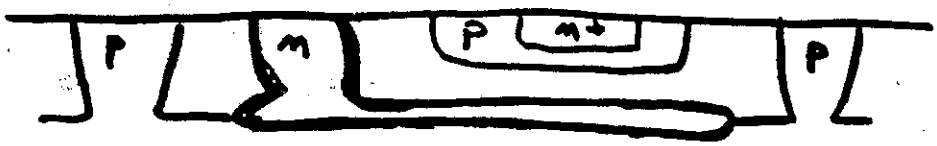
NPN device works by injecting electrons from the emitter to the base.
They diffuse across the base and are collected by the collector.

The intrinsic speed is set by the base width, dimension controlled by 2 implants. (~ 0.1μ)

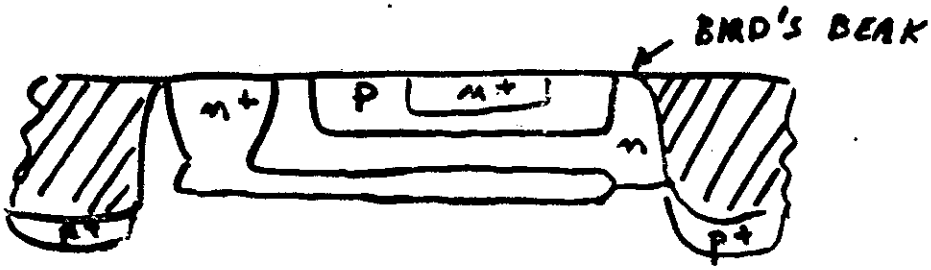
TRIPLE DIFFUSED



JUNCTION ISOLATED with buried layer



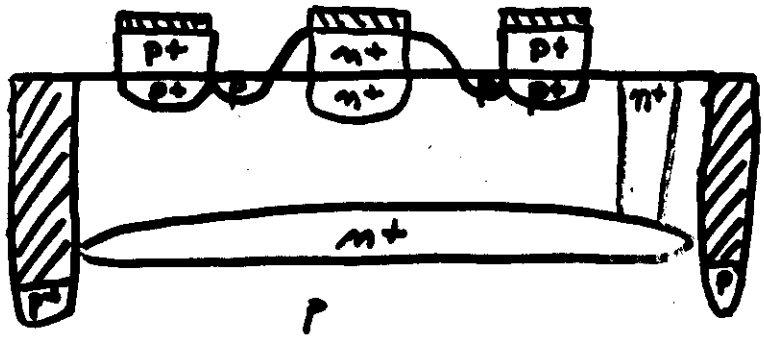
OXIDE - ISOLATED (LOCOS STYLE)



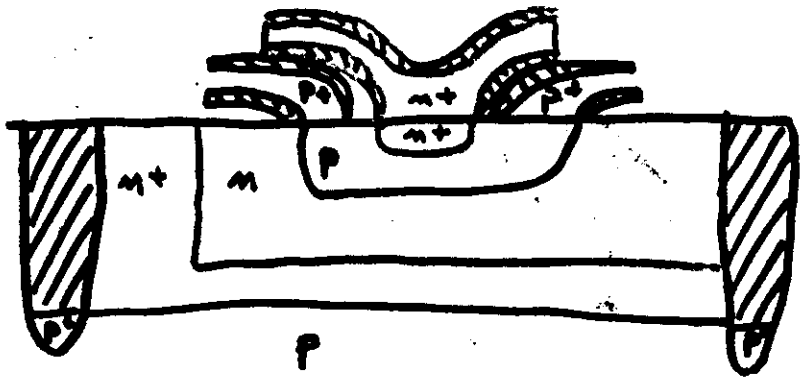
Bipolar Today (add. topics)

- Poly emitters
- Trenches

SINGLE POLY



DOUBLE POLY



Basic operation

Base-emitter forward biased

Base-collector reverse biased

$$I_c = \frac{q D_n n_i^2 A_e}{N_A W_b} e^{\frac{q V_{be}}{kT}}$$

for circuits: $I_c = I_s e^{\frac{V_{be}}{V_T}}$ $\qquad V_T = \frac{kT}{q}$

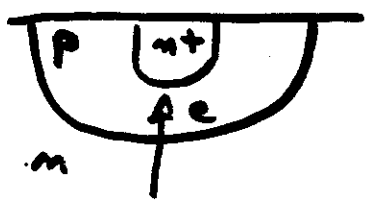
V_T	Temp °C
23.5	0
25.9	27
30.6	85
34.3	125

$$\beta = \frac{I_c}{I_B}$$

Bipolar device (cont'd)

SATURATION ⇒ C·B junctions are forward biased

The upward acting trs



It works the same way as the down trs, but smaller β because of area mismatch (can be 5 ~ 10)

When saturation starts ? When there is an appreciable current

$$\frac{i_{up}}{i_{down}} \simeq e^{-V_{cc}/V_T}$$

So V_{bc} can be positive (400 mV or less) without serious problems ("soft saturation")

Additional charge stores in the base of the device

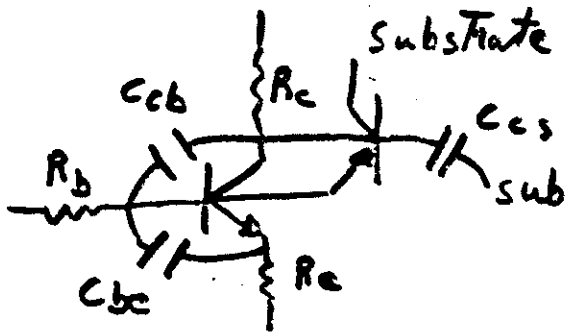
It should be avoided ! !

NORMAL $Q = i_c \cdot \tau_F$

SATURATION $Q = i_{ip}\tau_{up} + i_{down}\tau_{down}$

$i = i_{down} - i_{up}$

$\tau_{up} >> \tau_{down}$



TODAY'S TYPICAL VALUES

C_{eb} 6-8 fF

C_{bc} 8-12 fF

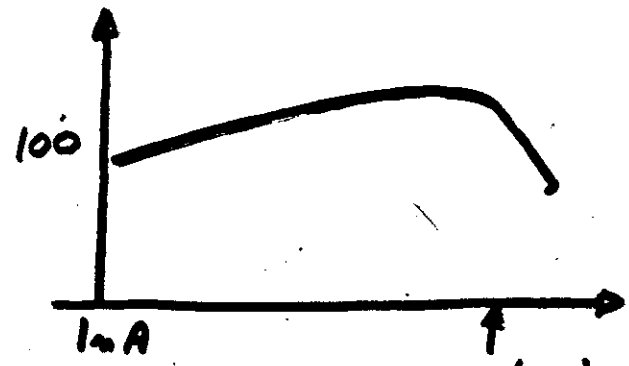
C_{cs} 25-30 fF

Bipolar (and Imp)

$$f_T = \frac{1}{2\pi\left(1+\frac{C_{je}+C_{jc}}{g_m r_p}\right)\tau_F} \simeq \frac{1}{2\pi\tau_F} \qquad \tau_F \simeq 10\text{-}15\,ps$$

$\simeq$ 10-15 GHz typical

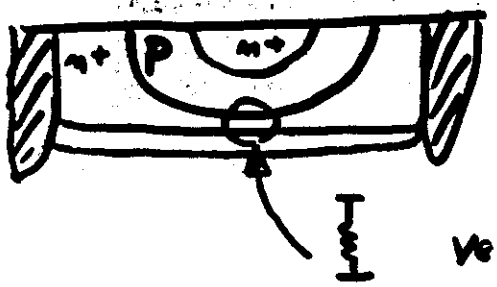
Beta



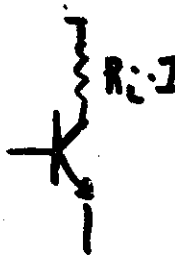
typical 200 μA/□μ current density

instead of e^{V/V_T} $e^{V/2V_T}$ 'high level injection'

Rc

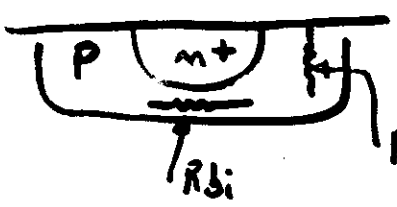


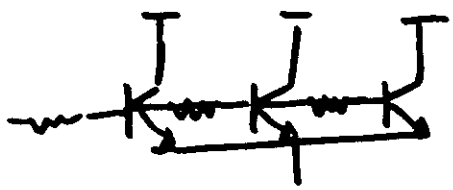
vertical part under emitter $R_c \simeq 80\text{-}100\,\Omega$



Big R_c easy saturation

$R_b = R_{bi} + R_{be}$ typical $\simeq$ 200-500 Ω/□





At higher current voltage drop

It will certainly be the tech. of the 90's, but only if there will be a different implementation in the Gate Arrays. (If 2 bipolar trs are used in each cell, then too much wasted area)

2 ways to apply BiCMOS

) Large-Swing (CMOS like)

) Small-Swing (ECL like)

arge number of possible GOOD circuits !!

Good properties of bipolar

) High i/area

) high i/cap

) good matching

) high gain/gm

Watch out for:

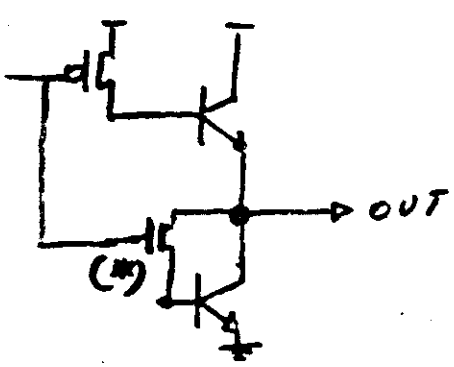
1) Saturation

2) Voltage drop

3) Noise

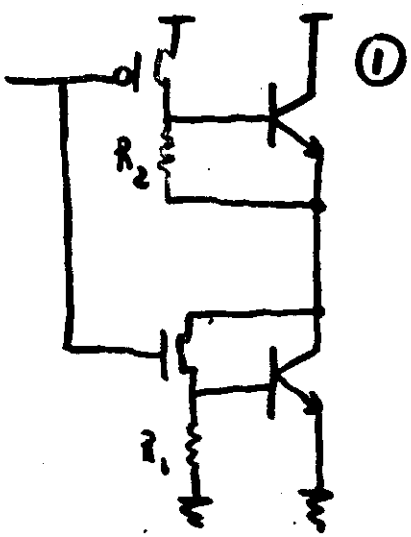
4) High current effects

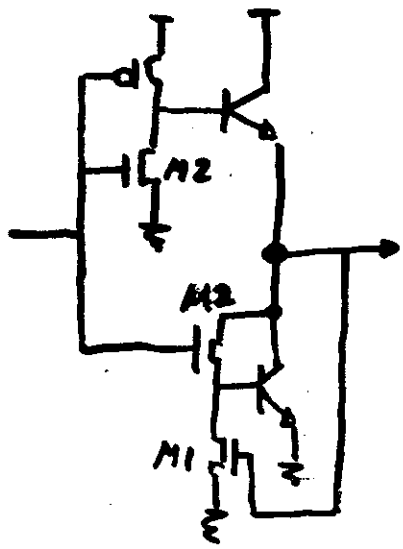
The classical circuit



(*) Keeps the bipolar out of saturation

Other options: (to turn off bipolar when not active)





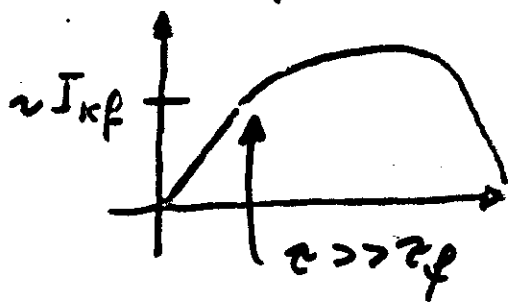
& R_2 large so they
n't steal too much
rrent but need to keep
vice off

M_1 small compared to M_3
M_2 small

What side bipolars?

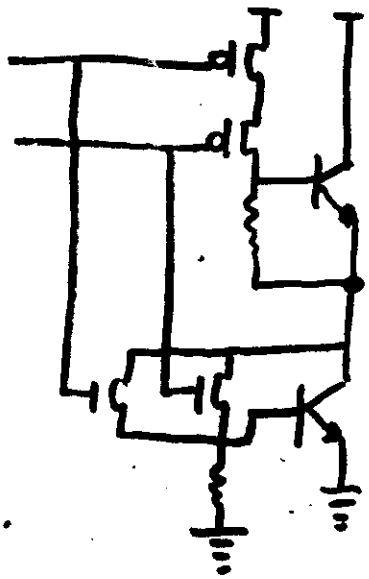
Larger ⇒ more area
more cap.
more current

$I \propto e^{V/V_T}$ but.....
after a point fts falls apart



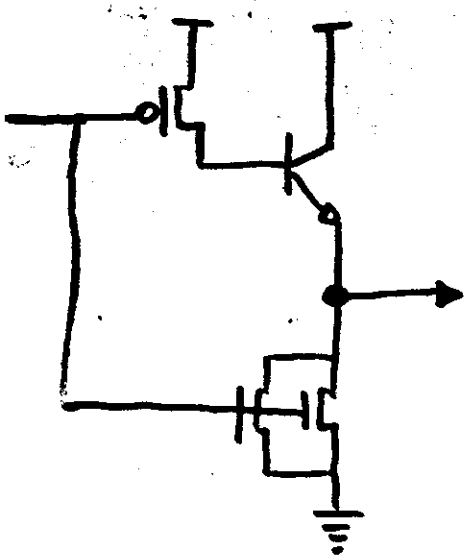
BiCMOS (addendum #3)

A BiCMOS buffer can do logic too:



NOR Implementation

Why should we use 2 bipolars in each cell?

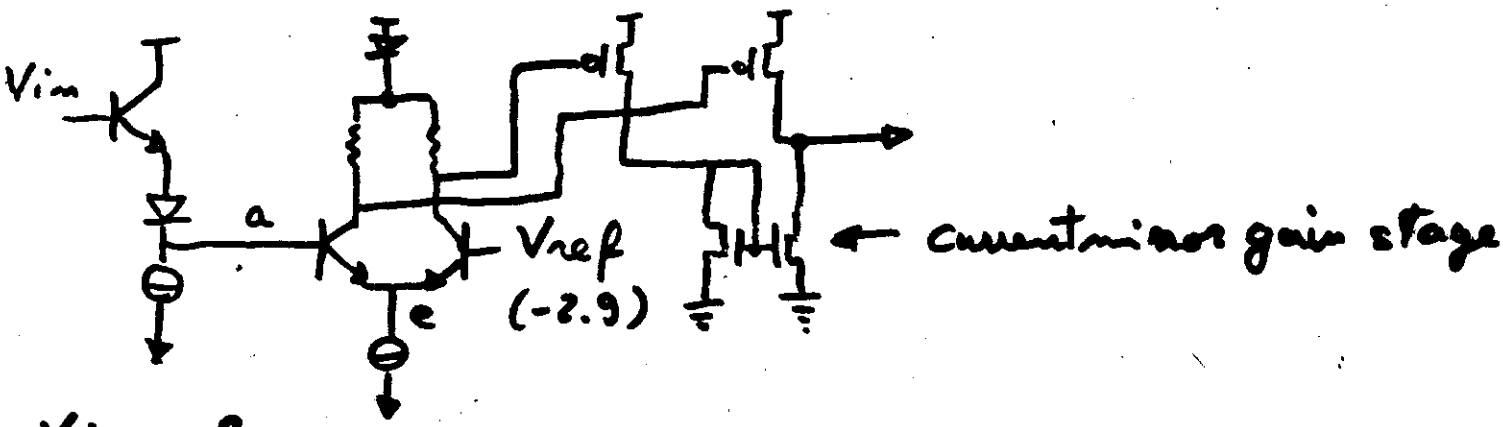


Only ↗ improved by the bipolar. ↘ is good enough in many cases.

In a gate array implementation, this saves a lot of space. But if we have a very large capacitance?

Level conversion

Basic Idea (Hitachi)



$V_{in} = .9$
$V_a = -2.5$
$V_e = -3.7$

From Addison-Wesley
VLSI Systems Series
listing:

- Analog VLSI and Neural Systems by Mead, 1989
- Computer Aids for VLSI Design by Rubin, 1984
- Principles of CMOS VLSI Design: A Systems Perspective by Weste and Eshraghian, 1985
- The Design and Analysis of VLSI Circuits, by Glasser and Dobberpuhl, 1985.
- Introduction to VLSI Systems by Mead and Conway, 1980.