INTERNATIONAL ATOMIC ENERGY AGENCY
UNITED NATIONS EDUCATIONAL, SCIENTIFIC AND CULTURAL ORGANIZATION
INTERNATIONAL CENTRE FOR THEORETICAL PHYSICS
I.C.T.P., P.O. BOX 586, 34100 TRIESTE, ITALY, CABLE: CENTRATOM TRIESTE

UNITED NATIONS INDUSTRIAL DEVELOPMENT ORGANIZATION

INTERNATIONAL CENTRE FOR SCIENCE AND HIGH TECHNOLOGY
c/o INTERNATIONAL CENTRE FOR THEORETICAL PHYSICS 34100 TRIESTE (ITALY) VIA GRIGNANO, 9 (ADRIATICO PALACE) P.O. BOX 586 TELEPHONE 040-224572 TELEFAX 040-224575 TELEX 460449 APH I

SMR/542 - 7

ICTP-INFN
SECOND COURSE ON BASIC VLSI DESIGN TECHNIQUES
18 February - 15 March 1991

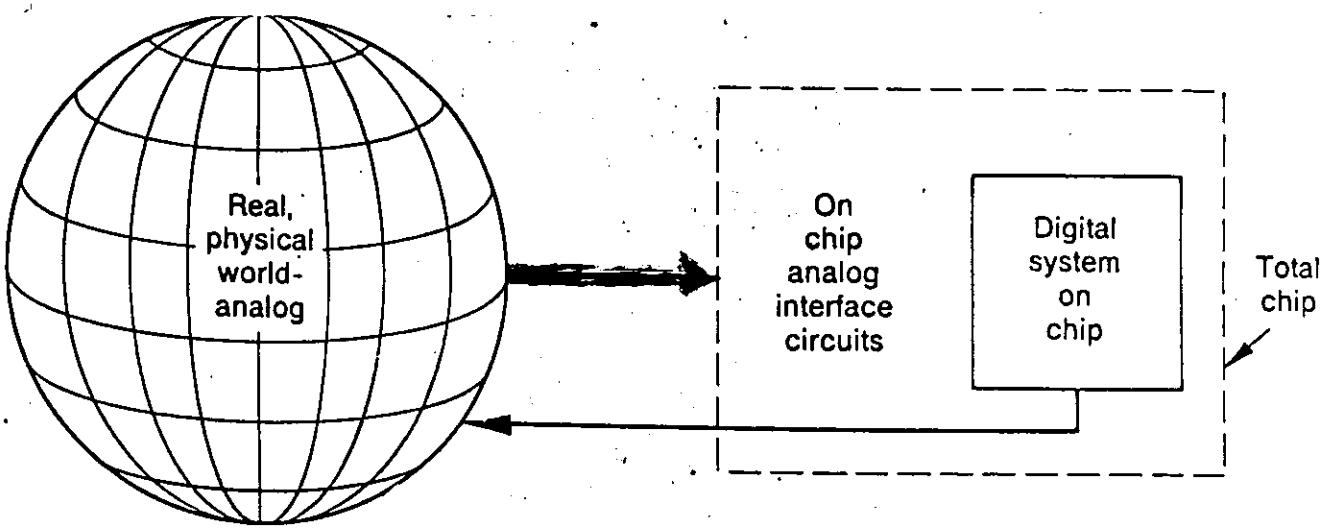
Analogue Integrated Circuits Technology and Design Techniques - Introduction -

Ignatius S.A. BEZZAM
Centre for Development of Advance Computing
Pune University Campus
Pune 411 007
India

Analog Integrated Circuits Technology & Design Techniques for Large Scale Integration

Ignatius S.A. Bezzam ,
Microprocessor Laboratory I.C.T.P. - INFN
email: bezzam@itsictp.bitnet

VLSI Design Centre (Dept. of Elec. Govt. of India)
Centre for Development of Advanced Computing
Pune - 411007 INDIA



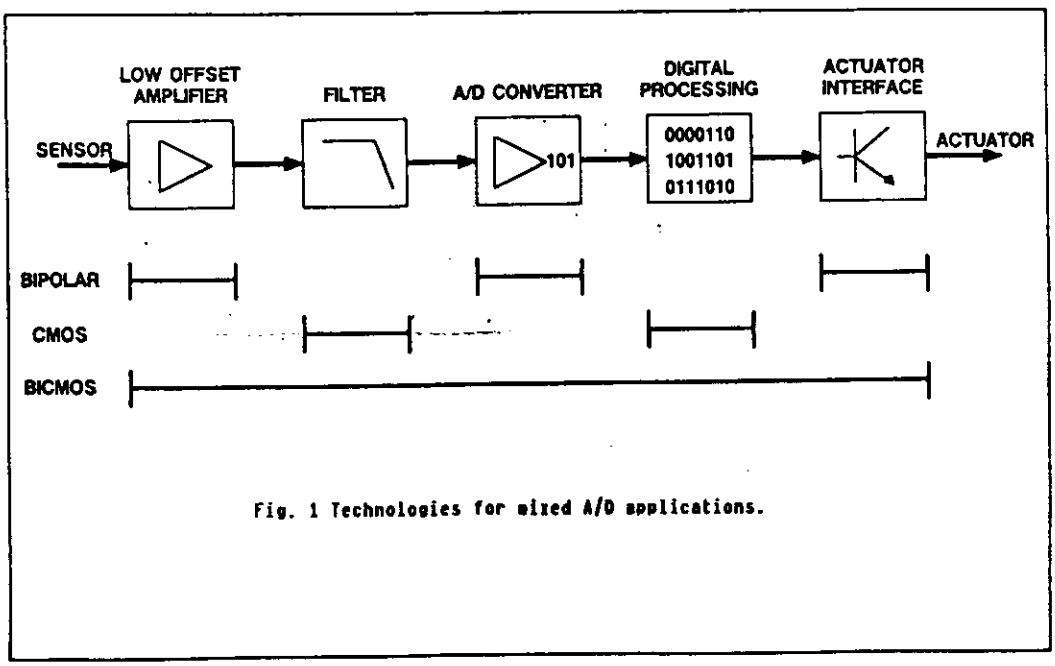
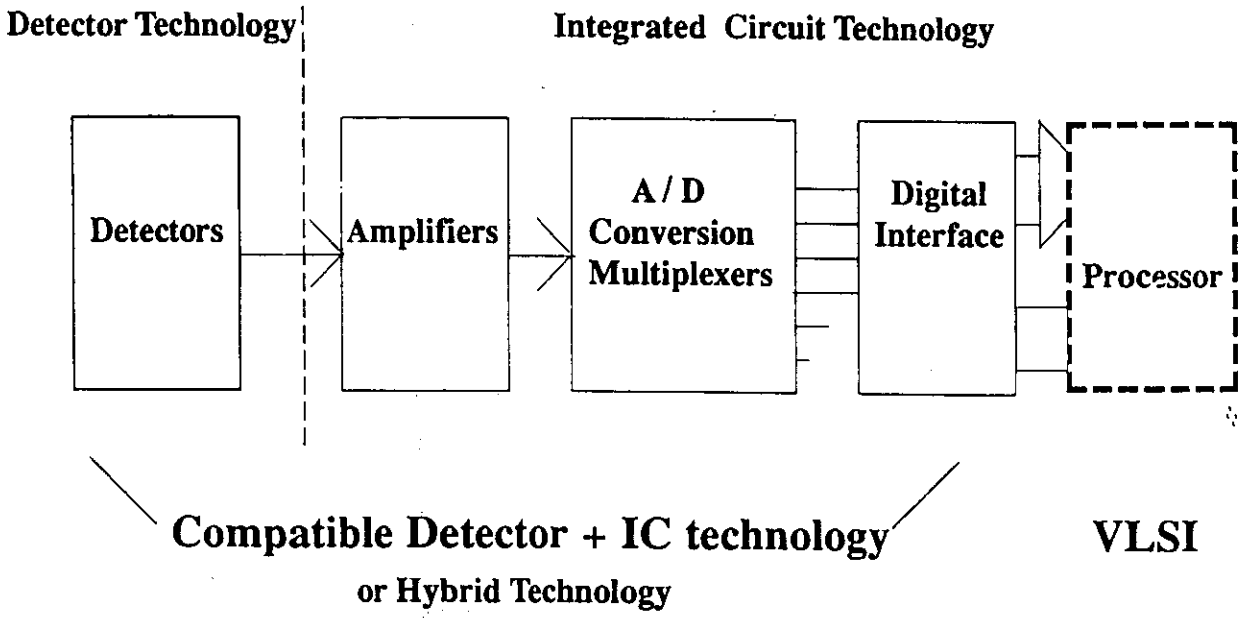


Fig. 1 Technologies for mixed A/D applications.



Analog Technology & Design Techniques
Requirements for Monolithic Integration

Scaling of operational devices -
to realize a large number of devices
on the same substrate

Isolation of the devices

Reliability & yield in production

Design Techniques
for (Very) Large Scale Integration

- Inductors can not be integrated
- Minimise the no. of passive components & values substitute resistors with active devices if possible.
- Active devices can be used in large numbers.
- Use ratio of parameters than absolute values
- Identify the really critical specifications to implement the right trade-offs
- If possible do the processing in Digital Domain

Ignatius S.A.Bezzam, ICTP'91

6

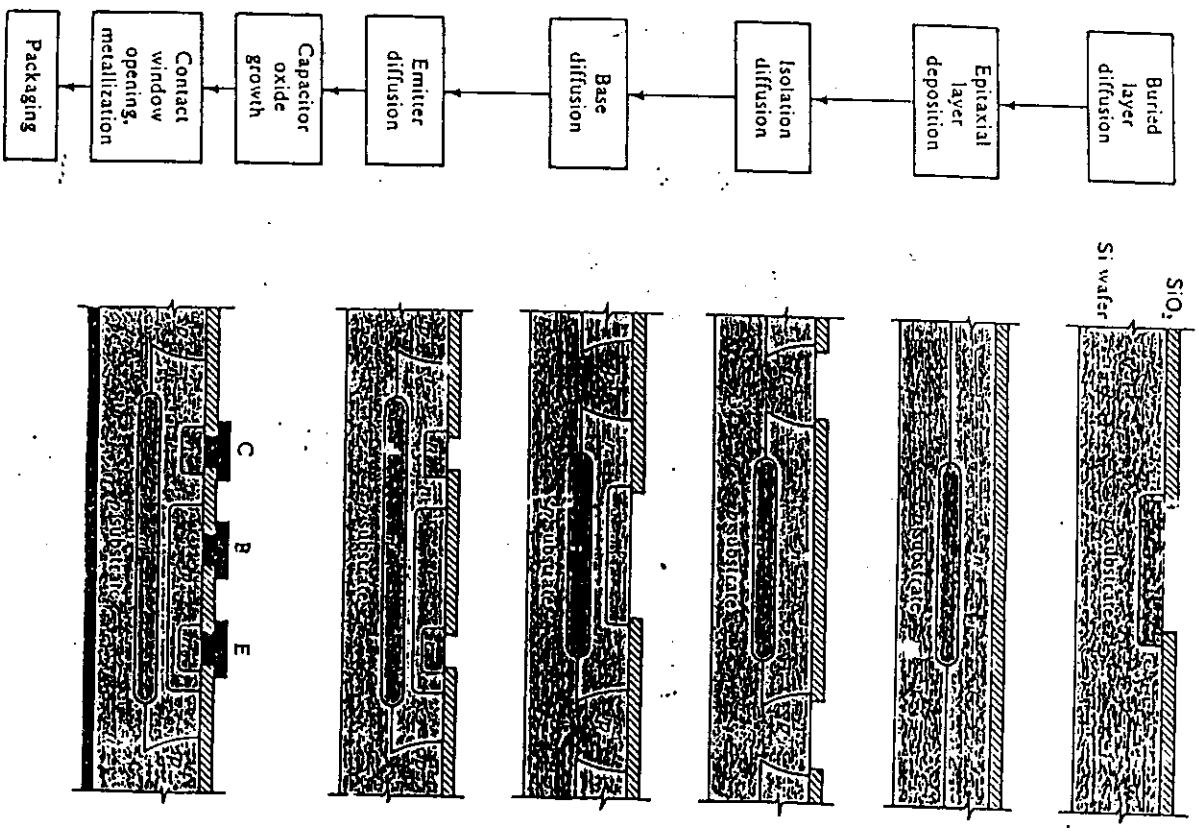


Fig. A.1 Standard bipolar integrated-circuit process.

7

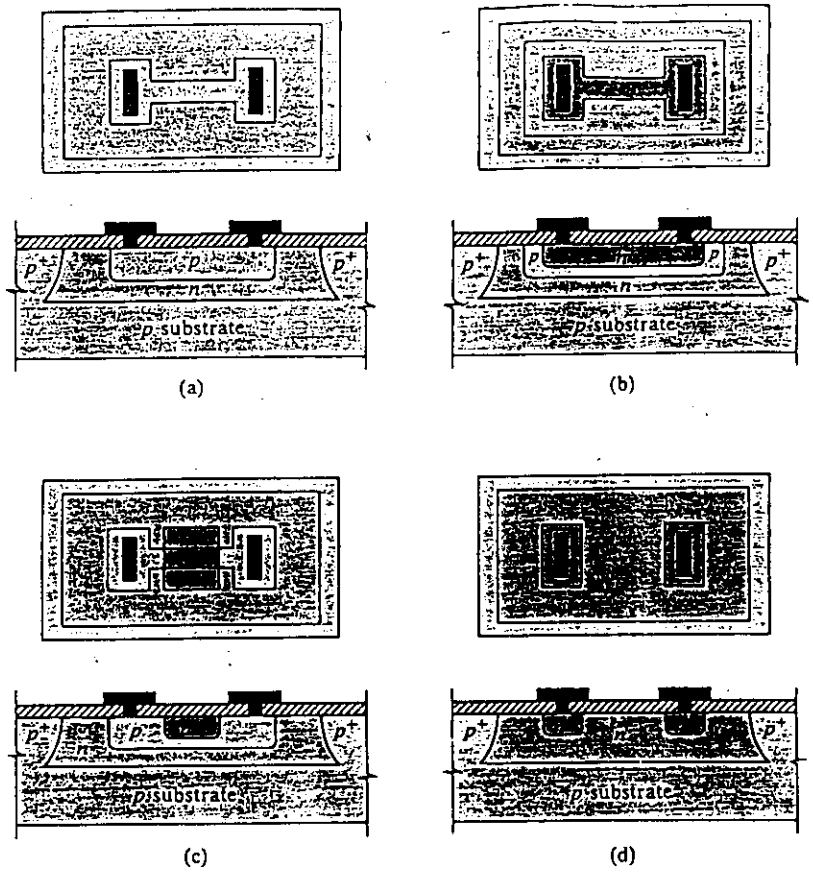


Fig. A.2 Integrated-circuit resistor structures. (a) Base resistor. (b) Emitter resistor. (c) Pinched base resistor. (d) Collector resistor.

Table A.1 DIFFUSED RESISTOR CHARACTERISTICS

	Resistor Type			
	Base	Emitter	Pinched Base	Collector
Range (ohms)	50–50 k	5–100	10 k–500 k	1 k–10 k
Tolerance	20%	20%	50%	50%
Matching	5%	5%	5%	5%
Temperature coefficient	0.1%/°C	0.2%/°C	0.5%/°C	0.8%/°C
Breakdown voltage (V)	40	6	6	70

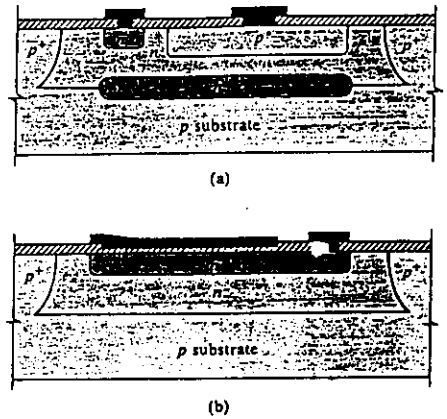


Fig. A.3 Integrated-circuit capacitor structures. (a) Collector-base junction capacitor. (b) Oxide capacitor.

Bipolar Junction Transistors

Three basic types of bipolar transistors are available: *npn*, *lateral pnp*, and *substrate pnp*. The *npn* structure is repeated in cross-section form in Fig. A.4. It has a beta typically of 100 to 500, a collector breakdown voltage of 40 V, and a cutoff frequency of 500 MHz. The normal operating-current range is from a few microamperes to

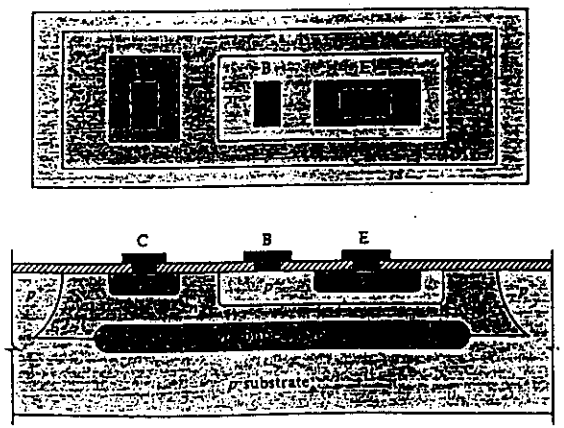


Fig. A.4 An *npn* bipolar transistor.

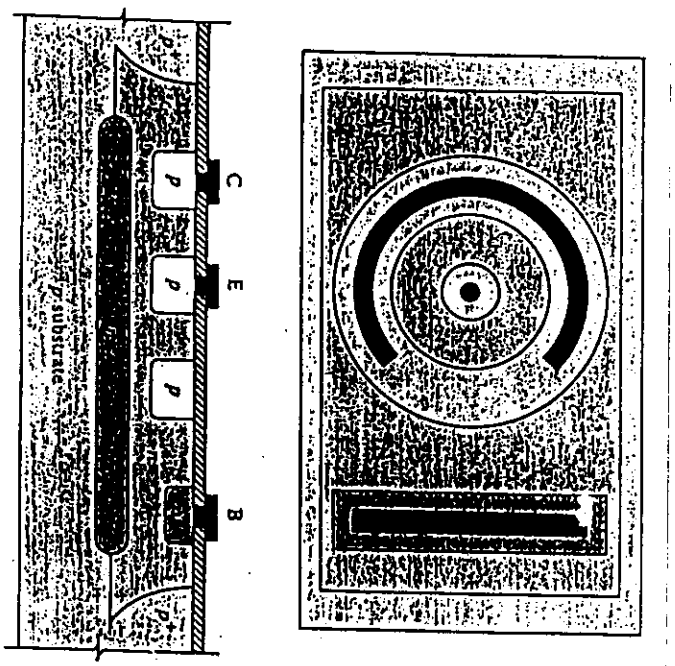
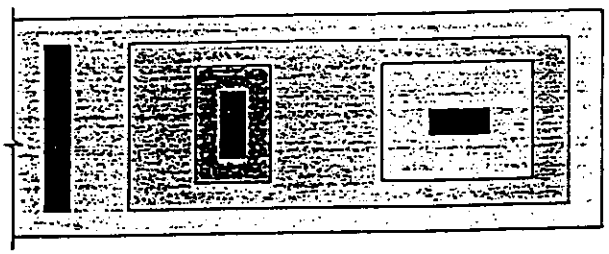


Fig. A.5 Lateral *pnp* bipolar transistor.



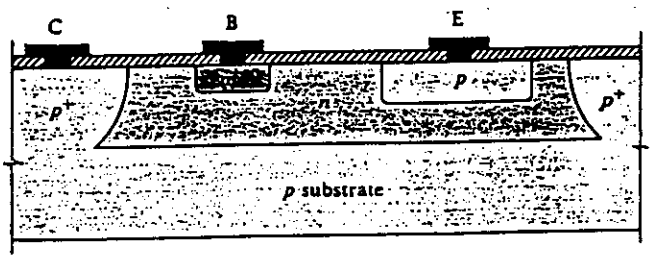
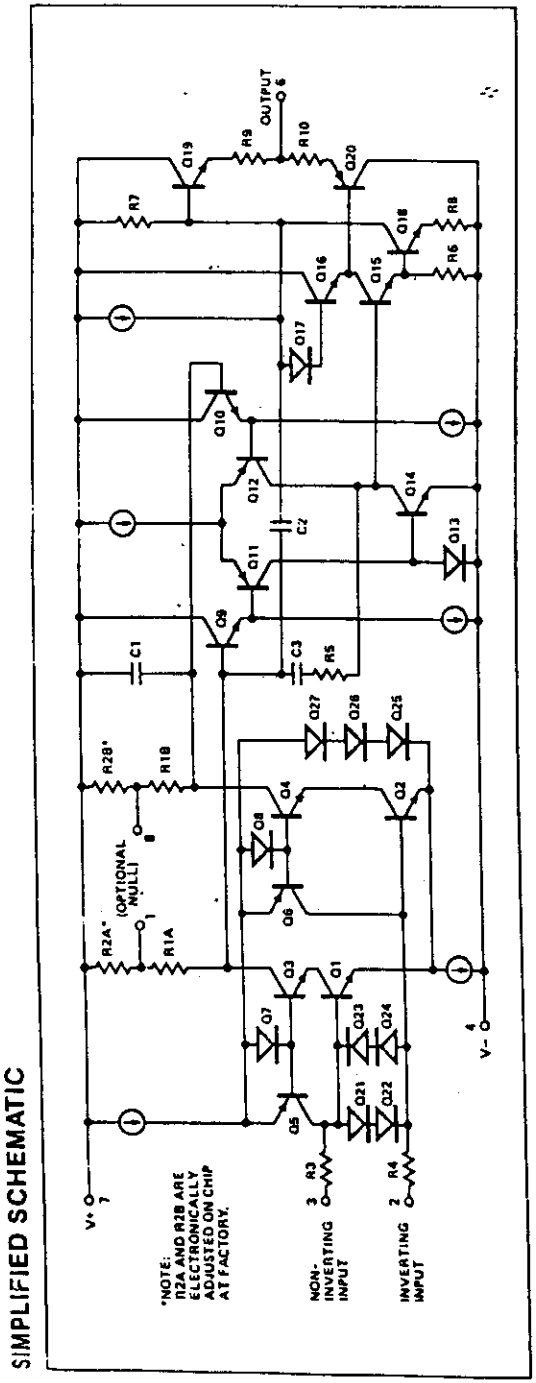


Fig. A.6. Substrate *pnp* bipolar transistor.

SIMPLIFIED SCHEMATIC



This preliminary product information is based on testing of a limited number of devices. Final specifications may vary. Please contact local sales office or distributor for final data sheet.

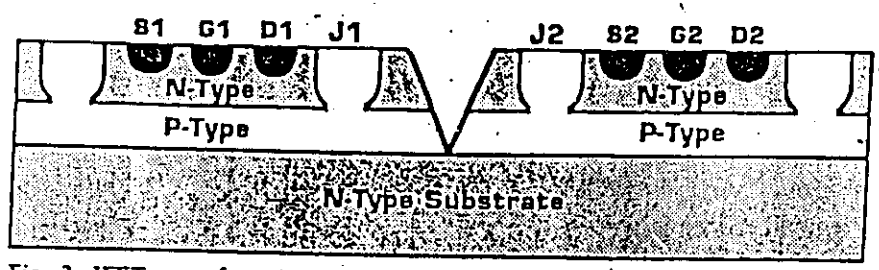


Fig. 3. JFET manufacturing process using double layer epitaxy and V-groove isolation.

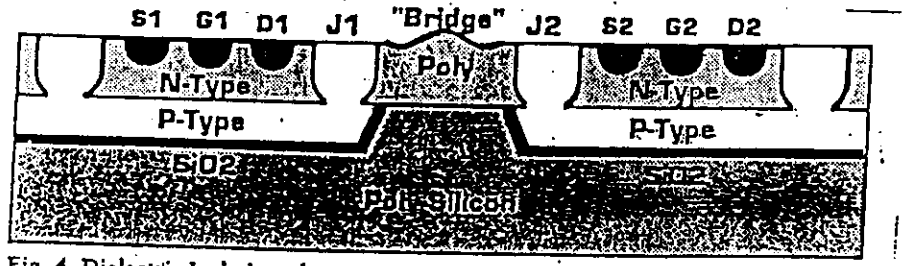


Fig. 4. Dielectric Isolation planar process.

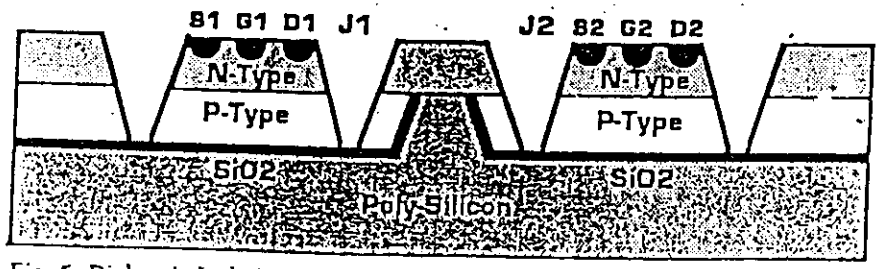
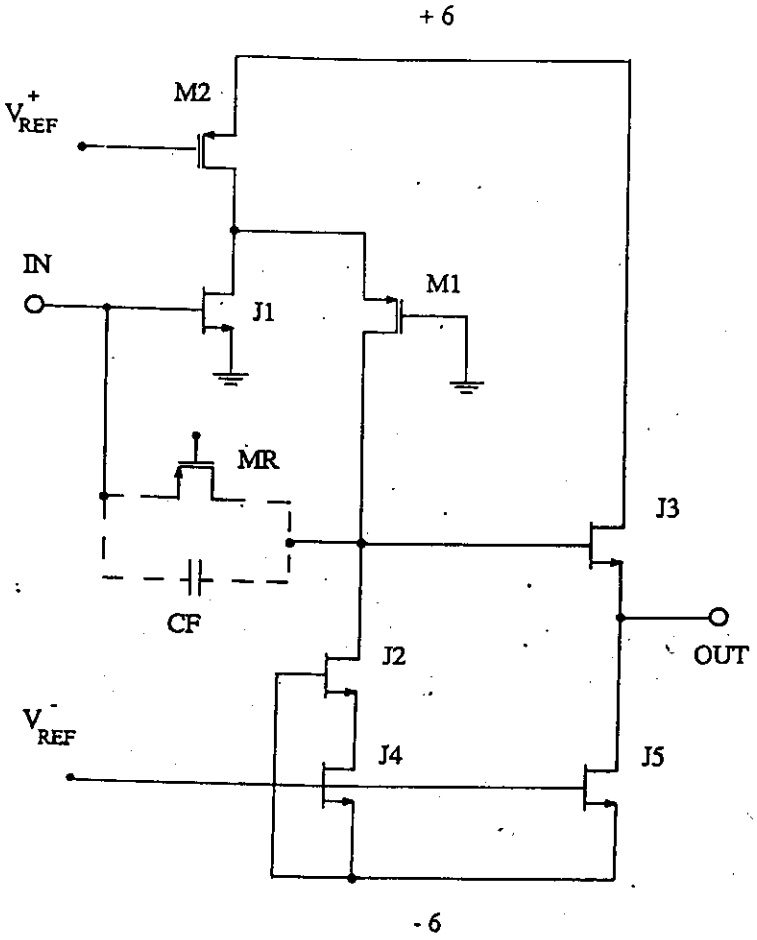
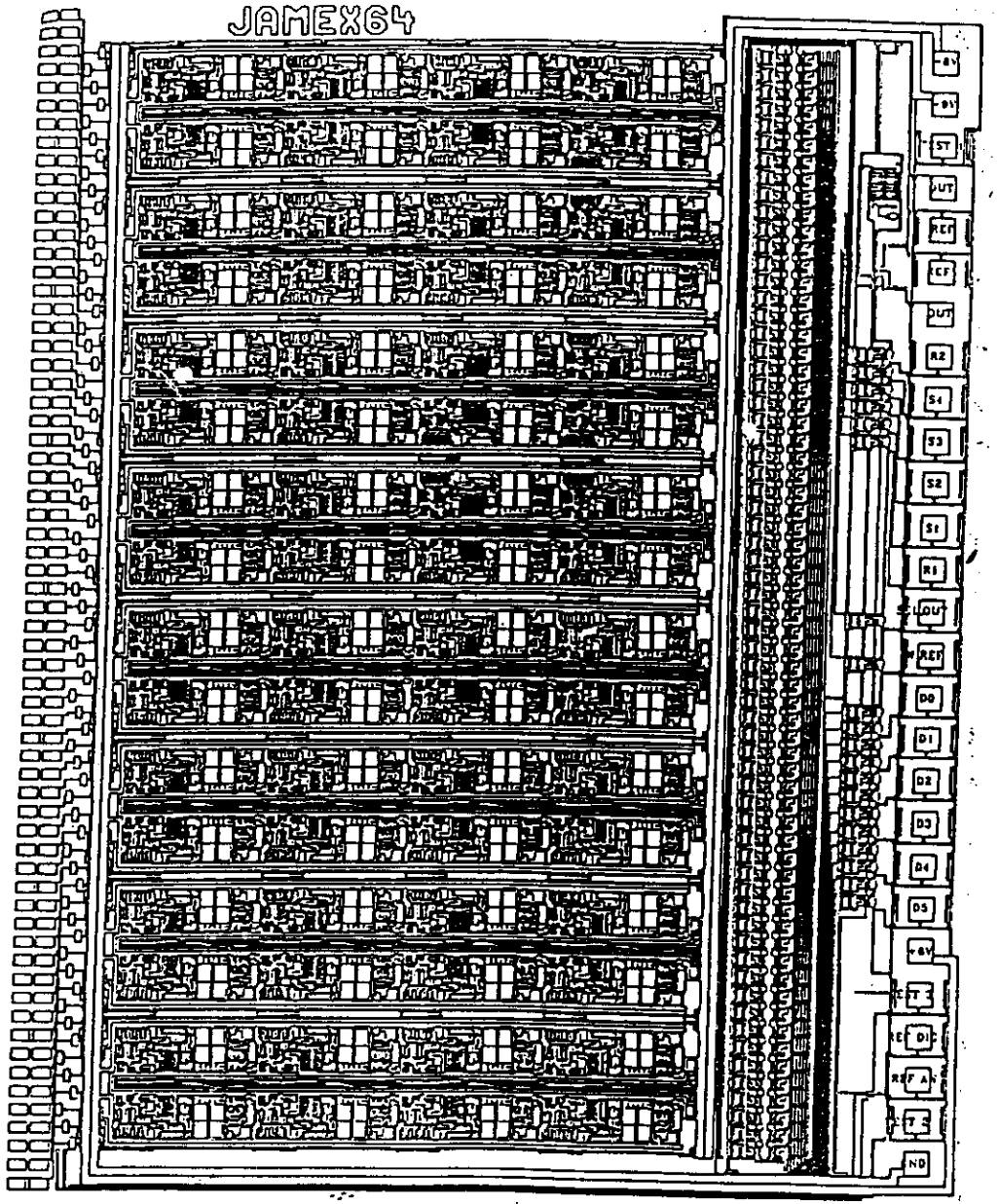
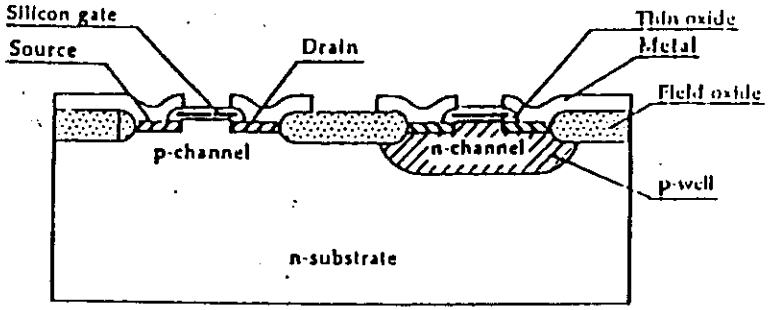


Fig. 5. Dielectric Isolation with single layer epitaxy. Mesa process, multiple tubs.

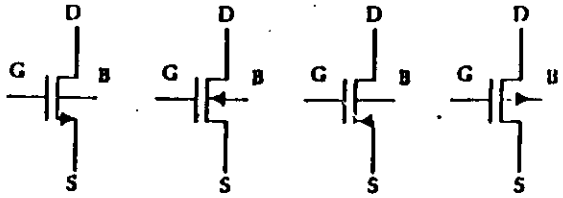

+ 6
M2
V_{REF}^{+}
IN
J1
M1
MR
J3
CF
J2
OUT
V_{REF}^{-}
J4
J5
- 6


JAMEX64

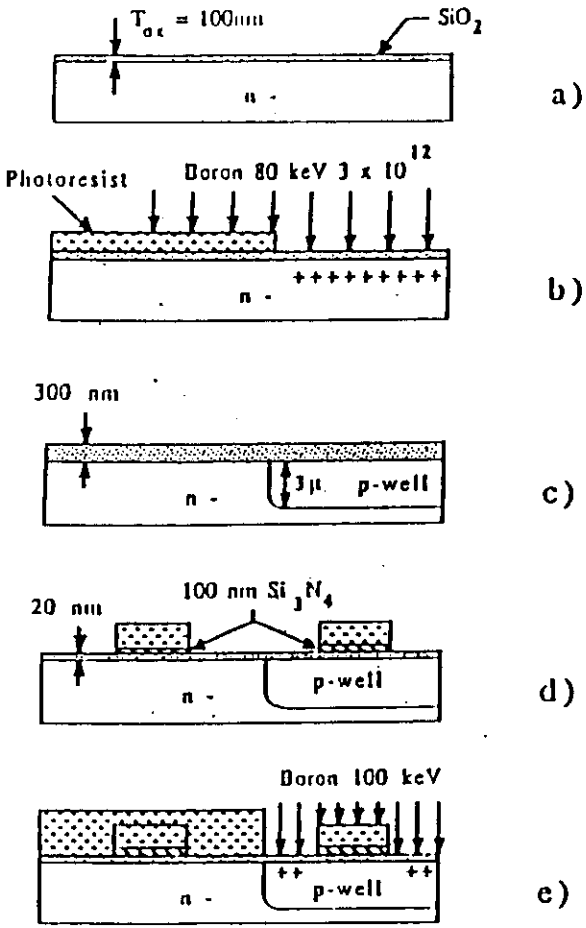
THE CMOS TECHNOLOGY

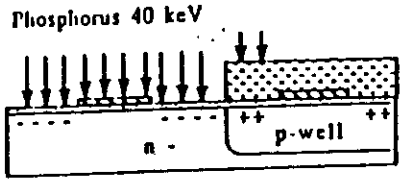


SYMBOLS OF THE MOS TRANSISTORS

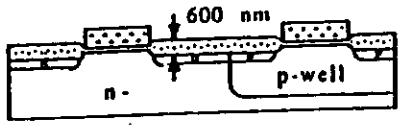


TYPICAL CMOS PROCESS

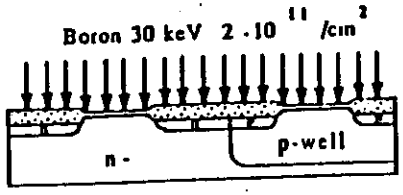



Phosphorus 40 keV
n -
p-well
++
++

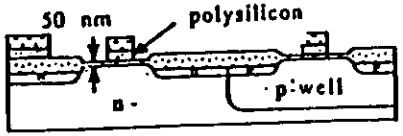
f)


600 nm
n -
p-well

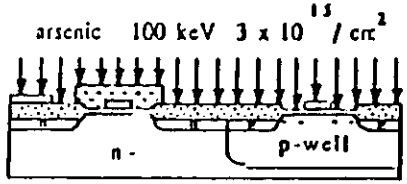
g)


Boron 30 keV 2 -10 11 /cm 2
n -
p-well

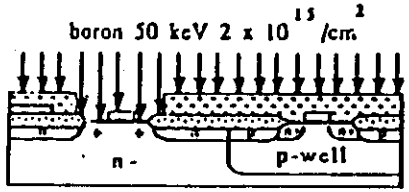
h)


50 nm
polysilicon
n -
p-well

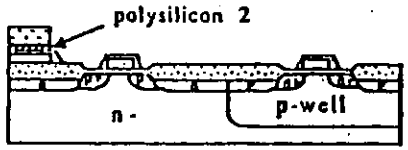
i)


arsenic 100 keV 3 x 10 15 / cm 2
n -
p-well

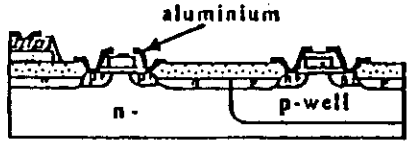
j)


boron 50 keV 2 x 10 15 /cm 2
n -
p-well

k)


polysilicon 2
n -
p-well

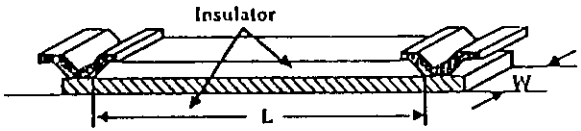
l)


aluminium
n -
p-well

m)

TYPES OF INTEGRATED RESISTORS

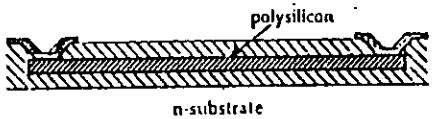
A resistor is made of a strip of resistive layer.

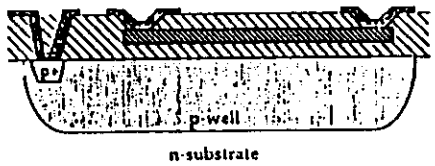


$$R = 2 \cdot R_{cont} + R_{\square} \frac{L}{W}$$

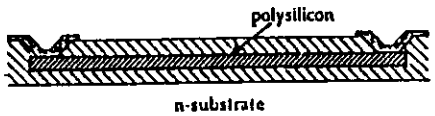
Type of layer	Sheet res. Ω/□	Accuracy %	TC ppm/°C	VC ppm/V
n+ diffusion	30-50	25-50	200-1K	50-300
p+ diffusion	50-150	25-50	200-1K	50-300
n-well	3K-5K	25	5K	10K
pinched p-well	5K-10K	50	10K	20K
pinched n-well	1K-3K	25	5K	10K
p-well	3K-6K	50	10K	20K
first poly	40-60	50	500-1.5K	20-200
second poly	25-40	50	500-1.5K	20-200

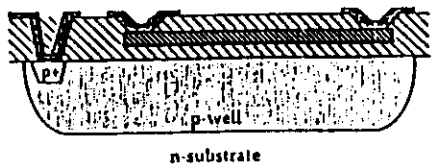
First poly resistance





Second poly resistance

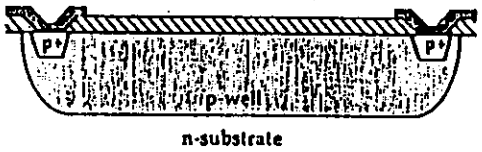




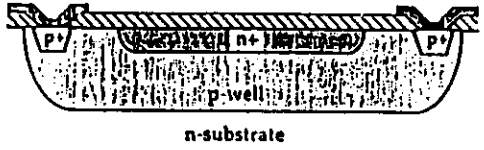
Types of resistances:

Diffused resistance

p-well (or n-well) resistance



Pinched p-well (or n-well) resistance



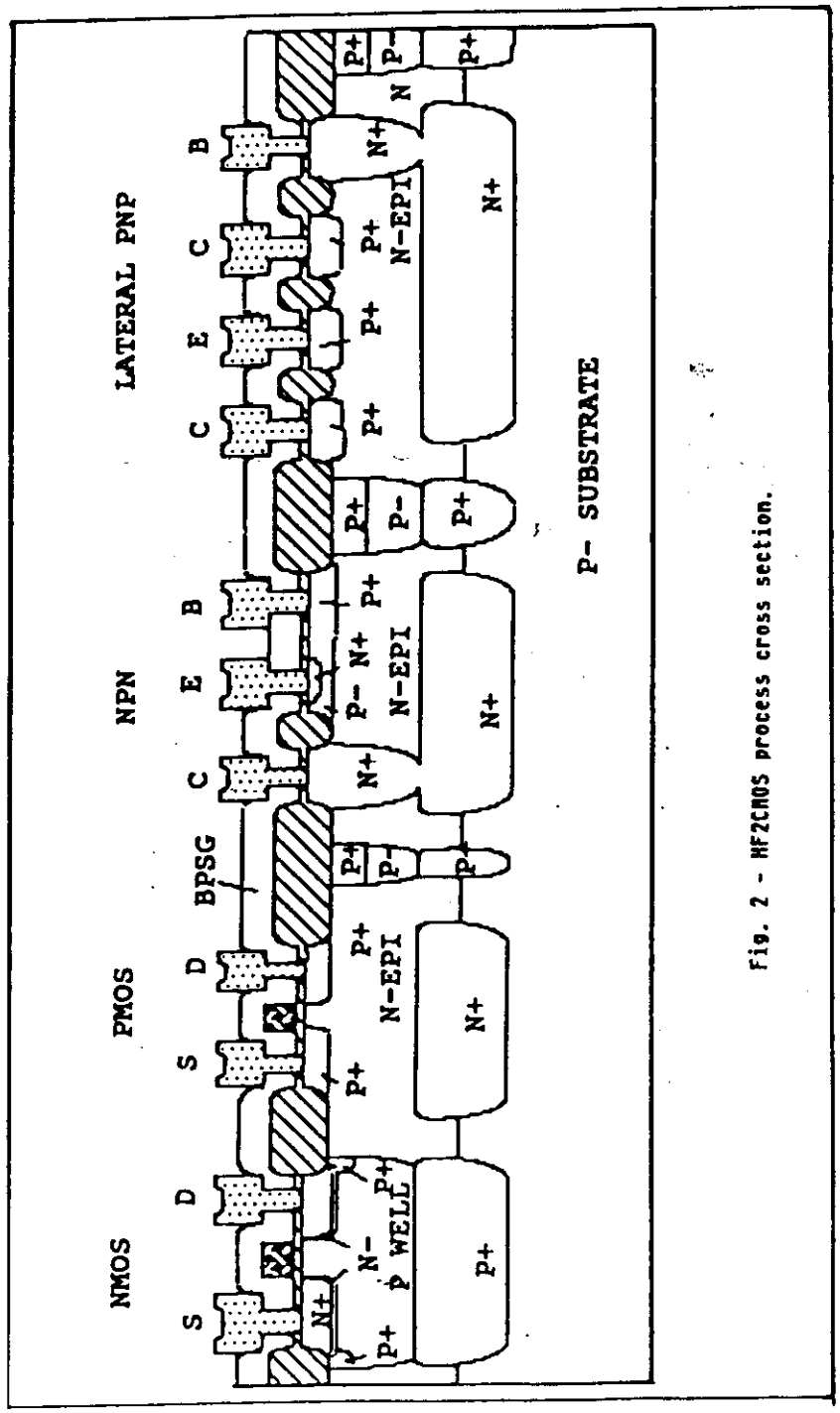


Fig. 2 - HF2CMOS process cross section.

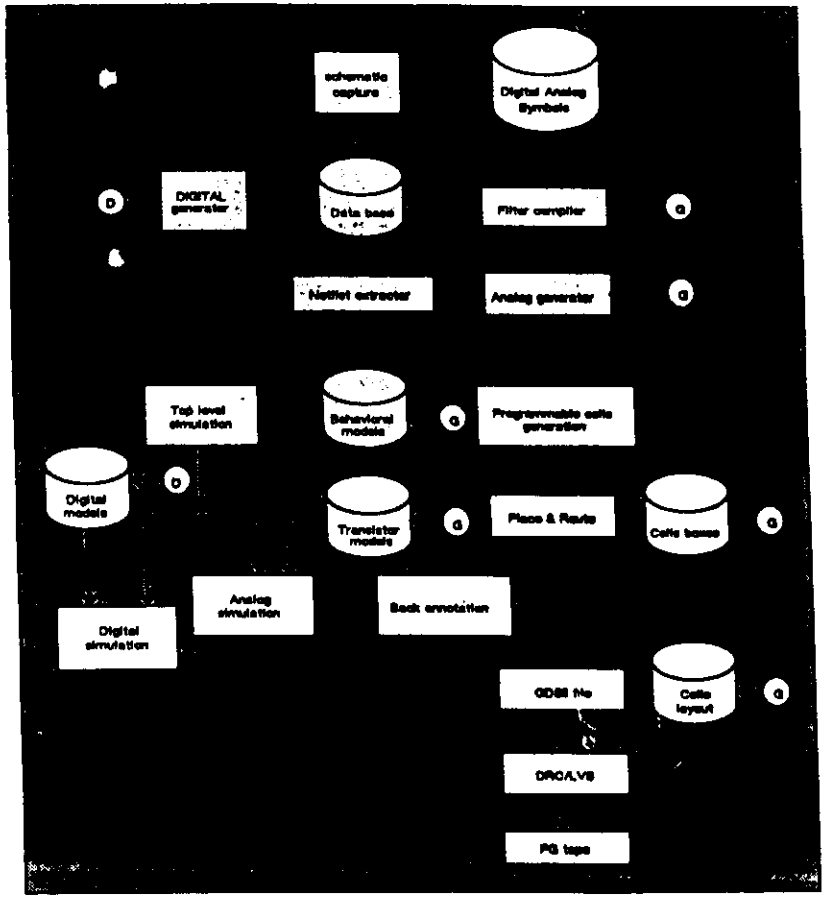


Fig.5 - A.D.S (Analog Design System) design flow.

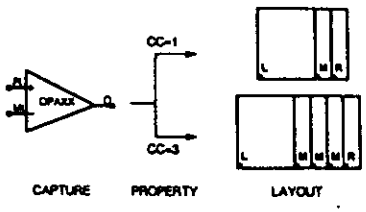
ANALOG LIBRARY AC ELECTRICAL CHARACTERISTICS ABSTRACT

Cell code	Description	Parameters Test conditions	Min	Typ	Max	Unit
CMP11	Static CMOS comparator	Propagation delay (overdrive = 5 mV) Offset		1 +/- 3	1.4 +/- 10	µs mV
CMP31	Static BICMOS comparator	Propagation delay (overdrive = 5 mV) Offset		90 +/- 2	110 +/- 7	ns mV
CPX11	Capacitor fields	Unit capacitance Capacitor value range Absolute accuracy Matching (capacitor ratio)	0.1	0.1 0.5	 50 +/- 15 1.0	pF pF % %
CPP11	Monolithic capacitor	Capacitor range Absolute accuracy	1		100 +/- 15	pF %
RPM/PPM	Resistor/Potentiometer P - Base	Resistor value range Absolute accuracy Matching Temperature coefficient Voltage coefficient	6.5		3000 +/- 20 +/- 1 0.2 0.05	KΩ % % % %
SW11	Analog switch	Elementary switch RON value Number of switches in parallel	1	5	25 3	KΩ
MN11	Telescopic NMOS transistor	RON value		100		Ω
OPA31	General purpose MOS Operational amplifier	Unity gain bandwidth Current consumption Phase margin (C1 = 100 pF, R2 = 10 KΩ) Offset		3.3 700 80 +/- 3	4.6 +/- 10	MHz uA ° mV
OPA41	Internal bipolar Op-Amp.	Unity gain-bandwidth current consumption Phase margin (CL = 15 pF, RL = 100 KΩ) Offset		9 240 62 +/- 1	40 +/- 5	MHz uA ° mV
OPA71	Rail to rail external MOS operational Amplifier	Unity gain bandwidth Current consumption Phase margin (CL = 100 pF, RL = 100 KΩ) Offset		2.3 380 80 +/- 3	 +/- 10	MHz uA ° mV
OTA11	MOS transconductance amplifier	Unity gain-bandwidth (CL = 2 pF)		24		MHz
POR11	Programmable power or Reset	Active level accuracy Hysteresis accuracy			+/- 5 +/- 5	% %
VRF11	Voltage bandgap reference	Output voltage accuracy Temperature coefficient Current consumption		 15	+/- 2 100	% ppm uA
OSC11	Programmable crystal oscillator	Frequency	0.1		20	MHz
OSC41P	RC oscillator	Frequency Stability versus temperature Stability versus voltage	1	100 0.01 0.5	800	KHz %/°C %/V
OSC31P	One pad I.C oscillator	Frequency Stability versus temperature Stability versus voltage	2	 0.01 0.5	200	KHz %/°C %/V
SCF	Filters	Order Center frequency	2		12 100	 KHz
ADC81	8 bit analog to digital converter	Conversion time Integral non linearity Differential non linearity			5 +/- 0.5 +/- 0.5	µs LSB LSB
DAC81	8 bit digital to analog converter	Conversion time (CL = 2 pF) Integral non linearity			1 +/- 0.5	µs LSB

TABLE 1 : STKM2000 Analog Library abstract

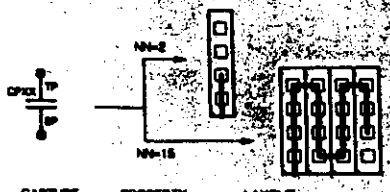
Fig. 4 : MIXED A/D LIBRARY MANAGEMENT

A - TELESCOPIC CELLS



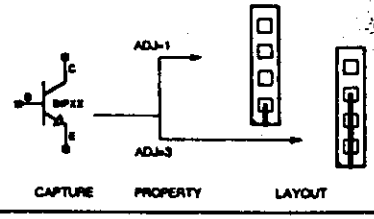
- Cell is compiled by abutment of subcells, selected among a library of leaf cells: one left-side subcell, then a given number of middle subcells, to reach the value selected by the property, and finely one rigth-side subcell.
- Concerned cells in STKM2000 library are: digital output buffers, operational amplifiers, monolithic capacitors, MOS transistors, ...

B - PARAMETRISABLE CELLS

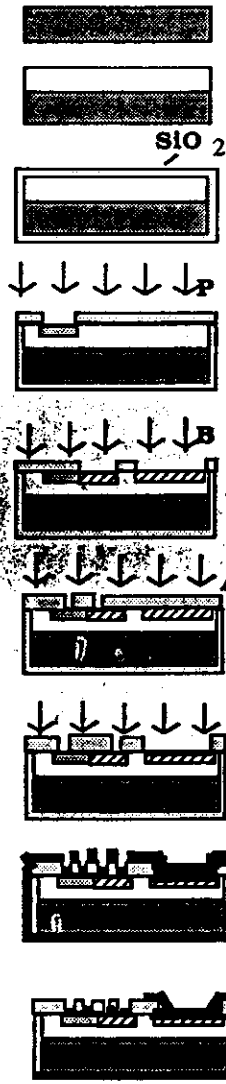


- An array of devices is compiled by abuttment of subcells. Some end cells are added at the right of the array to fit a grid multiple cell width.
- A metal line is added to customize this field of devices (like a gate array personalization) at the exact value.
- Concerned cells in STKM2000 library are: capacitance fields (3 different kinds) and resistance fields (5 different kinds).

C - ADJUSTABLE CELLS



- Personalization figures are added upon a predesigned cell to customize its functionality.
- Concerned cells in STKM2000 library are: bipolar transistors, switches, power-on-reset, pull-up and pull-down resistances, ...



n + Si -starting wafer

Epitaxial growth of Intrinsic layer 300-500µ,(5-6 hours)

Oxide passivation

Opening windows and N well implant

Oxide protection (not shown)

Opening windows and implant of P wells & Detectors Oxide protection

Opening windows and n+ implant (for circuitry)

Opening windows and p+ implant for circuitry & PIN structure

Al metallisation

Contact Mask Al pattern

Bulk contact

CONCLUSIONS

1. Analog Ic Design is strongly dependant on the IMPLEMENTATION-TECHNOLOGY and the choice of components available within

2. Design implementations use -
   Maximum no. of active components and minimum no. and value of passive compone

3. Design with ratio of parameters than absolute valu

4. Technological choices

   Bipolar, JFET } Bulk technology (LSI)
   Isolation problems.

   CMOS → "Surface technology (VLSI)
   Low power / lower performance of gain etc.
   Self isolated (sic)

   Bi CMOS → Largest range of options.
   Expensive.

   Special purpose CMOS → for low-noise applications high speed.

5. Design automation is minimal.
   Custom design more prevalent.

General information on foundries

1. MOSIS - Fast prototyping services for full custom VLSI
   Low cost (~$500 for 4 parts)
   (Available for users in USA) - 2 yr / 1 yr
   Information can be obtained without being user.
   Email to University of Southern California.
   Betnet: MOSIS %MOSIS.EDU@MOSIS.EDU
   Mosis currently offers low-noise analog process by ORBIT

2. ORBIT Semiconductor
   1230 Bordeaux Dr.
   Sunnyvale, CA 94089
   Tel: 408 744 1263
   ORBIT FORESIGHT PROGRAM - (low cost, fast turnaround)
   ~$1500 for 12 parts)
   No restrictions.

   Contact person: ALASDAIR DENTON-MILLER
   17 Bridge Street, Leatherhead, Surrey
   KT 22 8BL ENGLAND.
   Tel: (0372) 376848.

3. SGS-THOMSON Microelectronics
   Avenue de Martyrs
   Grenoble, FRANCE

   Powerful Bi-CMOS process and design automation tools.

4. INVOMEC - Belgium.