INTERNATIONAL ATOMIC ENERGY AGENCY
UNITED NATIONS EDUCATIONAL, SCIENTIFIC AND CULTURAL ORGANIZATION
INTERNATIONAL CENTRE FOR THEORETICAL PHYSICS
I.C.T.P., P.O. BOX 586, 34100 TRIESTE, ITALY, CABLE: CENTRATOM TRIESTE

UNITED NATIONS INDUSTRIAL DEVELOPMENT ORGANIZATION

INTERNATIONAL CENTRE FOR SCIENCE AND HIGH TECHNOLOGY
c/o INTERNATIONAL CENTRE FOR THEORETICAL PHYSICS 34100 TRIESTE (ITALY) VIA GRIGNANO, 9 (ADRIATICO PALACE) P.O. BOX 586 TELEPHONE 040-224572 TELEFAX 040-224575 TELEX 460449 APH I

SMR/542 - 8

ICTP-INFN
SECOND COURSE ON BASIC VLSI DESIGN TECHNIQUES
18 February - 15 March 1991

Additional material to lectures

by

Ignatius S.A. BEZZAM
Centre for Development of Advance Computing
Pune University Campus
Pune 411 007
India

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A HIGH FLEXIBILITY BICMOS LIBRARY FOR MIXED ANALOG/DIGITAL APPLICATIONS

1. INTRODUCTION :

Born as an extention of digital standard cells, mixed analog / digital standard cells have now reached a good maturity level. So it is possible today to mix on a same die analog functions with digital ones. As a result, integration density is increased, the number of external components and costs reduced. Some years ago, the only means to obtain analog functions on an integrated circuit was the full custom approach, only dedicated for high volume production.

To enlarge the use of analog in IC's, some linear standard cells appeared into digital CMOS libraries. But the use of such ones was quickly limited due to the lack of flexibility :
How to integrate resistors, capacitors or current of different values with standard cells ? How to integrate specific analog requirements with only a few standard cells ? This first step was jumped over with the introduction of programmable or parametrizable cell concept, managed by specific C.A.D tools : analog cell compilers or leaf cell compilers. Then the way was openned to design entirely an ASIC, from a standard library included into a safety design environement, implemented on a work station : Design flow fully checked from schematic capture to layout, by automatic C.A.D tools, without any manual operations during the design.
The TSGSM mixed analog digital CMOS library, with more than 250 cells, several of them programmable, allows to design most applications for all market segments.

A . D . S (Analog Design System) from SGS - THOMSON MICROELECTRONICS implemented on most popular engineering work stations is able to manage and help the user to design a chip with a high reliability level .
The next step was to increase the performances allowed by analog CMOS and yet improve the flexibility and the ergonomy of mixed A / D cell libraries. To achieve these goals, two strategic ways were choosen :
- First,the technology : the best way to mix high performance linear functions (accuracy, high speed, power) with a high digital integration density was to choose a BICMOS technology . A new innovative process , especially dedicated to mixed A / D applications was developped : HF2CMOS process (NPN - 6 GHz for bipolar and 1.5 µm channel length for CMOS, 2 poly, 2 metal layers).
- Secondly, the flexibility : several improvements had to be introduced to take into account more analog constraints : multi supply and power down capabilities, centralized biasing block automatically managed by C.A.D tools, simplified analog symbols, alternative cell management, more parameterized cells.
From these choices a new mixed A/D standard cell library was developped : STKM2000. It is a merge between two technologies (CMOS & BIPOLAR) and two worlds (analog & digital), which allows to cover all the range of analog functions from sensor to actuator in the data processing chain (Fig. 1), when implementing on a same die up to 10 K gates.

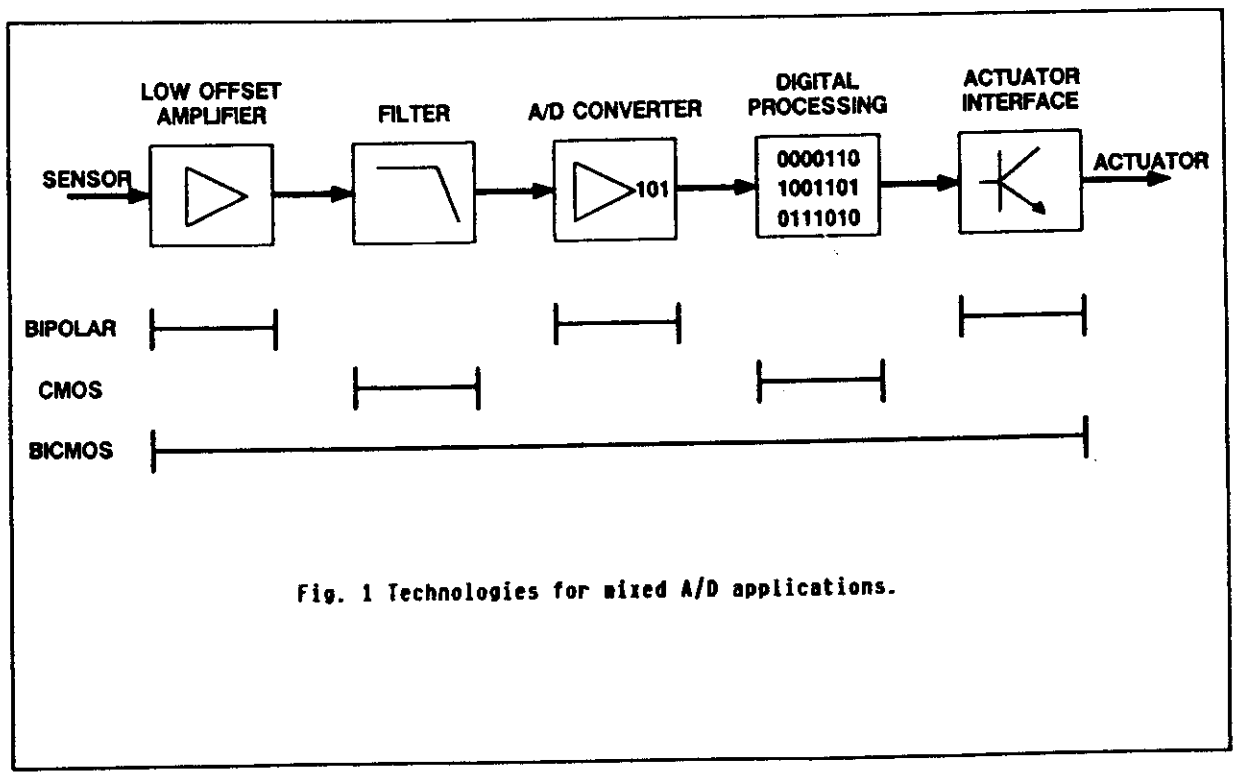


Fig. 1 Technologies for mixed A/D applications.

2. A NEW BICMOS PROCESS DEDICATED TO MIXED A/D APPLICATIONS.

The HF2CMOS process has been developped for mixed analog digital applications and has been optimized for telecommunication, video processing and analog semi-custom. It is a double poly, double metal Bipolar/CMOS technology. Five different kinds of transistors are available : NPN (15 V ; 6 GHz), lateral PNP (15 V ; 20 MHz), vertical PNP (15 V ; 2.5 GHz) , NMOS and PMOS. CMOS part is similar to a N well technology with the possibility to obtain isolated NMOS transistors. Two processes were optimized for 5 Volts and 10 Volts applications with only a different gate oxyde thickness. The minimum channel length in the 5 Volts process is 1.5 um. Concerning resistor possibilities, seven resistor types are available from 20 Ohms/□to 8 KOhms/□. It's also possible to implement two kinds of capacitors :
Poly/diffusion capacitor with a value of 500 pf/mm² and Poly/Poly capacitor with also 500pf/um². The technology has been optimized to reduce latch up phenomenon thanks to low resistive buried layers. The cross section of HF2CMOS process is given in Fig. 2.

3. STKM2000 DIGITAL LIBRARY.

In order to well adapt the library to the equipment needs, two digital libraries are available : one dedicated to 5 volts applications allows to achieve an operating frequency of 30 MHz. The second one is dedicated to 10 Volts applications when single supply and high voltage are requested. The choice between the two libraries is automatically managed by the C.A.D tools depending on supply voltage of the application. The digital library is composed of 60 internal hard macro cells (standard gates and flip flops, translators, multiplexers), several kinds of input or output buffers of which some of them are programmable depending on loads or current to deliver. In order to simplify the schematic capture of a digital system, a set of macro cell generators is available: N bits (synchronous) counters, N bits serial or parallel registors.Some others are under development and will be soon available: SRAM, ROM and PLA macro block generators.

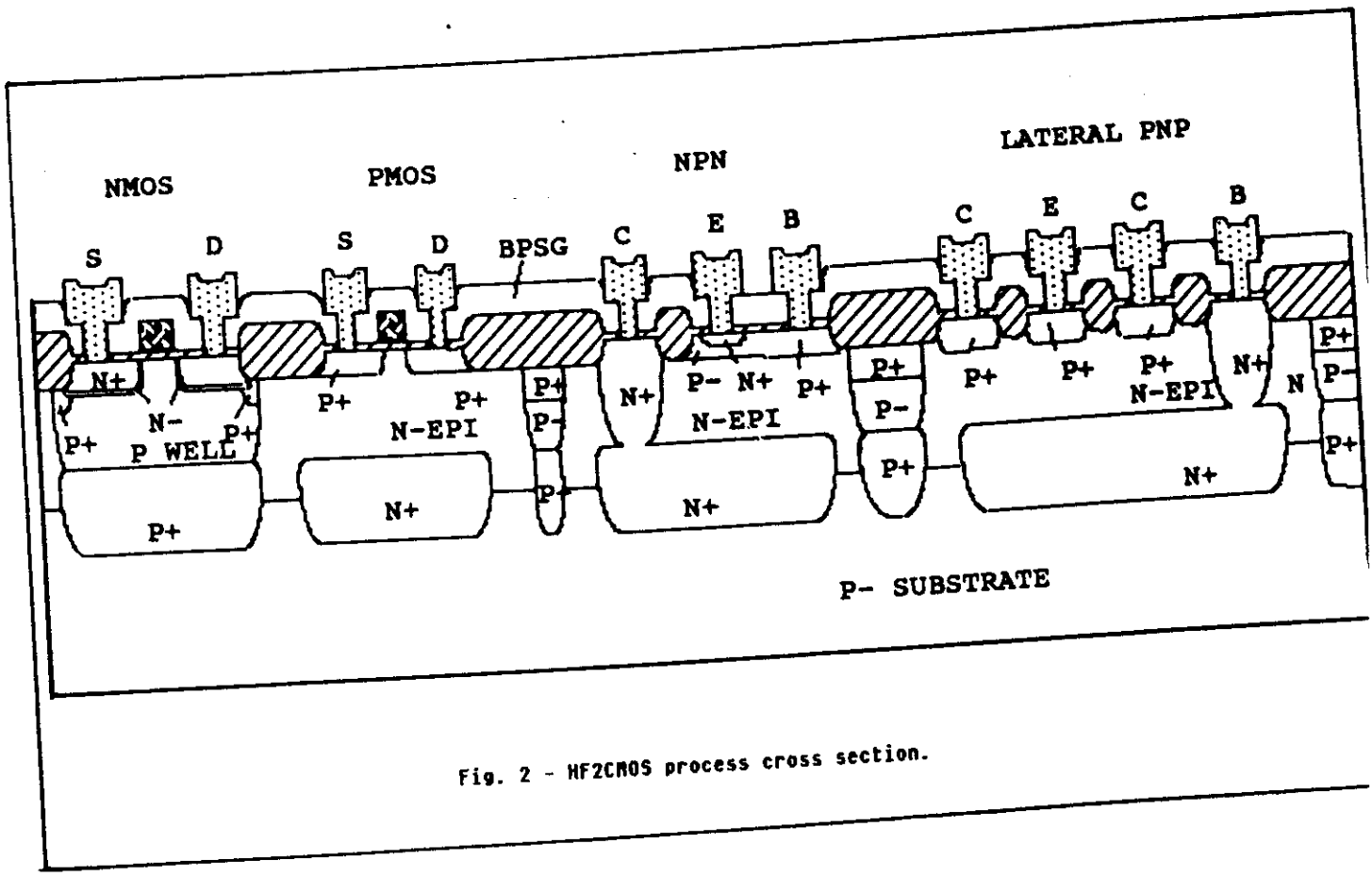


Fig. 2 - HF2CMOS process cross section.

STKM2000 ANALOG LIBRARY :

The analog part of STKM2000 library has been built from a basic principle : to offer a maximum flexibility, for a large range of applications. To achieve this goal, cell programmation has been widely used in most of analog cells. The programmation is used at different levels, from the programmation of a resistor value,to a filter compiler, passing through leaf cell compilation. Everything is ajustable step by step : resistors, capacitors, current values, power consumption, supply voltages, operationnal amplifiers features, comparator speed.. Even the amplifier phase margin can be ajusted, if needed, depending on the application. This intensive use of programmation allows to have the possibility of a full custom approach, with the safety and low turn-around time of a semicustom design. Programmation values captured during the schematic phase with attributes, are managed by an integrated C.A.D tool that checks all property values and automatically generates the user-required cell.

On the electrical point of view, the analog library takes advantages of BICMOS technology : for a high speed or low offset amplifier, bipolar transistors are used. For a high input impedance amplifier, CMOS input transistors are choosen. For some other applications the use of bipolar and MOS transistors into a same schematic is widely used. While CMOS is required for analog switches, multiplexor or S.C filters, bipolar transistors are essential for bandgap reference voltage, low noise amplifiers or output current drivers : the merge between bipolar and CMOS offers new schematic possibilities for analog functions.

Most of the analog library operates from 2.7 V to 11 V. All analog functions own a power down mode, and the possibility of power consumption adjustement. Biasing current or voltage, requested by analog functions, are automatically managed by C.A.D tools from a property. An other important feature of this library is the possibility to automatically manage the multi-supplies and then, it is possible to easily separate supply rails between different blocks in a same chip, thus reducing crosstalk : one more time, it is a global property which fixes the supply voltage for a part of a subcircuit, in the schematic capture.

An example of schematic capture with all component properties is given in Fig. 3 (simple triangular / square wave generator).

An analog library would have not been completed without macro-functions such as converters and filters. STKM2000 includes such functions : a switched capacitor filter compiler allows to generate any kind of filter up to twelfth order.From the specification up to the layout and simulation models, all the tasks are taken into account into the compilation procedure. Typical achievable toff frequencies are 150 KHz. With the possibility to design a low pass, high pass, band pass, band reject, all pass resonators with any kind of mathematical approximations, this compiler is one of the most powerfull of the world. The layout of this macro-block includes transconductor biasing block and 4 phases non-overlapping clock generator.

Concerning convertors, an 8 bit A/D and D/A convertors operating respectivily at 200 KHz and 1 MHz will be introduced at the end of the year. 12 bits A/D and D/A self calibration converters are under developpement.

8 bits video converters will be introduced next year, at the same time than video amplifiers and comparators.

An abstract of the STKM2000 analog library is given in table N°1.

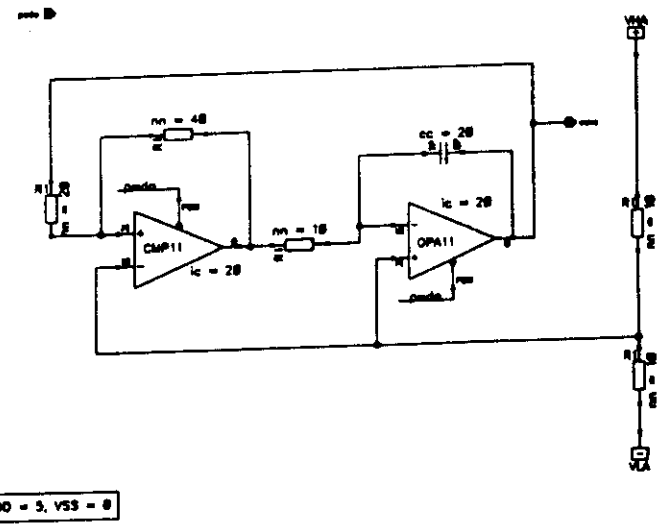


Fig. 3 - Triangle wave generator schematic capture

(nn, ic, cc, sup : cell programmation properties with "nn" for resistor values, "ic" for biasing current, "cc" for capacitor values and "sup" for global supply voltage).

Cell code	Description	Parameters Test conditions	Min	Typ	Max	Unit
CMP11	Static CMOS comparator	Propagation delay (overdrive = 5 mV) Offset		1 +/- 3	1.4 +/- 10	µs mV
CMP31	Static BICMOS comparator	Propagation delay (overdrive = 5 mV) Offset		90 +/- 2	110 +/- 7	ns mV
CPX11	Capacitor fields	Unit capacitance Capacitor value range Absolute accuracy Matching (capacitor ratio)	0.1	0.1 0.5	 50 +/- 15 1.0	pF pF % %
CPP11	Monolithic capacitor	Capacitor range Absolute accuracy	1		100 +/- 15	pF %
RPM/PPM	Resistor/Potentiometer P - Base	Resistor value range Absolute accuracy Matching Temperature coefficient Voltage coefficient	6.5		3000 +/- 20 +/- 1 0.2 0.05	KΩ % % % %
SWI1	Analog switch	Elementary switch RON value Number of switches in parallel	1	5	25 3	KΩ
MN11	Telescopic NMOS transistor	RON value		100		Ω
OPA31	General purpose MOS Operational amplifier	Unity gain bandwidth Current consumption Phase margin (C1 = 100 pF, R2 = 10 KΩ) Offset		3.3 700 60 +/- 3	4.6 +/- 10	MHz uA ° mV
OPA41	Internal bipolar Op-Amp.	Unity gain-bandwidth current consumption Phase margin (CL = 15 pF, RL = 100 KΩ) Offset		9 240 62 +/- 1	40 +/- 5	MHz uA ° mV
OPA71	Rail to rail external MOS operational Amplifier	Unity gain bandwidth Current consumption Phase margin (CL = 100 pF, RL = 100 KΩ) Offset		2.3 360 80 +/- 3	 +/- 10	MHz uA ° mV
OTA11	MOS transconductance amplifier	Unity gain-bandwidth (CL = 2 pF)		24		MHz
POR11	Programmable power or Reset	Active level accuracy Hysteresis accuracy			+/- 5 +/- 5	% %
VRF11	Voltage bandgap reference	Output voltage accuracy Temperature coefficient Current consumption		 15	+/- 2 100 	% ppm uA
OSC11	Programmable crystal oscillator	Frequency	0.1		20	MHz
OSC41P	RC oscillator	Frequency Stability versus temperature Stability versus voltage	1	100 0.01 0.5	800	KHz %/°C %/V
OSC31P	One pad I.C oscillator	Frequency Stability versus temperature Stability versus voltage	2	 0.01 0.5	200	KHz %/°C %/V
SCF	Filters	Order Center frequency	2		12 100	 KHz
ADC81	8 bit analog to digital converter	Conversion time Integral non linearity Differential non linearity			5 +/- 0.5 +/- 0.5	µs LSB LSB
DAC81	8 bit digital to analog converter	Conversion time (CL = 2 pF) Integral non linearity			1 +/- 0.5	µs LSB

TABLE 1 : STKM2000 Analog Library abstract

This compiler allows to generate automatically a switched capacitor filter from a specification up to the layout. Models for simulation and footprint icons for place and route are also computed and delivered into the compiled cell library. The compiler is composed of 3 main parts :

- Mathematical filter synthesis which allows to find the well adapted function according to initial specifications.
- Switched capacitor schematic synthesis and netlist generation for simulation and layout: SWITCAP netlist format is used as a standard one.
- Layout generation from SWITCAP netlist: A GDS2 format is delivered by the compiler.

MATHEMATICAL FILTER SYNTHESIS :

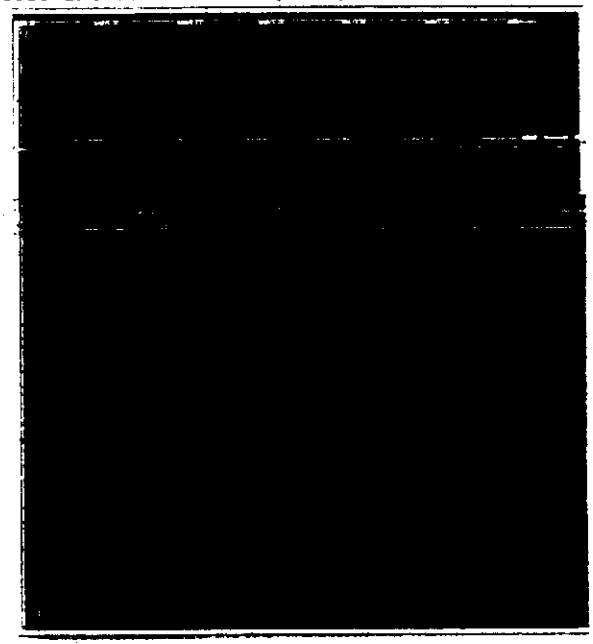
FILCAD software is used for the computation of the filter in accordance with initial specifications. Input data are introduced during an inter-active session.
Several input modes are available to introduce data : lossless / frequency specifications, poles and zeros locations, cascaded biquadratic coefficients, F (p) or F (z) transfer functions.
Any kind of filter up to the 12th order is computerizable : low pass, high pass, band pass, notch, band reject , all pass resonators. Possible mathematical are : Cauer, Chebyshev, Bessel, inverse Chebyshev, Butter-worth. A non classical filter can be optimized thanks to a specific optimization software, which delivers poles and zeros.
At the end of this step, standard data are transmitted to the next module ; switched capacitor filter synthesis.

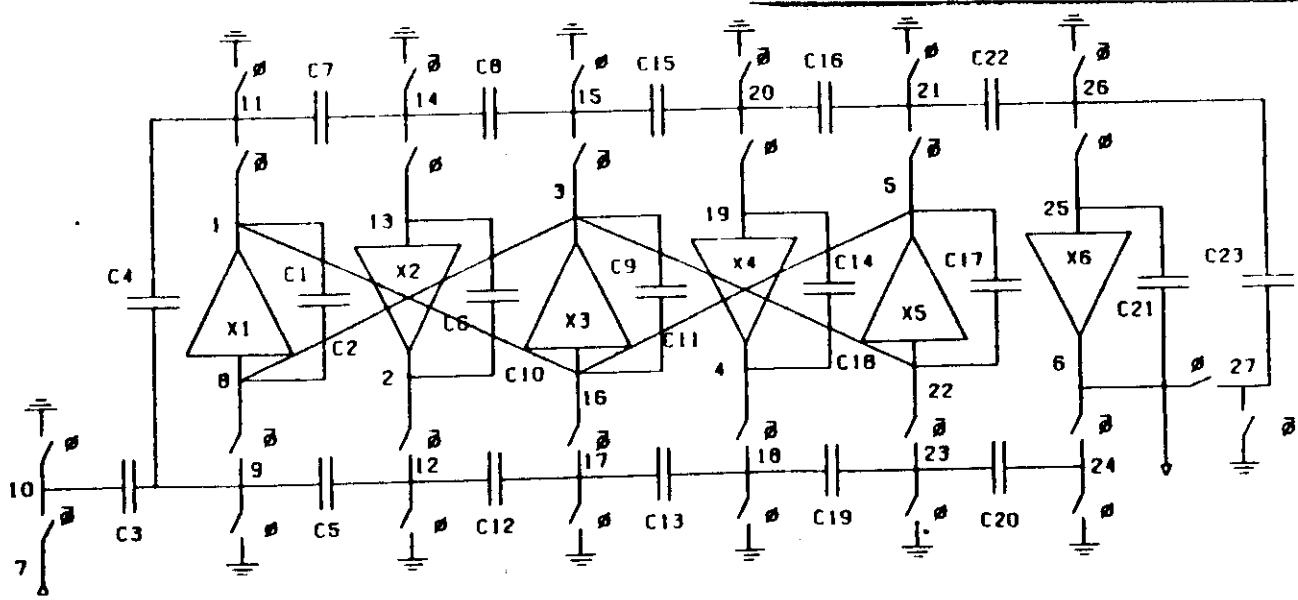
SWITCHED CAPACITOR FILTER SYNTHESIS :

From standard mathematical data a bilinear or LDI transformation is performed depending on the user request. Then the filter schematic is delivered in a SWITCAP netlist. Cascaded biquadratic and leapfrog structures are available.
An inter-active session allows to perform dynamic equalization on each amplifier and to fix absolute value for each lower capacitance. At the end of this task the updated netlist can be used to perform a SWITCAP simulation and a MONTE CARLO analysis. The min / max curves can be compared to the initial specification. Several feedbacks are possible during this step, until the final filter schematic is performed. The final SWITCAP netlist is stored in a reference file in order to perform the following step : filter layout.

S.C FILTER LAYOUT GENERATION :

SWITCAP netlist is the standard input format for this layout compiler. From the number of used amplifiers, the block width is fixed. Op. Amp. biasing block, CMOS switches and 4 phases non overlapping clock generators are automatically added into the layout. From capacitor values, the unit capacitor array is optimized in order to reduce area and crosstalk. The capacitor field grows only in the vertical direction in order to obtain a rectangular macro block. Interconnections between these blocks are routed from SWITCAP netlist. A place & route icon for circuit layout (footprint) is issued from GDS II layout.
An example of S.C filter performed in BICMOS technology is given hereafter : SC filter 6th order low pass filter schematic and associated layout performed on Silicon.





In order to manage the design of a chip with the STKM2000 library, a novel approach of C.A.D has been developped, that improves flexibility and safety in analog design and reduces design time.
A.D.S, the SGS-THOMSON Microelectronics Analog Design System, has been built as an integrated system, offering coherent solutions from schematic capture to mask generation, through simulation steps.
The fields mainly covered by ADS, in addition to well known standard features such as delay evaluation and design rules checking, are mixed library management and analog design automation.

The STKM2000 product is one of the best examples of synergy between design and C.A.D. . C.A.D tools have been developped to fit the library requirements, and the library has been designed to be easily handled by the software.
The result of such a developement methodology is a higher flexibility and safety in the design :
Schematic capture is done using a reduced set of analog icons in order to make the choice among the library easier. Properties is then added by the user on the instance to customize the function, depending on the design needs. The software will generate for this particular instance representations for each step of the design : propagation times for digital behavioral model, transistor level netlist for accurate electrical simulation, cell footprint to be used by the automatic placement and routing program, netlist for LVS (Layout Versus Schematic) check and, of course, the GDS2 layout representation.

- An operational amplifier may be generated according to the biasing current (property IC) that controls major parameters of amplifier : gain, bandwith, slew rate, power consumption,... and the frequency compensation (propertiy CC) that allows to adjust and optimize the dynamic parameters versus the capacitive and resistive load. Its layout is compiled by automatic selection and abutment of leaf cells, using the TELESCOPIC CELL feature (see Fig. 4-A).

- An other kind of programmation is offered by the PARAMETRIZABLE feature (see Fig. 4-B). The user can use in the design some devices (resistances or capacitances), giving to them the exact value he needs (property NN). A cell is generated to fit this value, with a resolution of 0.1 picofarads for capacitances and 300 Ohms for resistances. To allow design of switched capacitors systems or resistive dividers, the device is generated using a repetitive structure. A field of unit devices is created as a telescopic cell, then automatically personnalized by metal lines to reach the required value.

- Last kind of programmable feature is the ADJUSTABLE CELL (see Fig. 4-C). It is used for functions containing a device that must be adjusted to tune a parameter : RON of a switch, percentage of hysteresis of a power-on reset or current in a bipolar transistor.. The property ADJ corresponds to this feature.
An Analog Design Expert System allows a reduction of human errors in some very specific analog parts and a significant speed-up of the design by automation of the routine tasks.

So are handled automatic cell biasing, multi power supplying and power down mode management.

- Most analog cells (operational amplifiers,comparators, oscillators, ...) need to be biased by a current. As previously explained, the biasing value is given for each cell by the property IC. The design is scanned to evaluate global design needs in biasing currents, and a synthesis is performed to calculate the reference current to be generated. This current will be then reproduced and multiplied using current mirroring. A centralized block is generated by abutment of a bias generator subcell with the current mirror cells required to bias every analog cell. Connections from the biasing block to each analog cell are automatically added during placement and routing.

- Analog chips often have more than one pair of power pads. To allow design of such chips, and to avoid connecting each cell to power nets during the schematic capture, a novel property-based approach has been developped. Capture is done with icons having no supply pins, then a property is given by the user on parts of the design to be supplied by extra pads (property SUP). Simulation netlists (both electrical and digital) will be generated according to properties. At last, the floorplanning is prepared by cell partitionning in different classes to allow an easy separation between parts of the chip to be supplied with separate power nets. A typical application of this feature is the split of analog and digital supplies in order to reduce crosstalk effects.

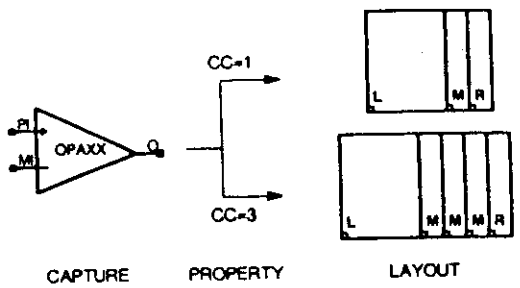
- Most analog cells have an optional power down mode, driven by a command pin available on the icon. When these pins are put in the active state, consumption of the cell is suppressed. A typical application of this feature is the design of chips having a watch mode and beeing supplied with a battery. If the power down mode is not used in a chip, the command pin may be left unconnected at capture step. The programs scans the design to check connectivity of these pins. When left unconnected, they are tied to an inactive state by a metal line wired inside the cell outline.

All these tasks are performed by CORAIL the heart of SGS-THOMSON Microelectronics analog ASIC CAD system.
The digital and analog design management is assumed by CORAIL too, it deals with :

- previsional routing capacitance evaluation, depending on design connectivity,
- check of load driven by the output of a cell versus a maximum allowed value,
- digital electrical rules checking, such as paralleled outputs or unconnected inputs,

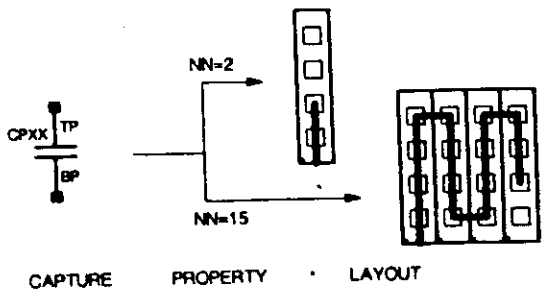
Fig. 4 : MIXED A/D LIBRARY MANAGEMENT

A - TELESCOPIC CELLS



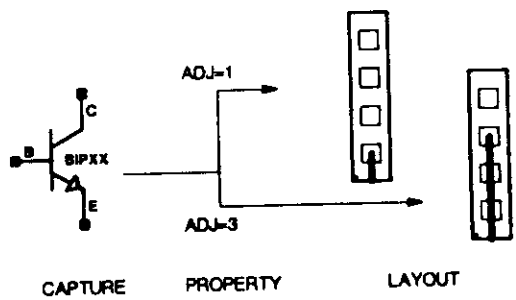
- Cell is compiled by abutment of subcells, selected among a library of leaf cells: one left-side subcell, then a given number of middle subcells, to reach the value selected by the property, and finely one rigth-side subcell.
- Concerned cells in STKM2000 library are: digital output buffers, operational amplifiers, monolithic capacitors, MOS transistors, ...

B - PARAMETRISABLE CELLS



- An array of devices is compiled by abuttment of subcells. Some end cells are added at the right of the array to fit a grid multiple cell width.
- A metal line is added to customize this field of devices (like a gate array personalization) at the exact value.
- Concerned cells in STKM2000 library are: capacitance fields (3 different kinds) and resistance fields (5 different kinds).

C - ADJUSTABLE CELLS



- Personalization figures are added upon a predesigned cell to customize its functionality.
- Concerned cells in STKM2000 library are: bipolar transistors, switches, power-on-reset, pull-up and pull-down resistances, ...

- analog electrical rules checking, such as current or supply compatibility,
- design informations transfer towards electrical, digital and mixed mode simulators, placement and routing programs, and Layout Versus Schematic checker,
- exact routing capacitance extraction and back annotation after placement and routing phases.

CORAIL is integrated in A.D.S (Analog Design System), a design environment that assumes the design flow integrity time. A.D.S checks that each step is performed at the right time only if the previous task has been error free performed.

The design flow of A.D.S is given in Fig. 5.

A.D.S is available on following platforms :

- VAX™ VMS operating system + SILVAR LISCO™ softwares
- SUN™ UNIX operating system + CADENCE™ softwares
- MENTOR™ workstations
- DAISY™ workstations.

CORAIL is available as standalone tool on VAX™ / VMS, SUN™ / UNIX, APOLLO™ / AEGIS and DAISY™ / DNIX.

CONCLUSIONS.

The STKM2000 library is really a merged library:a merge between bipolar and CMOS technologies, a merge between analog and digital functions, a merge between C.A.D and design concepts. This " merged " library is able to answer to most of system requirements between sensors and actuators, from lower to video frequencies, from 2.7 V to 11 V applications, with the possibility of accurate functions. With the possibility to implement on a same die 10 K gates with all analog functions, STKM2000 opens the door towards the one chip solutions in equipments.

Its availability on major of standard workstations with a " friendly " human interface and design manager allows to everybody to design himself mixed Analog / Digital applications.

C. CAILLON - P. BERNARD
JM SANCHEZ - S. SCOTTI
SGS-THOMSON MICROELECTRONICS

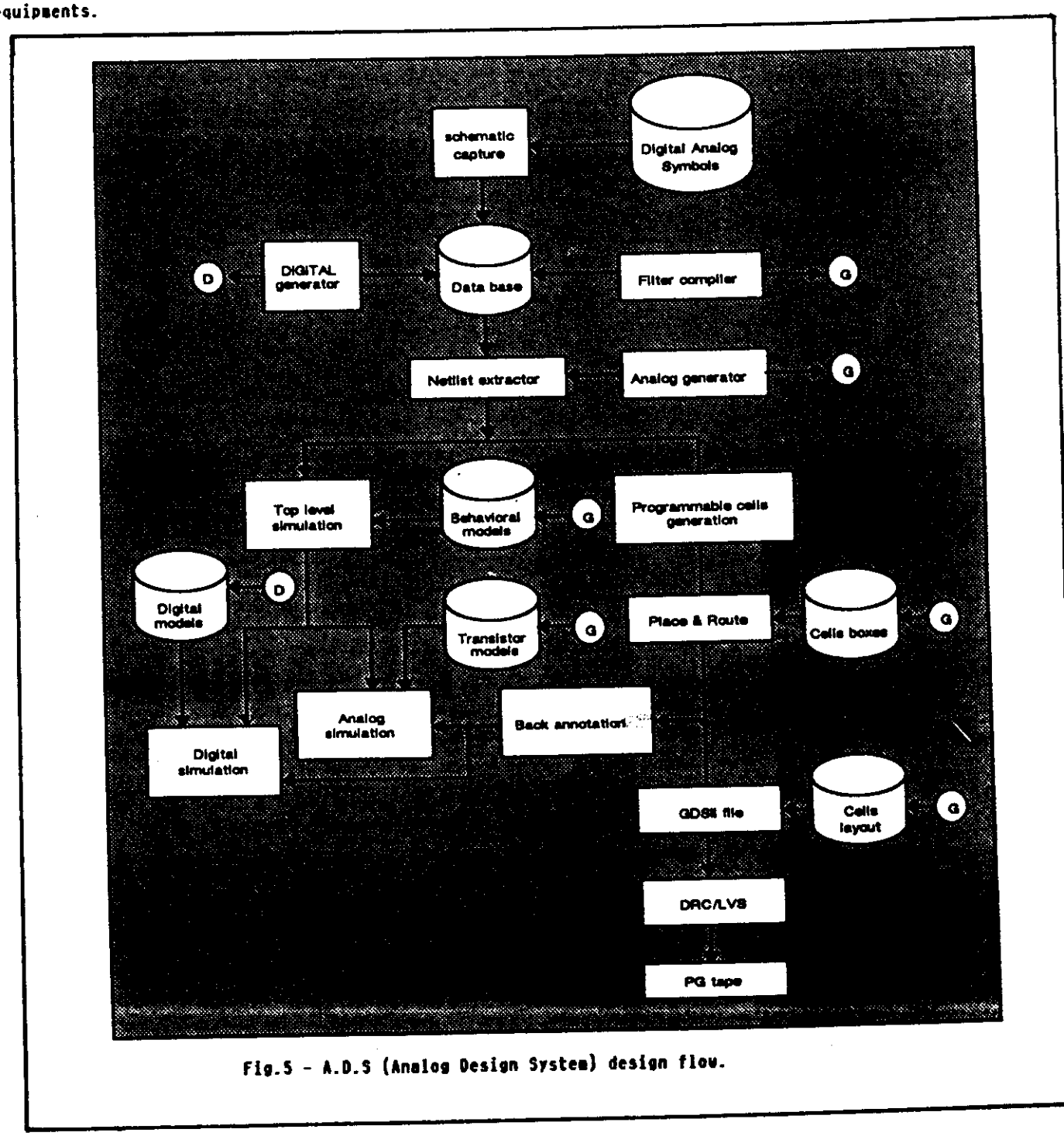


Fig.5 - A.D.S (Analog Design System) design flow.

INVOMEC activities

Support of a Training Program for students in microelectronics

INVOMEC has set up a PTT-network, linking 16 universities and polytechnics in Belgium to the central computer infrastructure in IMEC. About 300 students per year are trained in VLSI design using centralised industrial CAD software in IMEC. The available CAD packages are schematic entry, simulation, semi-custom layout generation with standard cells, a full custom layout editor and a silicon assembler. INVOMEC offers the MPC service for the prototyping of student designs.

VLSI Training for Industry

INVOMEC organises practical custom tailored training courses for industry and R&D labs. Engineers are trained in ASIC (Application Specific Integrated Circuit) design, either in a custom or semi-custom environment. As examples are taken circuits defined by the customers.

As part of such a custom tailored training, INVOMEC offers full support in prototype development, resulting in low cost implementation on MPC.

Digital Design Support

INVOMEC offers support in the design of ASICs to unexperienced commercial firms. Starting from specs or schematics, INVOMEC will develop an integrated circuit. For digital circuits, the semi-custom approach using standard cells will allow a fast and low cost development time.

Support in the Development of Analog Low Noise Particle Detection Systems

For analog designs, INVOMEC is experienced in the design of low noise front-end read-out electronics for particle detectors. Low noise charge amplifiers are developed in close cooperation with CERN, Geneva and are available as standard building blocks. It has been proven that the MIETEC 3 µm CMOS technology is radiation hard up to 80 kRad and is well suited for these High Energy Physics applications.

Development of Technology Independent Modules for DSP Applications

INVOMEC is developping a set of technology independent modules (multiplier, register file, FIFO, RAM, ROM, PLA, ALU_core) for the CATHEDRAL silicon compiler. CATHEDRAL is a silicon compiler, developed by the VSDM division of IMEC, for the generation of DSP circuits from formal specification to layout. These modules can also be generated on your request for other applications.

Multi Project Chip Service

Since 1984 INVOMEC has been providing a prototyping service for VLSI design by merging designs from universities, polytechnics, R&D centres and commercial firms onto Multi Project Chip wafer runs. This results in low risk, low cost ASIC development.

1-Dec-1989

MPC reduces the risk and the cost of VLSI design

Lower Cost

Since 1984 INVOMEC has been providing a prototyping service for VLSI design by merging designs from universities, polytechnics, R&D centres and commercial firms onto Multi Project Chip wafer runs.

Instead of paying 1,200,000 Bfr. to 3,000,000 Bfr. or even more for a single prototype run, you can get low cost prototypes by participating on the INVOMEC MPC service. You pay a price proportional to the area of your submitted design with a minimum charge of only 50,000 Bfr. Your design will be checked on Design Rule (DRC) and Electrical Rule (ERC) violations. You will receive 10 to 12 weeks later 20 untested prototypes for evaluation.

Industrial Technologies

INVOMEC supports 2 CMOS technologies of MIETEC (Oudenaarde, Belgium). Both are :

* 3 µm n-well CMOS double-level poly and double-level metal
* 1.5 µm n-well CMOS double-level poly and double-level metal

Projects can be designed using design rules from INVOMEC or MIETEC. INVOMEC also distributes the standard cell library of MIETEC in the 3 µm technology for semi-custom design. Special building blocks like PLA's, RAM, ROM, SC-filters, ... can be generated by INVOMEC.

Design Tools and Interface

Layouts are accepted in GDS-II stream format as defined by Calma Corporation, the Caltech Intermediate Form (CIF) 2.0 format as defined by Mead and Conway in "Introduction to VLSI Systems", Addison-Wesley, 1980 or the FDR format (Silvar-Lisco).

INVOMEC has a complete set of Design Verfication Product (DVP) software available, including Design Rule Check, Electrical Rule Check and Netlist Comparison Check. INVOMEC has gained a lot of experience in back-end verification. INVOMEC can offer you a complete design check before processing, reducing the time and cost for prototyping. A complete DVP-check takes about 5 to 10 days.

1-Dec-1989

PROTOTYPE ORDER FORM
for participation on the INVOMEC MPC processing

This order form has to be filled in completely and returned to IMEC before the closing date of the MPC run. Only at these conditions IMEC accepts your participation on the MPC run.

This order form and any other communication should be addressed to :

IMEC v.z.w. - INVOMEC division
Dr. Carl DAS - Manager MPC services
Kapeldreef 75
B-3030 Leuven-Heverlee
Belgium

Telex : 26.152 imecb
Telefax : (016)229400
Tel.: (016)281211
(016)281248

1. CONDITIONS

* The INVOMEC MPC service accepts the prototype designs, submitted in CALMA GDS-II stream format, CIF 2.0 format or FDR format (Silvar-Lisco).
* The INVOMEC MPC service shall provide fabrication of 20 untested packaged or unpackaged prototypes.
* After fabrication all the wafers have passed the parametric tests of the wafer fab and those of INVOMEC. INVOMEC sends a SPICE level 3 parameter extraction report together with the prototypes. INVOMEC does not guarantee that the prototypes will be functional.
* Together with the tape, the customer has to send a bonding diagram and a drawing of the design on A4-format. If the customer does not submit a bonding diagram, INVOMEC will choose the best bonding diagram.
* **INVOMEC/IMEC shall not be responsible for any direct, indirect, incidental or consequential damages the customer will suffer relating to the use of the MPC service. INVOMEC/IMEC is not responsible for the functional working of the prototypes.**
* **INVOMEC/IMEC and the customer recognize that the information exchanged by participation of the customer on the INVOMEC MPC service is of a confidential and proprietary nature.**

2. CUSTOMER INFORMATION

Company name : .....
Company division : .....
Address : .....
Contact person : .....
Phone : .....telex : .....
Telefax : .....

Customer's CODE for MPC participation (if known) : .....

Purchase order number : .....

3. DESIGN INFORMATION

Any inaccuracies concerning the information about the design data could result in processing delays or cancellation of the customer's participation on the MPC. Any

efforts by INVOMEC to correct design errors (detected by DRC) or errors in the database can be charged to the customer.

Tape and design information

Filenames : .....

Date of tape creation : .....

Tape density : .....

Label : .....

Design format : .....

The above information must be marked on the tape.

Grid size (0.5 µm for 3 µm CMOS and 0.25 µm for 1.5 µm CMOS) : .....

Origin in left lower corner of the chip. Done ? .....

Drawing of the designs on A4 included ? .....

Bonding diagram included ? (if not INVOMEC will choose the best).....

Ceramic or Plastic packaging ? ..... Number of pins : .....

Which IMEC design rule spec's and revision is used ? .....

Which rules are used for placement of bonding pads ? .....

Design information

Check the design :

CMOS 3 micron n-well double poly, single metal .....

CMOS 3 micron n-well double poly, double metal .....

CMOS 1.5 micron n-well double poly, double metal .....

Important : if a project with single metal is submitted on a double metal MPC, via-mask and metal-2-mask have to be generated by the designer (bonding pads have to be copied to metal 2 and the via's between the metal levels on the bonding pads).

The size has to be calculated as a rectangle covering the whole design.

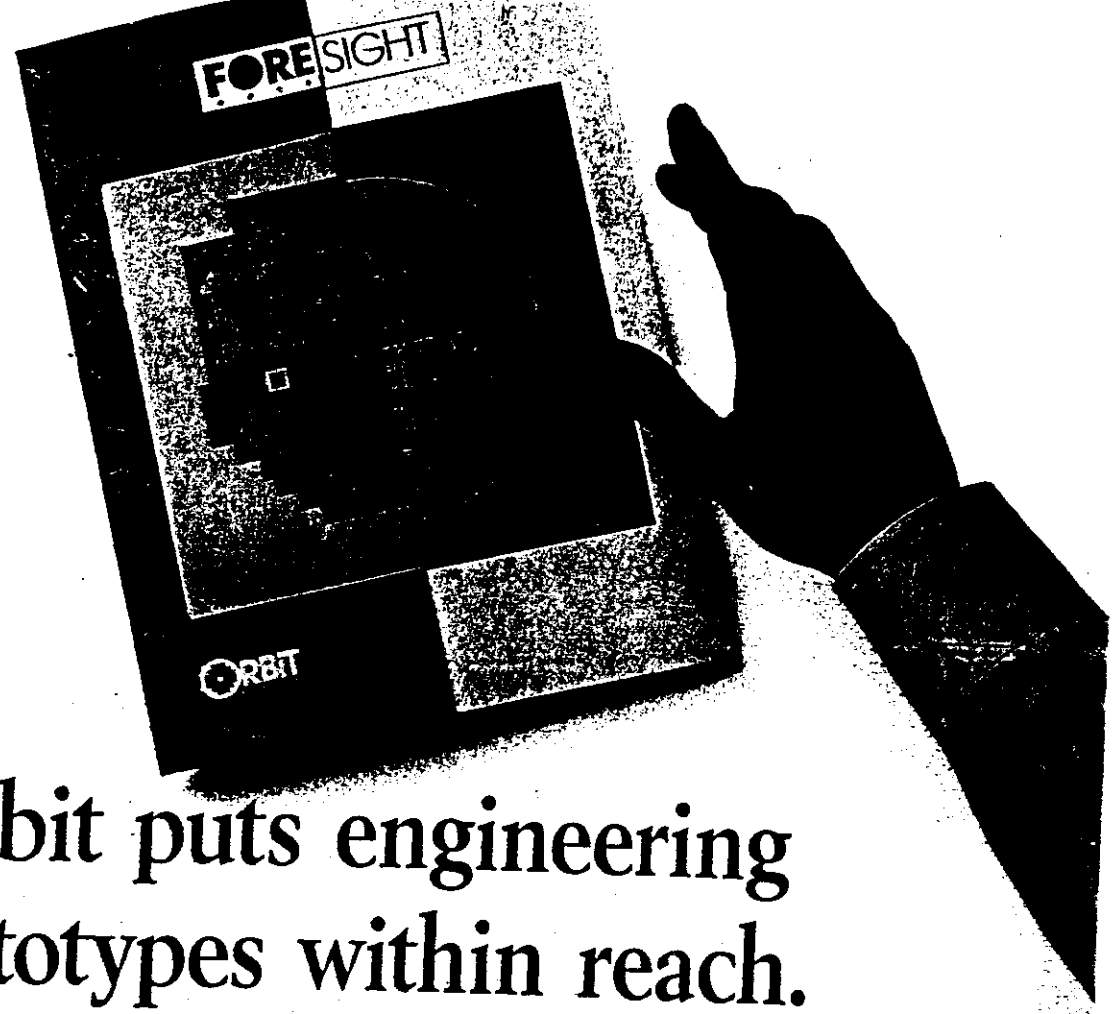
5. CUSTOMER AUTHORIZATION

Name : .....

Title : .....

Dated : .....

Customer signature : .....



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Now you can cut NRE expense and save valuable time on engineering prototype runs just by using a little foresight. Foresight, Orbit's new multi-project wafer processing service, puts the engineering prototypes you need within reach. In record time. And at a record low cost.

Orbit's new Foresight accommodates generic CMOS processes with feature sizes down to 1.2 microns with maximum die sizes of 300 mils on a side. Getting in on a run is as easy as supplying a database tape by our monthly start date.

Available processes:

- Single Poly/Single Metal
- Double Poly/Single Metal
- Single Poly/Double Metal
- Double Poly/Double Metal

Don't wait until high NRE costs and slipped deadlines put you in a bind. Design rules and information on Orbit's new Foresight service are within reach today by contacting Foresight Marketing or the international rep nearest you. Orbit Semiconductor, Inc. 1230 Bordeaux Drive. Sunnyvale, CA 94089. FAX (408) 747-1263. Or call (800) 331-4617. In California (800) 647-0222 or (408) 744-1800.

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