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SECOND COLLEGE ON
MICROPROCESSOR-BASED REAL-TIME CONTROL -
PRINCIPLES AND APPLICATIONS IN PHYSICS
5 - 30 October 1992

PC-BASED SYSTEMS

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SOFTWARE AND HARDWARE INTERFACING THE IBM PC

A Set of Three Lectures

Prof. Gustavo Cancelo

Universidad Nacional de La Plata, Argentina

* Generalities. (one hour)
* Introduction to the PC hardware and software (one hour)
* The AT Bus. Example of an AT bus interface (one hour)

THE IBM PC FAMILY

1974-1978 8 bit personal computers: Intel 8080, Zilog Z-80, etc.

1981 IBM PC (Intel 8088)	4.77 MHz clock 256K RAM memory 360 Kby floppy computing power of about 1/4 MIPS
1983 IBM XT model	same speed & comp. power introduces hard disk support(10Mby disk) clones start making XT compatible models (p.e Tandy 1000, TI business Pro, etc.)
1984 IBM AT model (Intel 80286)	12 MHz clock up to 16 Mby of RAM memory virtual memory hardware multitasking
1987 IBM PS-2 Line (Intel 80286/386 16 MHz)	Microchannel bus Protected mode OS/2 operating system
1987 PC clones (Intel 80386 16 MHz)	keep using ISA bus also support protected mode
1989 PC clones (Intel 80486 25 MHz)	on chip floating point coprocessor + EISA bus

1993? 586 PCs announced by late 1992 but later delayed due to market reasons

The PC- Introduction:

The PC constitutes a real family both in the sense of having a history, hence, a genealogical tree, but also in the diversity of products that coexist in the same generation.

Around 1980 when the idea of a PC was conceived at IBM, the market of personal computers was dominated by the so called 8 bit machines. They had 8 bit data bus paths both inside and outside the microprocessor. The PC was initially thought as another 8 bit machine but later turned as a 16 bit inside and 8 bit outside. Some IBM people thought the 8 bit machines had a short life and decided to use a 16 bit microprocessor. However, back in early 80s 16 bit peripherals were not so common and they were expensive, so they decide to use an Intel 8088 that has the architecture of a 16 bit processor (the 8086) but with an 8 bit data bus to the outside world.

After over a decade, a lot of water has passed under the bridge, the newer models go way far beyond the old PC in computational power and in every part of the PC computer where we look at.

The PC bus is an open standard, any one of us can start a business making PC boards of any kind. That helped a lot to place the PC as the most used computer in the world and the best cost effective. Nowadays, we can buy the fastest 486 PC starting at about U$A 2000.

ADVANTAGES OF USING PCs:

There are approximately 50.000.000 PCs in the world.

Cheap (400-5.000 U$A), reliable, service available everywhere in the world. The first commodity computer.

The largest assortment of add-on boards and application programs. All known languages available.

MS-DOS, small, fast, it has no Input-Output protection. The user can change without restriction the interrupt vectors, etc. Most of the times a multitasking, multiuser environment is not needed. (pity the 640 kb limit).

It can handle different operating systems :

MS-DOS, DR DOS (romable) (640 kb limit)

XENIX , UNIX like

UNIX , multitasking, multiuser, large and slow;

Santa Cruz Operation (U$A 2.000)

Mark Williams (only US$100)

MINIX, UNIX like, public domain

WINDOWS 3.0, multitasking, uses all the memory
but it needs compatible programs. They are coming out fast.

OS-2 Multitasking, uses all the memory.

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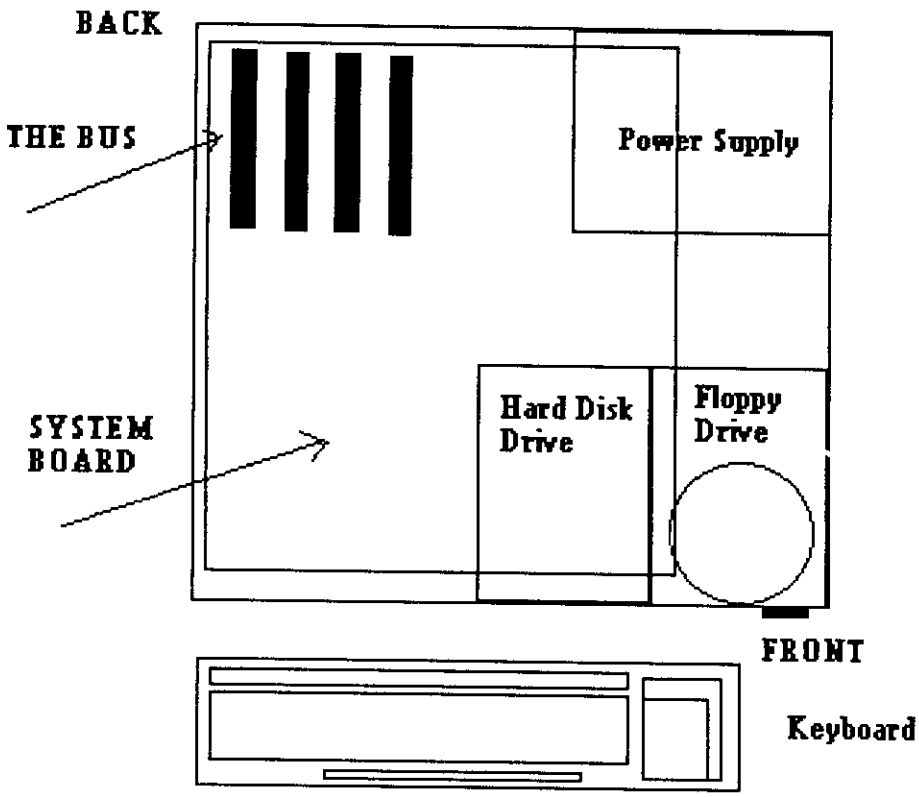
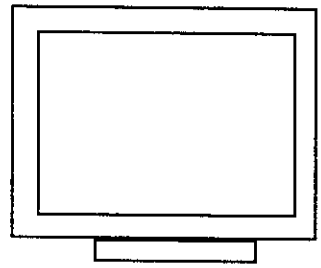
DISADVANTAGES OF THE PC FAMILY

It shouldn't be used for teaching. Memory segmentation is difficult to understand and manage. The new 80386 and 486 driven systems could be used as teaching platforms, but without MS-DOS.

THE WORSE OFFENDER IS MS-DOS ITSELF WITH ITS 640 KB MEMORY LIMIT. Otherwise we would live in a mono-computer world.

THE PARTS OF AN IBM XT LIKE COMPUTER





CRT Display

OPTIONS

Video Display :

monochrome Display Adapter (MCDA)
Hercules
Colour Graphics Adapter (CGA)
Enhanced Graphic Adapter (EGA)
Professional Graphics Adapter (PGA)
Video Graphics Array (VGA)

All the above video monitors and adapter are supported in all models of the PCs and DOS versions.

Floppy Drives :

5 1/4" drives 160kb-1.2 Mb
3 1/2" drives 720 kb - 1.4 Mb

DOS versions 3.2 and under don't not support 3 1/2" drives.

DOS FLOPPY DISK FORMATS

FORMAT	TRACKS	SECTORS PER TRACK	TOTAL USABLE SECTORS	CAPACITY
SSDD	40	8	320	160 KB
DSDD	40	8	640	320 KB
SSDD-9	40	9	360	180 KB
DSDD-9	40	9	720	360 KB
QD-9	80	9	1420	720 KB
QD-15	80	15	2400	1.2 MB
QD-18	80	18	2880	1.4 MB

Hard Disks :

Capacities from 10 Mb to 1 Gb. Disk controllers available in MFM, RLL, IDE, SCSI, etc.

Tape drives :

Open reel and cartridges from 60 to 500 Mb.

ETC, ETC

(9)

Intel processors

Intel 8088

-16 bit internal architecture

-8 bit external data path

-1 Mby memory addressing

-14 word register set

-24 operand addressing modes

-byte, word and block operations

-5 and 8 MHz clock

-Minimum/Maximum operation modes

-Multiplexed bus. Address and data low bytes are multiplexed (AD0-7). Addresses are valid during T1 clock and data during T2, T3, Tw and T4.

-A16-19 are also multiplexed with S6-3

-DEN* and AEN provide demux. timing.

-8284A controller is used together with the 8088 in Maximum mode. Generate bus control timing and higher current at the outputs.

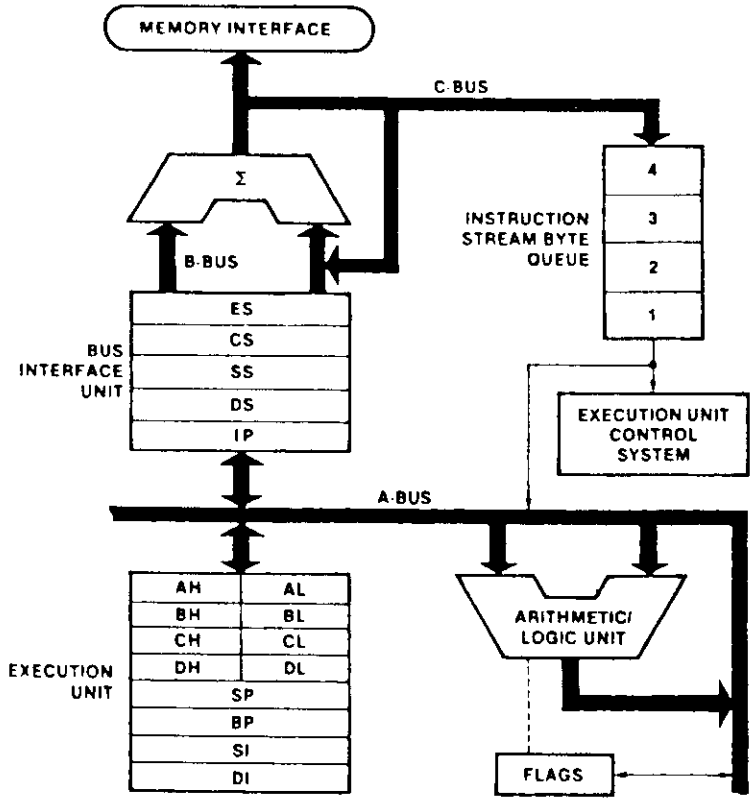


Figure 1. 8088 CPU Functional Block Diagram

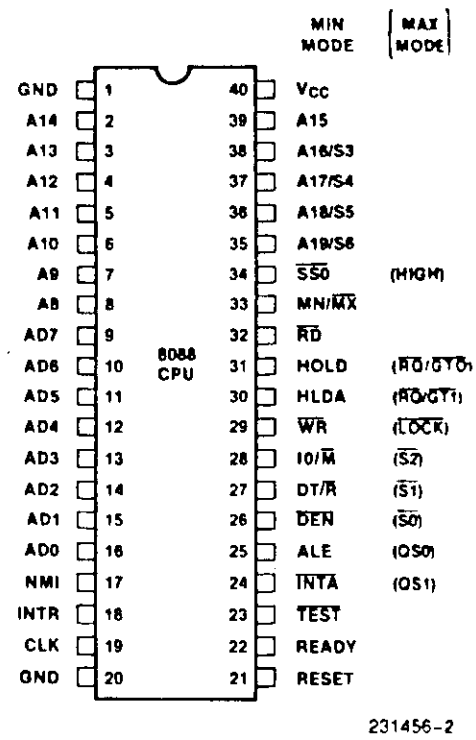
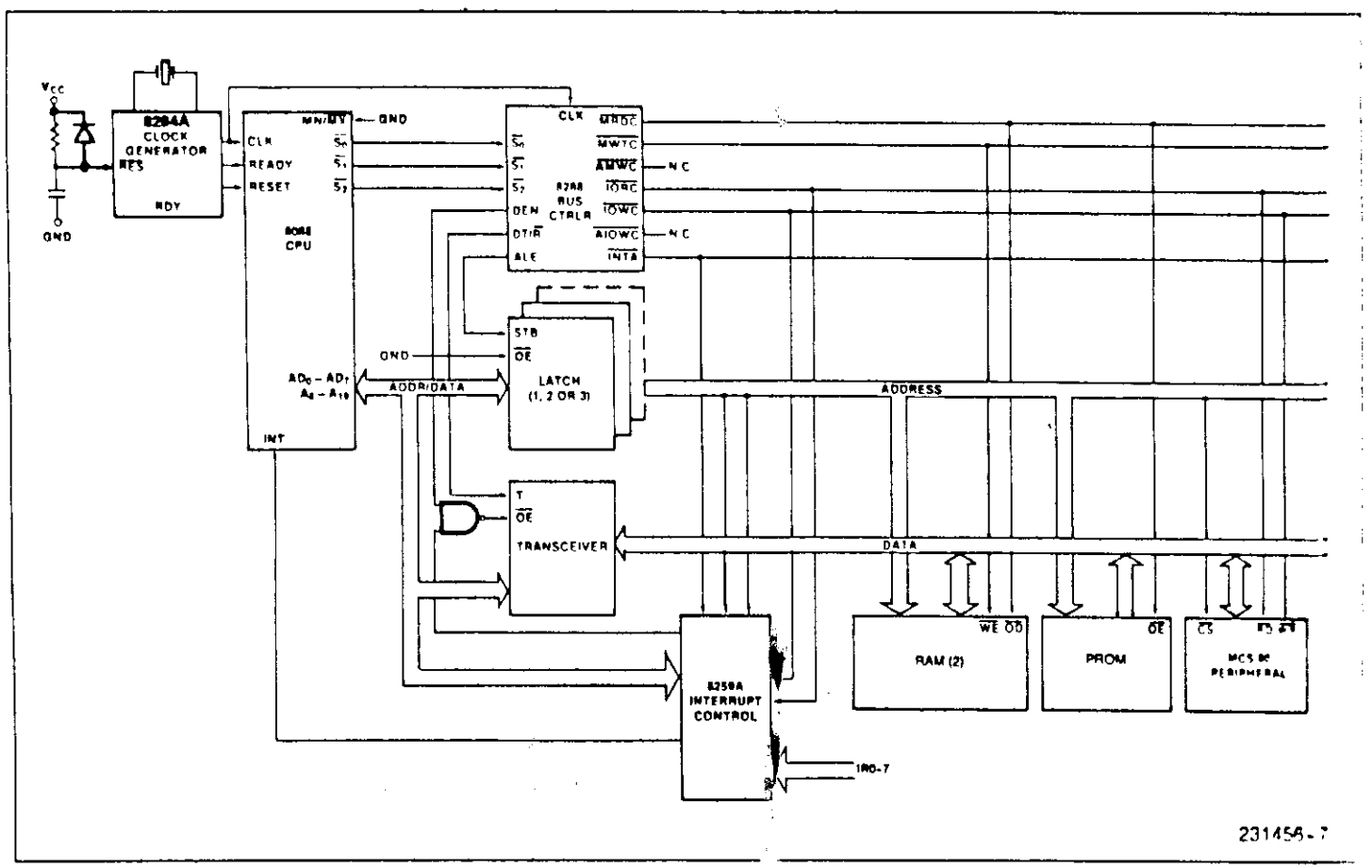


Figure 2. 8088 Pin Configuration

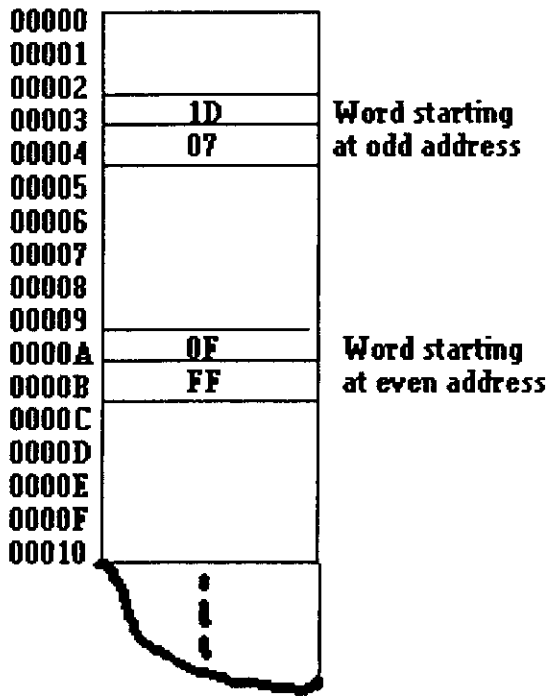

V_{CC}
8284A
CLOCK
GENERATOR
RES
RDY
GND
CLK
READY
RESET
MN/MX
GND
8088
CPU
$AD_0 - AD_7$
$A_8 - A_{19}$
ADDR/DATA
INT
CLK
$\overline{S_0}$
$\overline{S_1}$
$\overline{S_2}$
DEN
DT/$\overline{R}$
ALE
8288
BUS
CTRLR
$\overline{MRDC}$
$\overline{MWTC}$
$\overline{AMWC}$
$\overline{IORC}$
$\overline{IOWC}$
$\overline{AIOWC}$
$\overline{INTA}$
N C
N C
STB
$\overline{OE}$
LATCH
(1, 2 OR 3)
GND
ADDRESS
T
$\overline{OE}$
TRANSCEIVER
DATA
8259A
INTERRUPT
CONTROL
IR0-7
RAM (2)
WE OE
PROM
OE
CS
MCS 80
PERIPHERAL
231456-7

The 8086 and the 8088 differ in the external data bus. The 8088 is an 8-bit bus version of the 8086. Its instruction set and basic architecture are identical to the 8086. They differ also in speed, generally the 8088 is a 4.77 MHz chip (the NEC V20 reaches 12 MHz) while the 8086 is an 8 MHz chip.

The 8088/86 memory structure

The chips manage up to 1 Mbyte of memory from 00000 to FFFFF in hexadecimal notation. It requires 20 bit for the external bus address.

Two consecutive bytes form a word.
The smallest of the two byte addresses is the *word address*.
When the address of the word is an even number, the word is said to start at an *even address*, else it is an *odd address*.



In a word, bits from 0-7 are called the *low order byte*, while bits from 8-15 is the high order byte.
The address of the word is the lower of the two addresses of the bytes comprising the word, consequently the byte with the lower address is the low order byte of the word.
MOTOROLA STORES A WORD IN EXACTLY THE OPPOSITE ORDER.

In the 8088-86 memory structure words appear as being stored backwards.

The words stored in memory at odd and even addresses are :

071Dh and FF0Fh

A *paragraph* is a piece of contiguous memory containing 16 bytes. The *paragraph address* is the address of the lowest byte contained in the *paragraph*. The 1 Mb address space of the 8088 in paragraphs can be seen as

Paragraph address	**Bytes within the paragraph**
00000	00000-0000F
00010	00010-0001F
....	....
FFFF0	FFFF0-FFFFF

There is a total of 64k paragraphs in the 1 Mb memory space.

Memory segmentation

The absolute address of a byte or word requires 20 bits. However the 8088 is a 16 bit CPU. To obtain a 20 bit address out of 16 bit register Intel organised the memory space in segments. (this is the reason why the 8088 is no good for teaching)

One *segment* is any number of bytes up to a maximum of 64 kbytes. A *segment* may start at any place in memory as long as it is in a paragraph boundary. This means that the absolute address of any segment will always start with address that ends with a 0. (i.e. xxxx0h)

The *segment address* is 16 bit number.

To reference a byte within a segment, as the segment is 64 kb long, we need another 16 bit number (*the byte offset*)

The 8088-86 chip has 16 bit register, this means that the largest "address" that can be internally calculated is 16 bits long. But as we want to address 1Mb of extern memory we need a 20 bit address.

a) By splitting memory into paragraphs (16 bytes) any paragraph in memory can be represented by a 16 bit number.

b) Since a segment (64 kb) starts at a paragraph boundary, a byte can be referenced by means of a 16 bit offset from the start of the segment boundary plus the segment address.

Memory Segmentation and Segment registers

Any program running under MS-DOS is allowed to specify up to four distinct segments for simultaneous use within the program. Because any segment is limited to 64 kb, the programs is limited to referencing a total of 254 kb.

The intended purpose of each of these segments is identified by its name :

Code Segment : is the segment that contains the program instructions.

Data Segment : contains the program's data.

Extra Segment : may be used for storing additional data or for holding and manipulating strings.

Stack Segment : contains the programs run time stack, used for calling subroutines and passing arguments between routines.

REGISTERS IN THE 8088-86 ARCHITECTURE

General Registers : AX, BX, CX and DX are 16 bit general purpose registers which can also be considered as two 8 bit registers called AL, AH, BL, BH, etc.

Pointer and Index registers : The Stack Pointer points to the current top of the stack "within the stack segment". The Base Pointer contains an offset from the stack pointer to retrieve data placed on the stack. The Source Index and Destination Index are used for string operations but they are also general purpose index registers. The string instructions are a subset of the 8088 instruction set.

Segment Registers : CS, DS, ES and SS point to segments as explained before.

Program Counter : (instruction pointer) points to the next instruction to be executed. It is used with the CS register to fetch the next instruction from memory.

FLAGS

Nine flags that indicate the condition of the chip after the execution of the last instruction. The flags are tested and according to the result of the test the 8088 continues with the execution of the next instruction or branches to some other address.

FLAG	MNEMONIC AND NAME	FUNCTION
OF	overflow	Set if result has overflowed a range.
DF	Direction Flag	Determines the direction of string instructions.
IF	InterruptEnable	Allows-disallows interrupts to be processed.
TF	Trap Flag	If set the 8088 single steps, for program debugging.
SF	Sign Flag	Set when result is negative
ZF	Zero Flag	Set when result is zero.
AF	Auxiliary Flag	Set when a carry is generated from the least significant four bits of the last result.
PF	Parity Flag	Set when parity of result is even
CF	Carry Flag	Set if result has generated a carry.

INPUT/OUTPUT STRUCTURE

There are special instruction to address I/O ports, IN and OUT. The 8088 is capable of addressing 64 k ports.

INTERRUPTS

An interrupt allows the computer to suspend whatever it was doing and switch to some other task based on something that causes the interruption.
When the micro is interrupted "a record" of what it was doing is kept on the stack in order for the micro to resume the work where it left it.

There are three types of interrupts : hardware interrupts, exception interrupts and software interrupts.
You have already heard a lot about hardware and software interrupts.

Exception interrupts are generated when during the execution of a program the chip finds an instruction that, for example doesn't exist in its "repertoire" or when we are trying to divide by zero. In the previous cases the chip generates an "exception interrupt" to abort what it was doing ,that was irreparably flawed, and recover itself from the difficulty.

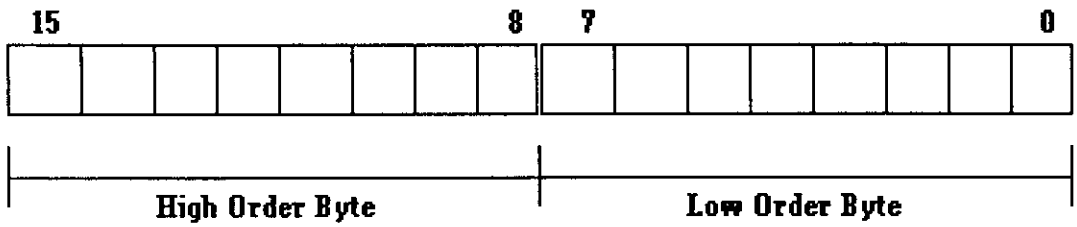
FLAGS

GENERAL PURPOSE REGISTERS

AX	AH	AL
BX	BH	BL
CX	CH	CL
DX	DH	DL

SP- Stack Pointer
BP- Base Pointer
SI- Source Index
DI- Destination Index
PC- Program Counter

CS- Code Segment
DS- Data Segment
SS- Stack Segment
ES- Extra Segment



A single 16 bit register comprised og two eight bit bytes

Intel 80286

-High speed CHMOS technology

-16 bit internal/external architecture

-16 Mby memory addressing

-14 word register set

-8 operand addressing modes

-byte, word and block operations

-12 MHz clock (5 times faster than a 5 MHz 8088)

-Minimum/Maximum operation modes

-Upward software compatibility with 8088

-Protected virtual address mode. 4 levels of privilege
for Kernel, System services, Op Sys Extensions, Applications

ROM-BIOS (Basic Input Output Service routines)

-Interrupt-driven service calls

-BIOS routines are re-entrant

-Service routines are grouped by speciality within the same interrupt level

BIOS service routines

-Boot strap service

-Equipment list

-Time services

-Video service

-Print-screen

-Memory size

-Disk services

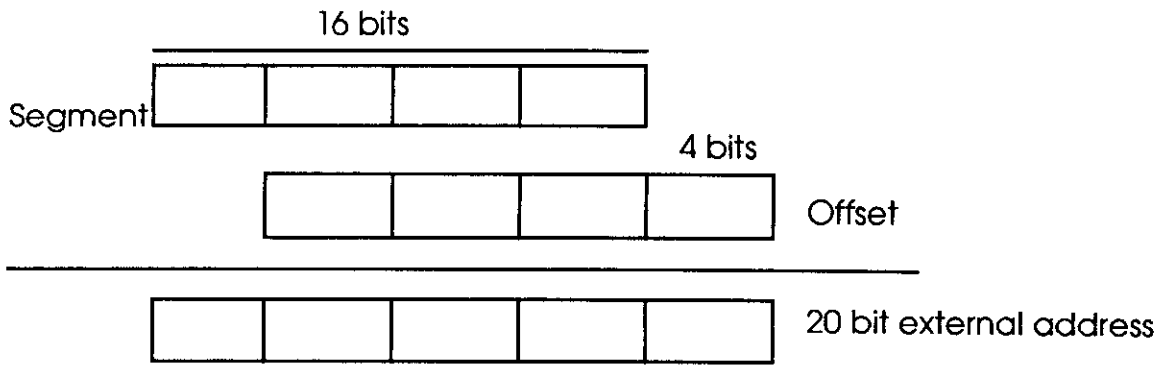
-Serial port (RS-232) service

-Parallel port service

-Keyboard service

-Tape service

Memory models



Six well known memory models

Tiny: code, data and stack fit in 64K. CS,DS,SS,ES are set to the same constant segment

Small: Uses two different segments one for code (CS) and another one for data and stack (DS,SS,ES)

Medium: Data segment fixed, allowing only 64K. Code segment can be variable

Compact: The inverse of Medium model

Large: Variable segments for either code and data

Huge: Variable segments for either code and data. Static data allowed to be > 64K

Large and huge also differ in the way they increment the segment and offset when used from a high level language compiler.

PC Memory issues

-real memory space 1Mby

-user working memory area 640 Kby

Memory expansion

-extended memory

    -virtual memory - VDISK

    -protected mode

-expanded memory

    EMM memory manager

PC limitations

Memory addressing

-AT 286 can install 16 Mby of memory in extended space

-VDISK can access that memory as virtual memory with limitations

-DOS lives in a 1 Mby memory space

-Printer spoolers and TSR (resident) programs make things worse

Static Memory manager

-DOS was built based on a CPU with no memory management capabilities

-Once loaded, DOS applications "own" the physical memory and they cannot be moved around.

Memory integrity

-DOS sees the memory as a single block.

-DOS makes no distinction between user and operating system or privileged applications.

-Application errors usually affect the entire system and halt the machine, avoiding the possibility of debugging the error.

-Multitasking systems need protection between user memory and system memory.

PC limitations

I/O control

-DOS I/O devices are accessed by interrupts to the BIOS

-Since there are no privileges in DOS, applications can modify the interrupt vector table and configure their own drivers

-This practice is forbidden in a multitasking system

Multitasking

-Multitasking in DOS is almost impossible because it is not re-entrant

-Multiple tasks under DOS using the mechanism of PC-DOS I/O extension are impossible to coexist.

The OS/2 environment

-Runs the 286 processor in protected mode

-Allows 16 Mby of real (physical) memory

-Virtual memory support. Segment swapping, page fault.

-Memory isolation/protection. User programs are terminated when violate user memory rules.

-Provides user program error debugging

-I/O protection

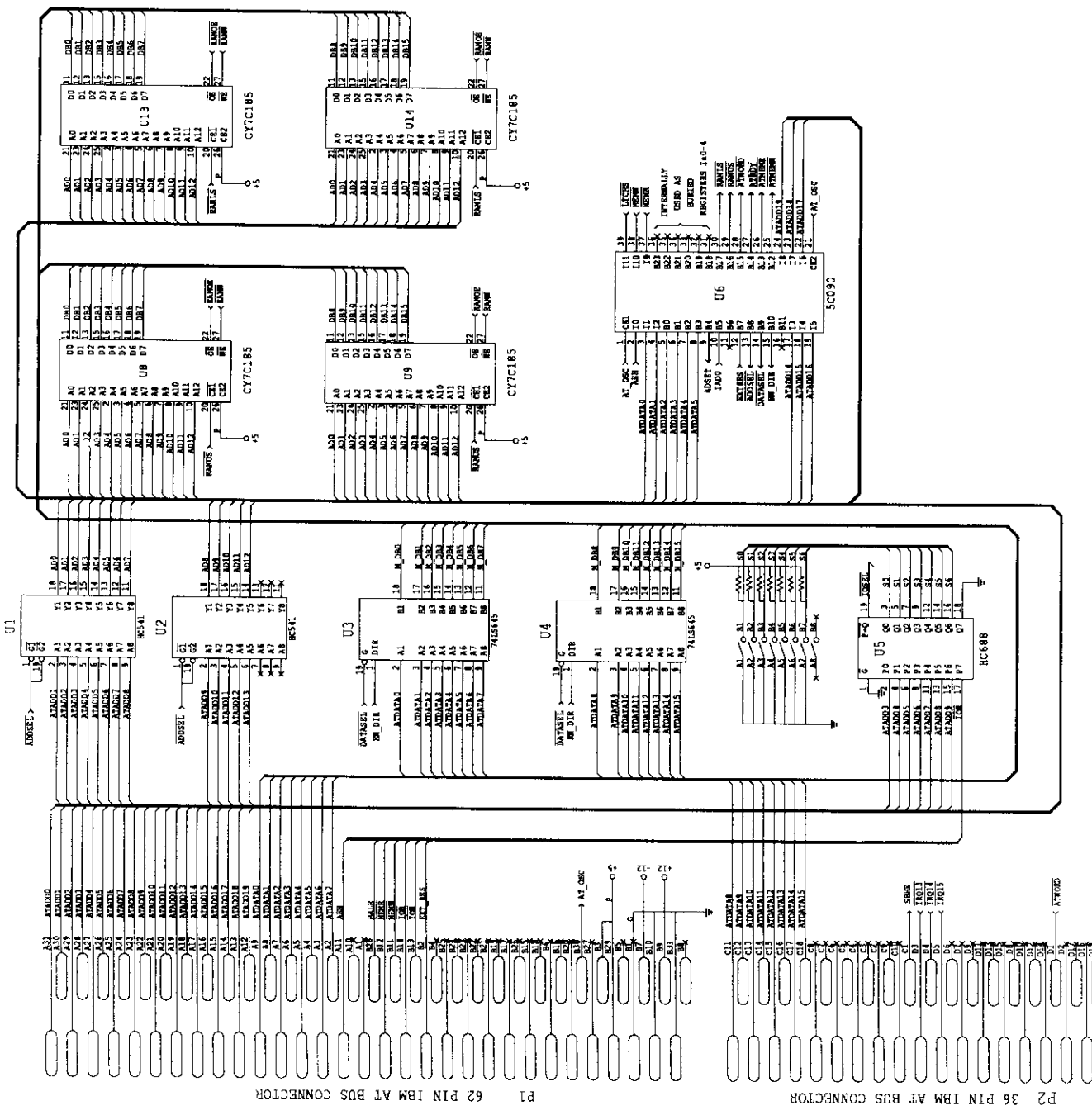
Design of an AT-PC board interface

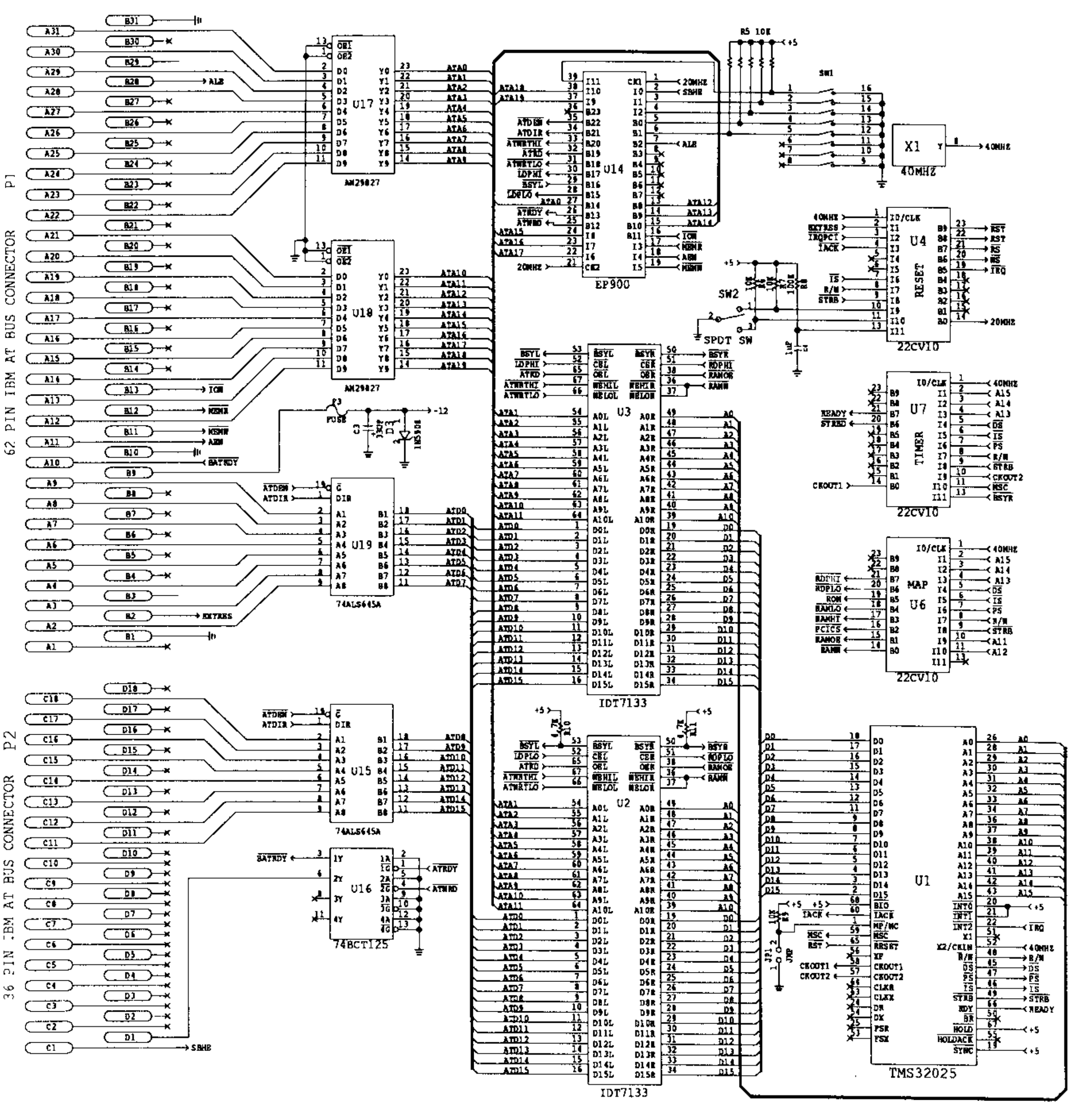
-I/O location configurable by switches.

-Software configurable Dual Port Memory in PCs memory space.

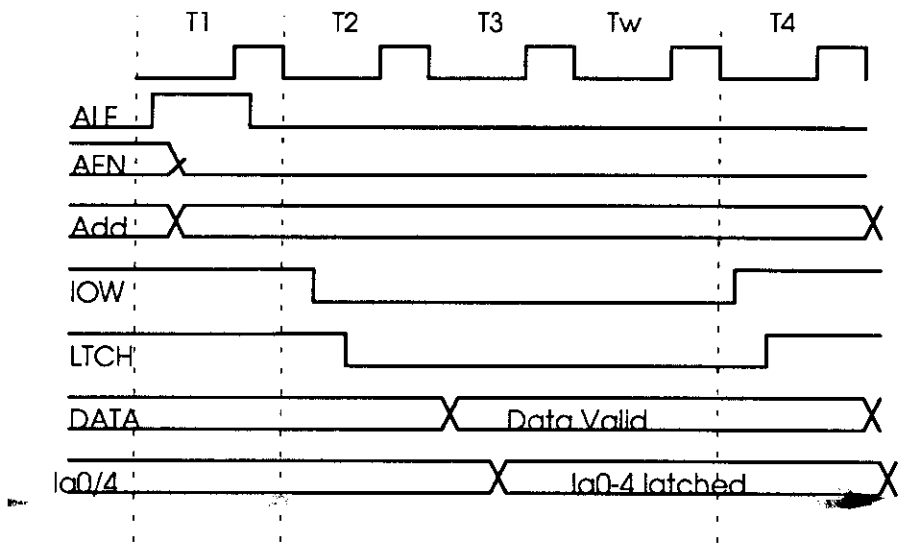
-High speed access. 0 wait state.

-Low power consumption. HCMOS technology.


P1 62 PIN IBM AT BUS CONNECTOR
P2 36 PIN IBM AT BUS CONNECTOR


62 PIN IBM AT BUS CONNECTOR P1
36 PIN IBM AT BUS CONNECTOR P2
U17
AM29827
U18
AM29827
U14
EP900
U3
IDT7133
U2
IDT7133
U19
74ALS645A
U15
74ALS645A
U16
74BCT125
U4
RESET
22CV10
U7
TIMER
22CV10
MAP
U6
22CV10
U1
TMS32025
X1
40MHZ
SW1
SW2
SPDT SW
R5 10K
FUSE
1N5908

I/O write timming diagram



I/O write timming diagram

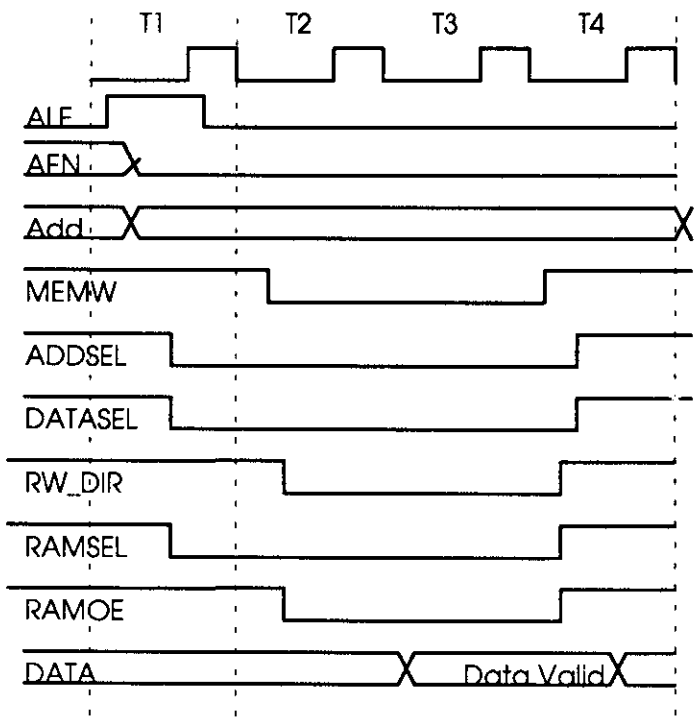


FIG. 2 EP900 BLOCK DIAGRAM

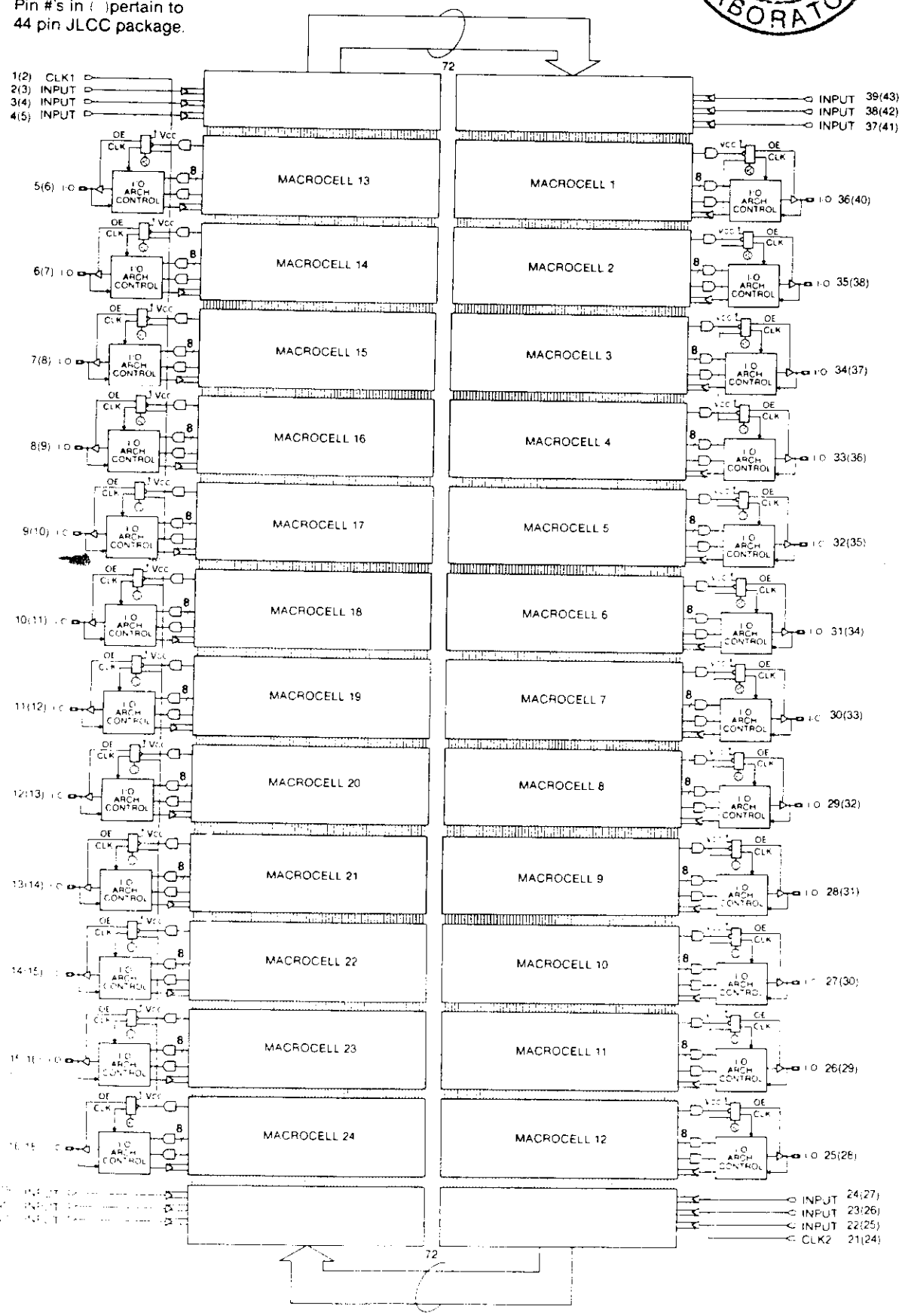
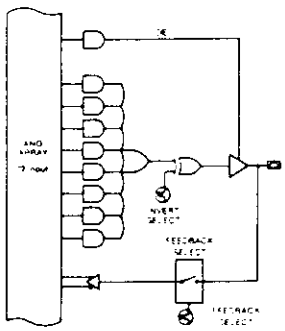


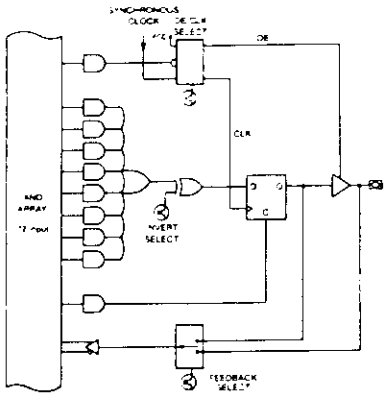
Figure 4. I/O Configurations



COMBINATORIAL

I/O SELECTION

OUTPUT/POLARITY	FEEDBACK
Combinatorial: High	Pin, None
Combinatorial/Low	Pin, None
None	Pin



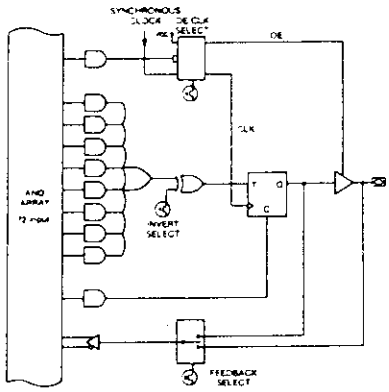
D-TYPE FLIP-FLOP

I/O SELECTION

OUTPUT/POLARITY	FEEDBACK
D-Register/High	D-Register, Pin, None
D-Register/Low	D-Register, Pin, None
None	D-Registered
None	Pin

FUNCTION TABLE

D	Q_n	Q_{n-1}
0	0	0
0	1	0
1	0	1
1	1	1



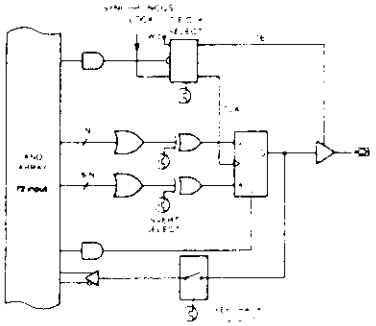
TOGGLE FLIP-FLOP

I/O SELECTION

OUTPUT/POLARITY	FEEDBACK
T-Register / High	T-Register, Pin, None
T-Register / Low	T-Register, Pin, None
None	T-Register
None	Pin

FUNCTION TABLE

T	Q_n	Q_{n-1}
0	0	0
0	1	1
1	0	1
1	1	0



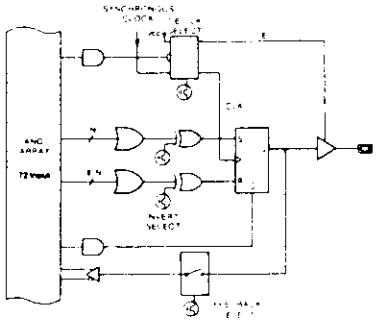
JK FLIP-FLOP

I/O SELECTION

OUTPUT/POLARITY	FEEDBACK
JK Register/High	JK Register, None
JK Register/Low	JK Register, None
None	JK Register

FUNCTION TABLE

J	K	Q_n	Q_{n-1}
0	0	0	0
0	0	1	1
0	1	0	0
0	1	1	0
1	0	0	1
1	0	1	1
1	1	0	1
1	1	1	0



SR FLIP-FLOP

I/O SELECTION

OUTPUT/POLARITY	FEEDBACK
SR Register/High	SR Register, None
SR Register/Low	SR Register, None
None	SR Register

FUNCTION TABLE

S	R	Q_n	Q_{n-1}
0	0	0	0
0	0	1	1
0	1	0	0
0	1	1	0
1	0	0	1
1	0	1	1

31

THE IBM PC BUS (I/O CHANNEL)

The IBM bus (I/O channel) is a set of 62 lines connected to five card-edge connectors. Non system hardware is added to the PC by simply plugging cards into the connectors. (see pin-out in next transparency)

The lines can be classified according to the function they perform : (details in the IBM spec-sheets)

Address - A0-A19

Data - D0-D7

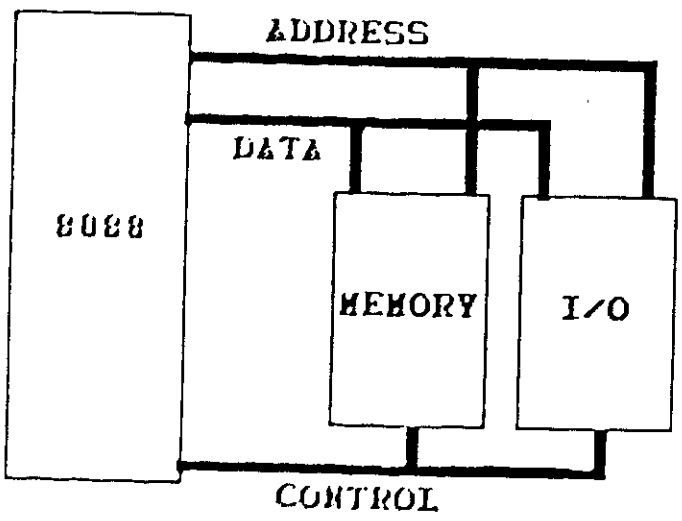
Control - MEMW, MEMR, IOR, IOW (All active low), ALE, AEN, I/O CH RDY, RESET DRV

Direct Memory Addressing (DMA) - DRQ1-DRQ3, DACK1-DACK3, TC

Interrupt - IRQ2-IRQ7

Clocks - OSC, CLK

Power Supply - +5, -5, +12, -12, GND



The address lines are 20. They can code memory addresses from 00000h to FFFFFh (1 Mb).

But only 16 lines are active during an I/O cycle . This limits the I/O port to addresses from 0000h to 0FFFFh (64 k). In the IBM PC only the lower 10 of these lines are decoded during an I/O instruction limiting further the range of I/O channels to 1 k.

The main control lines needed to connect an I/O card are :

IOR I/O read, active low during I/O read.
IOW I/O write, active low during I/O write.

A memory read or write cycle uses four clock cycles while an I/O read or write uses five clock cycles that can even be complemented by several wait cucles under request from the I/O card.

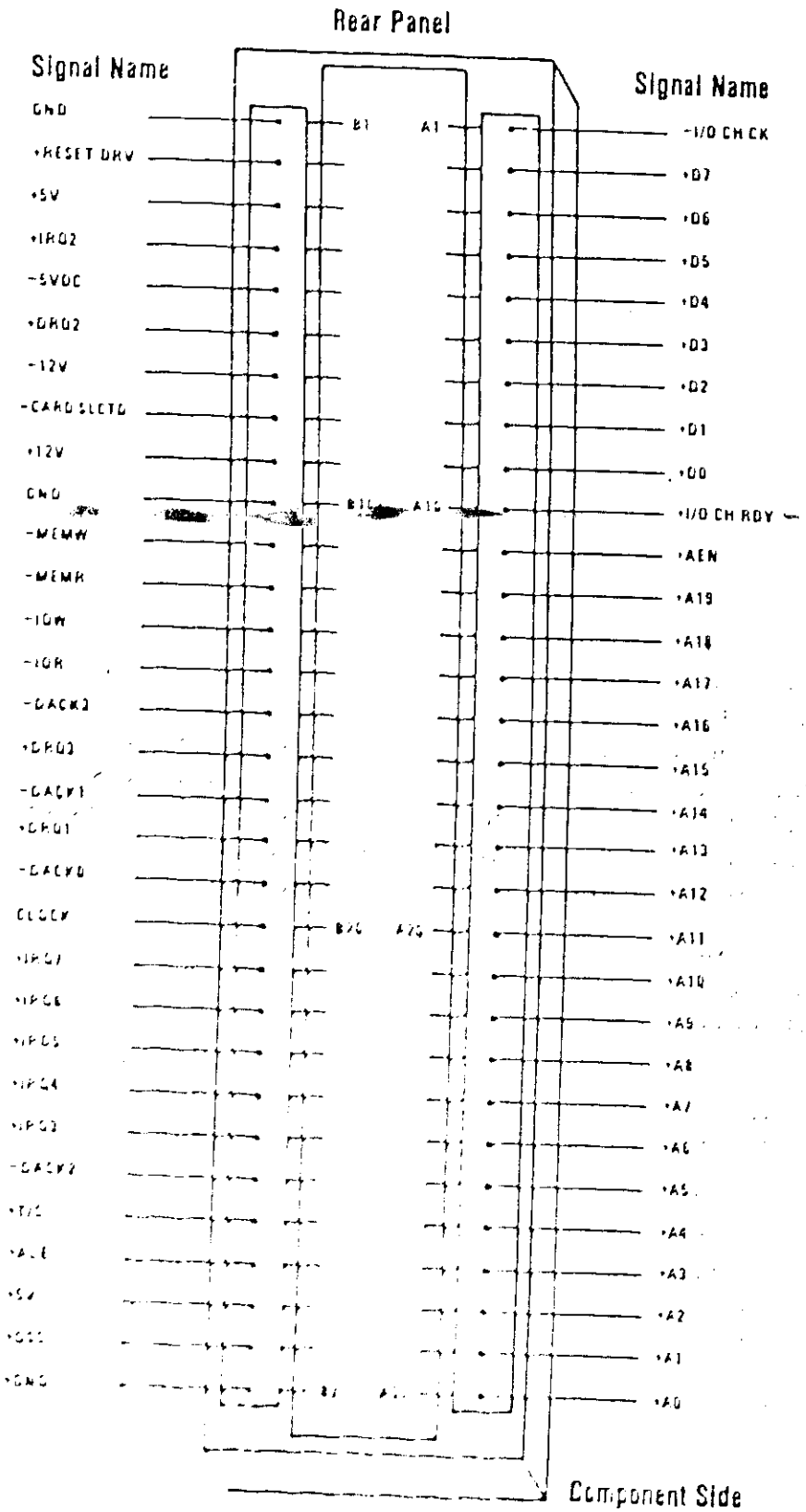
PROCESSOR INITIATED BUS CYCLES

Designing an interface requires a good understanding of bus cycles and of its timing restrictions.

We are only interested in I/O read and write cycles although a memory cycle is not much different.

The clock signal is a 2 to 1 mark space ratio with a low time of 140 ns and a high of 70. A single bus access requires five clock cycles. Hence, an I/O cycle can be completed in a minimum of 1.02 microsec at 4.77 MHz.

You can extend the I/O read-write cycle by a period asserting the I/I CH RDY line .The PC senses this level on the leading edge of T2.



I/O Channel Diagram

I/O Channel Description

The following is a description of the IBM Personal Computer XT I/O Channel. All lines are TTL-compatible.

Signal	I/O	Description
OSC	O	Oscillator: High-speed clock with a 70-ns period (14.31818 MHz). It has a 50% duty cycle.
CLK	O	System clock: It is a divide-by-three of the oscillator and has a period of 210 ns (4.77 MHz). The clock has a 33% duty cycle.
RESET DRV	O	This line is used to reset or initialize system logic upon power-up or during a low line voltage outage. This signal is synchronized to the falling edge of clock and is active high.
A0-A19	O	Address bits 0 to 19: These lines are used to address memory and I/O devices within the system. The 20 address lines allow access of up to 1 megabyte of memory. A0 is the least significant bit (LSB) and A19 is the most significant bit (MSB). These lines are generated by either the processor or DMA controller. They are active high.
D0-D7	I/O	Data Bits 0 to 7: These lines provide data bus bits 0 to 7 for the processor, memory, and I/O devices. D0 is the least significant bit (LSB) and D7 is the most significant bit (MSB). These lines are active high.
ALE	O	Address Latch Enable: This line is provided by the 8288 Bus Controller and is used on the system board to latch valid addresses from the processor. It is available to the I/O channel as an indicator of a valid processor address (when used with AEN). Processor addresses are latched with the failing edge of ALE.
$\overline{\text{I/O CH CK}}$	I	-I/O Channel Check: This line provides the processor with parity (error) information on memory or devices in the I/O channel. When this signal is active low, a parity error is indicated.

Signal	I/O	Description
I/O CH RDY	I	I/O Channel Ready: This line, normally high (ready), is pulled low (not ready) by a memory or I/O device to lengthen I/O or memory cycles. It allows slower devices to attach to the I/O channel with a minimum of difficulty. Any slow device using this line should drive it low immediately upon detecting a valid address and a read or write command. This line should never be held low longer than 10 clock cycles. Machine cycles (I/O or memory) are extended by an integral number of CLK cycles (210 ns).
IRQ2-IRQ7	I	Interrupt Request 2 to 7: These lines are used to signal the processor that an I/O device requires attention. They are prioritized with IRQ2 as the highest priority and IRQ7 as the lowest. An Interrupt Request is generated by raising an IRQ line (low to high) and holding it high until it is acknowledged by the processor (Interrupt service routine).
$\overline{\text{IOR}}$	O	-I/O Read Command: This command line instructs an I/O device to drive its data onto the data bus. It may be driven by the processor or the DMA controller. This signal is active low.
$\overline{\text{IOW}}$	O	-I/O Write Command: This command line instructs an I/O device to read the data on the data bus. It may be driven by the processor or the DMA controller. This signal is active low.
$\overline{\text{MEMR}}$	O	Memory Read Command: This command line instructs the memory to drive its data onto the data bus. It may be driven by the processor or the DMA controller. This signal is active low.
$\overline{\text{MEMW}}$	O	Memory Write Command: This command line instructs the memory to store the data present on the data bus. It may be driven by the processor or the DMA controller. This signal is active low.

Signal	I/O	Description
DRQ1-DRQ3	I	DMA Request 1 to 3: These lines are asynchronous channel requests used by peripheral devices to gain DMA service. They are prioritized with DRQ3 being the lowest and DRQ1 being the highest. A request is generated by bringing a DRQ line to an active level (high). A DRQ line must be held high until the corresponding DACK line goes active.
$\overline{\text{DACK0}}$-$\overline{\text{DACK3}}$	O	-DMA Acknowledge 0 to 3: These lines are used to acknowledge DMA requests (DRQ1-DRQ3) and to refresh system dynamic memory (DACK0). They are active low.
AEN	O	Address Enable: This line is used to de-gate the processor and other devices from the I/O channel to allow DMA transfers to take place. When this line is active (high), the DMA controller has control of the address bus, data bus, read command lines (memory and I/O), and the write command lines (memory and I/O).
T/C	O	Terminal Count: This line provides a pulse when the terminal count for any DMA channel is reached. This signal is active high.
$\overline{\text{CARD SLCTD}}$	I	-Card Selected: This line is activated by cards in expansion slot J8. It signals the system board that the card has been selected and that appropriate drivers on the system board should be directed to either read from, or write to, expansion slot J8. Connectors J1 through J8 are tied together at this pin, but the system board does not use their signal. This line should be driven by an open collector device.

The following voltages are available on the system-board I/O channel:

+5 Vdc ± 5%, located on 2 connector pins
-5 Vdc ± 10%, located on 1 connector pin
+12 Vdc ± 5%, located on 1 connector pin
-12 Vdc ± 10%, located on 1 connector pin
GND (Ground), located on 3 connector pins

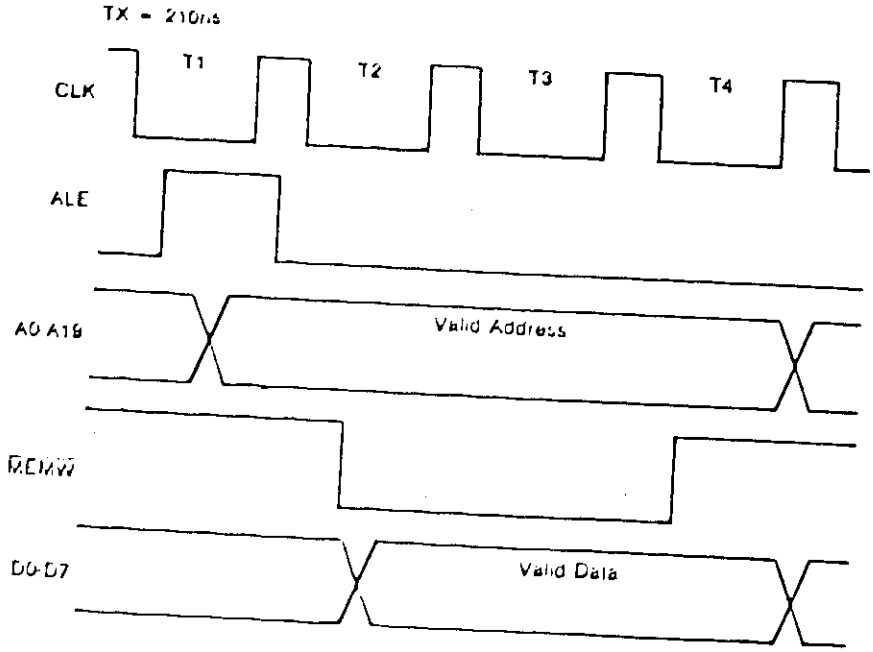


Figure 14.5 Memory-Write Bus Cycle

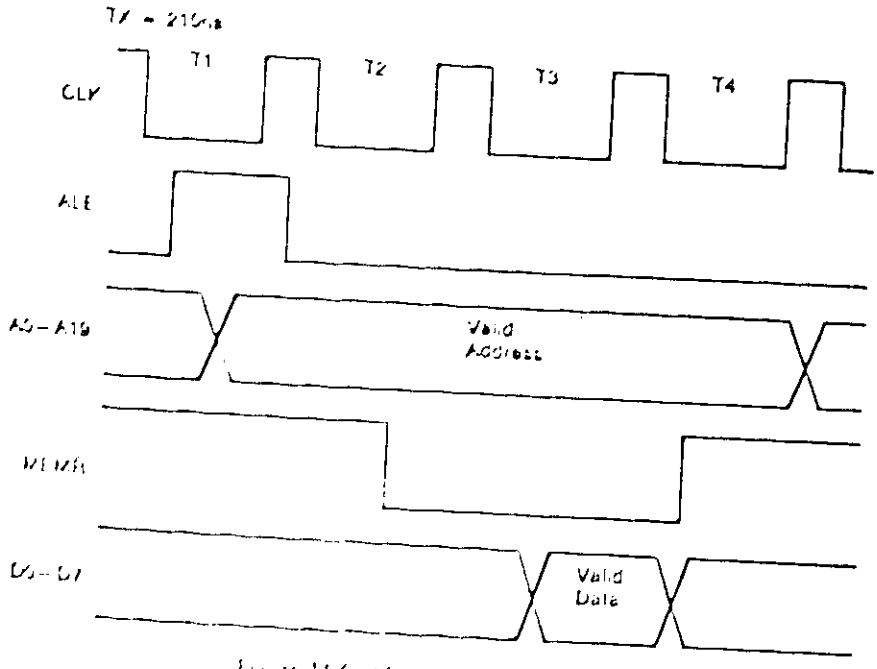
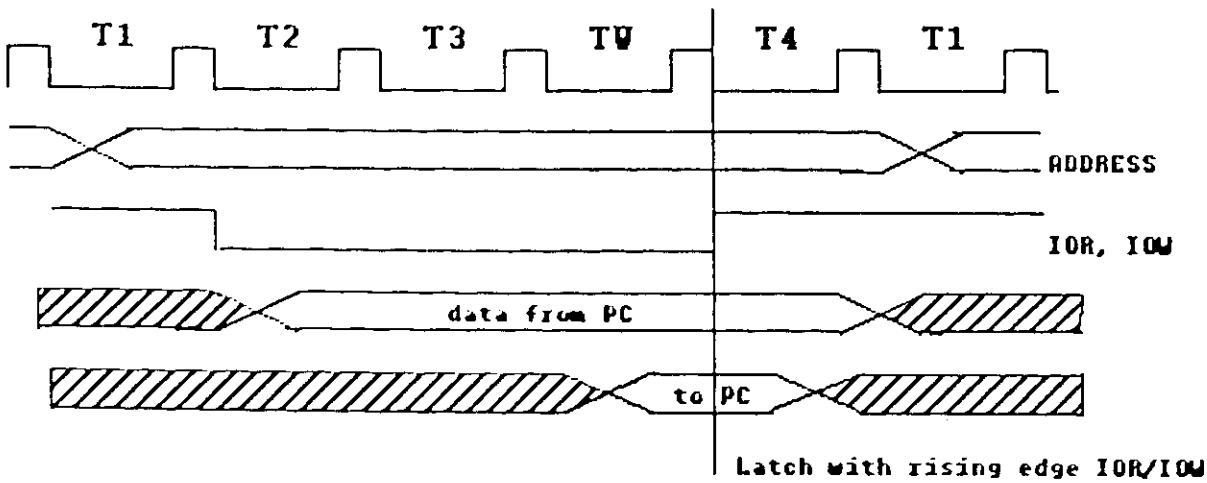


Figure 14.6 Memory-Read Bus Cycle



I/O cycle , Ti210 ns. No I/O CH RDY asserted else TW1 would be inserted before TW.

As we said before, the IBM PC has the annoying restriction that only A0-A9 are decoded when performing I/O. IBM assigns standard I/O locations to many devices in this 1 k space. These assignments are shown in the corresponding table. A free address position has to be found before plugging in a card.