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UNITED NATIONS INDUSTRIAL DEVELOPMENT ORGANIZATION

INTERNATIONAL CENTRE FOR SCIENCE AND HIGH TECHNOLOGY

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SMR/643 - 4

SECOND COLLEGE ON
MICROPROCESSOR-BASED REAL-TIME CONTROL -
PRINCIPLES AND APPLICATIONS IN PHYSICS
5 - 30 October 1992

RECALL OF THE M6809 ROSY JUNIOR & Assembly Language Programming

(Part 1)

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Recall of the M6809, ROSY Junior & Assembly Language Programming

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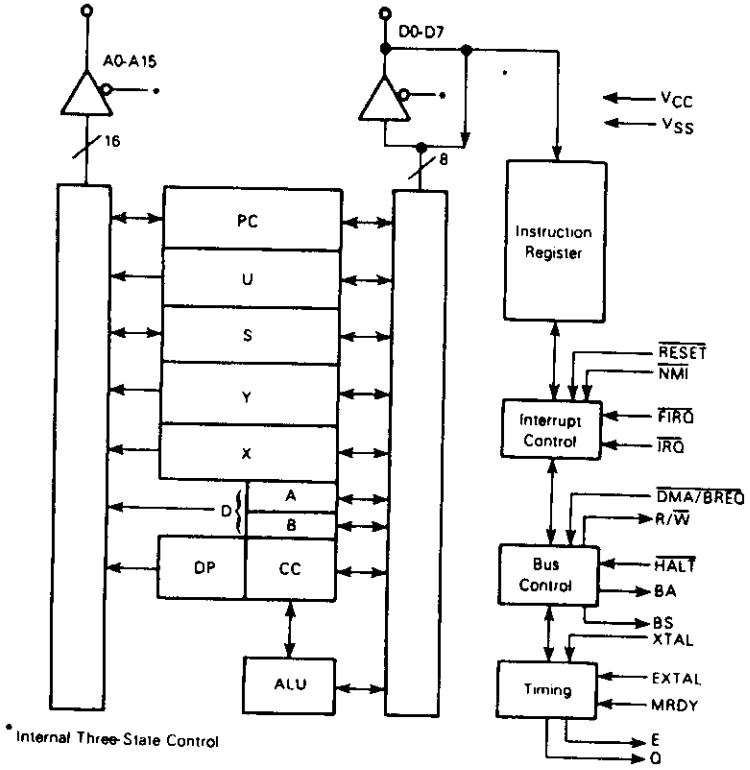
Outline of Lectures

- Recall of the M6809 System
  - ➢ Microprocessor
  - ➢ Parallel and Serial Interface Adapters
  - ➢ Programmable Timer
  - ➢ Memory Devices
  - ➢ Floppy Disk Controller
  - ➢ Direct Memory Access Controller
- ROSY Junior
  - ➢ System Overview
  - ➢ Memory Subsystem
  - ➢ Peripheral Subsystem
  - ➢ Disk System
- Recall of Assembly Language Programming
  - ➢ M6809 Instruction Set Summary
  - ➢ Examples of Assembly Language Programs
  - ➢ The OS-9 Assembler

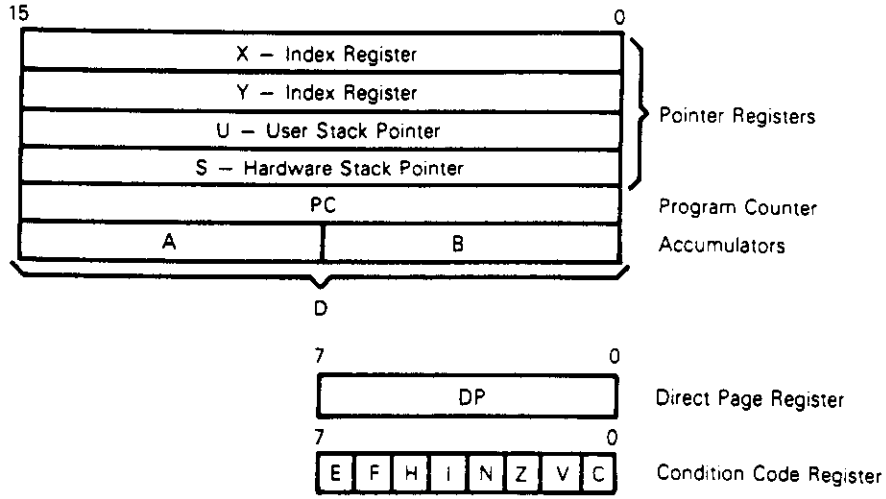
Highlights of M6809

- **Hardware**
  - Clock: 1, 1.5 or 2 MHz (on-chip oscillator or external)
  - Address bus: 16 lines; data bus: 8 lines
  - Interrupts: NMI, FIRQ, IRQ
  - Features for DMA & slow memory access
  - Synchronization to external event
  - M6800 family compatible
- **Software**
  - 10 addressing modes
  - 59 opcodes, 1464 instructions
  - 16-bit arithmetic, 8×8 unsigned multiplication
  - Good stack manipulation
  - Load effective address

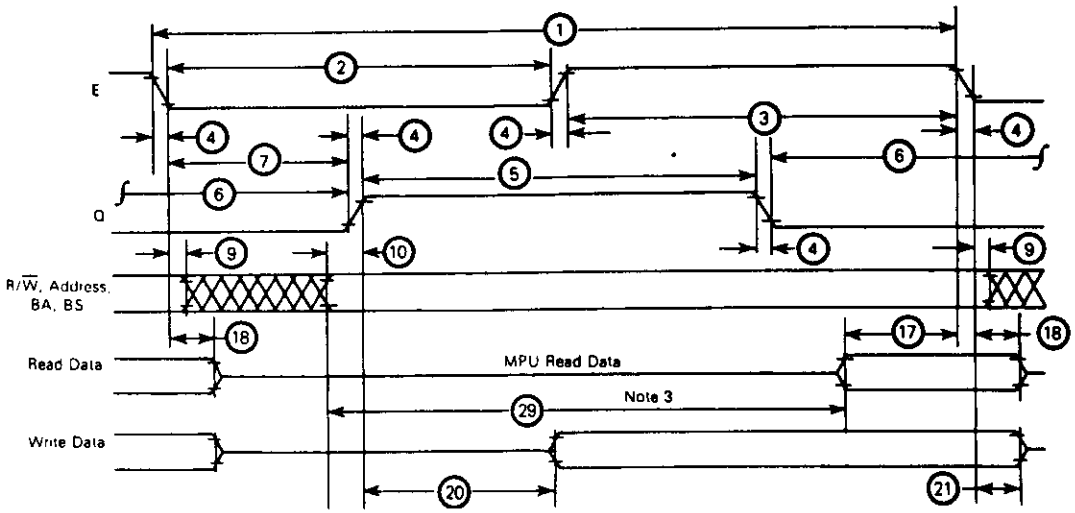
MC6809 Block Diagram



M6809 Programming Model



M6809 Bus Timing



BUS TIMING CHARACTERISTICS (See Notes 1 and 2)

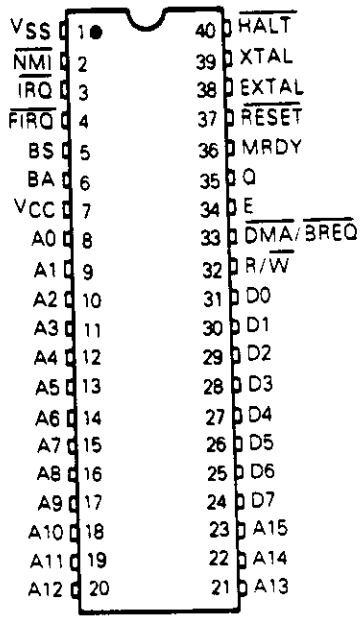
Ident. Number	Characteristics	Symbol	MC6809		MC68A09		MC68B09		Unit
			Min	Max	Min	Max	Min	Max	
1	Cycle Time (See Note 5)	t_{cyc}	1.0	10	0.667	10	0.5	10	µs
2	Pulse Width, E Low	PW_{EL}	430	5000	280	5000	210	5000	ns
3	Pulse Width, E High	PW_{EH}	450	15500	280	15700	220	15700	ns
4	Clock Rise and Fall Time	t_r, t_f	–	25	–	25	–	20	ns
5	Pulse Width, Q High	PW_{QH}	430	5000	280	5000	210	5000	ns
6	Pulse Width, Q Low	PW_{QL}	450	15500	280	15700	220	15700	ns
7	Delay Time, E to Q Rise	t_{AVS}	200	250	130	165	80	125	ns
9	Address Hold Time* (See Note 4)	t_{AH}	20	–	20	–	20	–	ns
10	BA, BS, R/W, and Address Valid Time to Q Rise	t_{AQ}	50	–	25	–	15	–	ns
17	Read Data Setup Time	t_{DSR}	80	–	60	–	40	–	ns
18	Read Data Hold Time*	t_{DHR}	10	–	10	–	10	–	ns
20	Data Delay Time from Q	t_{DDQ}	–	200	–	140	–	110	ns
21	Write Data Hold Time*	t_{DHW}	30	–	30	–	30	–	ns
29	Usable Access Time (See Note 3)	t_{ACC}	695	–	440	–	330	–	ns
	Processor Control Setup Time (MRDY, Interrupts, DMA/BREQ, HALT, RESET) (Figures 6, 8, 9, 10, 12, and 13)	t_{PCS}	200	–	140	–	110	–	ns
	Crystal Oscillator Start Time (Figures 6 and 7)	t_{RC}	–	100	–	100	–	100	ms
	Processor Control Rise and Fall Time (Figures 6 and 8)	t_{PCr}, t_{PCf}	–	100	–	100	–	100	ns

*Address and data hold times are periodically tested rather than 100% tested.

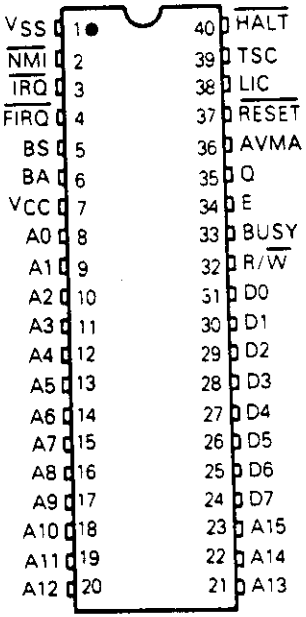
NOTES
1. Voltage levels shown are V_L 0.4 V, V_H 2.4 V, unless otherwise specified.
2. Measurement points shown are 0.8 V and 2.0 V, unless otherwise specified.
3. Usable access time is computed by: 1 4 7 max 10 17

Differences between MC6809 & MC6809E

MC6809



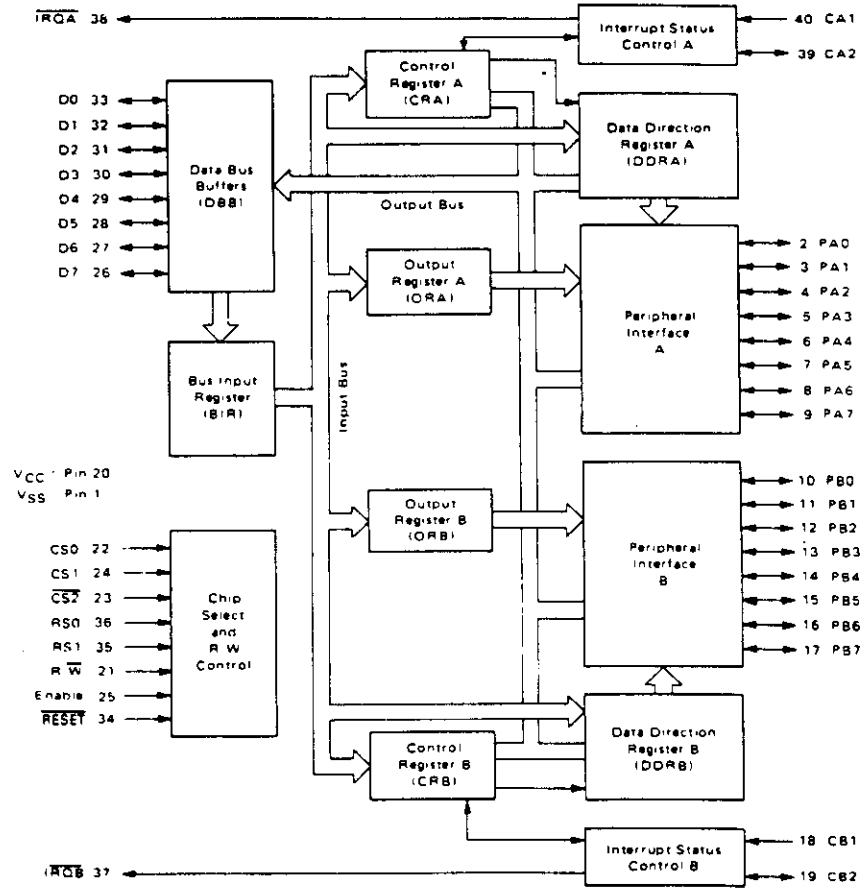
MC6809E



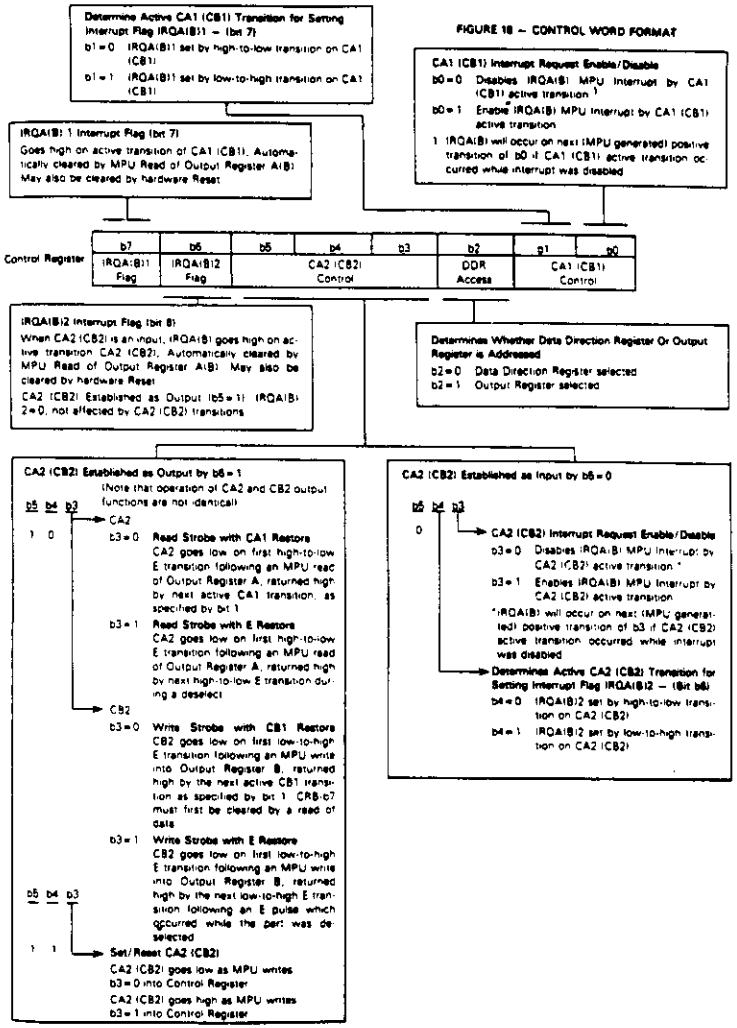
Highlights of MC6821 PIA

- Peripheral Interface Adapter that provides *universal* means of interfacing with a high degree of flexibility
- 8-bit data bus for communicating with MPU
- Two 8-bit I/O ports with handshake control logic
- Two programmable control registers
- Two programmable data direction registers
- Four individually controlled interrupt input lines, two usable as peripheral control outputs
- Handshake control logic for input and output peripheral operation
- Program controlled interrupt and interrupt disable capability
- high impedance tri-state and direct transistor drive peripheral lines

MC6821 PIA Block Diagram



MC6821 PIA Control Registers



PIA Programming Exercise

Write a subroutine to initialize port A of a PIA as inputs and port B as outputs. Assume that the PIA is at $EC10 – $EC13, conventional configuration.

Write an endless loop program to read the status of port A and send it to port B.

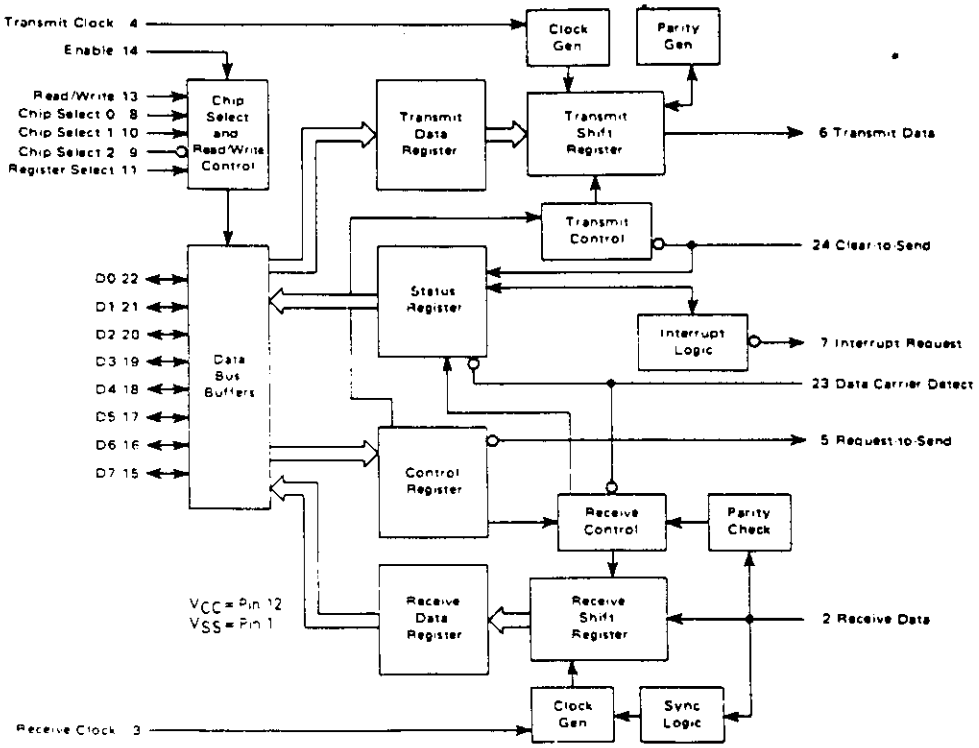
Asynchronous Communications Interface Adapter

- **Serial Communications**
  - Synchronous, BSC or *bisync*, HDLC
  - Asynchronous, RS232C or CCITT V.24
- **RS232C**
  - Serial data timing format
  - Data Terminal Equipment (DTE)
  - Data Communications Equipment (DCE)
  - Signal lines: TxD, RxD, RTS, CTS, DSR, DCD, DTR

Highlights of MC6850 ACIA

- Asynchronous Communications Interface Adapter that provides data formatting and control to interface serial asynchronous data communications information to bus organized systems.
- The parallel data of the bus system is serially transmitted and received by ACIA with proper formatting and error checking.
- A programmable control register provides variable word lengths, clock division ratios, transmit control, receive control, and interrupt control.
- Control lines are provided for peripheral or modem operation.
- 8- or 9-bit transmission.
- Optional odd or even parity.
- Parity, overrun and framing error checking.
- Optional $\div 1$, $\div 16$, and $\div 64$ clock modes.

MC6850 ACIA Block Diagram



MC6850 ACIA Control Register

7	6	5	4	3	2	1	0

Receive Int. Enable

RDBF
Overrun
$\overline{DCD}$

Transmit Control

$\overline{RTS}$	Trans. Interr.
0	Disable
0	Enable
1	Disable
0	Disable & Break

Word Select

7 + E + 2
7 + O + 2
7 + E + 1
7 + O + 1
8 + 2
8 + 1
8 + E + 1
8 + O + 1

Counter Divide Select & Master Reset

0 0	1
0 1	16
1 0	64
1 1	Master Reset (Clear Status Reg.)

MC6850 ACIA Status Register

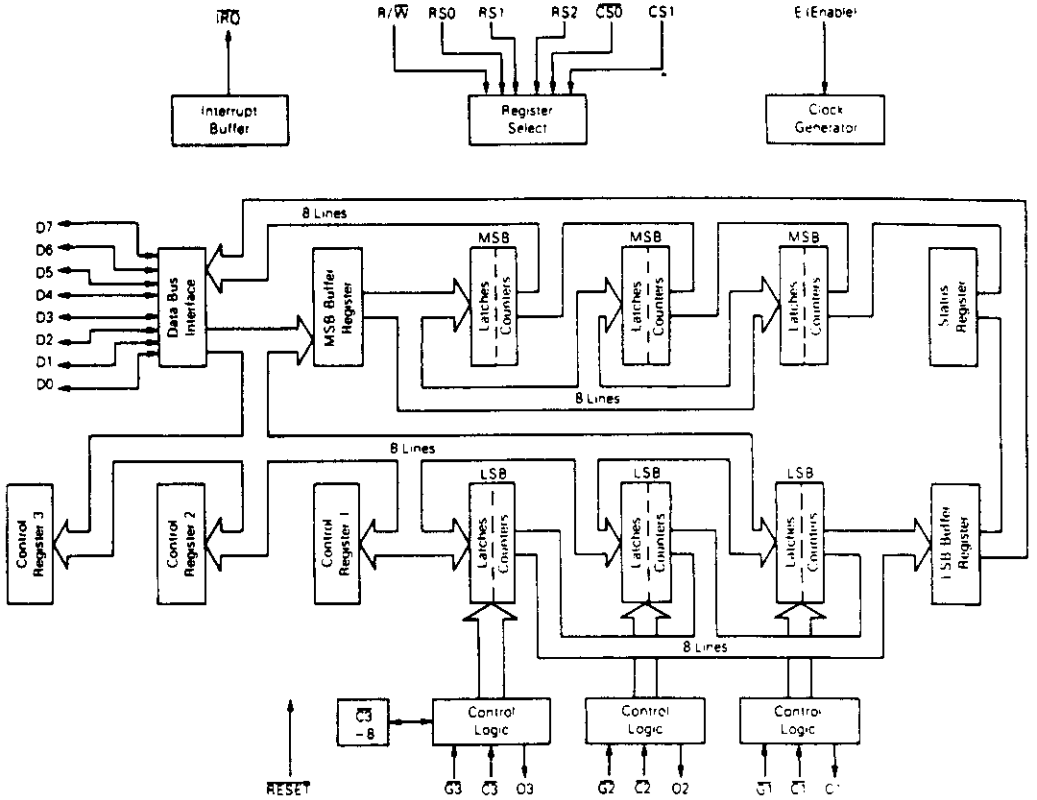
7	6	5	4	3	2	1	0
IRQ	PE	OVRN	FE	$\overline{CTS}$	$\overline{DCD}$	TDRE	RDRF

Highlights of MC6840 PTM

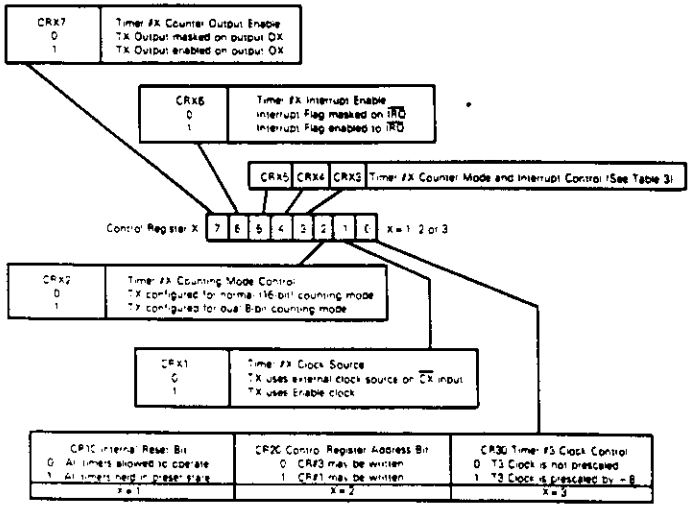
- Programmable Timer Module that provides timing and counting facility.
- Three 16-bit binary counters, three corresponding control registers, and a status register.
- Used for tasks such as frequency measurement, event counting, interval measuring, pulse generation and square wave generation.

PTM

MC6840 PTM Block Diagram



MC6840 PTM Control Register



MC6840 PTM Status Register

Bits 0, 1, and 2 are individual flag bits for Timers 1, 2, and 3 respectively.

Bit 7 is a Composite Interrupt Flag.

MC6840 PTM Timer Operating Modes

- **Wave synthesis modes**
  - Continuous operating mode
  - Single-shot
- **Wave measurement modes**
  - Frequency comparison or period measurement mode
  - Pulse width comparison mode

Read Only Memories

- Two types of high density EPROMs
- TMM27512, 64 Kbytes
- μPD27C1001D, 128 Kbytes

Random Access Memories

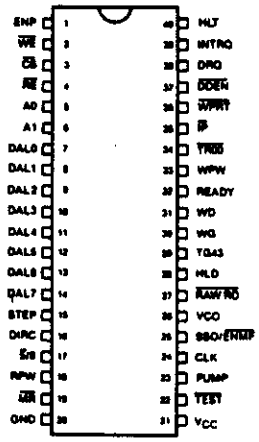
- TC55257, 32 Kbytes

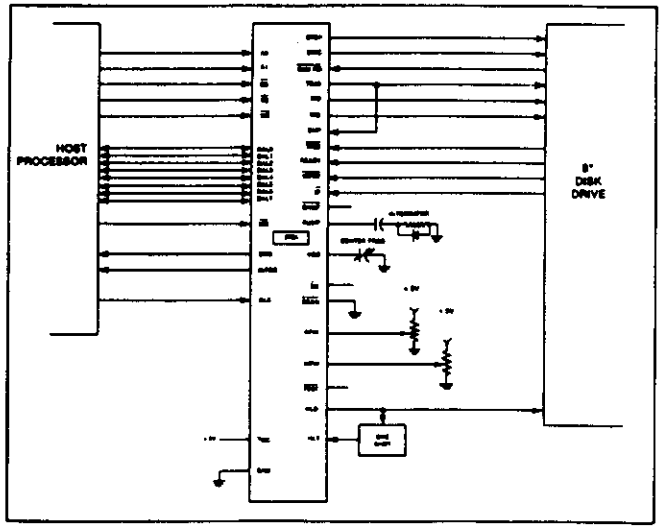
Floppy Disk Storage

- Bulk long-term storage
- Secondary storage
- Medium for programs/data transfer
- 3.5 inch microfloppy disks (1980s)
  - Capacity: 0.5 Mbytes/side, 80 tracks at 8000 bits/in
  - Track density: 48 tracks/in or 96 tracks/in
  - Data transfer rates: 125 Kbits/s or 250 Kbits/s
- Principle of recording: frequency modulation (FM) & modified frequency modulation (MFM)
- Floppy disk controller & direct memory access
- New development: perpendicular recording

WD2793 Floppy Disk Controller

- Performs the function of controller and formatter for floppy, mini-floppy and microfloppy disks.
- Accommodates single and double density formats (FM & MFM).
- Phase-lock-loop data separator.
- 8-bit bidirectional bus for data, status and control word transfer.

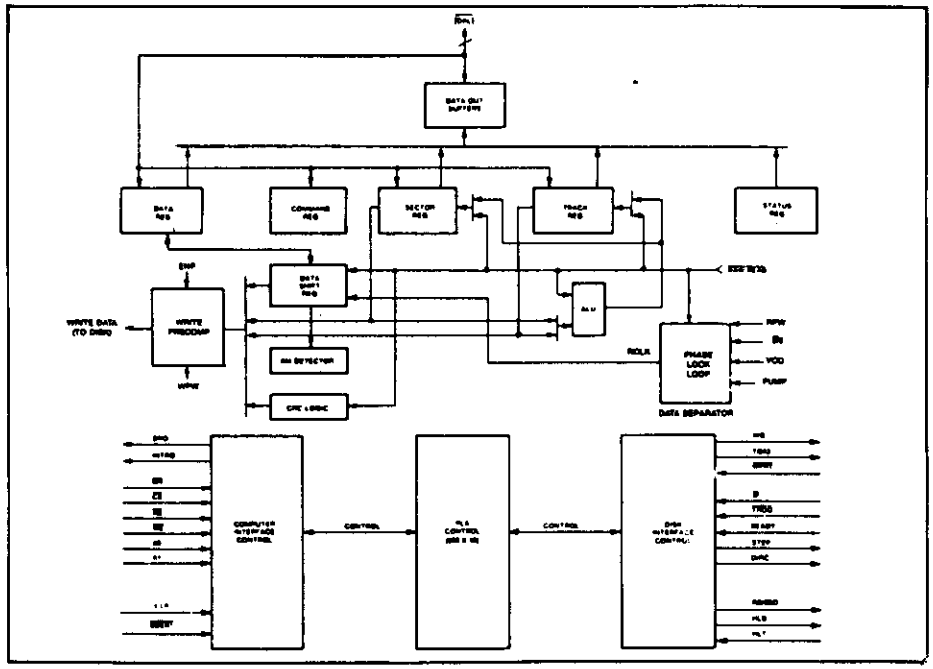




Floppy Disk Controller Interfacing

- Interfaces to processor via eight data access lines and associated control signals.
- Usual access of registers by Chip Select, Read Enable, Write Enable and two address lines.
- Interfaces to disk drive via 11 control and sensing lines.

FDC Block Diagram



Functions of FDC

- Test function.
- Sector lengths: 128, 256, 512 or 1024 bytes.
- Cyclic redundancy check (V.41): $G(x) = x^{16} + x^{12} + x^5 + 1$
- Commands: Restore, seek, step, step-in, step-out, read sector, write sector, read address, read track, write track, force interrupt.
- IBM standards. IBM3740: 128 bytes, 26 sectors/track. System 34: 256 bytes, 26 sectors/track.

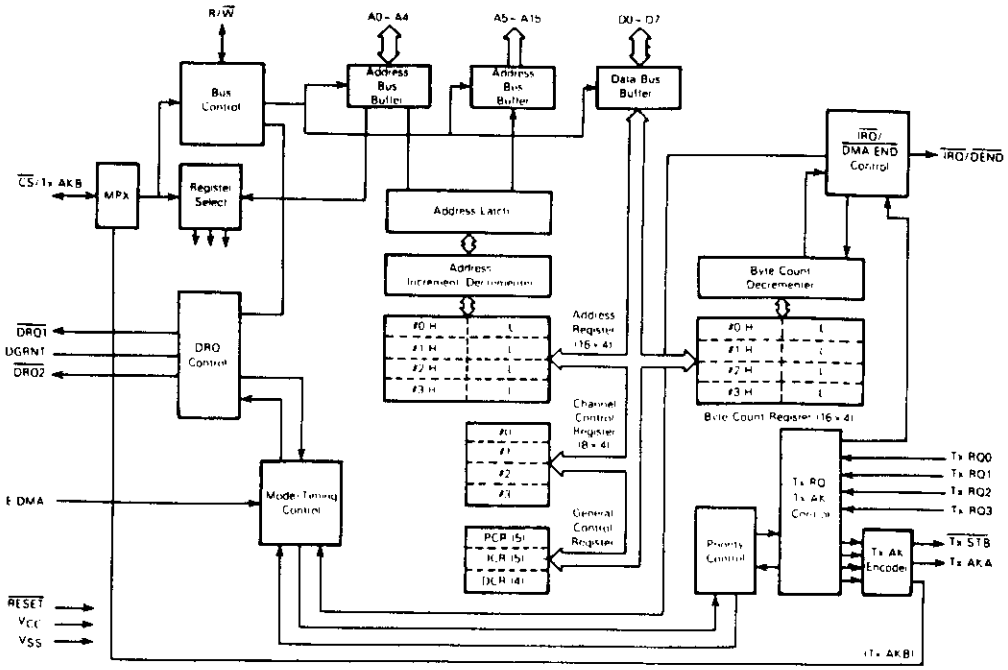
Direct Memory Access

- Necessity of DMA.
- Direct Memory Access Controller (DMAC) transfers data directly between memory and peripheral device controller such as the FDC by taking over the control of address and data bus of MPU.
- In ROSY Junior the data rate is 125 Kbits/s or 250 Kbits/s.

Highlights of MC6844 DMAC

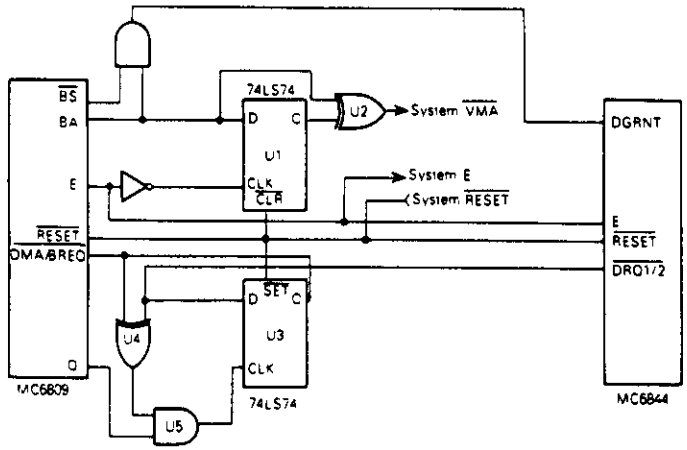
- A direct memory access controller for the M6800 family.
- Four DMA channels, each can be independently configured.
- Each channel: 16-bit address register and 16-bit byte counter register.
- 2 Mbytes/s maximum data transfer.
- Fixed or rotating priority service control.
- Data chain function for large burst of data.

MC6844 DMAC Block Diagram



MC6844 DMAC Functions

- Software initialization
- Hardware initialization
- Bus control
- Transfer modes
- MC6844/MC6809 bus arbitration



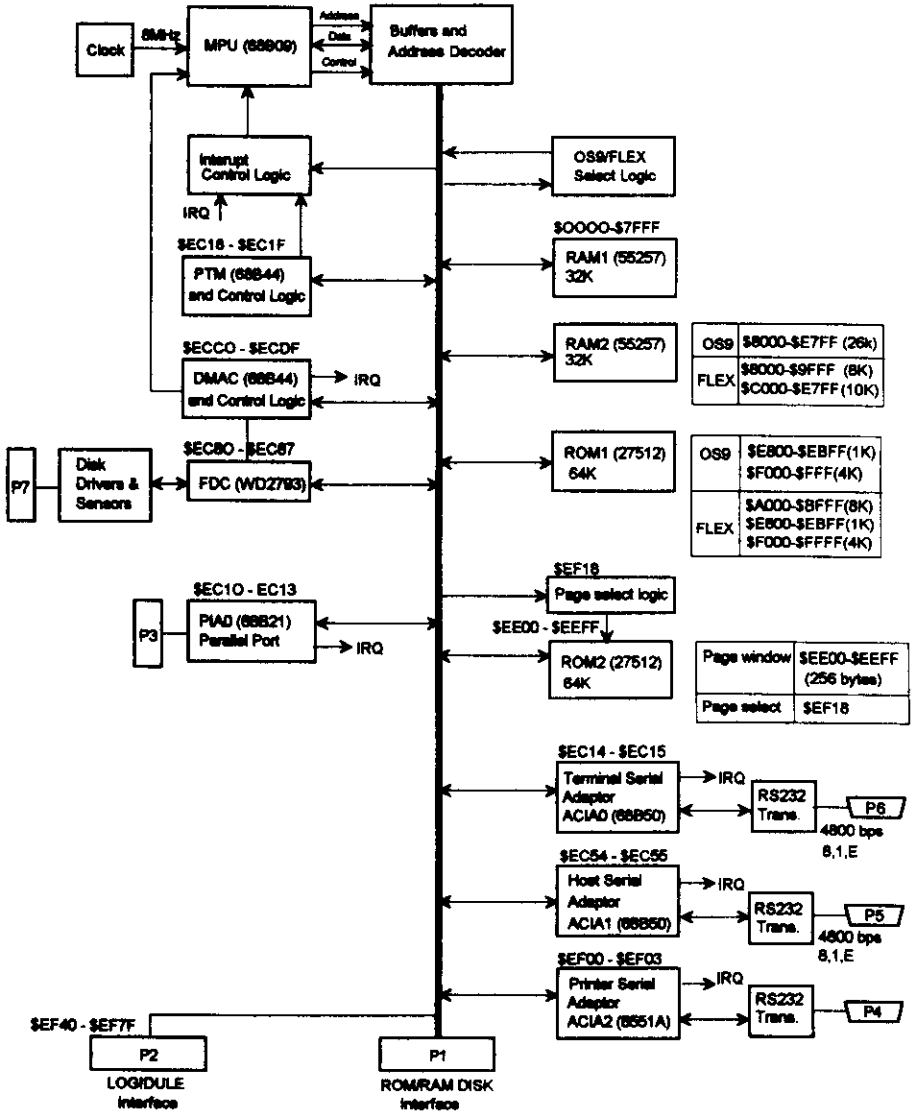
ROSY Junior Overview

- A bit of history
- A 6809 development system featuring
  - Dual microfloppy disks
  - Virtual disks
  - Resident OS - ROSY
  - DOS — FLEX & OS-9
  - Two-page memory
  - Compact design
  - Compatible with ROSY

ROSY Junior Hardware Features

- MC68B09 2 MHz MPU
- 128 Kbytes EPROM (2 pages)
- 64 Kbytes RAM (2 pages)
- Two 3.5 in floppy disks (single & double density)
- Three serial links for terminal, host & printer
- One parallel interface for general use
- Extension bus
- Plugged-on memory unit with 640 Kbytes EPROM & 160 Kbytes RAM
- DMA for floppy disk transfer
- PALs as glue chips

ROSY Junior Block Diagram



ROSY Junior Memory Map

Address	Operating System[1]	
	FLEX	*OS-9*
$0000 - $7FFF	32K **RAM1**	32K **RAM1**
$8000 - $9FFF	8K **RAM2**	8K **RAM2**
$A000 - $BFFF	8K ROM1 *ROSY Monitor*	
$C000 - $E7FF	10K **RAM2**	
$E800 - $EBFF	1K ROM1 *FLOPPY Disk Driver*	1K ROM1 *FLOPPY Disk Driver*
$EC00 - $EFFF		
$F000 - $FFFF	4K ROM1 *ROSY Monitor*	4K ROM1 *OS-9 Kernel*

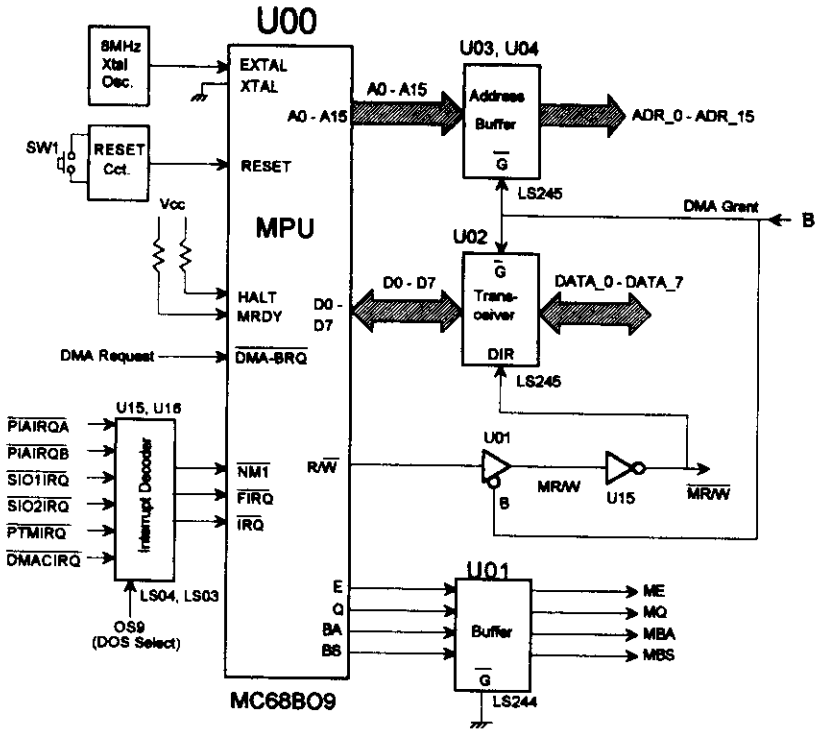
[1] ROSY Junior supports two operating systems: FLEX/ROSY and OS-9. Bit-0 of location $EF10 determines the active operating system: bit-0 = 0 for FLEX/ROSY, bit-0 = 1 for OS-9. On power-up, the default is bit-0 = 0 or FLEX/ROSY.

[2] See separate table (I/O Memory Map) for details.

ROSY Junior I/O Map

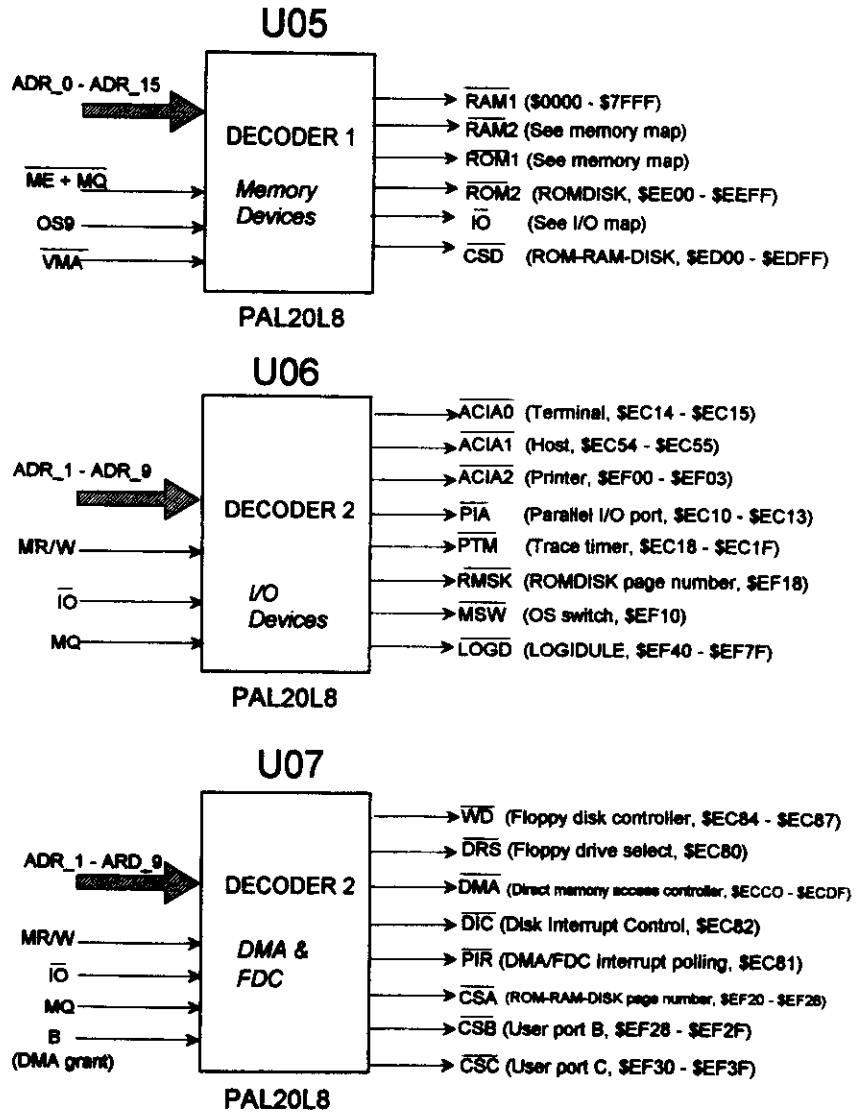
Address	Device	Name	Function
$EC10 - $EC13	MC68B21 (U23)	PIA0	Parallel I/O Port
$EC14 - $EC15	MC68B50 (U19)	ACIA0	Terminal Port
$EC18 - $EC1F	MC68B40 (U13)	PTM	Trace Timer
$EC54 - $EC55	MC68B50 (U18)	ACIA1	Host Port
$EC80	74LS273 (U32)	DRS	Floppy Drive Select
$EC81	74LS245 (U30)	PIR	DMA/FDC Interrupt Polling
$EC82	74LS74 (U29)	DIC	FDC Interrupt Control
$EC84 - $EC87	WD2793 (U28)	WD	Floppy Disk Controller (FDC)
$ECC0 - $ECDF	MC68B44 (U24)	DMA	Direct Memory Access Controller
$ED00 - $EDFF	Extension Bus (P1)	CSD	ROM-RAM-DISK Window
$EE00 - $EEFF	TMM27512 (U9)	ROM2	ROMDISK Window
$EF00 - $EF03	SY6551A (U20)	ACIA2	Printer Port
$EF10	74LS74 (U35)	MSW	OS Select Register
$EF18	74LS273 (U12)	RMSK	ROMDISK Page Register
$EF20 - $EF27	Extension Bus (P1)	CSA	ROM-RAM-DISK Page Register
$EF28 - $EF2F	Extension Bus (P1)	CSB	User Port B
$EF30 - $EF37	Extension Bus (P1)	CSC	User Port C
$EF40 - $EF7F	I/O Port (P2)	LOGD	LOGIDULE Port

ROSY Junior MPU & Buffers



DOS	PIAIRQA	PIAIRQB	SIO1IRQ	SIO2IRQ	PTMIRQ	DMACIRQ
OS-9	FIRQ/IRQ (Selectable)	FIRQ/IRQ (Selectable)	IRQ	IRQ	IRQ	IRQ
FLEX			NMI	-	NMI	IRQ

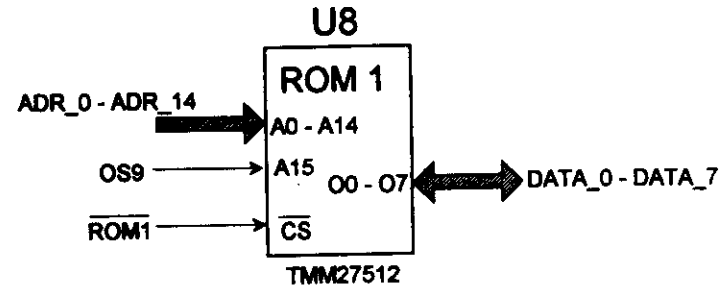
ROSY Junior Address Decoders



ROSY Junior Memory Subsystem

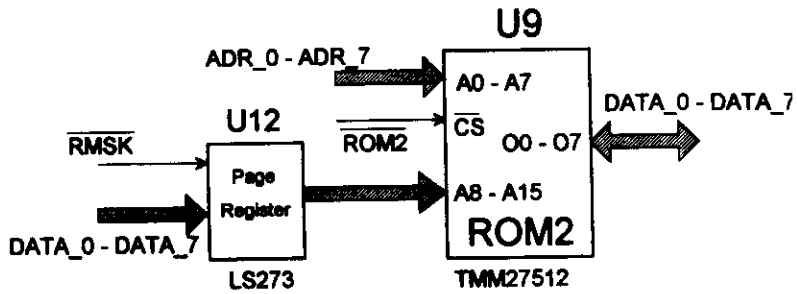
- Supports two operating systems by page swapping.
- One 64-Kbyte EPROM (U08) is split into two pages by a select signal (OS9); lower half for ROSY monitor and upper half for OS-9 kernel.
- Another 64-Kbyte EPROM (U09) is used as ROMDISK.
- One 32-Kbyte RAM (U10) provides contiguous memory block $0000–$7FFF.
- Another 32-Kbyte RAM (U11) is used partly for ROSY/FLEX (18 Kbytes) and partly for OS-9 (26 Kbytes).
- Page or OS select signal (OS9) is at $EF10. Writing a 1 selects OS-9 operating system; a 0 selects ROSY/FLEX operating system. On power-up, ROSY/FLEX is selected.

ROSY Junior ROM Subsystem



ROSY & OS-9 Kernel

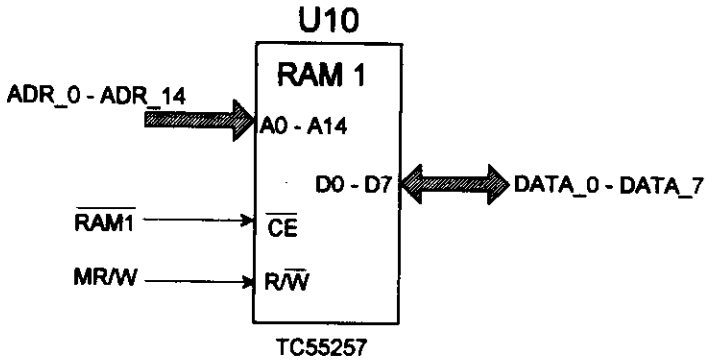
- The upper 32K is reserved for OS-9 while the lower 32K for ROSY/FLEX.
- Each section is only partially used. See memory map for details.



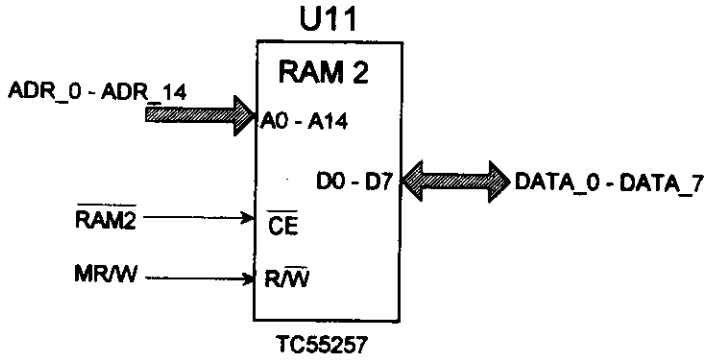
Virtual Disk

- ROM2 provides 64K of virtual disk space.
- Access is page oriented.
- Each page is 256 bytes at $EE00 - $EEFF.
- Page register is at $EF18 (RMSK).

ROSY Junior RAM Subsystem



- RAM1 provides 32K memory ($0000 - $7FFF).
- The memory space is common for both OS-9 and FLEX..



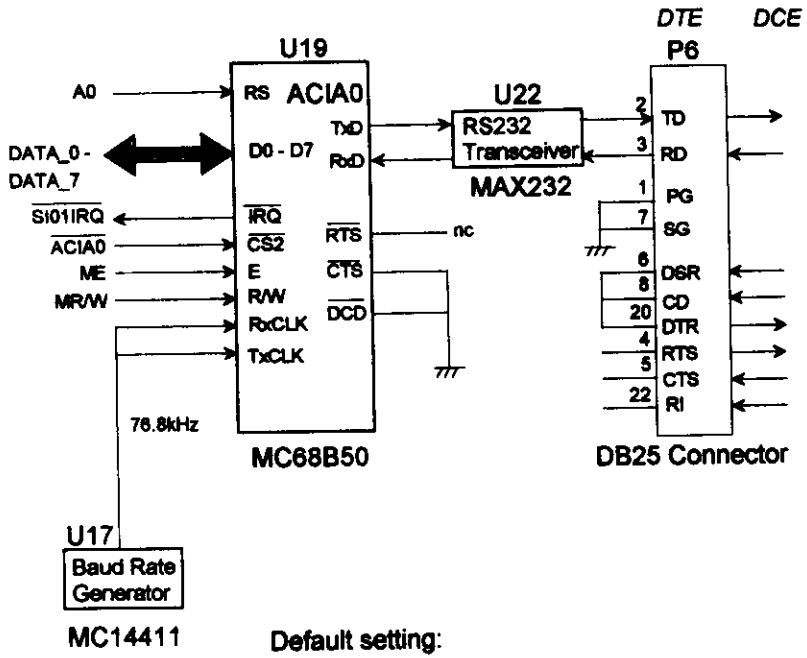
- RAM2 provides 26K static memory ($8000 - $E7FF) for OS-9.
- Or 18K static memory ($8000 - $9FFF & $C000 - $E7FF) for FLEX.
- As in RAM1, the memory space is common for both the operating systems.

Peripheral Subsystem

- **Serial Interface**
  - MC68B50 ACIA (U18) for TERMINAL
  - MC68B50 ACIA (U19) for HOST
  - SY6551A ACIA (U20) for PRINTER
  - MAX232 (U21, U22) as RS232C interface (single 5V supply)
  - Interrupts of U18, U19: NMI in ROSY/FLEX mode, IRQ in OS-9 mode.
  - Interrupts of U20: no interrupt in ROSY/FLEX mode, IRQ in OS-9 mode.

ROSY Junior Serial Interface

Terminal Serial Link

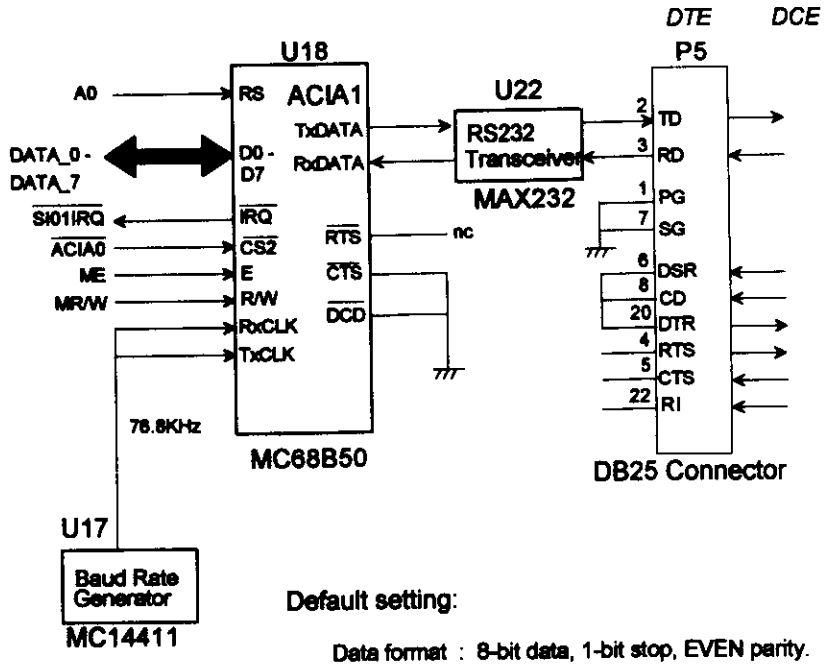


Default setting:

Data format : 8-bit data, 1-bit stop, EVEN parity.
Baud rate : 4800 bps

ROSY Junior Serial Interface

HOST Communication

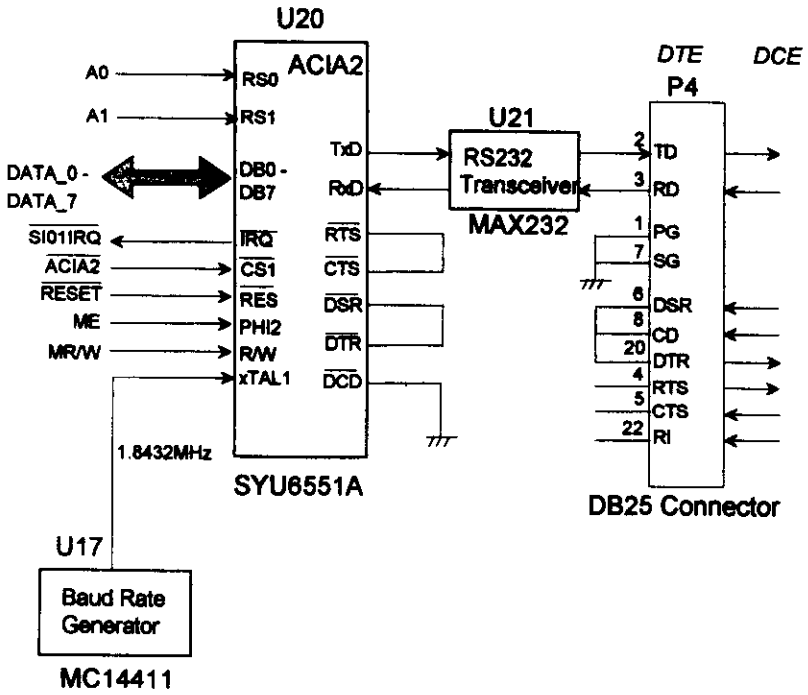


Default setting:

Data format : 8-bit data, 1-bit stop, EVEN parity.
Baud rate : 4800 bps

ROSY Junior Serial Interface

Printer Serial Link



Default setting:

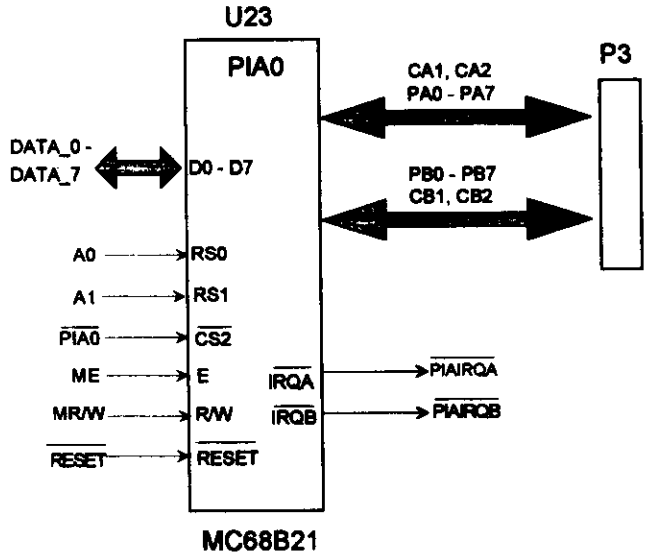
Data format : 8-bit data, 1-bit stop, EVEN parity.
Baud rate : 4800 bps

Peripheral Subsystem

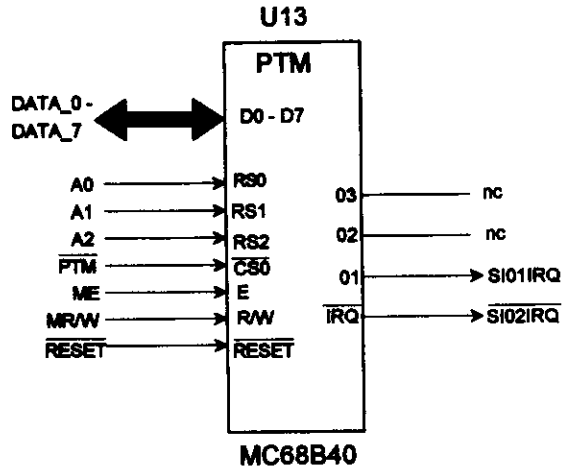
- **Parallel Interface**
  - MC68B21 (U23) provides parallel interface for general use
  - Jumper selectable IRQ/FIRQ
- **Programmable Timers**
  - MC68B40 PTM provides programmable timers
  - One channel provides 100-Hz signal for real-time clock
  - Interrupts: NMI in ROSY/FLEX mode, IRQ in OS-9 mode.

ROSY Junior Parallel Interface

Parallel I/O Port



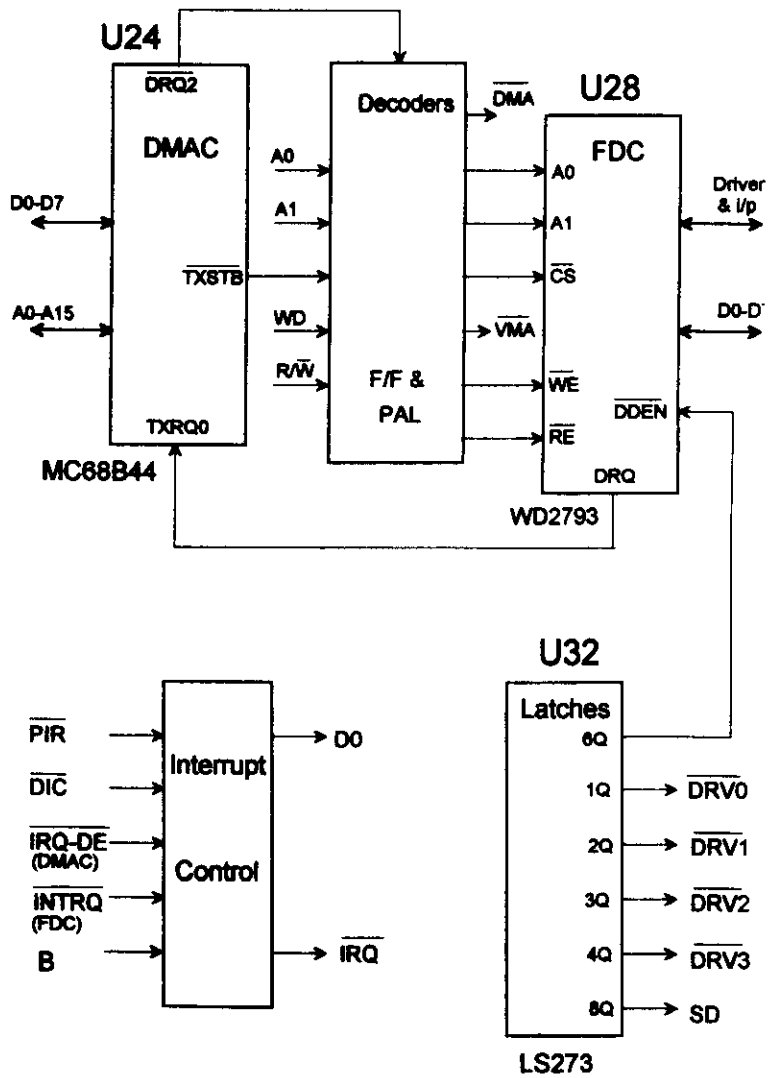
ROSY Junior Programmable Timer Module



Floppy Disk Subsystem

- Two 3.5 inch microfloppy disks
  - Data rate: 125 Kbits/s or 250 Kbits/s
  - Single or double sided
  - 48 or 96 tracks/inch
- WD2793 (U28) floppy disk controller
- A 74LS273 octal D flip-flop (U32) as disk select register at $EC80
  - Bit 0–3 select drive
  - Bit 5 selects density
  - Bit 7 selects side
- MC68B44 DMAC (U24) for data transfer
  - Uses Mode 2 (single byte transfer) so that system regains bus control after each byte transfer to support multitasking.
  - Bus arbitration problem
  - Interrupt technique

ROSY Junior Floppy Disk & DMA



Disk operation *involving* data transfer (DMA)

Example: Read a sector

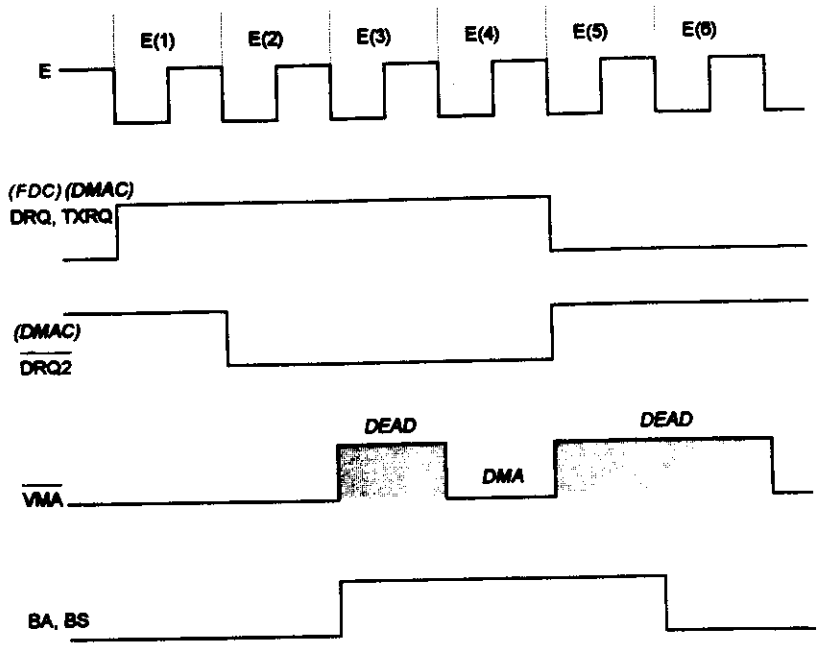
1. MPU sets up parameters in DMAC & FDC.
2. When disk is ready for data transfer, FDC sets **DRQ=1,** resulting in **TXRQ0=1** in DMAC.
3. DMAC sets **DRQ2=0.**
4. On E(1)↓ **DMA=0** (MPU).
5. On E(2)↓, MPU releases bus:**BA=BS=1 VMA=1** to prevent illegal access (dead cycles).
6. On E(3)↓, **VMA=0,** DMAC starts DMA cycle.
7. On E(4)↓, DMAC sets **DRQ2=1** to cancel REQ. **VMA=1** (dead cycles), **DMA=1** (MPU).
8. On E(5)↓, MPU senses end of DMA and resets **BA, BS.**
9. On E(6)↓, **VMA=0,** normal MPU control.

Disk operation *without* data transfer

Example: Restore, seek etc.

1. MPU initiates FDC by setting necessary parameters & writing command word into command register.
2. Then MPU polls FDC by checking the status register to see whether the job is done.

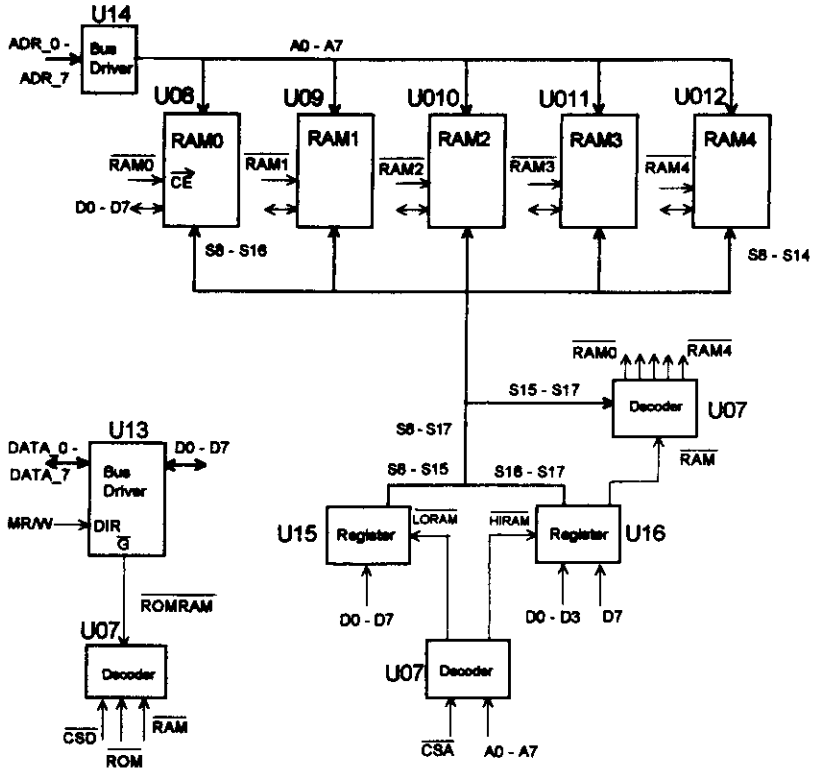
ROSY Junior DMA Bus Timing



ROSY Junior ROM-RAM-DISK

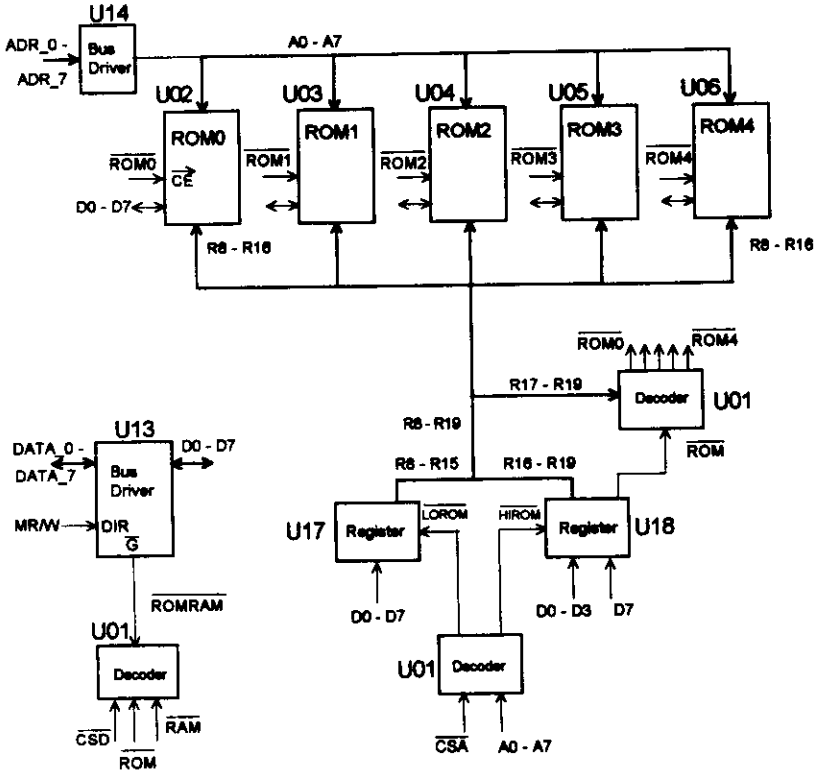
- Memory extension board uses as **virtual disks**.
- 640K EPROM read-only virtual disk (**ROMDISK**).
- 160K RAM read-write virtual disk (**RAMDISK**).
- Accessed from MPU via a 256-byte (page) **window** at $ED00-$EDFF.
- ROMDISK has **2560** pages distributed over five 128-K EPROMs (μPD27C1001D).
- RAMDISK has **640** pages distributed over five 32-K RAMs (TC55257).
- In OS-9, ROMDISK: **r0**, RAMDISK: **r1**.

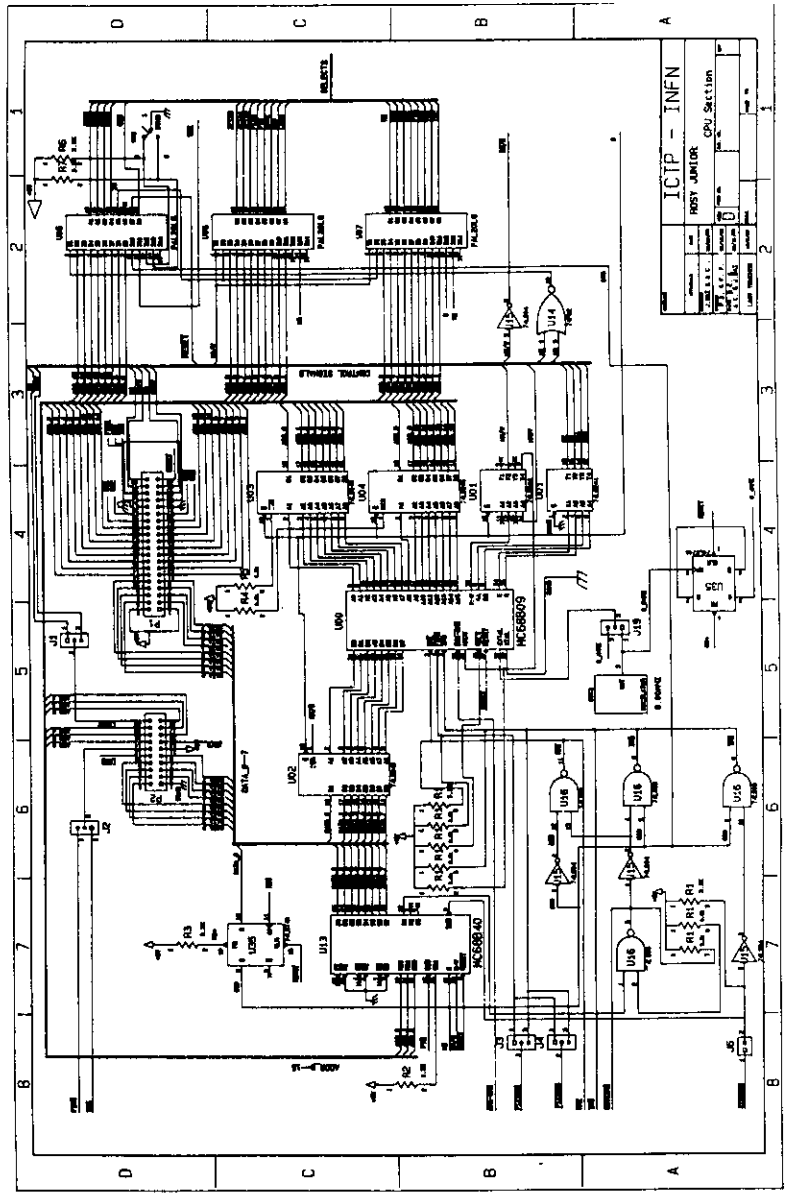
ROSY Junior ROM-RAM-DISK
RAM Section

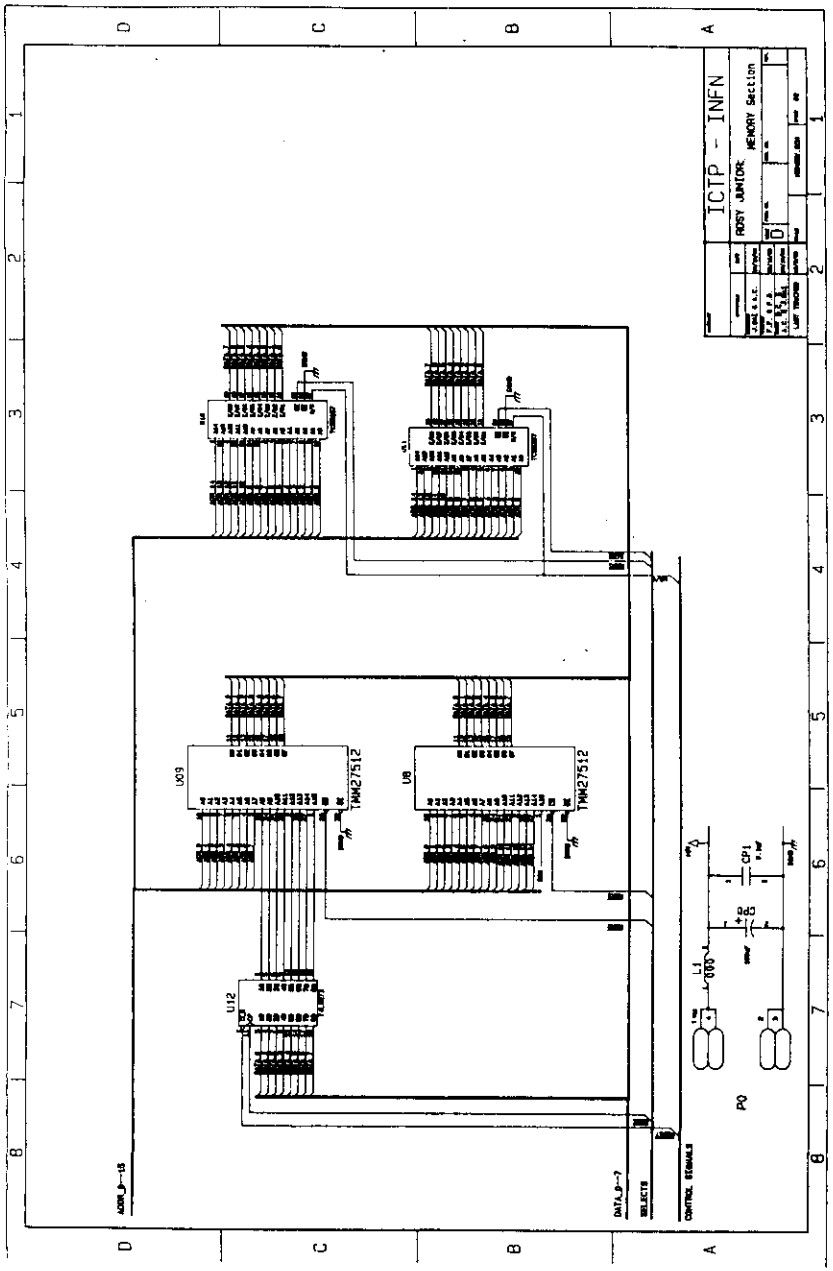


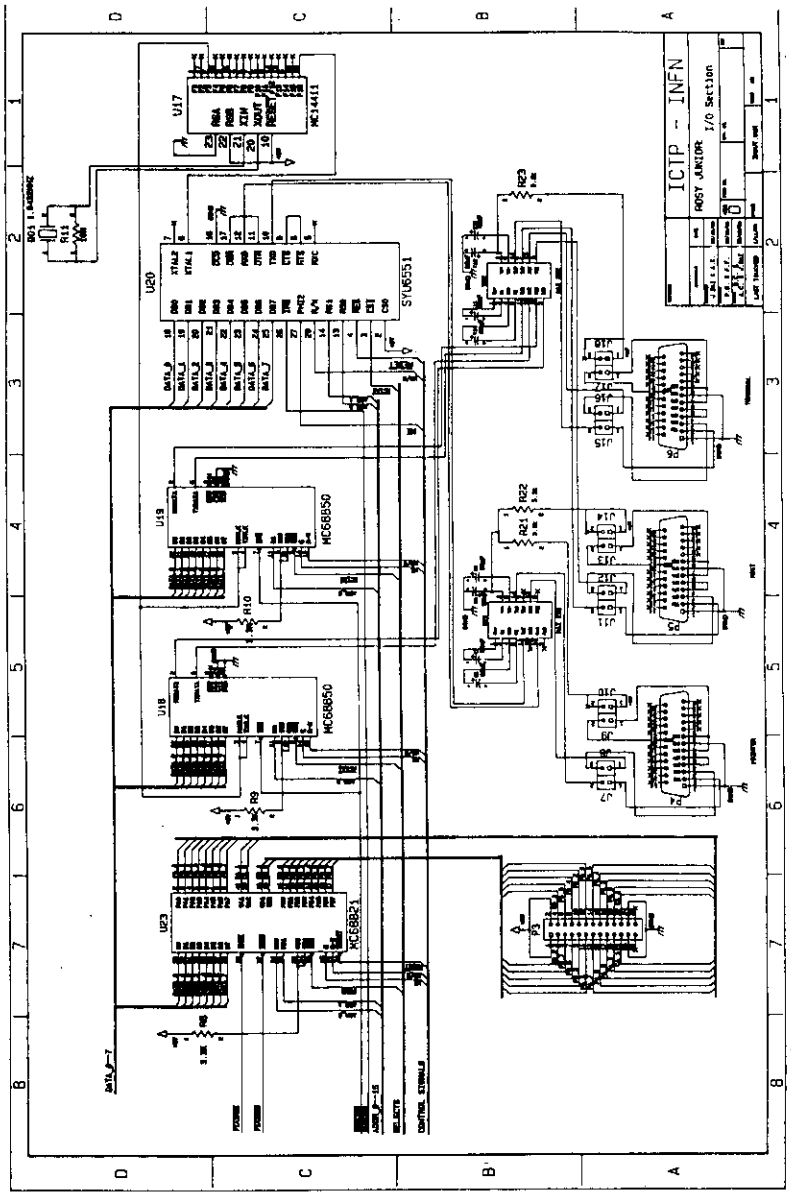
ROSY Junior ROM-RAM-DISK

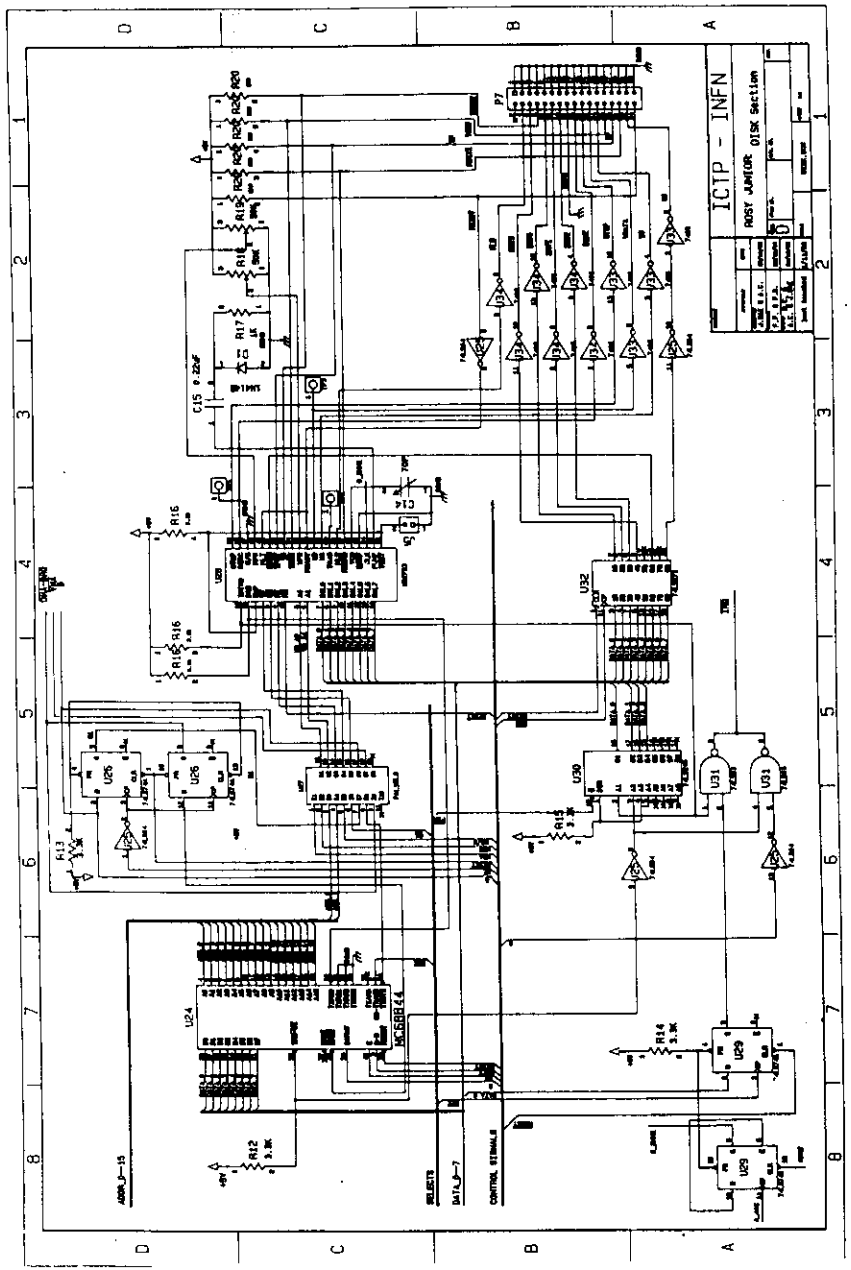
ROM Section

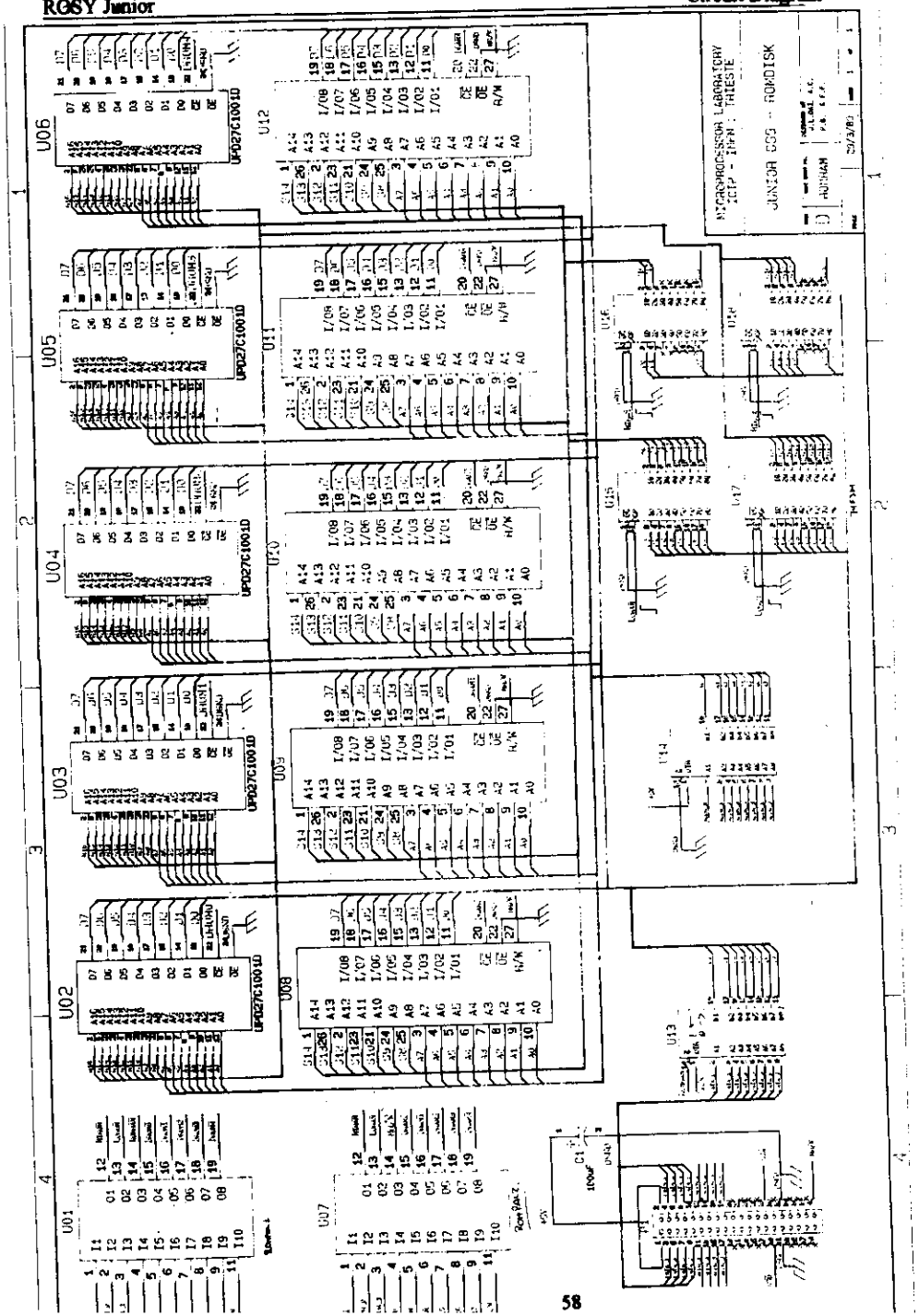





ICTP - INFN
ROSY JUNIOR MEMORY Section
U09
TMM27512
U8
TMM27512
U12
CP1
P0
DATA_0--7
SELECTS
CONTROL SIGNALS


ICTP - INFN
ROSY JUNIOR I/O Section
U17
MC14411
U20
ST16551
U19
MC68B50
U18
MC68B50
U23
MC68B21
R23
R22
R21
R10
R9
P3


ICTP - INFN
ROSY JUNIOR
DISK Section


MICROPROCESSOR LABORATORY
ICTP - INFN - TRIESTE
JUNIOR DISK - FLOPPY DISK