



SMR/748 - 11

**ICTP-INFN-UNU-MICROPROCESSOR LABORATORY
THIRD COURSE ON BASIC VLSI DESIGN TECHNIQUES
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SPICE

Part II

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These are preliminary lecture notes, intended only for distribution to participants.

SPICE: Examples and Applications

Introduction to SPICE

- Voltage sources
- A simple ohmic circuit
- Low-Pass and High Pass passive Filter
- Low-Pass and High-Pass Active Filter
- Band-Pass filter
- Bode Diagrams

DC Characteristics of MOS and GaAs transistors

- NMOS, PMOS and D-MESFET: Transconductance, output conductance, linear and saturation region.
- Two inverters: CMOS and BFL (dc transfer curve)

Comparison of Two Logical Families: CMOS (Si) and BFL (GaAs)

- Logic swing and noise margin
- Power consumption
- Rise and fall time, delay propagation time
- Speed-power product (and the power/area problem)
- Fan-out
- Ring Oscillators

Independent Sources

- Pulse**

General Form: PULSE (V1 V2 TD TR TF PW PER)

Parameters

V1: initial value
V2: pulsed value
TD: delay time
TR: rise time
TF: fall time
PW: pulse width
PER: period

time	value
0	V1
TD	V1
TD+TR	V2
TD+TR+PW	V2
TD+TR+PW+TF	V1

Intermediate points are determined by linear interpolation.

- Sinusoidal**

General Form SIN (V0 VA FREQ TD THETA)

Parameters

V0: Offset
VA: Amplitud
FREQ: Frequency
TD: Delay
THETA: Damping Factor

The shape of the waveform is described by the following table:

time	value
0 to TD	V0
TD to TSTOP	$V0 + VA \cdot e^{-(t-TD) \cdot THETA} \sin[2\pi \cdot FREQ \cdot (t + TD)]$

- **Exponential**

General Form EXP (V1 V2 TD1 TAU1 TD2 TAU2)

Parameters

V1: initial value
V2: pulsed value
TD1: rise delay time
TAU1: rise time constant
TD2: fall delay time
TAU2: fall time constant

The shape of the waveform is described by the following table:

time	value
0 to TD1	V1
TD1 to TD2	$V1 + (V2 - V1) \left[1 - e^{\frac{-(t-TD1)}{TAU1}} \right]$
TD2 to TSTOP	$V1 + (V2 - V1) \left[1 - e^{\frac{-(t-TD1)}{TAU1}} \right] + (V1 - V2) \left[1 - e^{\frac{-(t-TD2)}{TAU2}} \right]$

- **Piece-Wise Linear**

General Form: PWL (T1 V1 <T2 V2 T3 V3 T4 V4 ...>)

Parameters

T1: time1
V1: value at the time:T1
T2: time2
V2: value at the time: T2
etc.

The shape of the wave form is the linear interpolation between successive pairs (Ti,Vi)

- **Single-Frequency FM**

General Form: SFFM (V0 VA FC MDI FS)

Parameters

V0: Offset (Volts)
 VA: Amplitud (volts)
 FC: Carrier Frequency (Hz)
 MDI: Modulation index
 FS: Signal Frequency (Hz)

The shape of the waveform is described by the following equation:

$$V(t) = V0 + VA \cdot \sin[2\pi \cdot FC + MDI \cdot \sin(2\pi \cdot FS \cdot t)]$$

Non Linear Dependent Sources

General Form: bxxxxxx N+ N- V = f(v(1), v(2), ...) (voltage)
 I = f(v(1), v(2), ...) (current)

N+, N- : positive and negative node respect. of the sources

The expressions given for V or I may be any function of voltages and currents through voltages sources in the system. The following functions of real variables are defined:

abs	cos	cosh	sin
acos	atan	exp	sinh
acosh	atanh	ln	sqrt
asin	cos	log	tan

The following operations are defined:

+ - * / ^

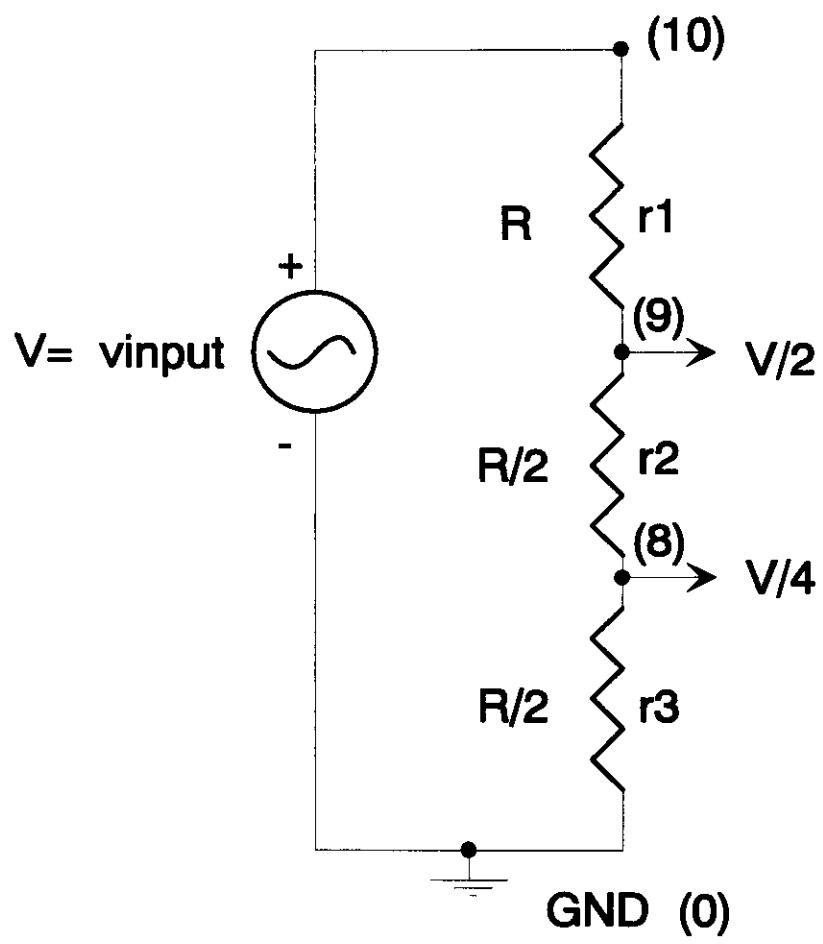
Linear Voltage-Controlled Voltage Sources

General Form : EXXXXXXX N+ N- NC+ NC- VALUE

N+ is the positive node, and N- is the negative node. NC+ and NC_ are the positive and negative controlling nodes, respectively. VALUE is the voltage gain.

In similar way there are:

- **Linear Voltage-Controlled Current Sources**
- **Linear Current-Controlled Voltage Sources**



OHMIC CIRCUIT (title of the SPICE description file, must be the first line)

* <any comment> (any comment line starts with ' * ')

* ELEMENTE LINES:

*voltage source

* name N+ N- value

vinput 10 0 16v

*Resistors (the name of resistors must start with: " r ")

r1 10 9 1k

r2 9 8 0.5K

r3 8 0 500

*Calling the subcircuit: ' divider '

* (the name of subcircuits must starts with ' x ')

x1 10 6 5 divider

*SUBCIRCUITS

*a subcircuit definition is begun with a .SUBCKT line

* name nodes (Ground (0) is always global)

.subckt divider 1 2 3

rr1 1 2 1000

rr2 2 3 500

rr3 3 0 0.5k

.ends divider

* The line ' .ends <subcircuit name> ' must be the last one
* for any subcircuit definition

*CONTROL LINES:

* DC Analysis: this line defines the dc transfer

* curve, source and sweep limits:

.dc vinput 0 8 0.001

* This line must always be the last in the description file:

.end

*Interactive Commands:

* source Aohm.raw

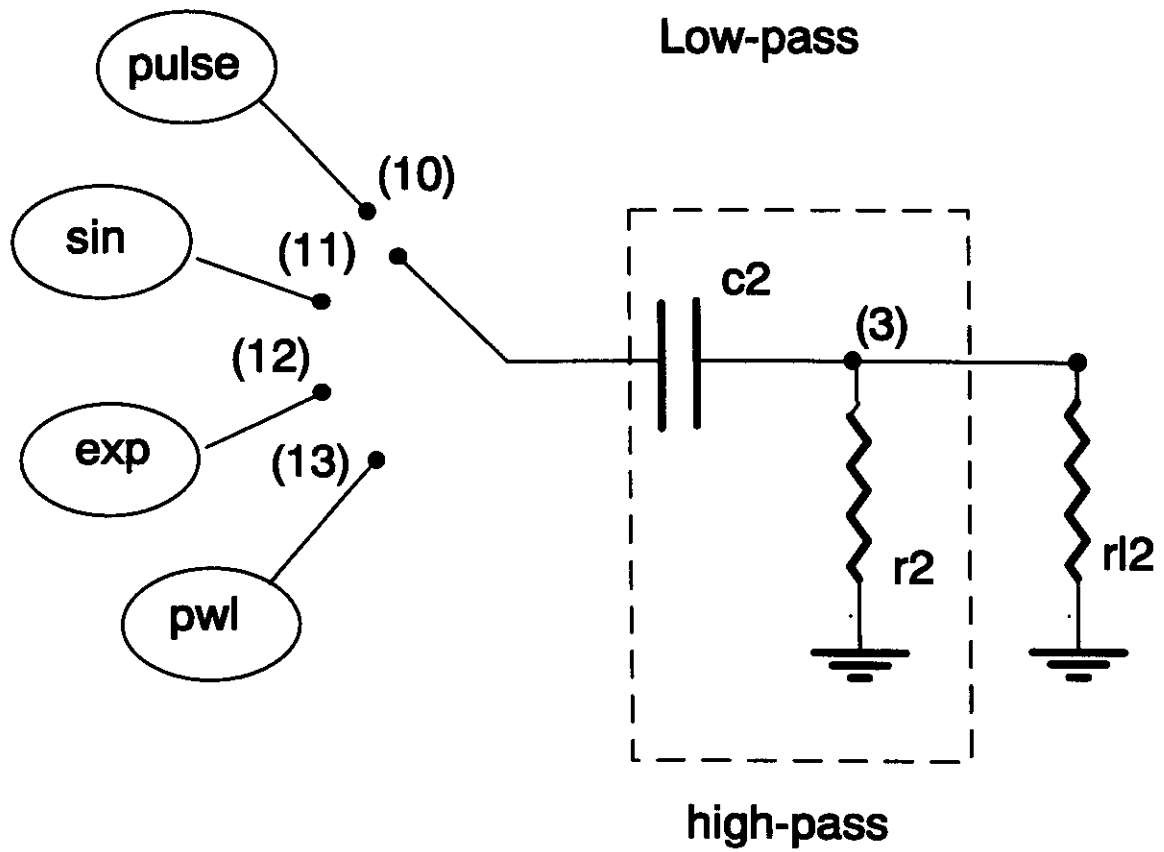
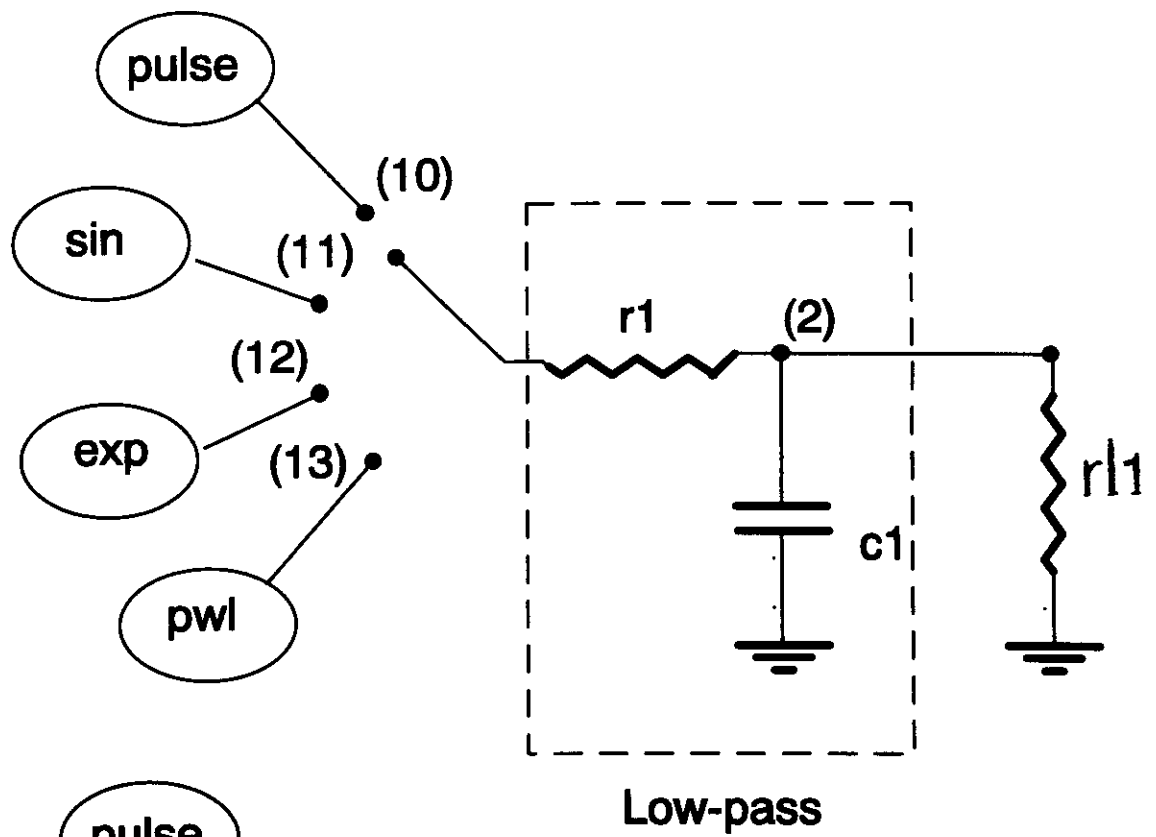
* listing

* run

* plot v(10) v(9) v(8)

* plot v(10) v(6) v(5)

FILTERS (passive)



```
*RC circuits as low pass and high pass filters (passive)
*****
```

```
*Stimulus: (independent voltage sources)
```

```
vin1 10 0 dc ac pulse(0v 5v 5ns 1ps 1ps 10ns 20ns)
```

```
vin2 11 0 dc ac sin(2.5v 2v 0.1Ghz 1ns)
```

```
vin3 12 0 dc ac exp(1v 4v 10ns 5ns 50ns 35ns)
```

```
vin4 13 0 dc ac pwl(5ns 2v 10ns 5v 20ns 1.5v 35ns 2v)
```

```
*****
```

```
*Non-Linear Dependent Source
```

```
bvin15 15 0 v=sin(v(100))
```

```
bvin16 16 0 v=ln(v(100)+1)
```

```
bvin17 17 0 v=sqrt(v(15),16))
```

```
bvin18 18 0 v=v(108)+v(109)/2+v(110)/4
```

```
*we use v(100) (just as parameters) to generate v(15) and v(16).
```

```
vin7 100 0 dc ac pwl(0s 1v 100ns 100v)
```

```
vin8 108 0 dc ac sin(2.5v 2v 0.01Ghz 1ns)
```

```
vin9 109 0 dc ac sin(2.5v 2v 0.1Ghz 1ns)
```

```
vin10 110 0 dc ac sin(2.5v 2v 1Ghz 1ns)
```

```
*****
```

```
**Low-pass
```

```
r1 13 2 1000
```

```
c1 2 0 20pf
```

```
r11 2 0 50Meg
```

```
**High pass
```

```
c2 2 3 200pf
```

```
r2 3 0 100K
```

```
r12 3 0 50Meg
```

```
*****
```

```
*****
```

```
* (lin-oct-dec)-(numb.point) freq.inf. freq.sup.
```

```
*.ac dec 100 100 100G
```

```
* tstep(plot) tstop tstart tmax(maximum step calc.)
```

```
.tran 100ps 100ns 0 100ps
```

```
.end
```

```
*****
```

```
* source RCpas_1.raw
```

```
* run
```

```
* plot v(10) v(11) v(12) v(13) v(15) v(16) v(17) v(18)
```

```
* plot v(108) v(109) v(110)
```

```
* *****
```

```
* ac dec 100 10 10Ghz
```

```
* plot db(v(3)/v(10)) db(v(2)/v(10)) vs Log(frequency)
```

```
* plot phase(v(3))*(360/6.28) vs Log(frequency)
```

```
* plot db(v(3)/v(10)) vs Log(frequency)
```

```
* plot phase(v(3)) vs Log(frequency)
```

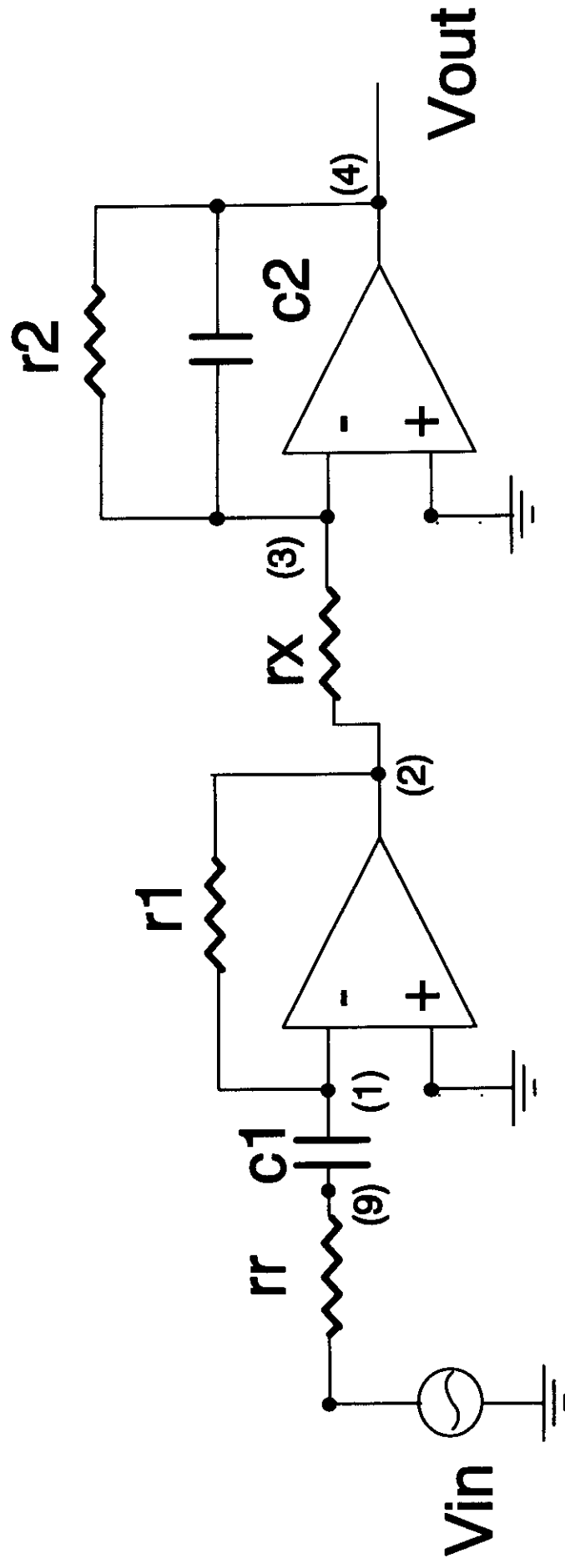
```
* *****
```

```
* run
```

```
* plot v(13) v(2)
```

```
* plot v(13) v(3)
```

BAND-PASS FILTER



high-pass

low-pass

*RC circuits as low pass and high pass filters (active)

*Stimulus:

vin1 10 0 dc ac pulse(0v 5v 5ns 1ps 1ps 20ns 40ns)

vin2 11 0 dc ac sin(2.5v 2v 0.1Ghz 5ns)

vin3 12 0 dc ac exp(1v 4v 10ns 5ns 50ns 35ns)

vin4 13 0 dc ac pwl(5ns 2v 10ns 5v 20ns 1.5v 35ns 2v)

*Active filters

*first almost-ideal opamp:

*EX N+ N- NC+ NC- VALUE

eop1 2 0 0 1 100G

*second almost-ideal opamp:

*EX N+ N- NC+ NC- VALUE

eop2 4 0 0 3 100G

*differentiator

rr 12 9 1k

c1 9 1 1uf

r1 1 2 1k

*Integrator

rx 3 4 1k

c2 3 4 100ff

r2 12 3 1k

*.ac dec 100 100 100 G

.tran 100ps 100ns 0 100ps

.end

* source RCact_1.raw

* run

* This is for the "high pass"

* ac dec 100 10 10Ghz

* plot db(v(2)/v(12)) vs log(frequency)

* plot 180+(360/6.28)*phase(v(2)) vs Log(frequency)

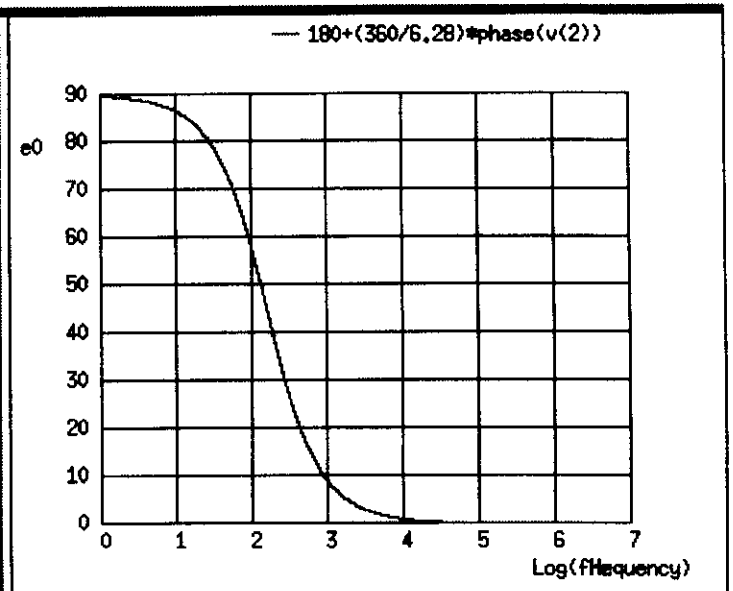
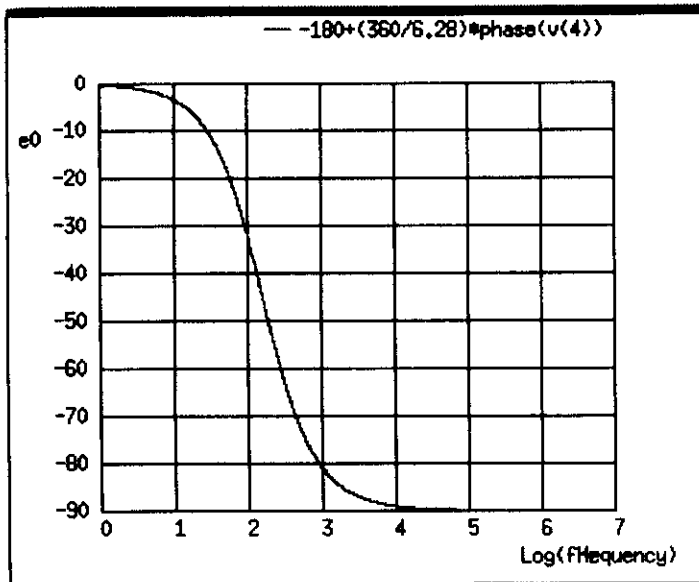
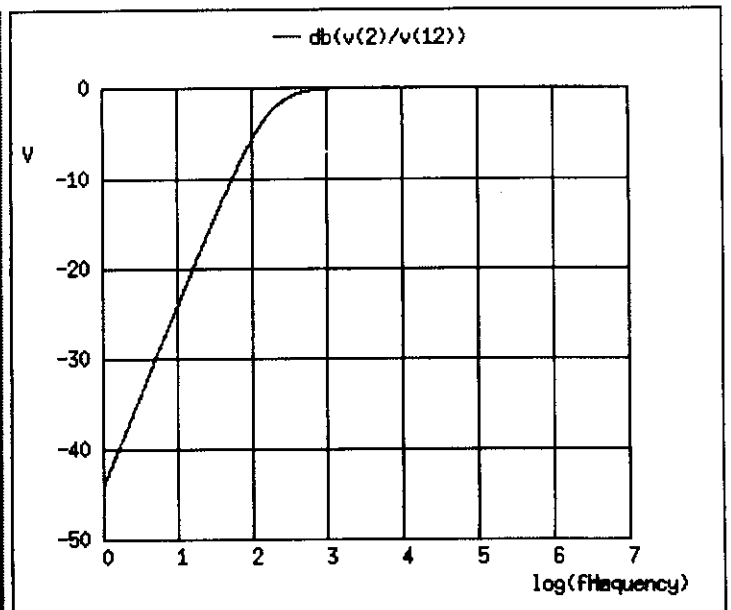
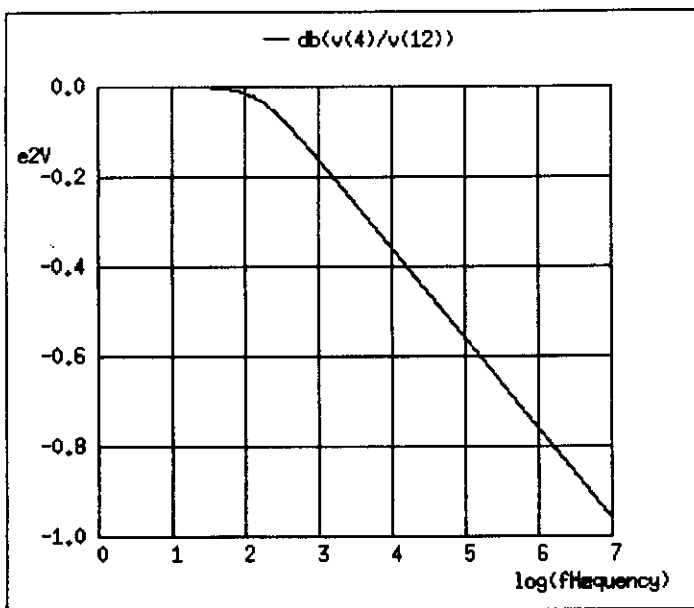
* This is for the Low-Pass (and for the band-pass)

* plot db(v(4)/v(12)) vs log(frequency)

* plot -180+(360/6.28)*phase(v(4)) vs Log(frequency)

*

* To have a band-pass change the node 12 in " r2 " by 2 (putting
 * the integrator after the differentiator) and resimulate it .-



As we see the Bode diagrams
corresponding to the filter,
abstracted.

M

MOSFET

(P.Spice)

General Form

```

M<name> <(drain) node> <(gate) node> <(source) node>
+      <(bulk/substrate) node> <(model) name>
+      [L=<value>] [W=<value>]
+      [AD=<value>] [AS=<value>]
+      [PD=<value>] [PS=<value>]
+      [NRD=<value>] [NRS=<value>]
+      [NRG=<value>] [NRB=<value>]
+      [M=<value>]
  
```

Examples

```

M1 14 2 13 0 PNOM L=25u W=12u
M13 15 3 0 0 PSTRONG
M16 17 3 0 0 PSTRONG M=2
M28 0 2 100 100 NWEAK L=33u W=12u
+ AD=288p AS=288p PD=60u PS=60u NRD=14 NRS=24 NRG=10
  
```

Model Forms

.MODEL <(model) name> NMOS [(model parameters)]

.MODEL <(model) name> PMOS [(model parameters)]

As shown in Figure 11, the MOSFET is modeled as an intrinsic MOSFET with ohmic resistances in series with the drain, source, gate, and bulk (substrate). There is also a shunt resistance (RDS) in parallel with the drain-source channel.

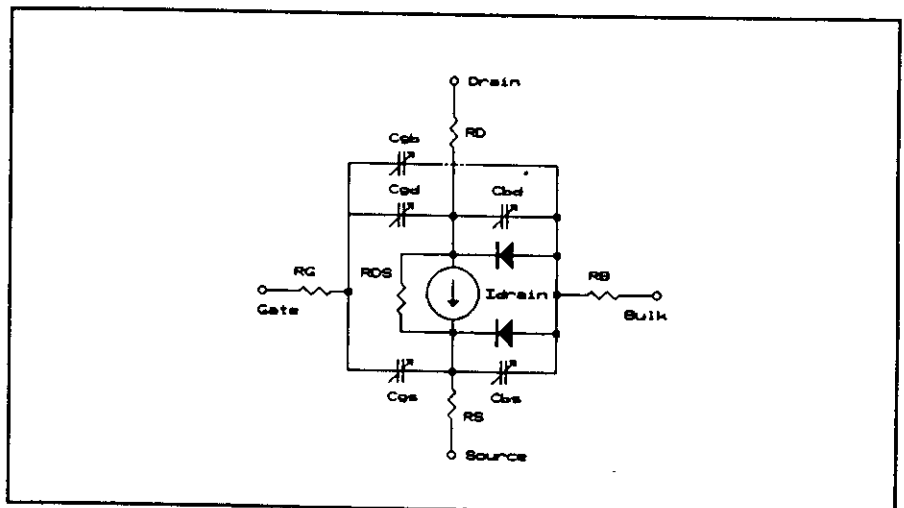


Figure 11 MOSFET model.

PSpice provides four MOSFET device models, which differ in the formulation of the I-V characteristic. The LEVEL parameter selects between different models:

LEVEL=1 is the Shichman-Hodges model (see reference [1])
LEVEL=2 is a geometry-based, analytic model (see reference [2])
LEVEL=3 is a semi-empirical, short-channel model (see reference [2])
LEVEL=4 is the BSIM model (see reference [3])

L and W are the channel length and width, and are decreased to get the effective channel length and width. L and W can be specified in the device, model, or .OPTION statements. The value in the device statement supersedes the value in the model statement which supersedes the value in the .OPTION statement.

AD and AS are the drain and source diffusion areas. PD and PS are the drain and source diffusion perimeters. The drain-bulk and source-bulk saturation currents can be specified either by JS, which is multiplied by AD and AS, or by IS, which is an absolute value. The zero-bias depletion capacitances can be specified by CJ, which is multiplied by AD and AS, and by CJSW, which is multiplied by PD and PS. Or they can be set by CBD and CBS, which are absolute values.

NRD, NRS, NRG, and NRB are the relative resistivities of the drain, source, gate, and substrate in squares. These parasitic (ohmic) resistances can be specified either by RSH, which is multiplied by NRD, NRS, NRG, and NRB respectively or by RD, RS, RG, and RB, which are absolute values.

PD and PS default to 0, NRD and NRS default to 1, and NRG and NRB default to 0. Defaults for L, W, AD, and AS may be set in the .OPTIONS statement. If AD or AS defaults are not set, they also default to 0. If L or W defaults are not set, they default to 100u.

M is a device "multiplier" (default = 1), which simulates the effect of multiple devices in parallel. The effective width, overlap and junction capacitances, and junction currents of the MOSFET are multiplied by M. The parasitic resistance values (e.g. RD, RS) are divided by M. Note the third example showing a device twice the size of the second example.

Model Levels 1, 2, and 3

The DC characteristics of the first three model levels are defined by the parameters VTO, KP, LAMBDA, PHI, and GAMMA. These are computed by *PSpice* if process parameters (TOX, NSUB, ...) are given, but the user-specified values always override (Note: the default value for TOX is 0.1 μ for model levels 2 and 3, but is unspecified for level 1 which "turns off" the use of process parameters). VTO is positive (negative) for enhancement mode and negative (positive) for depletion mode of N-channel (P-channel) devices.

Model Parameters (see MODEL statement)		Units	Default
LD	lateral diffusion (length)	meter	0
WD	lateral diffusion (width)	meter	0
VTO	zero-bias threshold voltage	volt	0
KP	transconductance coefficient	amp/volt ²	2E-5
LAMBDA	channel-length modulation (LEVEL = 1 or 2)	volt ⁻¹	0
PHI	surface potential	volt	0.6
GAMMA	bulk threshold parameter	volt ^{1/4}	calculated
TOX	oxide thickness	meter	see above
TPG	gate material type: +1 = opposite of substrate, -1 = same as substrate, 0 = aluminum		+1
NSUB	substrate doping density	1/cm ³	none
NSS	surface state density	1/cm ²	none
NFS	fast surface state density	1/cm ²	0
XJ	metallurgical junction depth	meter	0
UO	(u-oh, not u-zero) surface mobility	cm ² /volt·sec	600
UCRIT	mobility degradation critical field (LEVEL = 2)	volt/cm	1E4
UEXP	mobility degradation exponent (LEVEL = 2)		0
UTRA	(not used) mobility degradation transverse field coefficient		
VMAX	maximum drift velocity	meter/sec	0
NEFF	channel charge coefficient (LEVEL = 2)		1.0
XQC	fraction of channel charge attributed to drain		1.0
DELTA	width effect on threshold		0
THETA	mobility modulation (LEVEL = 3)	volt ⁻¹	0
ETA	static feedback (LEVEL = 3)		0
KAPPA	saturation field factor (LEVEL = 3)		0.2

For All Model Levels

The following list describes the parameters common to all model levels, which are primarily parasitic element values such as series resistance, overlap and junction capacitance, and so on.

Model Parameters (see MODEL statement)		Units	Default
LEVEL	model index		1
→ L	channel length	meter	DEFL
→ W	channel width	meter	DEFW
→ RD	drain ohmic resistance	ohm	0
→ RS	source ohmic resistance	ohm	0
→ RG	gate ohmic resistance	ohm	0
→ RB	bulk ohmic resistance	ohm	0
→ RDS	drain-source shunt resistance	ohm	infinite
→ RSH	drain, source diffusion sheet resistance	ohm/square	0
IS	bulk <i>p-n</i> saturation current	amp	1E-14
JS	bulk <i>p-n</i> saturation current/area	amp/meter ²	0
JSSW	bulk <i>p-n</i> saturation sidewall current/length	amp/meter	0
N	bulk <i>p-n</i> emission coefficient		1
PB	bulk <i>p-n</i> bottom potential	volt	0.8
PBSW	bulk <i>p-n</i> sidewall potential	volt	PB
CBD	zero-bias bulk-drain <i>p-n</i> capacitance	farad	0
CBS	zero-bias bulk-source <i>p-n</i> capacitance	farad	0
CJ	bulk <i>p-n</i> zero-bias bottom capacitance/area	farad/meter ²	0
CJSW	bulk <i>p-n</i> zero-bias sidewall capacitance/length	farad/meter	0
MJ	bulk <i>p-n</i> bottom grading coefficient		0.5
MJSW	bulk <i>p-n</i> sidewall grading coefficient		0.33
FC	bulk <i>p-n</i> forward-bias capacitance coefficient		0.5
TT	bulk <i>p-n</i> transit time	sec	0
CGSO	gate-source overlap capacitance/channel width	farad/meter	0
CGDO	gate-drain overlap capacitance/channel width	farad/meter	0
CGBO	gate-bulk overlap capacitance/channel length	farad/meter	0
KF	flicker noise coefficient		0
AF	flicker noise exponent		1

In the following equations:

V_{gs}	= intrinsic gate-intrinsic source voltage
V_{gd}	= intrinsic gate-intrinsic drain voltage
V_{ds}	= intrinsic drain-intrinsic source voltage
V_{bs}	= intrinsic substrate-intrinsic source voltage
V_{bd}	= intrinsic substrate-intrinsic drain voltage
V_t	= $k \cdot T/q$ (thermal voltage)
k	= Boltzmann's constant
q	= electron charge
T	= analysis temperature (°K)
T_{nom}	= nominal temperature (set with TNOM option)

Other variables are from the model parameter list. These equations describe an n-channel MOSFET. For p-channel devices, reverse the signs of all voltages and currents. Positive current is current flowing into a terminal (for example, positive drain current flows from the drain through the channel to the source).

DC Currents

Note: positive current is current flowing into a terminal.

I_g = gate current = 0

I_b = bulk current = $I_{bs} + I_{bd}$

I_{bs} = bulk-source leakage current = $I_{ss} \cdot (e^{V_{bs}/(N \cdot V_t)} - 1)$

I_{bd} = bulk-drain leakage current = $I_{ds} \cdot (e^{V_{bd}/(N \cdot V_t)} - 1)$

where if: $J_S = 0$, or $A_S = 0$, or $A_D = 0$

$I_{ss} = I_S$

$I_{ds} = I_S$

otherwise:

$I_{ss} = A_S \cdot J_S + P_S \cdot J_{SSW}$

$I_{ds} = A_D \cdot J_S + P_D \cdot J_{SSW}$

I_d = drain current = $I_{bd} - I_{drain}$

I_s = source current = $I_{ds} + I_{drain}$

Equations for I_{drain} : LEVEL=1

For: $V_{ds} \geq 0$ (normal mode)

and: $V_{gs} - V_{to} < 0$ (cutoff region)

$I_{drain} = 0$

and: $V_{ds} < V_{gs} - V_{to}$ (linear region)

$I_{drain} = (W/L) \cdot (KP/2) \cdot (1 + LAMBDA \cdot V_{ds}) \cdot V_{ds} \cdot (2 \cdot (V_{gs} - V_{to}) - V_{ds})$

and: $0 \leq V_{gs} - V_{to} \leq V_{ds}$ (saturation region)

$I_{drain} = (W/L) \cdot (KP/2) \cdot (1 + LAMBDA \cdot V_{ds}) \cdot (V_{gs} - V_{to})^2$

where $V_{to} = V_{TO} + GAMMA \cdot ((PHI - V_{bs})^{1/2} - PHI^{1/2})$

Sim.

For: $V_{ds} < 0$ (inverted mode)

Switch the source and drain in equations (above).

For LEVEL=2, or LEVEL=3, see reference [2] below for the equations describing I_{drain} .

Capacitance

Note: all capacitances are between terminals of the intrinsic MOSFET. That is, to the inside of the ohmic drain and source resistances.

C_{bs} = bulk-source capacitance = area cap. + sidewall cap. + transit time cap.

C_{bd} = bulk-drain capacitance = area cap. + sidewall cap. + transit time cap.

For: $CBS = 0$ and $CBD = 0$

$$C_{bs} = AS \cdot CJ \cdot C_{bsj} + PS \cdot CJSW \cdot C_{bss} + TT \cdot G_{bs}$$

$$C_{bd} = AD \cdot CJ \cdot C_{bdj} + PD \cdot CJSW \cdot C_{bds} + TT \cdot G_{ds}$$

otherwise

$$C_{bs} = CBS \cdot C_{bsj} + PS \cdot CJSW \cdot C_{bss} + TT \cdot G_{bs}$$

$$C_{bd} = CBD \cdot C_{bdj} + PD \cdot CJSW \cdot C_{bds} + TT \cdot G_{ds}$$

where

$$G_{bs} = \text{DC bulk-source conductance} = \frac{dI_{bs}}{dV_{bs}}$$

$$G_{bd} = \text{DC bulk-drain conductance} = \frac{dI_{bd}}{dV_{bd}}$$

For: $V_{bs} \leq FC \cdot PB$

$$C_{bsj} = (1 - V_{bs}/PB)^{-MJ}$$

$$C_{bss} = (1 - V_{bs}/PBSW)^{-MJSW}$$

For: $V_{bs} > FC \cdot PB$

$$C_{bsj} = (1 - FC)^{-(1+MJ)} \cdot (1 - FC \cdot (1 + MJ) + MJ \cdot V_{bs}/PB)$$

$$C_{bss} = (1 - FC)^{-(1+MJSW)} \cdot (1 - FC \cdot (1 + MJSW) + MJSW \cdot V_{bs}/PBSW)$$

For: $V_{bd} \leq FC \cdot PB$

$$C_{bdj} = (1 - V_{bd}/PB)^{-MJ}$$

$$C_{bds} = (1 - V_{bd}/PBSW)^{-MJSW}$$

For: $V_{bd} > FC \cdot PB$

$$C_{bdj} = (1 - FC)^{-(1+MJ)} \cdot (1 - FC \cdot (1 + MJ) + MJ \cdot V_{bd}/PB)$$

$$C_{bds} = (1 - FC)^{-(1+MJSW)} \cdot (1 - FC \cdot (1 + MJSW) + MJSW \cdot V_{bd}/PBSW)$$

C_{gs} = gate-source overlap capacitance = $CGSO \cdot W$

C_{gd} = gate-drain overlap capacitance = $CGDO \cdot W$

C_{gb} = gate-bulk overlap capacitance = $CGBO \cdot L$

See reference [2] for the equations describing the capacitances due to the channel charge.

Temperature Effects

$$IS(T) = IS \cdot e^{(Eg(Tnom) \cdot T/Tnom - Eg(T))/Vt}$$

$$JS(T) = JS \cdot e^{(Eg(Tnom) \cdot T/Tnom - Eg(T))/Vt}$$

$$JSSW(T) = JSSW \cdot e^{(Eg(Tnom) \cdot T/Tnom - Eg(T))/Vt}$$

$$PB(T) = PB \cdot T/Tnom - 3 \cdot Vt \cdot \ln(T/Tnom) - Eg(Tnom) \cdot T/Tnom + Eg(T)$$

$$PBSW(T) = PBSW \cdot T/Tnom - 3 \cdot Vt \cdot \ln(T/Tnom) - Eg(Tnom) \cdot T/Tnom + Eg(T)$$

$$PHI(T) = PHI \cdot T/Tnom - 3 \cdot Vt \cdot \ln(T/Tnom) - Eg(Tnom) \cdot T/Tnom + Eg(T)$$

where $Eg(T)$ = silicon bandgap energy = $1.16 - .000702 \cdot T^2/(T + 1108)$

$$CBD(T) = CBD \cdot (1 + MJ \cdot (.0004 \cdot (T - Tnom) + (1 - PB(T)/PB)))$$

$$CBS(T) = CBS \cdot (1 + MJ \cdot (.0004 \cdot (T - Tnom) + (1 - PB(T)/PB)))$$

$$CJ(T) = CJ \cdot (1 + MJ \cdot (.0004 \cdot (T - Tnom) + (1 - PB(T)/PB)))$$

$$CJSW(T) = CJSW \cdot (1 + MJSW \cdot (.0004 \cdot (T - Tnom) + (1 - PB(T)/PB)))$$

$$KP(T) = KP \cdot (T/Tnom)^{-3/2}$$

$$UO(T) = UO \cdot (T/Tnom)^{-3/2}$$

The ohmic (parasitic) resistances have no temperature dependence.

Noise

Noise is calculated assuming a 1 Hertz bandwidth, with the following spectral power densities (per unit bandwidth):

the parasitic resistances (R_d , R_g , R_s and R_b) generate thermal noise ...

$$Id^2 = 4 \cdot k \cdot T / R_d$$

$$Ig^2 = 4 \cdot k \cdot T / R_g$$

$$Is^2 = 4 \cdot k \cdot T / R_s$$

$$Ib^2 = 4 \cdot k \cdot T / R_b$$

the intrinsic MOSFET generates shot and flicker noise ...

$$Idrain^2 = 4 \cdot k \cdot T \cdot gm \cdot 2/3 + KF \cdot Idrain^{AF} / (FREQUENCY \cdot Kchan)$$

where

$$gm = dIdrain/dVgs \text{ (at the DC bias point)}$$

$$Kchan = (\text{effective length})^2 \cdot (\text{permittivity of SiO}_2) / TOX$$

References

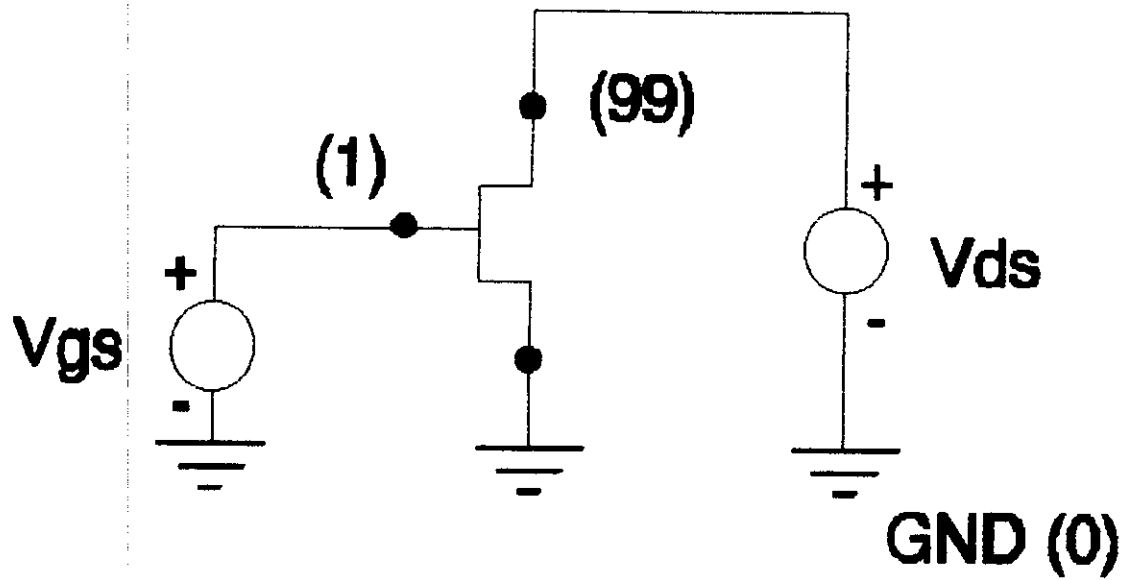
For a more complete description of the MOSFET models, see:

- [1] H. Shichman and D. A. Hodges, "Modeling and simulation of insulated-gate field-effect transistor switching circuits," *IEEE Journal of Solid-State Circuits*, SC-3, 285, September 1968
- [2] A. Vladimirescu, and S. Liu, *The Simulation of MOS Integrated Circuits Using SPICE2*, Memorandum No. M80/7, February 1980
- [3] B. J. Sheu, D. L. Scharfetter, P.-K. Ko, and M.-C. Jeng, "BSIM: Berkeley Short-Channel IGFET Model for MOS Transistors," *IEEE Journal of Solid-State Circuits*, SC-22, 558-566, August 1987
- [4] J. R. Pierret, *A MOS Parameter Extraction Program for the BSIM Model*, Memorandum No. M84/99 and M84/100, November 1984
- [5] P. Antognetti and G. Massobrio, *Semiconductor Device Modeling with SPICE*, McGraw-Hill, 1988

References [2] and [4] are available for \$10.00 (each) by sending a check payable to *The Regents of the University of California* to this address

Cindy Manly
EECS/ERL Industrial Support Office
497 Cory Hall
University of California
Berkeley, CA 94720

DC Curves: (I_{ds} vs V_{ds}) & (I_{ds} vs V_{gs})



Transconductance: $\left. \frac{\partial I_d}{\partial V_{gs}} \right|_{(V_{ds}, V_{gs})} \approx \left. \frac{\Delta I_d}{\Delta V_{gs}} \right|_{(V_{ds}, V_{gs})}$

Output Conductance: $\left. \frac{\partial I_d}{\partial V_{ds}} \right|_{(V_{ds}, V_{gs})} \approx \left. \frac{\Delta I_d}{\Delta V_{ds}} \right|_{(V_{ds}, V_{gs})}$

NMOS TRANSISTORS characteristics

* VLSI course/uProcessor Lab

* uLab A. CICUTTIN, and S. VENKATARAMAN - 1/Nov/94 - MO

* Model Parameters for the orbit's 1.2um CMOS process *

.MODEL NTRAN NMOS (

+ LEVEL = 2

+ UO = 521.3

+ VTO = 917E-3

+ NFS = 6E+11

+ TPG = 1

+ TOX = 22.5E-9

+ NSUB = 5.7E+16

+ UCRIT = 50.0E+3

+ UEXP = 85.6E-3

+ VMAX = 49.5E+3

+ RSH = 349.7

+ XJ = 300.0E-9

+ LD = 202.8E-9

+ DELTA = 5.28

+ PB = 0.8

+ JS = 10.0E-6

+ NEFF = 3.1

+ CJ = 556E-6

+ MJ = 435E-3

+ CJSW = 373.2E-12

+ MJSW = 344E-3

+ CGSO = 310E-12

+ CGDO = 310E-12

+ CGBO = 340E-12

+ FC = 500.0E-3

+ KP = 5.052E-29)

* The circuit description starts here *

*Independent voltages sources

* n+ n-

Vdd 99 0 dc 5v

Vg 1 0 dc 5v

** D G S S name length width areaD areaS perimeter numb. of squares

M1 99 1 0 0 NTRAN L=1.2U W=20U AD=75p AS=75p PD=32U PS=32U NRD=0.33 NRS=0.33

* Analysis *

*

*To plot Ids vs Vds with Vgs as parameter

.dc vdd 0 5 0.001 vg 0 2 0.4

.end

*Interactive commands

*

* to measure gm and gD: dc vdd 0 5 0.1 vg 2 2.1 0.02

*

*Interactive commands

* source nmos.cir

* run

* plot -vdd#branch

*

*To plot Ids vs Vgs with Vds as parameter

* dc vg 0 5 0.001 vdd 2 10 1

* plot -vdd#branch

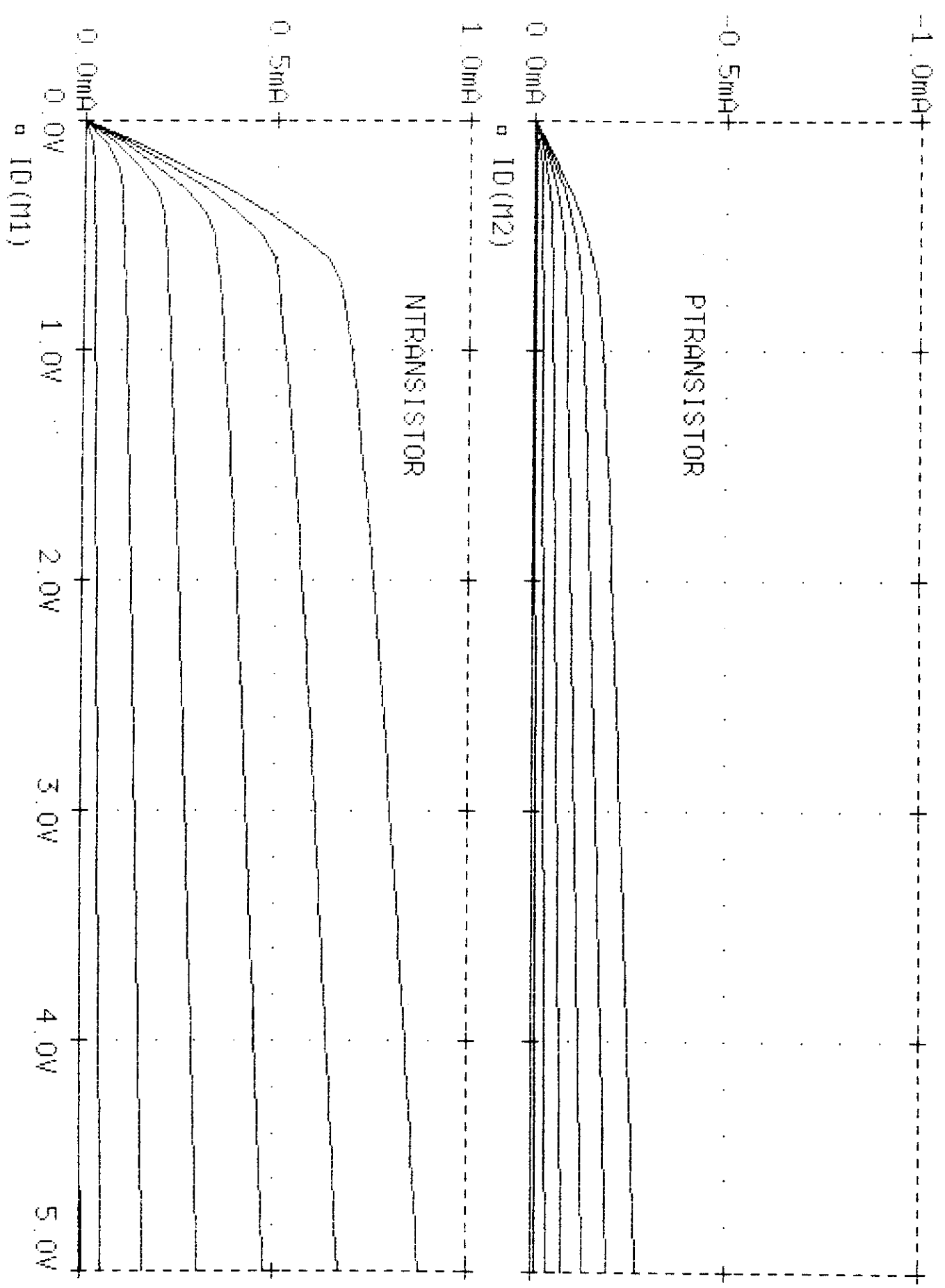
*

* With the mouse we can measure the slopes of the curves to obtain gm and gD

```

* PMOS TRANSISTOR characteristics
* VLSI course/uProcessor Lab
* uLab A. CICUTTIN, and S. VENKATARAMAN ~ 1/Nov/94 - MO
* Model Parameters for the orbit's 1.2um CMOS process *
*****
.MODEL PTRAN PMOS (
+ LEVEL = 2
+ UO = 167.5
+ VTO = -915E-3
+ NFS = 6.5E+11
+ TPG = -1
+ TOX = 22.5E-9
+ NSUB = 3.7E+16
+ UCRIT = 10.0E+3
+ UEXP = 99.3E-3
+ VMAX = 28.6E+3
+ RSH = 418.2
+ XJ = 300.0E-9
+ LD = 70.9E-9
+ DELTA = 2.15
+ PB = 0.8
+ JS = 10.0E-6
+ NEFF = 0.931
+ CJ = 448.6E-6
+ MJ = 404E-3
+ CJSW = 457E-12
+ MJSW = 334E-3
+ CGSO = 108E-12
+ CGDO = 108E-12
+ CGBO = 625E-12
+ FC = 500.0E-3
+ KF = 8.6E-30)
*****
* The circuit description starts here *
*Independent voltages sources
*      n+  n-
Vdd  99  0  dc 5v
Vg    1  0  dc 5v
*****
*      D  G  S  B  name length width
M2    99  1  0  0  PTRAN L=1.2U W=20U AD=75p AS=75p PD=32U PS=32U NRD=0.33 NRS=0.33
*****
* Analysis *
.dc vdd -5 0 0.1 vg -2 0 0.2
.end
*****
*Interactive commands:
* source pmos.cir
* run
* plot vdd#branch
* dc vg -2 0 0.001 vdd -10 -1 1
* plot vdd#branch

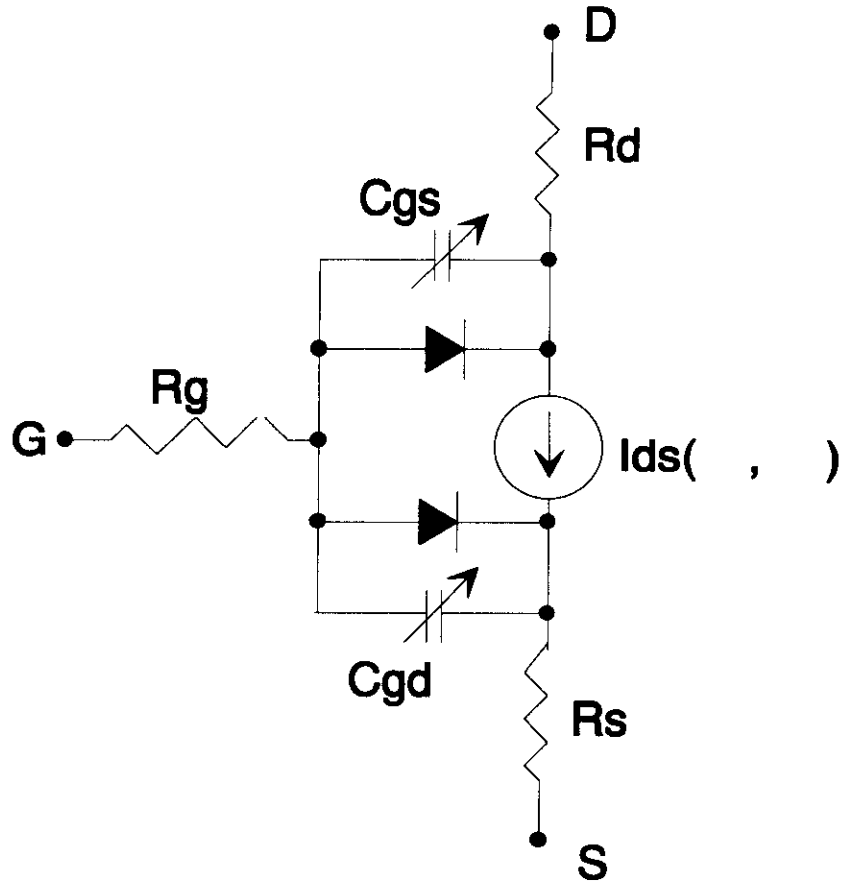
```



MESFET SPICE MODEL
(MEtal Semiconductor Field Effect Transistor)

Depletion MESFET (DMESFET)
normally on
threshold voltage (V_{to}) < 0V

Enhancement MESFET (EMESFET)
normally off
threshold voltage (V_{to}) > 0V



(Not algebraic) coupled equations:

$$V_{ds} - I_{ds}(V_{ds}, V_{gs}) * (R_s + R_d) = V_{ds}$$

$$V_{gs} - I_{ds}(V_{ds}, V_{gs}) * R_s = V_{gs}$$

SCHOTTKY DIODE

$$I_g = I_0 \left[\frac{V_{gs} - I_g(RG + (Rs * Rd) / (Rd + Rs))}{nkT} \right]$$

where

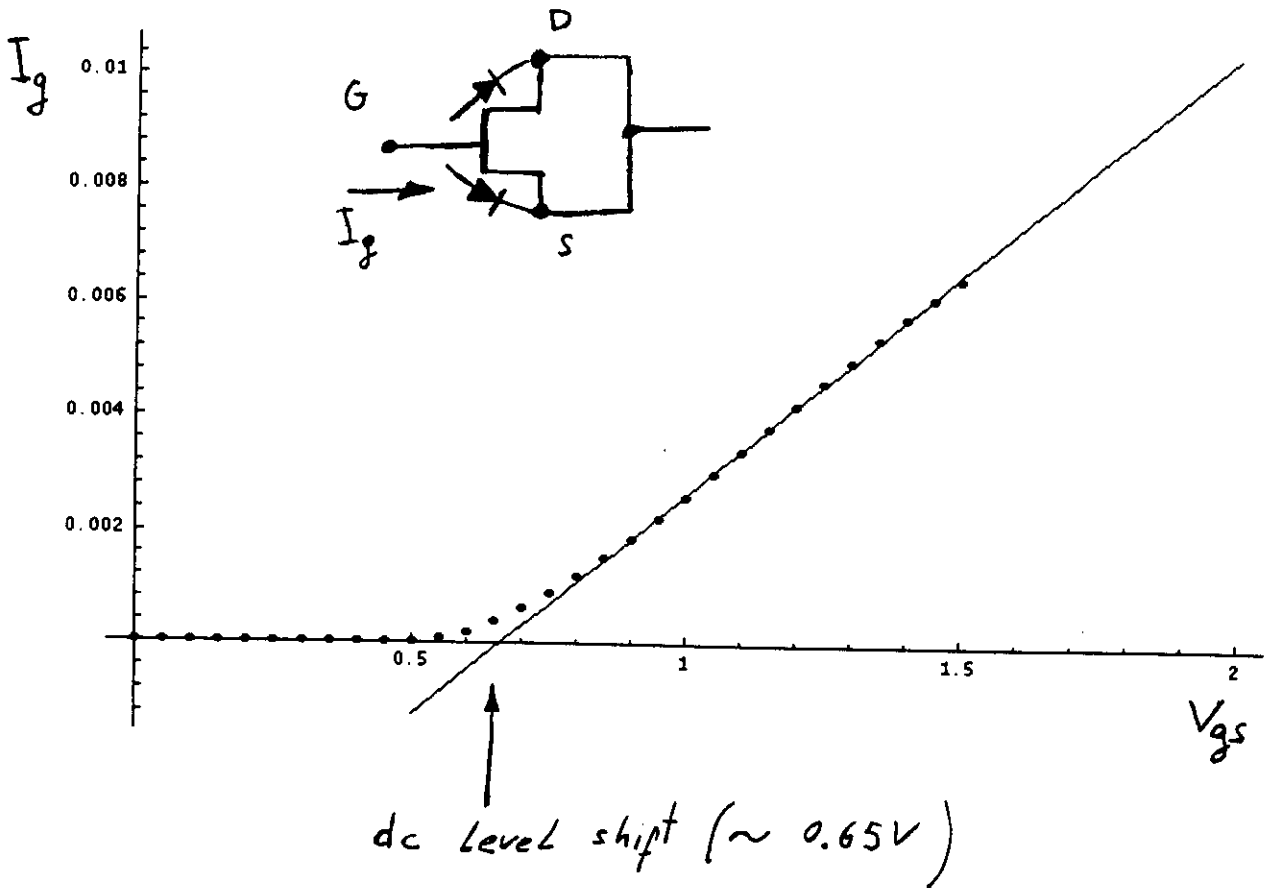
$$I_0 = A * T^2 L W \exp(V_{bi} / kT)$$

A: Richardson constant

n: ideality factor

V_{bi} : Schottky forward voltage

L, W : Length and width of the gate



MESFET Models (both N and P Channel)

spice. 3e1

The MESFET model is derived from the GaAs FET model of Statz et al. as described in [6]. The dc characteristics are defined by the parameters VTO, B, and BETA, which determine the variation of drain current with gate voltage, ALPHA, which determines saturation voltage, and LAMBDA, which determines the output conductance. The formula are given by:

$$I_d = \frac{\beta (V_{gs} - V_T)^2}{1 + b(V_{gs} - V_T)} \left[1 - \left[1 - \alpha \frac{V_{ds}}{3} \right]^3 \right] (1 + \lambda V_{ds}) \quad \text{for } 0 < V_{ds} < \frac{3}{\alpha}$$

$$I_d = \frac{\beta (V_{gs} - V_T)^2}{1 + b(V_{gs} - V_T)} (1 - \lambda V_{ds}) \quad \text{for } V_{ds} > \frac{3}{\alpha}$$

Two ohmic resistances, RD and RS, are included. Charge storage is modeled by total gate charge as a function of gate-drain and gate-source voltages and is defined by the parameters CGS, CGD, and PB.

	name	parameter	units	default	example	area
1	VTO	pinch-off voltage	V	-2.0	-2.0	
2	BETA	transconductance parameter	A/V ²	1.0e-4	1.0e-3	*
3	B	doping tail extending parameter	1/V	0.3	0.3	*
4	ALPHA	saturation voltage parameter	1/V	2	2	*
5	LAMBDA	channel length modulation parameter	1/V	0	1.0e-4	
6	RD	drain ohmic resistance	Ω	0	100	*
7	RS	source ohmic resistance	Ω	0	100	*
8	CGS	zero-bias G-S junction capacitance	F	0	5pF	*
9	CGD	zero-bias G-D junction capacitance	F	0	1pF	*
10	PB	gate junction potential	V	1	0.6	
11	KF	flicker noise coefficient	-	0		
12	AF	flicker noise exponent	-	1		
13	FC	coefficient for forward-bias depletion capacitance formula	-	0.5		

PSpice

Equations for Idrain: LEVEL=1

For: $V_{ds} \geq 0$ (normal mode)

and: $V_{gs} - V_{TO} < 0$ (cutoff region)

$$I_{drain} = 0$$

and: $V_{gs} - V_{TO} \geq 0$ (linear & saturation region)

$$I_{drain} = BETA \cdot (1 + LAMBDA \cdot V_{ds}) \cdot (V_{gs} - V_{TO})^2 \cdot \tanh(ALPHA \cdot V_{ds})$$

For: $V_{ds} < 0$ (inverted mode)

Switch the source and drain in equations (above).

Equations for Idrain: LEVEL=2 (Spice)

For: $V_{ds} \geq 0$ (normal mode)

and: $V_{gs} - V_{TO} < 0$ (cutoff region)

$$I_{drain} = 0$$

and: $V_{gs} - V_{TO} \geq 0$ (linear & saturation region)

$$I_{drain} = BETA \cdot (1 + LAMBDA \cdot V_{ds}) \cdot (V_{gs} - V_{TO})^2 \cdot K_t / (1 + E \cdot (V_{gs} - V_{TO}))$$

where K_t (a polynomial approximation of $\tanh$) is:

for: $0 < V_{ds} < 3/ALPHA$ (linear region)

$$K_t = 1 - (1 - V_{ds} \cdot ALPHA/3)^3$$

for: $V_{ds} \geq 3/ALPHA$ (saturation region)

$$K_t = 1$$

For: $V_{ds} < 0$ (inverted mode)

Switch the source and drain in equations (above).

```

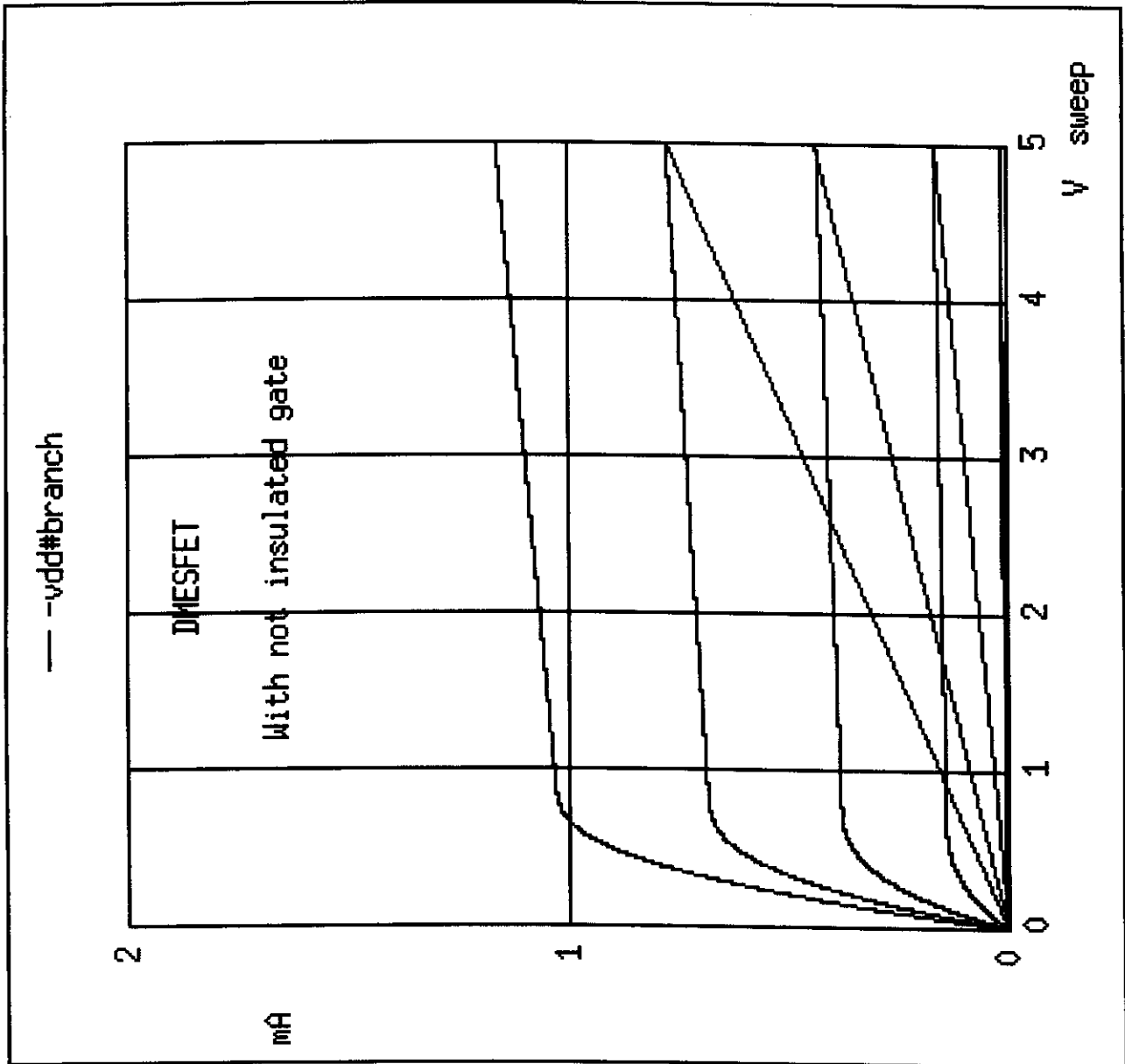
DMESFET characteristics
* VLSI course/uProcessor Lab
* uLab A. CICUTTIN, and S. VENKATARAMAN - 1/Nov/94 - MO
* Model Parameters for the vitesse's 0.8um GaAs process *
*****
.model dmesfet nmf(vto=-0.86 beta=2.68e-4 lambda=0.037 alpha=3.91
+ b=0.88 rs=1300 rd=1300 is=7.66e-14 cgs=1.4ff cgd=0.08ff pb=0.8)
*****
* The circuit description starts here *
*Independent voltages sources
*      n+   n-
Vdd  99   0   dc 5
vg    1   0   dc 5
vf    2   0   dc 5
*****
*   d g s model W

z1  99 1 0 dmesfet 10
*****
* to see the diodes
*z2 0 1 0 dmesfet 10
* dc vg 0 1 0.001
* We can obtain RS+RD from this curve (plot -vg#branch)
*****
* Analysis *
*   sweep i. f. step
.dc vdd 0 5 0.001 vg -1 0 0.2

.end

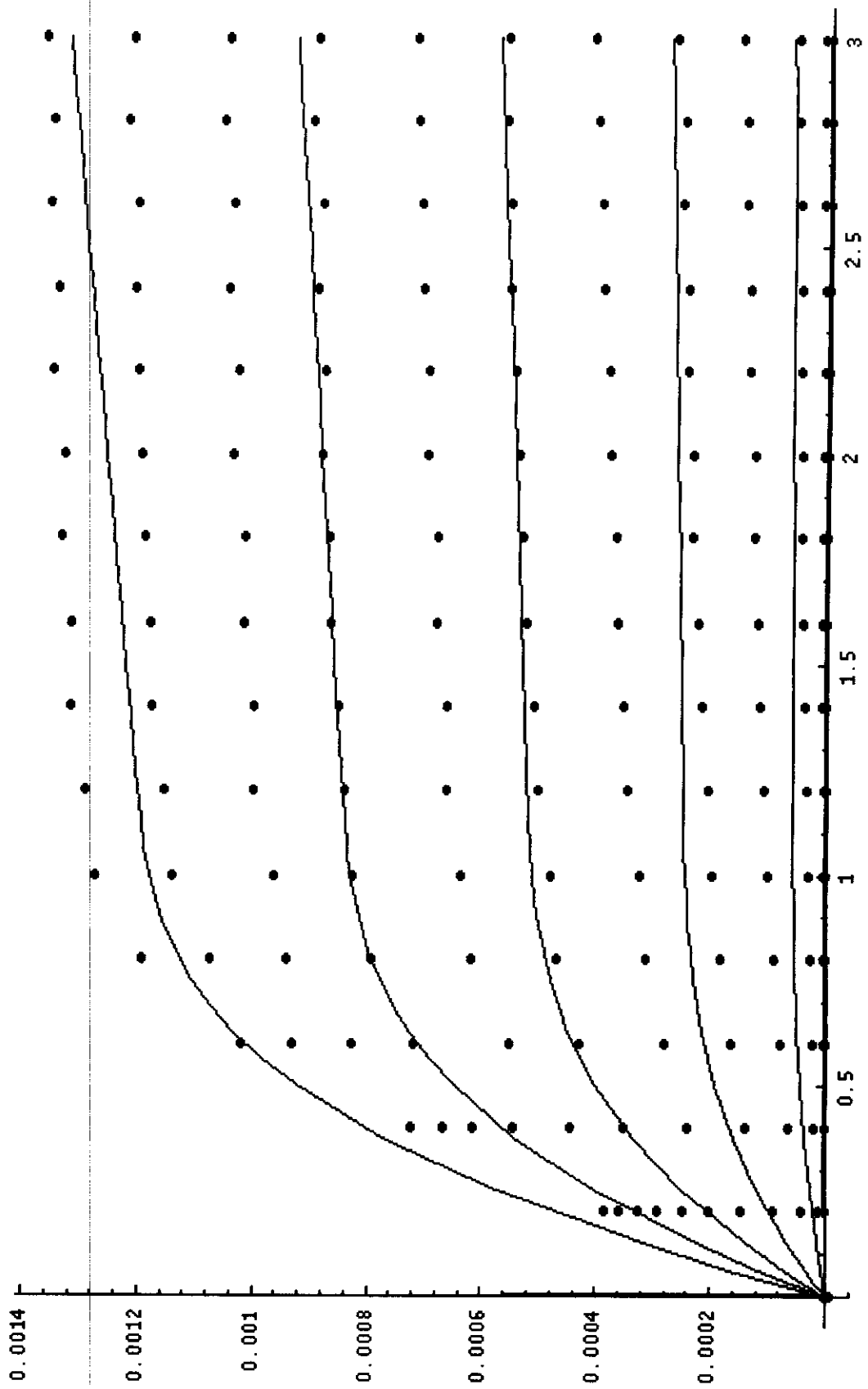
*****
*Interactive commands
*
* run
* plot -vdd#branch
* (to show the threshold voltage): dc vg -2 0 0.001 vdd 1 5 1
* plot -vdd#branch

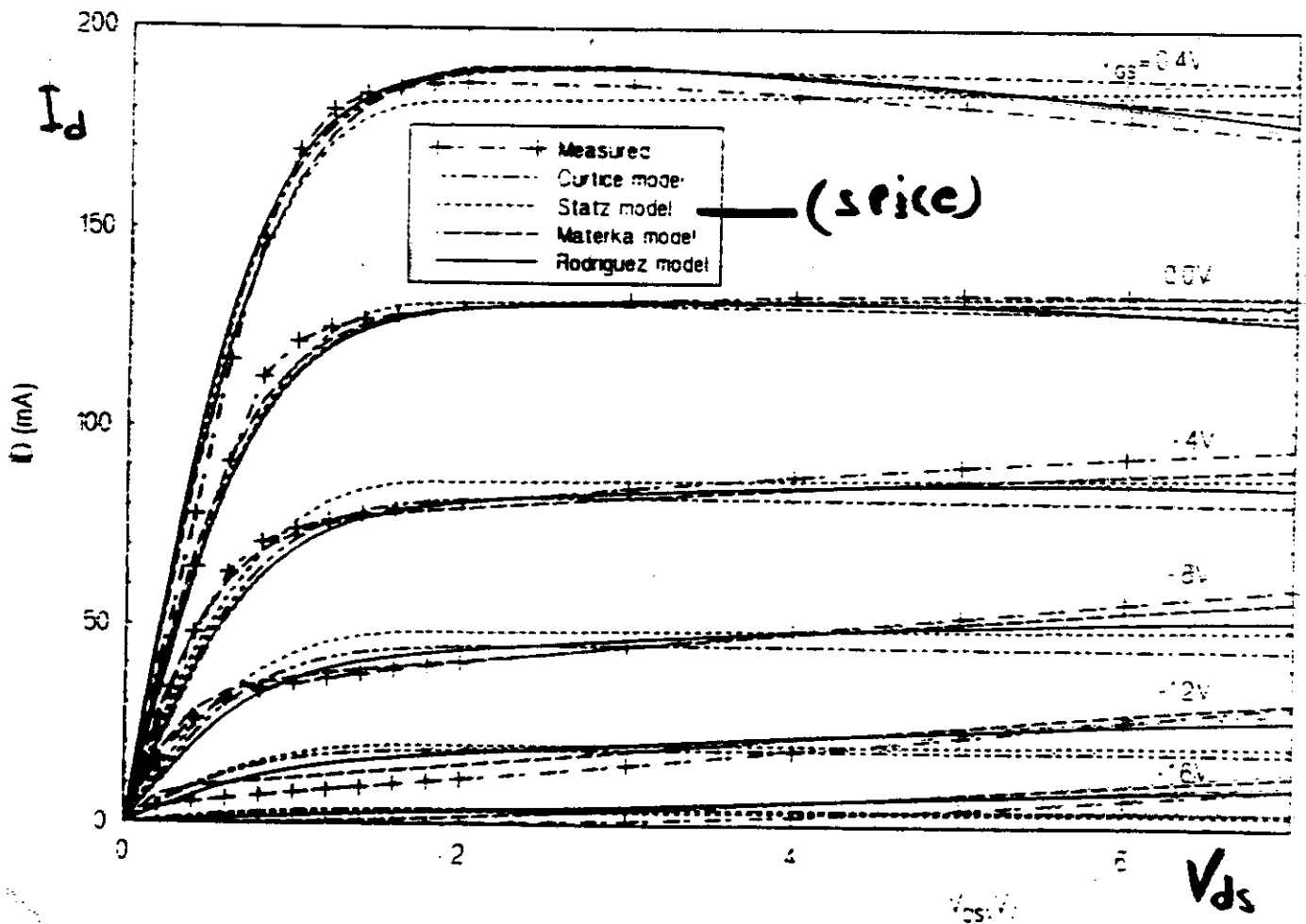
```



quit

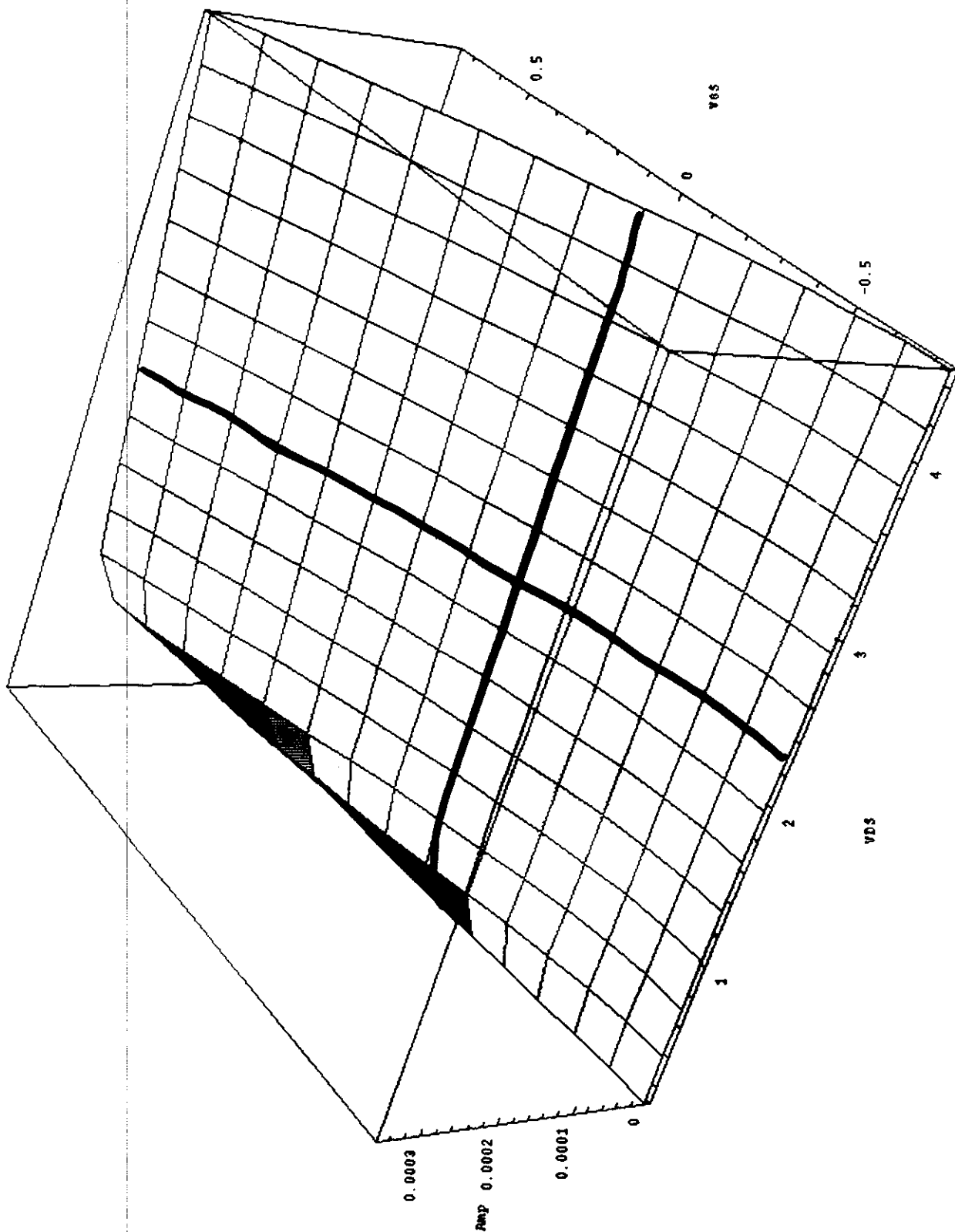
hardcopy





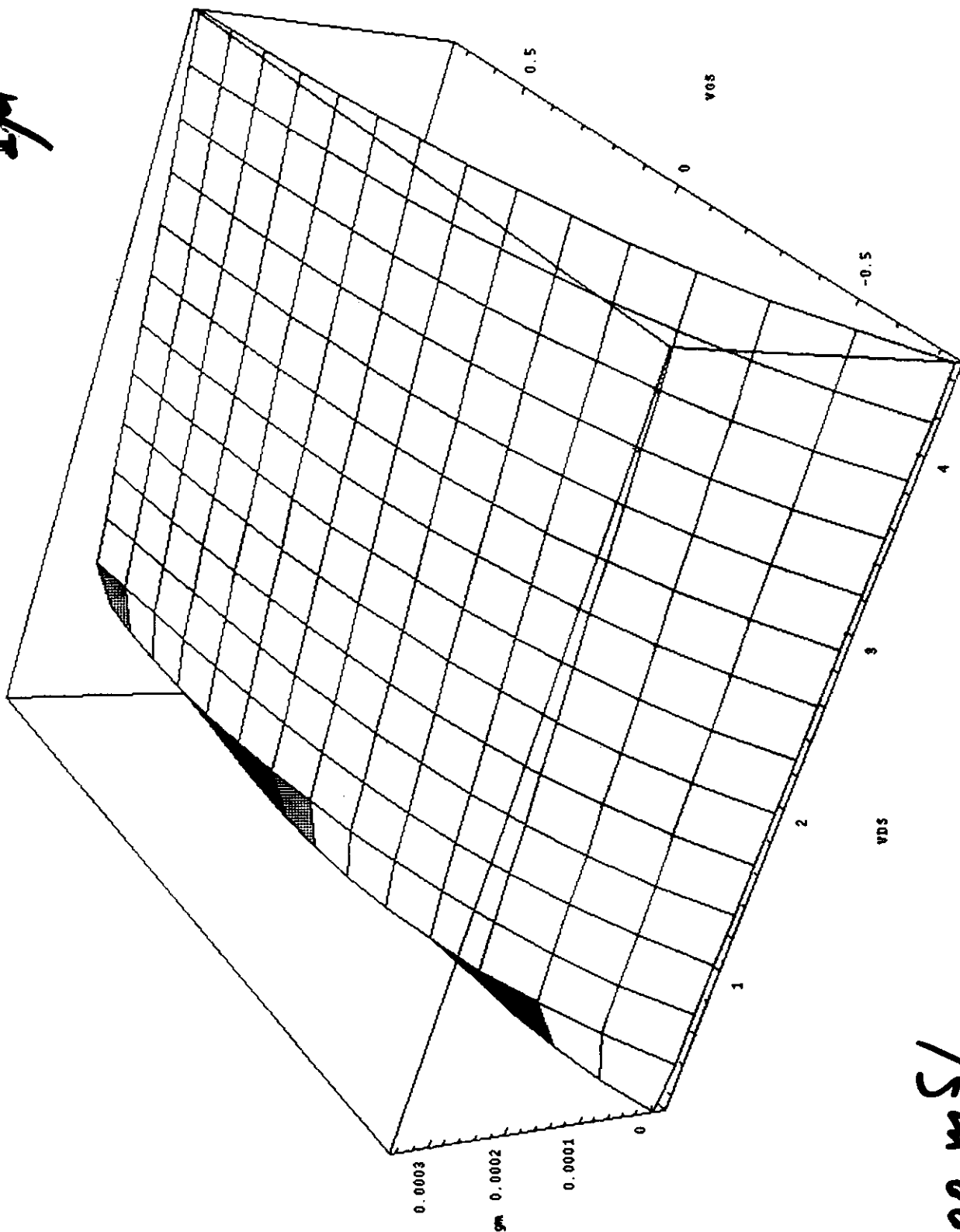
Comparison of measured and computed data for $6 \times 150 \mu m$ device.

I_{ds}



(Transconductance)

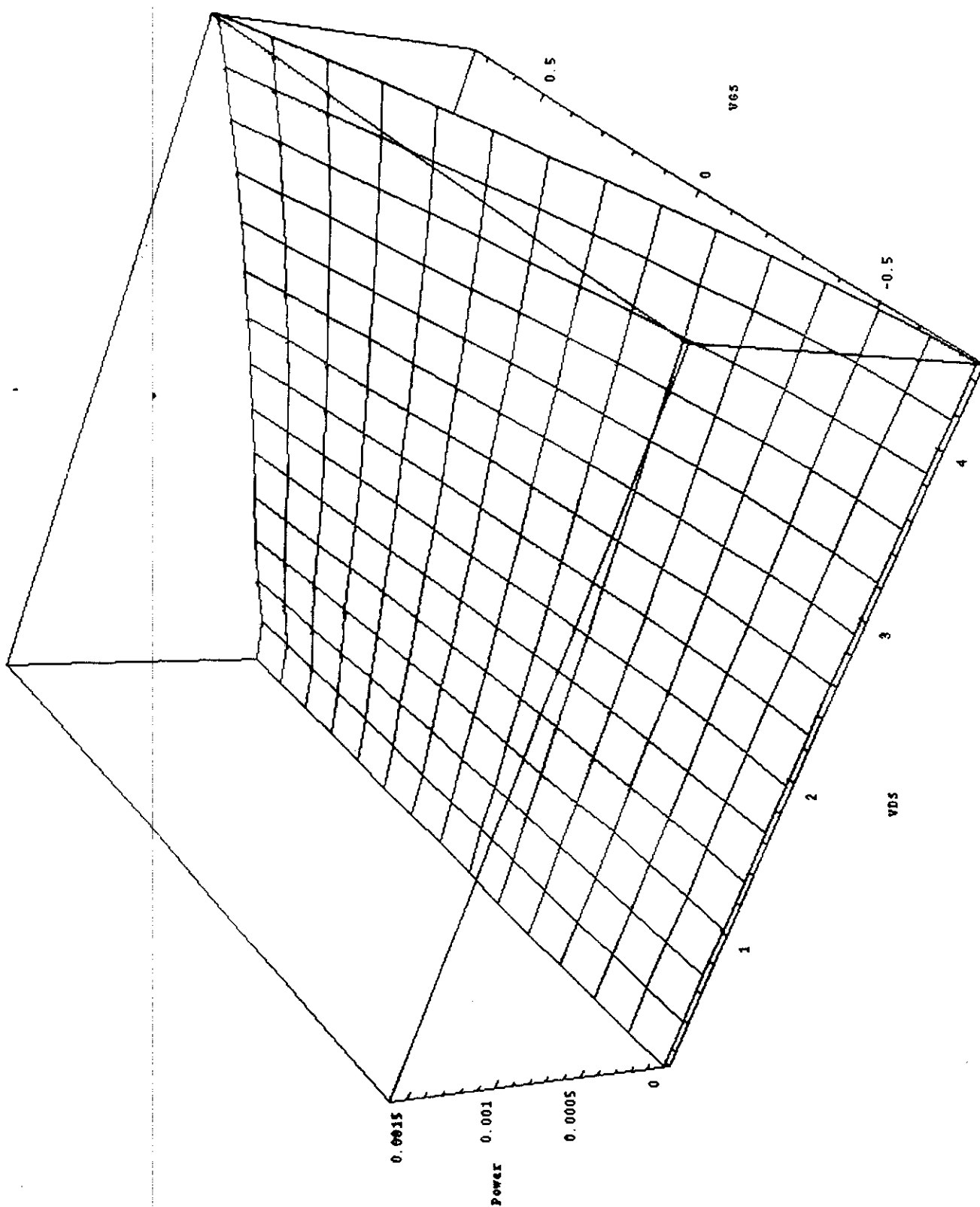
1/4



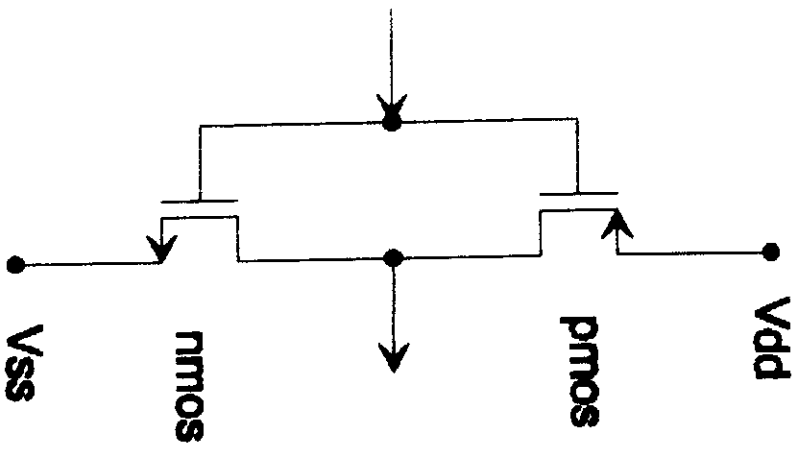
$g_m \sim 300 \text{ mS/mm}$

12-01 24-01 25-01 26-01 27-01 28-01 29-01 30-01 31-01 32-01 33-01 34-01 35-01 36-01 37-01 38-01 39-01 40-01 41-01 42-01 43-01 44-01 45-01 46-01 47-01 48-01 49-01 50-01 51-01 52-01 53-01 54-01 55-01 56-01 57-01 58-01 59-01 60-01 61-01 62-01 63-01 64-01 65-01 66-01 67-01 68-01 69-01 70-01 71-01 72-01 73-01 74-01 75-01 76-01 77-01 78-01 79-01 80-01 81-01 82-01 83-01 84-01 85-01 86-01 87-01 88-01 89-01 90-01 91-01 92-01 93-01 94-01 95-01 96-01 97-01 98-01 99-01 100-01

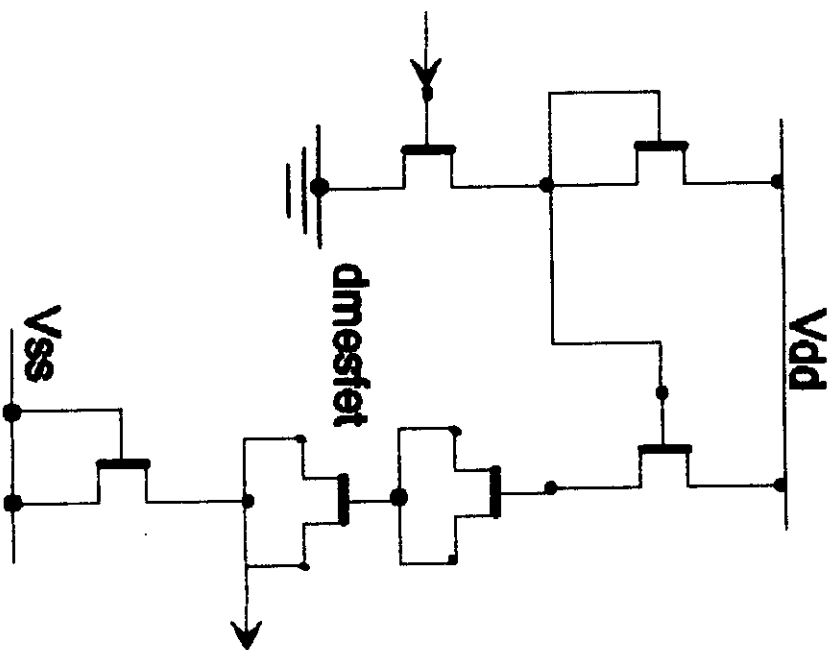
dissipation power



CMOS (Si)



BFL (GaAs)



```

*** CMOS - Inverter
*** technology : orbitn12
*** extraction style : orbitn12
*** Root Cell Nodes :
*** Vdd = 1 i = 3 f = 2
* M1 --> x = 193, y = 133
* M2 --> x = 193, y = 65
*****
vdd 1 0 dc 5v
vin 3 0 dc pulse(0 5 1ns 0.01ns 0.01ns 2ns 4ns)

* d g s b model width length

M1 2 3 1 1 PTRAN W=18U L=1.2U AD=67.8P AS=67.8P PD=22.2U PS=26.6U
M2 2 3 0 0 NTRAN W=6U L=1.2U AD=22.6P AS=22.6P PD=14.2U PS=14.2U
c2 2 0 20fF
*
.tran 10ps 6ns
*****
*Interactive commands:
* source CMOS.raw
* run
* " To measure fall, rise and prop. time delay: "
* plot v(3) v(2) 0.5 4.5 2.5
* show vdd (power dissipation)
* " To display the transfer function: "
* dc vin 0 5 0.001
* plot v(3) v(2)
* plot v(3) vs v(2) v(2) vs v(3)
*****
* Model of the transistors for the Orbit 1.2um Process*
*.op
*.options itl1=5000 itl4=5000
* Model Parameters for the orbit's 1.2um CMOS process *
*****
.MODEL NTRAN NMOS (
+ LEVEL = 2
+ UO = 521.3
+ VTO = 917E-3
+ NFS = 6E+11
+ TPG = 1
+ TOX = 22.5E-9
+ NSUB = 5.7E+16
+ UCRIT = 50.0E+3
+ UEXP = 85.6E-3
+ VMAX = 49.5E+3
+ RSH = 349.7
+ XJ = 300.0E-9
+ LD = 202.3E-9
+ DELTA = 5.28
+ PB = 0.8
+ JS = 10.0E-6
+ NEFF = 3.1
+ CJ = 556E-6
+ MJ = 435E-3
+ CJSW = 373.2E-12
+ MJSW = 344E-3
+ CGSO = 310E-12
+ CGDO = 310E-12
+ CGBO = 340E-12
+ FC = 500.0E-3
+ KF = 5.21E-28)
*****
.MODEL PTRAN PMOS (
+ LEVEL = 2
+ UO = 167.5
+ VTO = -915E-p
+ NFS = 6.5E+11
+ TPG = -1
+ TOX = 22.5E-9
+ NSUB = 3.7E+16
+ UCRIT = 10.0E+3
+ UEXP = 99.3E-3
+ VMAX = 28.6E+3
+ RSH = 418.2
+ XJ = 300.0E-9
+ LD = 70.9E-9
+ DELTA = 2.15
+ PB = 0.8
+ JS = 10.0E-6

```

```
+ NEFF = 0.931
+ CJ = 448.6E-6
+ MJ = 404E-3
+ CJSW = 457E-12
+ MJSW = 334E-3
+ CGSO = 108E-12
+ CGDO = 108E-12
+ CGBO = 625E-12
+ FC = 500.0E-3
+ KF = 8.6E-30)
*****
.end
```

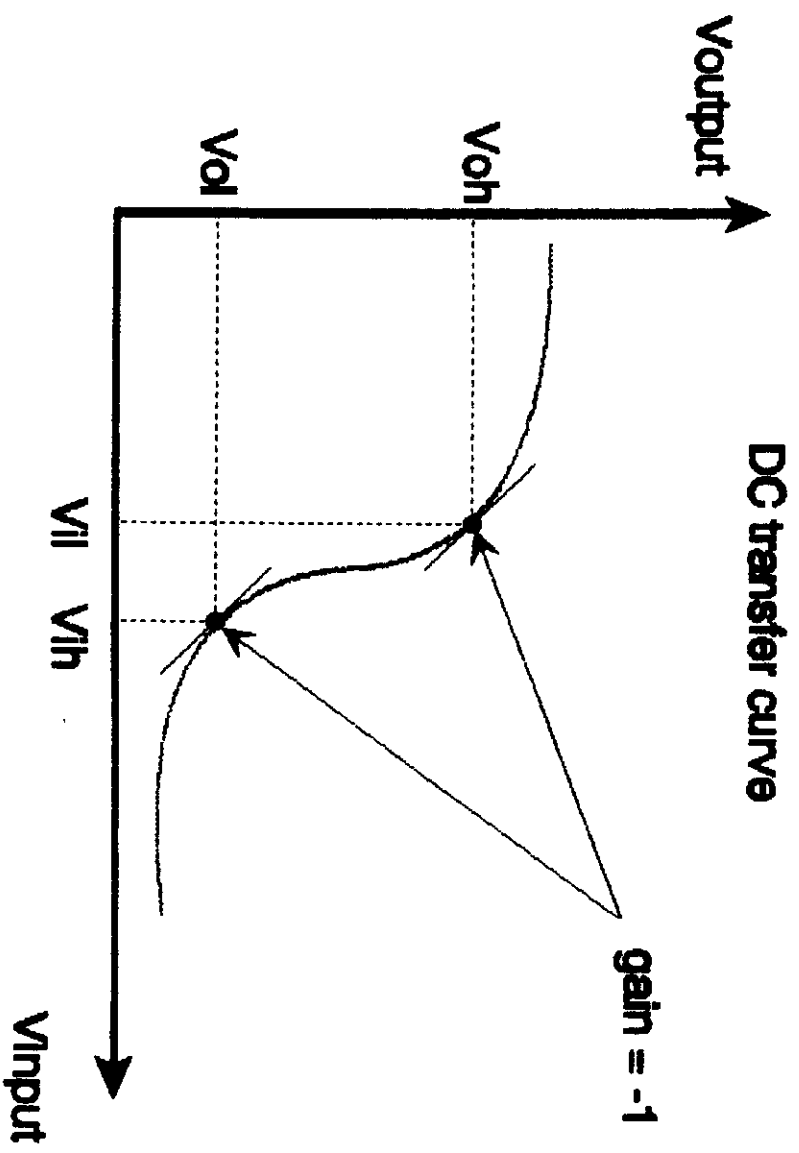
```

*BFL INVERTER - VITESSE for 1.2um
vdd 99 0 dc 2.5V
vss 88 0 dc -2.5V
vin 1 0 dc pulse(-1.75v 0v 100ps 5ps 5ps 2ns 4ns)
* L=1.2um W=1um depletion mode mesfet
*
*Inverter definition:
*   d   g   s
z1 99 2 2 dmesfet 2
z2 2 1 0 dmesfet 7
z3 99 2 3 dmesfet 10
z4 6 88 88 dmesfet 6
z5 4 3 4 dmesfet 2
z6 5 4 5 dmesfet 2
z7 6 5 6 dmesfet 2
*
*Output capacitive load:
c5 6 0 5ff
*Transient analysis : (taking points for plotting each 5ps, from 0s to
*                      5ns with 2ps of maximum step calculation )
.tran 5ps 5ns 0 2ps

*Parameters for MESFET model
.model dmesfet nmf(vto=-0.86 beta=2.68e-4 lambda=0.037 alpha=3.91
+ b=0.88 rs=1300 rd=1300 is=7.66e-14 cgs=1.4ff cgd=0.08ff pb=0.8)

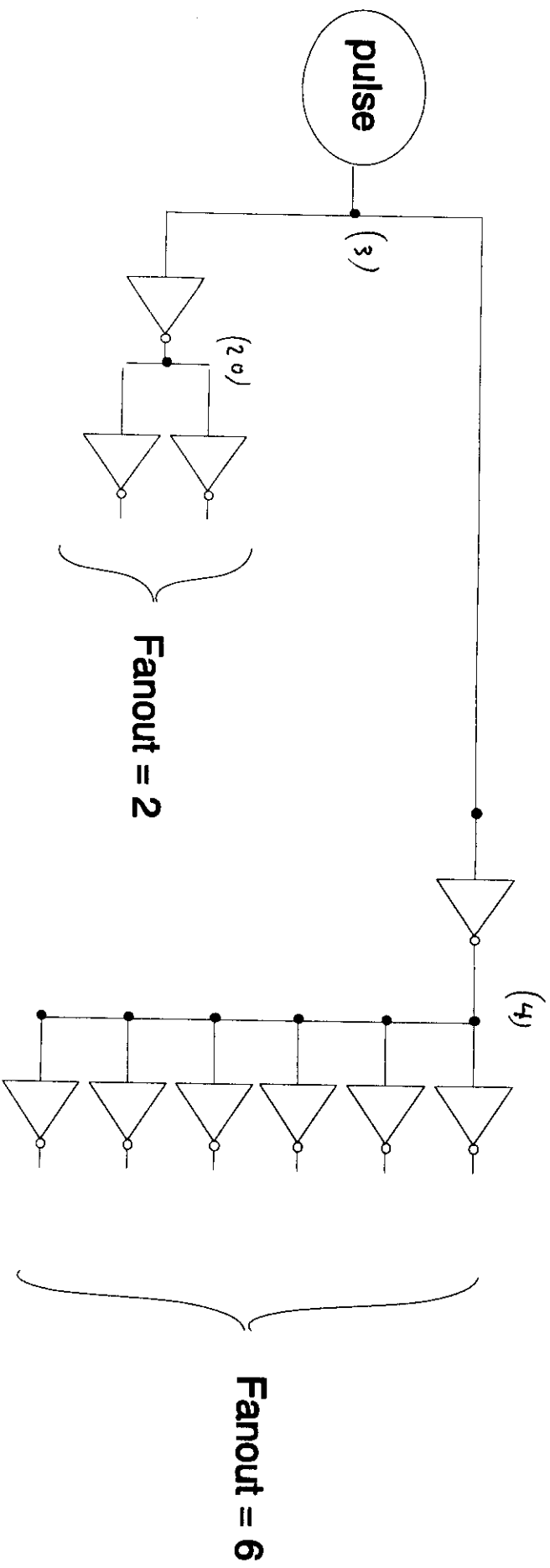
.end
*****
* Interactive commands:
* source BFL.raw
* run
* plot v(1) v(6)
* (zoom to mesure rise, fall and delay time)
* plot v(1) v(6) (-1.75+0.175) (-1.75/2) (-0.175)
*
*****
* dc vin -2 1 0.001
* plot v(1) v(6)
* plot v(6) v(5) v(4) v(3)
* plot v(6) vs v(1) v(1) vs v(6)

```

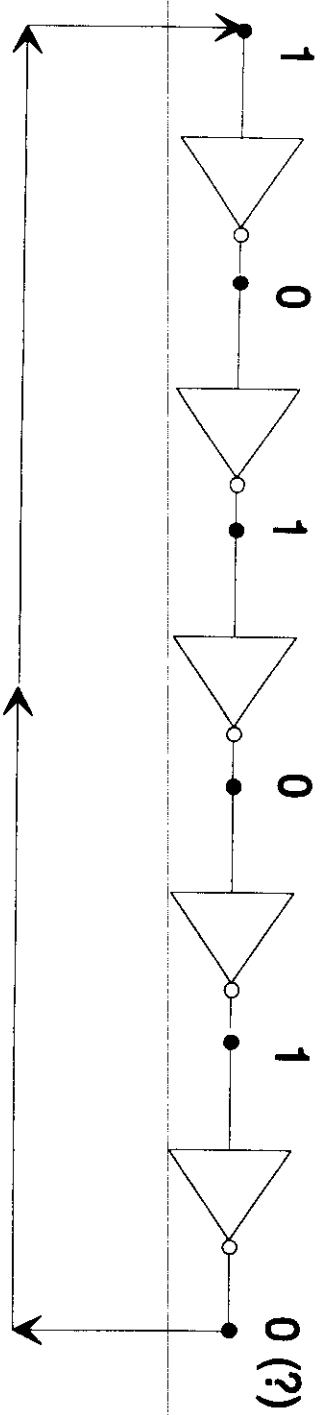


Noise Margine High = $V_{OH} - V_{IH}$

Noise Margine low = $V_{IH} - V_{OL}$



Ring Oscillator



```
*BFL INVERTER - VITESSE for 1.2um (chan. length)
vdd 99 0 2.5V
vss 88 0 -2.5V
vin 3 0 dc pulse(-1.75v 0v 100ps 5ps 5ps 2ns 4ns)
* depletion mesfet's
```

```
*Fan-out = 6
xinv6 3 4 99 88 inv
xinv11 4 5 99 88 inv
xinv12 4 6 99 88 inv
xinv13 4 7 99 88 inv
xinv14 4 8 99 88 inv
xinv15 4 9 99 88 inv
xinv16 4 10 99 88 inv
```

```
*fan-out = 2
```

```
xinv2 3 20 99 88 inv
xinv7 20 21 99 88 inv
xinv8 20 22 99 88 inv
.tran 10ps 10ns
```

```
*Interactive command
* plot v(1) v(2) v(7) (-0.157) (-1.57+0.157) (-1.57/2)
```

```
*subcircuit definition:
.subckt inv 1 6 99 88
*   d   g   s
z1 99 2 2 dmesfet 2
z2 2 1 0 dmesfet 7
z3 99 2 3 dmesfet 10
z4 6 88 88 dmesfet 6
z5 4 3 4 dmesfet 2
z6 5 4 5 dmesfet 2
z7 6 5 6 dmesfet 2
.ends
```

```
.tran 5ps 5ns 0 2ps
```

```
.model dmesfet nmf(vto=-0.86 beta=2.68e-4 lambda=0.037 alpha=3.91
+ b=0.88 rs=1300 rd=1300 is=7.66e-14 cgs=1.4ff cgd=0.08ff pb=0.8)
*.model sbd d(is=1.0e-14 rs=600 n=1.1 cj0=.001f vj=0.7 m=.33)
```

```
.end
```

```
*****
* Interactive commands
* source BFLfan.raw
* run
* plot v(3) v(4) v(20)
* zoom to mesure rise, fall and delay time
* plot v(3) v(4) v(20) (-0.175) (-1.75+0.175) (-1.75/2)
*
*****
```

```

*BFL INVERTER - VITESSE for 1.2um
vdd 99 0 2.5V
vss 88 0 -2.50V
* L=1.2um W=1um depletion mode mesfet

x1 1 2 99 88 inv
x2 2 3 99 88 inv
x3 3 4 99 88 inv
x4 4 5 99 88 inv
x5 5 1 99 88 inv

.subckt inv 1 6 99 88
z1 99 2 2 dmesfet 2
z2 2 1 0 dmesfet 7
z3 99 2 3 dmesfet 10
z4 6 88 88 dmesfet 6
z5 4 3 4 dmesfet 2
z6 5 4 5 dmesfet 2
z7 6 5 6 dmesfet 2
*c5 5 0 20fF
.ends inv
.tran 5ps 5ns 0 2ps

.model dmesfet nmf(vto=-0.86 beta=2.68e-4 lambda=0.037 alpha=3.91
+ b=0.88 rs=1300 rd=1300 is=7.66e-14 cgs=1.4ff cgd=0.08ff pb=0.8)
*.model sbd d(is=1.0e-14 rs=600 n=1.1 cj0=.001f vj=0.7 m=.33)

.end
*****
* Interactive commands
* source BFLrin.raw
* run
* plot v(1)
*****

```

CMOS * FAN-OUT

vdd 1 0 dc 5v

vin 3 0 dc pulse(0 5 1ns 0.01ns 0.01ns 2ns 4ns)

*vin 3 0 dc pulse(0 5 1ns 0.01ns 0.01ns 2ns 4ns)

*Fan-out = 6

xinv6 3 4 1 inv

xinv11 4 5 1 inv

xinv12 4 6 1 inv

xinv13 4 7 1 inv

xinv14 4 8 1 inv

xinv15 4 9 1 inv

xinv16 4 10 1 inv

*fan-out = 2

xinv2 3 20 1 inv

xinv7 20 21 1 inv

xinv8 20 22 1 inv

.tran 10ps 10ns

* d g s b model width length

.subckt inv 3 2 1

M1 2 3 1 1 PTRAN W=18U L=1.2U AD=47.2P AS=62.8P PD=22.2U PS=26.6U

M2 2 3 0 0 NTRAN W=6U L=1.2U AD=22.6P AS=22.6P PD=14.2U PS=14.2U

.ends

* Interactive commands:

* source CMOSfan.raw

* run

* plot v(4) v(20) v(3) 0.5 4.5 2.5

*

* Model of the transistors for the Orbit 1.2um Process*

.MODEL NTRAN NMOS (

+ LEVEL = 2

+ UO = 521.3

+ VTO = 917E-3

+ NFS = 6E+11

+ TPG = 1

+ TOX = 22.5E-9

+ NSUB = 5.7E+16

+ UCRIT = 50.0E+3

+ UEXP = 85.6E-3

+ VMAX = 49.5E+3

+ RSH = 349.7

+ XJ = 300.0E-9

+ LD = 202.3E-9

+ DELTA = 5.28

+ PB = 0.8

+ JS = 10.0E-6

+ NEFF = 3.1

+ CJ = 556E-6

+ MJ = 435E-3

+ CJSW = 373.2E-12

+ MJSW = 344E-3

+ CGSO = 310E-12

+ CGDO = 310E-12

+ CGBO = 340E-12

+ FC = 500.0E-3

+ KF = 5.21E-28)

.MODEL PTRAN PMOS (

+ LEVEL = 2

+ UO = 167.5

+ VTO = -915E-p

+ TPG = -1

+ TOX = 22.5E-9

+ NSUB = 3.7E+16

+ UCRIT = 10.0E+3

+ UEXP = 99.3E-3

+ VMAX = 28.6E+3

+ RSH = 418.2

+ XJ = 300.0E-9

+ LD = 70.9E-9

```
+ DELTA = 2.15
+ PB = 0.8
+ JS = 10.0E-6
+ NEFF = 0.931
+ CJ = 448.6E-6
+ MJ = 404E-3
+ CJSW = 457E-12
+ MJSW = 334E-3
+ CGSO = 108E-12
+ CGDO = 108E-12
+ CGBO = 625E-12
+ FC = 500.0E-3
+ KF = 8.6E-30)
*****
.end
```

CMOS * RING OSCILATOR

vdd 99 0 dc 5v

*vin 3 0 dc pulse(0 5 1ns 0.01ns 0.01ns 2ns 4ns)

*Ring Oscillator with 5 inverters

xinv1 1 2 99 inv

xinv2 2 3 99 inv

xinv3 3 4 99 inv

xinv4 4 5 99 inv

xinv5 5 1 99 inv

.tran 10ps 20ns

* Inverter definition: (the node-numbers: (2) (3) (1) are local)

.subckt inv 3 2 1

M1 2 3 1 1 PTRAN W=18U L=1.2U AD=47.2P AS=62.8P PD=22.2U PS=26.6U

M2 2 3 0 0 NTRAN W=6U L=1.2U AD=22.6P AS=22.6P PD=14.2U PS=14.2U

.ends inv

* Interactive commands:

* source CMOSrin.raw

* run

* plot v(1)

*

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```
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+ CGDO = 108E-12
+ CGBO = 625E-12
+ FC = 500.0E-3
+ KF = 8.6E-30)
*****
.end
```

