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The United Nations University

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ICTP-INFN-UNU-MICROPROCESSOR LABORATORY
THIRD COURSE ON BASIC VLSI DESIGN TECHNIQUES
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Additional Material to Lectures

by

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These are preliminary lecture notes, intended only for distribution to participants.

1149.1-compatible products

What do vendors have to offer?

This list indicates the products that I am currently aware of that support IEEE Std 1149.1. It has been complied from product literature, press announcements, editorial articles, and other sources. Some products are available now, while others are announced (but not shippable) products. Please check the product's status with the supplier.

Please note that:

- No guarantee is offered that the list is correct or complete •
- Inclusion of a product on this list does not imply any endorsement •
- Ownership of all trademarks and registered trademarks is acknowledged •

For more details on specific products, please contact the vendor concerned.

If you have a product that's not on this list or wish to correct a product listing, please let me know.

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List produced on December 8, 1993

ASIC Vendors

AT&T Microelectronics

Atmel

ATL-series	0.8um CMOS gate arrays
ATL-4-ATL160	Up to 167K gates and 360 pins

European Silicon Structures

SOLO 2030	

Fujitsu

	Soft macros

GEC Plessey Semiconductors

CLA60000	Includes BIST

Hitachi

HG625	0.8um CMOS gate array
HG62G	0.8um CMOS gate array

IBM

CMOS 4L	0.8um CMOS gate arrays, up to 230K gates, 320 pins
CMOS 4L	0.8um CMOS standard cell, up to 260K gates, 320 pins
CMOS 4LP	0.8um CMOS gate arrays, up to 230K gates, 320 pins
CMOS 4LP	0.8um CMOS standard cell, up to 260K gates, 320 pins
CMOS 5L	0.5um CMOS gate arrays, up to 1180K gates, 508 pins
CMOS 5L	0.5um CMOS standard cell, up to 1240K gates, 508 pins

LSI Logic

LEA 200K	0.7um CMOS gate arrays up to 307K gates

Matra

Motorola

MCA4	
H4C	

National Semiconductor

NEC

CMOS-8L	Gate arrays up to 627K gates
CMOS-8LCX	

Philips

PGT200	1.5um gate array
VSC120	1.5um cell design
VGT50	1.0um gate array
VSC350	1.0um cell design high speed
VSC370	1.0um cell design high density
VGT450	0.8um gate array
VSC450	0.8um cell design

SGS-Thomson

ISB24000 series	0.7um, up to 216K gates, 408 pins

Siemens

SCxD4	1.0um gate array
SCxE6	0.8um gate array
SCoE	0.8um cell design

Texas Instruments

TGB1000	BiCMOS gate array
TEB1000	
TGC1000	0.8um CMOS gate array
TGC1000LV	0.8um CMOS gate array
TEC1000	
TEC1000LV	
TSC700 series	1.0um CMOS standard cell

Thomson Composants Militaires et Spatiaux

TSBC3	CSAM design kit

Toshiba

TC110G	1.5um CMOS gate array (soft macros)
TC140G	1.0um CMOS gate array (soft macros)
TC14L	1.0um CMOS gate array (soft macros)
TC160G/E	0.8um CMOS gate array (soft macros)
TC24SC	1.0um CMOS standard cell (soft macros)
TC25SC	0.8um CMOS standard cell (soft macros)
TC165G/E	0.8um CMOS gate array (embedded scan circuitry, US only)

Vertex

V25-family	Gate arrays up to 172K gates
V50-family	Gate arrays up to 256K gates

VLSI Technology Inc

Catalog ICs

Advanced RISC Machines

ARM61	RISC microprocessor
ARM600	RISC processor
ARM610	RISC processor
ARM700	RISC processor; 33MHz @ 5V or 20MHz @ 3V
MEMC20	Memory controller
VIDC20	Video controller

Altera

Flex 8000 family	
EPF8282/V	PLD, 5K gates
EPF8820	PLD, 16K gates

AMD

Am29030/5	Common Imaging Engines
Am29200	RISC Microcontroller
Am79C864	FDDI PLC
Am79c940	Ethernet MACE
Mach 3 and 4 families	FPGAs up to 10K gates
Mach 355	3700 gate EPLD
Mach 445	4000 gate EPLD
Mach 465	10000 gate EPLD

Analog Devices

ADSP21010	Digital signal processor
ADSP21020	Digital signal processor

AT&T

ATT92010	32 bit RISC CPU (Hobbit chip set)
ATT92011	System interface functions (Hobbit chip set)
ATT92012	Memory card controller (Hobbit chip set)
ATT92013	Interface to AT-compatible bus (Hobbit chip set)
ATT92014	Flat-panel controller (Hobbit chip set)
1C03/../20	Optimised Reconfigurable Cell Array (FPGA) - 3-20K gates
WEDSP16C	Digital signal processor
WEDSP16J	Digital signal processor
WEDSP1610	Digital signal processor
WEDSP1616	Digital signal processor
BL497AA	Boundary-Scan Master -- allows control of boundary-scan paths from a parallel or serial PC interface. Can generate tests according to industry-standard algorithms.

Austria Mikro Systems International

AS3501	DSP with analog interface for GSM

Brooktree

Bt463	RAMDAC
Bt812	NTSC/PAL to RGB/YCrCb decoder

C-Cube Microsystems

CL4000	Image compression/expansion processor

Concurrent Logic	
CLi6000 series	FPGAs. Boundary-scan test 'macro' loaded in place of system logic.
Crosspoint Solutions	
CP20K	FPGA (TAP used for input of programming data)
DEC	
21066	Alpha processor, 160MHz
21068	Alpha processor, 66MHz
Fujitsu	
MB86930	SparcLITE™– SPARC-based controller
IBM Corporation	
PowerPC series	
I-Cube	
IQ160	160 port cross-bar switch (programmable interconnect controlled from 1149.1 interface)
IDT	
74ABT18xxx	245 (flow-through transceiver), 502 (universal transceiver), 504 (universal transceiver), 646 (registered transceiver)
8990	Test bus controller
8997	Scan path linker
79SR4400	Very high performance, highly integrated 64-bit CPU. Biamry compatible with R3000A
R4000A	50 and 67MHz versions
Integrated Information Technology Inc (IIT)	
VCP	32-bit RISC vision controller and processor
Intel	
i386EX	Microprocessor for embedded control
i486DX	50 MHz Microprocessor
i486SL	3.3V microprocessor, 25MHz and 33MHz
i486SX	16MHz/25MHZ microprocessor
i486DX2	Microprocessor - 50MHz
82490DX	Second level 80486DX cache SRAM
82495DX	Second level 80860DX cache controller
80860XP	RISC processor
82490XP	Second level 80860XP cache SRAM
82495XP	Second level 80860XP cache controller
iFX780	Flexlogic FPGA
Pentium	Microprocessor
Intellitech	
PSCAN-C	Parascan – IC for building active sockets, etc – 66 pins
Lattice Semiconductor	

pLSI2000	High density PLDs, up to 135MHz clock
ispLSI2000	High density PLDs, up to 135MHz clock
Motorola	
68040	32-bit microprocessor
68EC040	32-bit microprocessor
68LC040	32-bit microprocessor
68330	32-bit microcontroller
68340	32-bit microcontroller
68341	
68349	
68360	
88110	RISC processor
88410	Cache
	FDDI chip set
68HC11	8-bit microcontroller
PowerPC	Microprocessor
MPA10xx series	FPGAs, 3K to 9K gates
National Semiconductor	
SCAN™PSC100F	Parallel-to-serial converter for interfacing from microprocessor bus (etc) to 1149.1 TAP
SCAN™PSC110F	SCAN bridge, hierarchical and multidrop addressable JTAG port for system-wide test access
SCAN™18xxxT	18-bit testability chips (245, 373, 374, 540, 541)
SCAN™18xxxA	18-bit testability chips (2373, 2374, 2540, 2646, 2652, 2952)
SCAN™22CV10F	10nS 22V10 PLD with boundary-scan (equivalent to GAL22V10)
DP83266	MACSI device (FDDI media access controller and standard interface)
NCR	
53C920	SDP chip
NEC Electronics Inc	
uPD77016	DSP microprocessor
Philips (Faselec)	
PCF5081	GSM baseband signal processor
PMC Sierra	
PM5345	Suni ATM to host interface
Quality Semiconductor	
SCAN series	Second source for National Semiconductor SCAN18xxxT parts
SGS-Thomson	
RAM tester	IC that performs test of a RAM array under instruction through TAP
Glue logic tester	IC to help in testing non-1149.1 'glue' logic
T9000	Transputer

Siemens

PEB2465	Four-channel codec filter

Silicon Graphics

MIPS R4000	RISC processor

Texas Instruments

SN74BCT8xxx	Octal parts: 8240 (buffer), 8244 (buffer), 8245 (transceiver), 8373 (latch), and 8374 (flip-flop).
SN74ABT8xxx	Octal parts: 8240 (buffer), 8244 (buffer), 8245 (transceiver), 8373 (latch), 8374 (flip-flop), 8543 (latched transceiver), 8646 (registered transceiver), 8652 (registered transceiver) and 8952 (clocked transceiver).
SN74ABT18xxx	Widebus parts: 18245 (transceiver), 18502 (universal transceiver), 18504 (universal transceiver), 18640, 18646 (registered transceiver), and 18652 (register transceiver).
SN74LVT18xxx	3.3volt 18- and 20-bit bus devices (245, 502, 504, 640, 646, 652)
SN74LVT38xxx	3.3 volt 36- and 40-bit bus devices
SN74ACT8990	Controller. Allows control of boundary-scan paths from a parallel PC interface.
SN74ACT8994	Digital Bus Monitor – 16-bit logic/signature analyser on a chip
SN74ACT8997	Scan path linker
SN74ACT8999	Scan path selector – allows selection between multiple boundary-scan paths on a board
TMS29F816	'Diary' – Serially-accessible memory that can hold board ID and revision, maintenance/repair data, etc.
TMS320C40	Floating point digital signal processor
TMS320C50	Fixed point digital signal processor
TMS320C51	Fixed point digital signal processor
TMS320C52	Fixed point digital signal processor
TMS320C53	Fixed point digital signal processor
TMS34082	Floating point processor
TMS390S10	microSPARC RISC processor
TMS390Z50	superSPARC RISC processor
TMS390Z55	Multicache controller
TFB2002	FutureBus+ protocol I/O controller
TFB2010	FutureBus+ arbitration controller
TFB2011	FutureBus+ programmable arbiter
TFB2022	FutureBus+ data path unit
TPC12 series	FPGA (up to 8K gates)
TPC14 series	FPGA

TRW LSI Products

TMC22190	Digital video encoder

VLSI Technology Inc

VY86C060	32-bit RISC processor (ARM60 kernel)
VY86C600	32-bit RISC processor (ARM600 kernel)
VY86C620	32-bit RISC processor (ARM600 kernel)

Xilynx

4000 series Programmable gate arrays

Testers, Instrumentation, and TPG Tools

Alpine Image Systems

proTEST-PC Plus	Plug in board for PC with software
Mux/4	4-port multiplexor for use with proTEST-PC
ScanBox Probe/128	128-channel 1149.1-to-parallel interface, e.g. for external connection to edge connector during test
ScanRack	16-slot chassis. Accommodates ScanBox cards giving up to 2048 'channel' capability.
AVL	Test language for scan testing. Product can read data created by Teradyne Victory software.
AVLcpp	Converts AVL to ANSI C.
Convert!!	Converts simulator output into AVL.

Brothers Electronics Inc

BST800	MDA/Boundary-Scan tester

Cadence/IMS

XLScan	Prototype test system
MCM Test Station	ATS! Blazer test station combined with Teradyne Victory software

Corelis

BA-1149.1	1149.1 analyser for use with HP1650/16500 logic analysers
PC-1149.1	PC-AT plug-in board for PC with software
PC-1149.1/100F	As PC1149.1 with memory behind the pin
CET-1149.1	Ethernet to boundary-scan converter
SCANIO/280	280 individually controlled boundary-scan test channels
SCANIO/616	616 individually controlled boundary-scan test channels
CVME-SCANIO/280	VMEbus module with 280 individually controlled boundary-scan test channels
CVME-1149.1	B-size VME/VXIbus boundary-scan controller
CVXI-1149.1	C-size VXI-bus boundary-scan controller board
CVXI-1149.1/IM	C-size VXI-bus boundary-scan controller board with memory behind the pin
CVXI-SCANIO/616	C-size VXIbus I/O module with 616 individually controlled boundary-scan test channels
CVXI-1149.1/616	C-size VXI-bus boundary-scan controller board combined with 616 individually controlled boundary-scan test channels

Computer Automation

S20	In-circuit tester with boundary-scan test option
S2000	Functional test system

Electronic KTS

	Integration of Model 2005i MDA with AIS proTEST boundary-scan test module

Fluke

PM8683	1149.1 Dissassembler for PM3580 logic analyser family

GenRad

BasicSCAN™	Software to generate in-circuit tests from BSDL descriptions for GR227X and GR228X testers
Pathfinder™	Boundary-scan toolkit

Gopel Electronic

MFC1149.1	Plug-in board for PC with software (CASCON100)

Hewlett-Packard

HP3065	Board tester
HP307x	Board testers
HP82000	IC tester
HP82000/FT	2000MHz board tester
HP82000/MCM	200MHz MCM/board tester
InterconnectPlus™	Boundary-scan test software for HP307x testers. Also Silicon Nail™ generates tests for 'conventional' ICs that are applied using a mix of real nails and boundary-scan cells.

JTAG Technologies

PF2111 10	64 channel digital input/output boundary-scan module, cascadable to 640 channels
PF2114 10	Keep-alive scan module (as PF2111 with memory test mode)
PF2150	BST demoboard
PF21[illegible]	Vector interface package for Corelis PC1149.1 PC-AT bus 1149.1 controller
PF2[illegible]	Vector interface package for Corelis CVXI-1149-1 VXI bus 1149.1 controller
PM[illegible]	BST-Explorer - Notebook-PC-based tester
PM[illegible]	Vectorblaster 19" IEEE488-compatible boundary-scan tester
PM[illegible]	BTPG test pattern generation software
PM[illegible]	BSD boundary-scan diagnostics

Also [illegible] source for Corelis products

Michael [illegible] Consulting

SV[illegible]	Converts Serial Vector Format to run on IMS Logic Master testers

Innovate

900[illegible]	Board test system

Mainboard [illegible] Systems

PC-[illegible]	PC-AT bus test card for PC with software

Marconi

B[illegible] function card	
	... for M505, M511, and M515 in-circuit test systems
42[illegible]	Multi-strategy test system

MCT

MC[illegible]	Boundary-Scan IC Test System (up to 960 pins)

Schlumberger

T[illegible] S2000	IC tester for scan and boundary-scan devices

Series 700	CATE software
Sonitech International Inc	
Brahma	MSPD/JTAG Debugger/Emulator for TMS320C3x and TMS 320C40
Tektronix	
VX4491	Serial test module (VXI)
Teradyne	
Victory™	Automatic test-pattern generation, testability analysis, and diagnostics, including custom and standard output to automatic test equipment (ATE), including Teradyne's Z1800 and L300 board testers. Supports IEEE 1149.1 and BSDL standards and SVF.
BICT	Automatic generation of boundary in-circuit (BICT) patterns and diagnostics for boundary-scan parts, including analysis of device constraints and automatic disabling VIT. Automatic generation of virtual interconnect tests (VIT) for detecting and diagnosing stuck-at pin faults, shorts, and opens between boundary-scan parts, and shorts between boundary-scan and conventional nets
VCCT	Automatic test-pattern generation for virtual component/cluster tests (VCCT) for testing conventional non-scan devices or clusters of devices through the boundary-scan path using a combination of real and boundary-scan channels
BFT	Automatic generation of boundary functional tests (BFT) to verify the internal circuitry of boundary-scan devices, including the core logic and the TAP and 1149.1 registers, using INTEST, BIST, and internal scan.
Access Analyzer™	Automatic analysis of scan and non-scan nets for controllability and observability, including reports recommending testpoint placement for optimal testability.
Texas Instruments	
ASSET™	Software plus PC plug-in board; Teradyne Victory software option

CAD Tools

AT&T

BSIT	Automated generation of boundary-scan circuitry for AT&T ASICs
TAPDANCE	Conformance test generator

Compass Design Automation

Test Assistant	Compiles 1149.1 circuitry

Crosscheck

	ASIC design-for-test tools that lead to design-for-test circuitry accessible via IEEE Std 1149.1

Dassault

Frenchip	VHDL-based synthesis tool

DixiCAD

	Tool for boundary-scan test generation and diagnostics for wiring interconnect faults

European Silicon Structures

SOLO2030	ASIC design software

GenRad

HiDESIGN A	Automated design of 1149.1 circuitry

Gould/AMI

NETTAG	Automatic insertion of 1149.1 logic into ASICs

Intel

Flexlogic	Loads Flexlogic device implementation files through JTAG loader kit

LSI Logic

ScanBuilder	

Mentor Graphics

Virtual test builder	Identifies nodes that are boundary-scan testable and marks as "nail free". (Based on Teradyne Victory)

Philips Electronic Designs and Tools

TimNet	Automatic insertion of 1149.1 logic into ASICs
TimPat	Generates test patterns for 1149.1 circuitry in ICs
PantherExpert	Silicon 'test' compiler

Racal-HHB

Intelligen™	Partial-scan-based design-for-test and test pattern generation

Synopsys

TestCompiler	Automatic insertion of 1149.1 circuitry

TestCompiler Plus	Automatic insertion of 1149.1 circuitry

Assembled Modules Offering 1149.1 Interfaces

Data Translation Inc

DT3801	Mixed signal measurement card for PC

Loughborough Sound Images Ltd

ADSP21020	DSP board for PC AT and compatibles (uses Analog Devices DSP)

Books

IEEE Computer Society Press

Maunder, CM and Tulloss, RE, "The Test Access Port and Boundary-Scan Architecture", 1990, ISBN 0-8186-9070-4, 372 pages

IEEE Standards

IEEE Std 1149.1-1990, "Standard Test Access Port and Boundary-Scan Architecture"

Kluwer Academic Press

Bleeker, H et al, "Boundary-Scan Test—A Practical Approach", 1993, ISBN 0-7923-9296-5, 225 pages

Parker, KP, "The Boundary-Scan Handbook", 1992, ISBN 0-7923-9270-1, 2262pages

Services, miscellaneous products

Intellitech

Test program development for TI ASSET

FPGA 'programs' to download 1149.1 test logic

Texas Instruments

SATB002A	Scan Educator educational tool (free of charge)
SATB006	Testability videotape (describes 1149.1 and its application)
SATB007	Testability CD-ROM (includes on-line copy of 1149.1 standard)

From nascent@netcom.com (Nascent Technology)
Newsgroups: comp.lsi.cad
Subject: ANNOUNCE: Electronic Design Tools from Nascent
Date: Fri, 18 Nov 1994 23:08:33 GMT

Electronic Design Tools from Nascent
Version 2.0

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The Nascent CDROM contains the most recent and comprehensive collection of freely available tools for the design and fabrication of integrated circuits. Tools include Magic, Spice, Chipmunk, Olympus, Sis and espresso, Ocean, and Alliance. Together they support behavorial design; simulation at the logic, switch, and circuit level; multi-level combinatorial and sequential logic synthesis; VLSI layout; and sea-of-gates place and route. All tools run under the X11 graphical interface provided with the Nascent CDROM, and come with extensive documentation and interactive tutorials.

[Magic VLSI Layout editor] Magic is a graphical CAD tool for generating physical layout descriptions of VLSI circuits. The Magic system includes the Magic layout editor, the switch-level circuit simulator IRSIM, and utilities for converting extracted netlists to various simulation-compatible formats (SPICE, SCALD, IRSIM, CIF, GDS2). The layout editor features on-the-fly design rule checking, flagging design errors directly on the layout. The interactive IRSIM simulator can display logic values by touching portions of the layout during simulation. Magic comes configured for the MOSIS process library.

[Spice Analog Simulator] Spice is a general purpose circuit simulation program for nonlinear dc, nonlinear transient, and linear ac analyses. Circuits may contain resistors, capacitors, inductors, mutual inductors, independent voltage and current sources, four types of dependent sources, transmission lines, switches, and the five most common semiconductor devices: diodes, BJTs, JFETs, MESFETs, and MOSFETs. Node voltage waveforms can be viewed in X11 using the nutmeg display post-processor for spice.

[Olympus Behavioral Synthesis] The Olympus Synthesis System is a set of tools for designing integrated circuits from behavioral descriptions. Olympus supports synthesis with timing constraints at the behavioral, structural, and logic levels. It includes behavioral, structural, and logic synthesis, technology mapping, and simulation. Behavioral models are written in a hardware description language called HardwareC, a derivative of the C language. Both the high level behavioral description and a corresponding synthesized gate-level netlist can be simulated. A graphical logic waveform display is also included.

[SIS Logic Synthesis] SIS is a sequential logic synthesis program. It takes as input a state transition table, a signal

transition table, or a logic description of a sequential circuit. Logic can be optimized for area, delay, and testability, and mapped into a user-specified cell library. SIS uses state-of-the-art logic optimization and verification algorithms to optimize across latches and among state assignments in a synchronous design. SIS may also be used to synthesize asynchronous circuits.

[Ocean Sea-of-Gates Design System] Ocean is a set of tools for the synthesis and verification of semi-custom sea-of-gates and gate array chips from circuit level descriptions. Ocean uses one of three different prefabricated master images, or regular pattern of transistors, to automatically layout a gate-level netlist from a cell library. Cells are first placed on the image, and then connected together. A transistor-level netlist can then be extracted with parasistic capacitances and resistances, and resimulated to verify the layout.

Ocean includes three sea-of-gates images, cell libraries, and a template chip. Ocean may also be used with the SIS logic Synthesis tool to automatically synthesize and layout hardware from a logic description.

[The Alliance VHDL RTL simulator] Alliance allows the specification of logic in an RTL subset of VHDL. It includes VHDL behavioral and structural simulation, logic synthesis, layout synthesis, hierarchical design rule checking, layout extraction, and a formal proof analyzer. A comprehensive CMOS standard cell library is included. Each cell is has a corresponding circuit schematic, VHDL behavior, and layout. Alliance supports several standard VLSI description formats (SPICE, EDIF, VHDL, CIF, GDS2).

[Chipmunk VLSI layout and schematic editor] Chipmunk includes a schematic editor, analog and digital simulator, netlist generator, netlist comparator, layout editor, and an automatic cell layout composer. Simulation logic values can be displayed as different node colors during logic simulation. The layout editor can generate labeled postscript figures for inclusion in documents that can import postscript, such as and .

The Linux from Nascentdistribution on CDROM includes the Linux operating system and over 1000 applications for Linux. It comes with an easy to use Xwindowsinterface with the OpenLook window manager to allow access to graphical applications over a network. Networking is integrated into the operating system kernel.

The professionally bound User Guide included with the Nascent CDROM gives step-by-step instructions on how to install and administer Linux on your computer. Xwindow configuration, mail/news administration, system backups, strategies for mounting harddisks over networks, upgrading packages, filesystem structure, program development, and a troubleshooting section are included.

The Linux from Nascent CDROM, Version 2.0, is only 59.95 plus shipping and handling, and comes with an 30-day unconditional money-back guarantee. If you aren't completely satisfied, return the package with your receipt within 30 days and the purchase price, excluding shipping and handling, will be refunded to you.

In addition, Nascent offers the Linux from Nascent Plus package for only 119.95, which includes six months of email support and a 30 discount off a future release of the Nascent CDROM.

Nascent separately provides the SWiM OSF/Motifcompatible Window Manager and application development library and tools. It includes the window manager, shared and static libraries, UIL compiler, on-line documentation, and complete printed OSF/Motif User's Guide.

A list of the applications included on the Nascent CDROM, hardware compatibility list, order form, as well as a current copy of this announcement may be obtained via anonymous ftp from ftp.netcom.com:/pub/nascent.

BOOKS ON DIGITAL TESTING

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2 - Amersekera, E. A., and D. S. Campbell, ***Failure Mechanisms in Semicon- ductor Devices***, Wiley, 1987.

3 - Bardell, P. H., W. H. McAnney, and J. Savir, ***Built-In Test for VLSI : Pseudorandom Techniques***, Wiley, 1987.

4 - Bateson, J., ***In-circuit Testing***, Van Nostrand Reinhold, 1985.

5 - Bennetts, R. G., ***Introduction to Digital Board Testing***, Crane Russak, 1982.

6 - Bennetts, R. G., ***Design of Testable Logic Circuits***, Addison-Wesley, 1984.

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